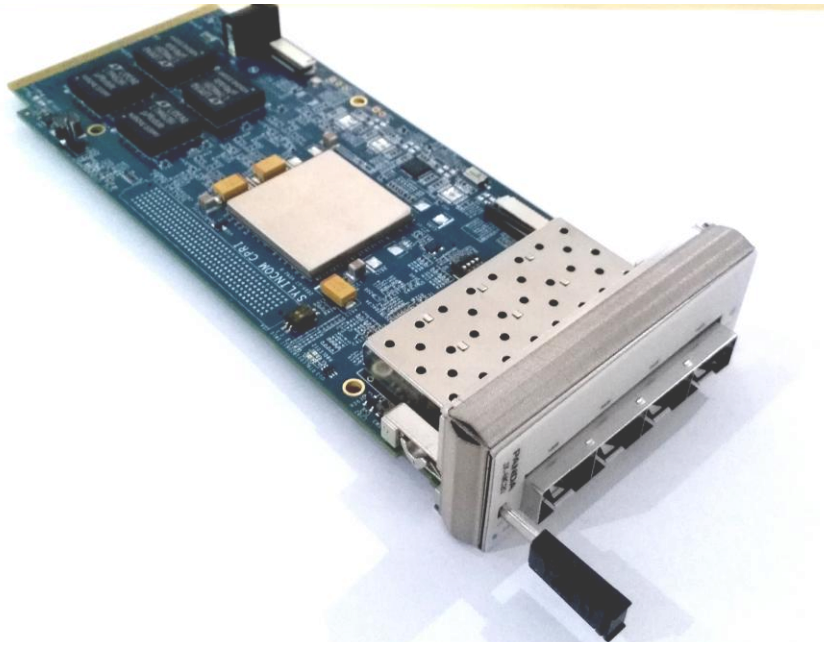
JX-MC20

Multiple CPRI links card-AMC-K7



Key Feature

- Xilinx Kintex-7 FPGA
- XC7K325T standard build; cost effective; support X16 GTX
- 8GbX16-1333 DDR3 SDRAMs for the multiple high bandwidth buses
- One 1GbX8 DDR3 SDRAM for embedded cpu
- "Fat pipe" connections direct from AMC backplane 4-7, 8-11 to FPGA; Support X4 SRIO interface at up to 20Gbps
- Dual GbE from FPGA to backplane
- Four front panel SFP+ optical interfaces configurable as CPRI, OBSAI, GigE, SRIO or other standards
- the console interface is the USB serial port or Ethernet
- Mezzanine site for additional I/O, including 106 GPIOs and X2 GTX
- Front-I/O: X4 SFP+
- Support SPI/BPI/JTAG configuration
- Single width Advanced Mezzanine Card, PICMG AMC.0 Rev. 2.0; can also run standalone
- Full-size standard product
- Standard LEDs according to AMC.0 specification

Overview

The JX-MC20 is a high density, high FPGA-based interface and signal processing card for the MicroTCA platforms. A powerful on-board processor is high density Xilinx Kintex-7 FPGA. It is aimed at high performance FPGA processing and wireless radio applications as well as optical data interfacing applications.

The board supports four SFP+ optical interfaces which can be configured to support CPRI at up to 6.144Gbps per link for advanced multi-rate LTE applications, giving clock synchronisation through the optical link. As well as , these SFP+ optical interfaces can be configured as CPRI, OBSAI, GigE, SRIO or other standards.

The K7 FPGA provides dual Gigabit Ethernet to the backplane, as well as the fat pipes on AMC ports 4-7 and 8-11 which can support PCI Express (with build option), SRIO, XAUI , at up to 20 Gbps per link.

The board provides flexible high-speed signal processing and can be updated over Ethernet or Flash on the board.

Changes are possible for our customers.

Applications

Wireless baseband, Software-defined radio platform, Signal processing, FPGA verification

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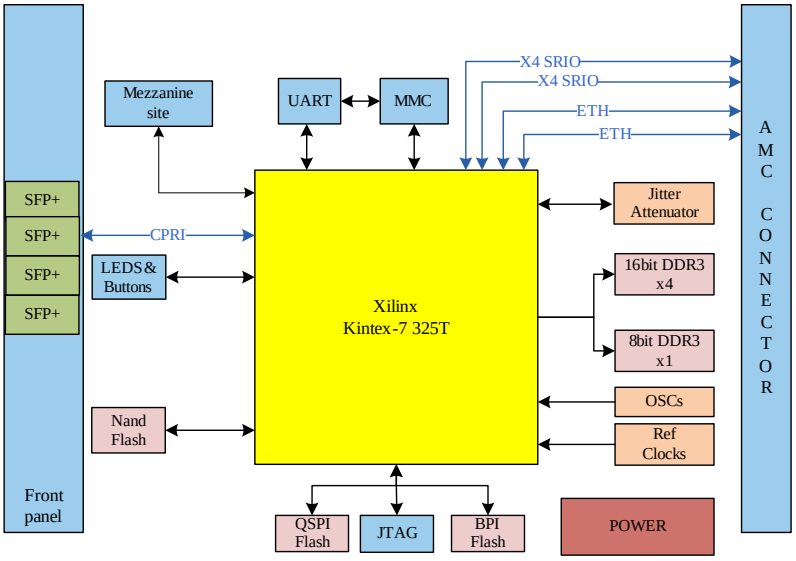
JX-MC20 Block Diagram



Hardware Specifications

FPGA： Xilinx Kintex-7 FPGA:

- Standard configuration is XC7K325T
- Configuration from UART or Ethernet
- Four 2GbX16 DDR3 SDRAMs for the multiple high bandwidth buses
- One 1GbX8 DDR3 SDRAM
- Two 20Gbps 4XSRIO V2.1 links to MCH
- Two Ethernet ports to MCH
- 4X front panel SFP+ at up to 6.144Gbps
- 2X GTX to Mezzanine connector
- 3X CLK to AMC ports12-15

Form Factor：

- Single-width Advanced Mezzanine Card, AMC Rev2.0 compliant
- Full size standard product
- "Fat pipe" connections direct from AMC backplane 4-7, 8-11 to FPGA; Support X4 SRIO interface at up to 20Gbps
- Hot swap support

Timing： Full timing:

- AMC Telecom clock A-D support
- SFP+ recovered clock support
- OSCs Si5326/Si570 support

Front panel I/O：

- Four SFP+ at up to 6.144Gbps: CPRI, OBSAI, SRIO, GigE etc
- 1X Micro USB-B for debug

Mezzanine site：

- 106 GPIOs and X2 GTX

Debug：

- Support the PC Configure FPGA From Ethernet or front USB serial port
- Support SPI/BPI/JTAG configuration

Module management Controller：

- AMC.0 IPMB_L interface
- FRU EEPROM data
- Power, temperature monitoring

Operating environment :

- Operating temperature: -10℃-55℃ 90% non-condensing humidity
- Power consumption: up to 28W max
- Storage temperature range: -40 ℃ to +70 ℃ @ 95% relative humidity

Software Specifications

- Support SRIO data transfer to X4 CPRI.
- Support general board control by Ethernet or UART.
- Updating the FPGA code on-line.

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