1.

a),b),c),d), e)

A= 79625

B=81329

F1

A3=6=0110

F1= $\sum_{A,B}$ (1,2)=0110

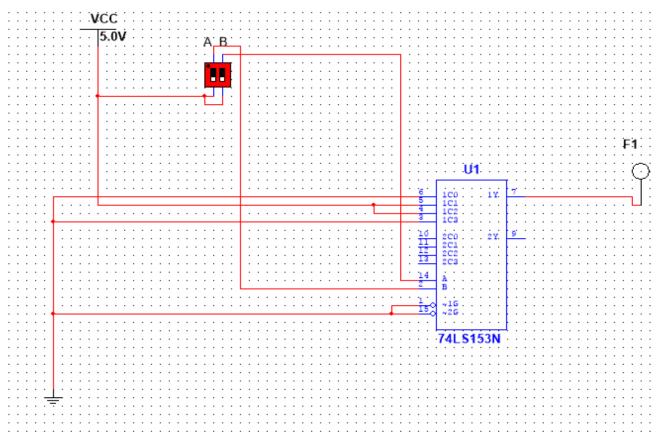
l	Α	В	F1	
	0	0	0	
	0	1	1	6
	1	0	1	
	1	1	0	

Y0=0

Y1=1

Y2=1

Y3=0



$F2=\sum_{A,B,C}(2,5,7)$

=00100101

Α	В	С	F2	
0	0	0	0	
0	0	1	0	2
0	1	0	1	
0	1	1	0	
1	0	0	0	
1	0	1	1	5
1	1	0	0	
1	1	1	1	

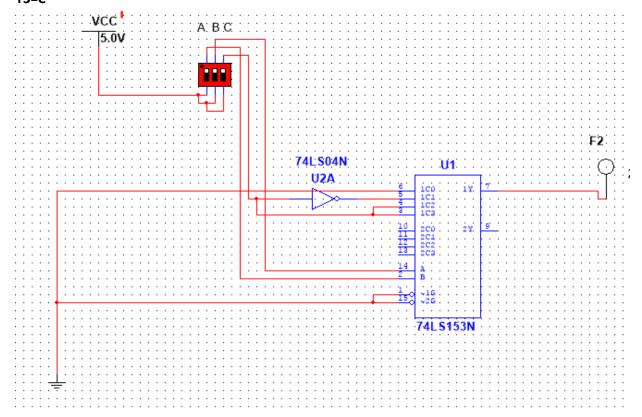
С	00	01	11	10
0	0	1	0	0
1	0	0	1	1

Y0=0

Y1=C'

Y2=C

Y3=C



B2=1=0001

B3= 3=0011

B4=2=0010

B5=1001

F3=0001001100100101

F3= $\sum_{A,B,C,D}$ (3,6,7,10,12,15)

AB CD	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	1	1	0	0
10	0	1	1	1

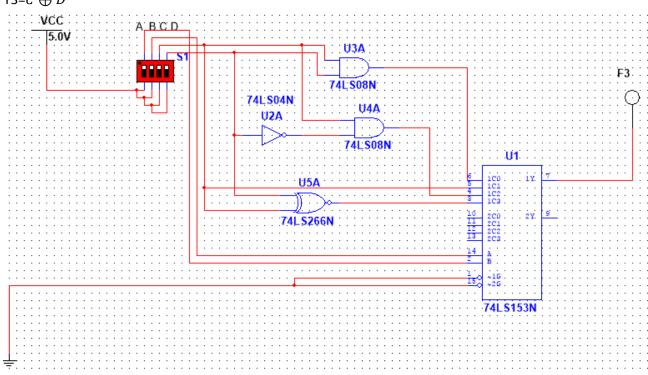
					_
Α	В	С	D	F3	
0	0	0	0	0	
0	0	0	1	0	1
0	0	1	0	0	
0	0	1	1	1	
0	1	0	0	0	
0	1	0	1	0	3
0	1	1	0	1	
0	1	1	1	1	
1	0	0	0	0	
1	0	0	1	0	2
1	0	1	0	1	
1	0	1	1	0	
1	1	0	0	1	
1	1	0	1	0	9
1	1	1	0	0	
1	1	1	1	1	

Y0=CD

Y1=C

Y2=CD'

Y3= $\overline{C \oplus D}$



2.

a).b)

A= 79625

B=81329

Α	В	С	Dispositivos habilitados		
0	0	0	D(A2), D(B4)	D9,D2	
0	0	1	D(A3)	D6	
0	1	0	D(B1), D(A5)	D8,D5	
0	1	1	D(B3), D(A1), D(A4)	D3,D7,D2	
1	0	0	D(A5)	D5	
1	0	1	D(B2), D(A5)	D1,D5	
1	1	0	D(B1), D(B4)	D8,D2	
1	1	1	D(B5), D(A2), D(A3)	D9,D9,D6	

D0=0

D1= $\overline{Z5}$

 $D2=\overline{Z0}+\overline{Z3}+\overline{Z6}$

D3= $\overline{Z3}$

D4=0

D5= $\overline{Z4}$ + $\overline{Z2}$ + $\overline{Z5}$

 $D6=\overline{Z7}+\overline{Z1}$

D7= $\overline{Z3}$

 $D8=\overline{Z2}+\overline{Z6}$

 $D9=\overline{Z0}+\overline{Z7}$

c)Pode-se utilizar um descodificador 2:4 como um *decoder* 3:8, utilizando 2 *decoders* 2:4 para que haja 8 saídas e utiliza-se a entrada do ENABLE para o MSB, neste caso A, para isso utiliza-se um NOT para que o ENABLE de cada *decoder* seja ativado quando o ENABLE do outro *decoder* não o esteja.

