컴퓨터구조

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Project #4

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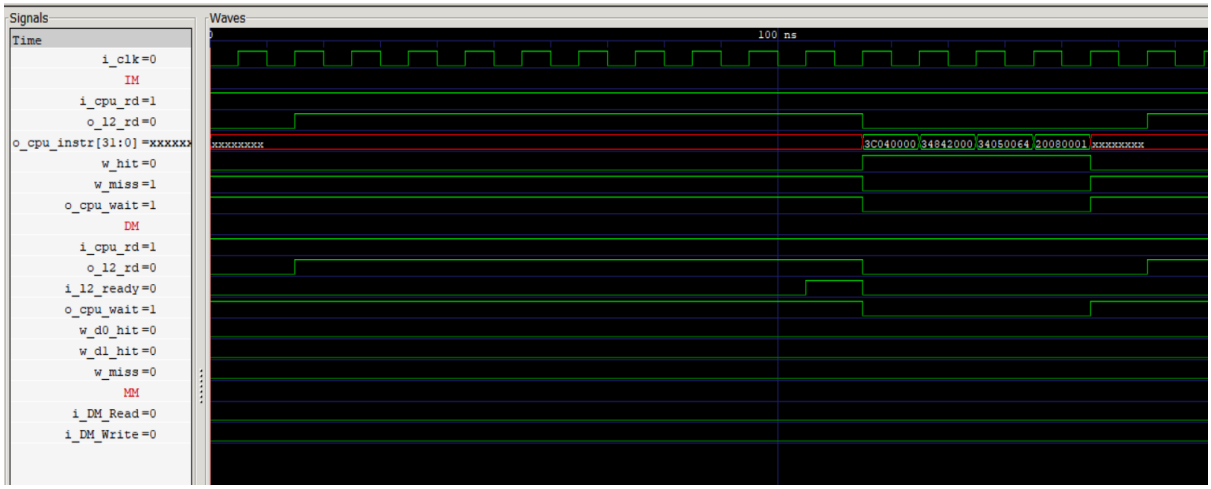
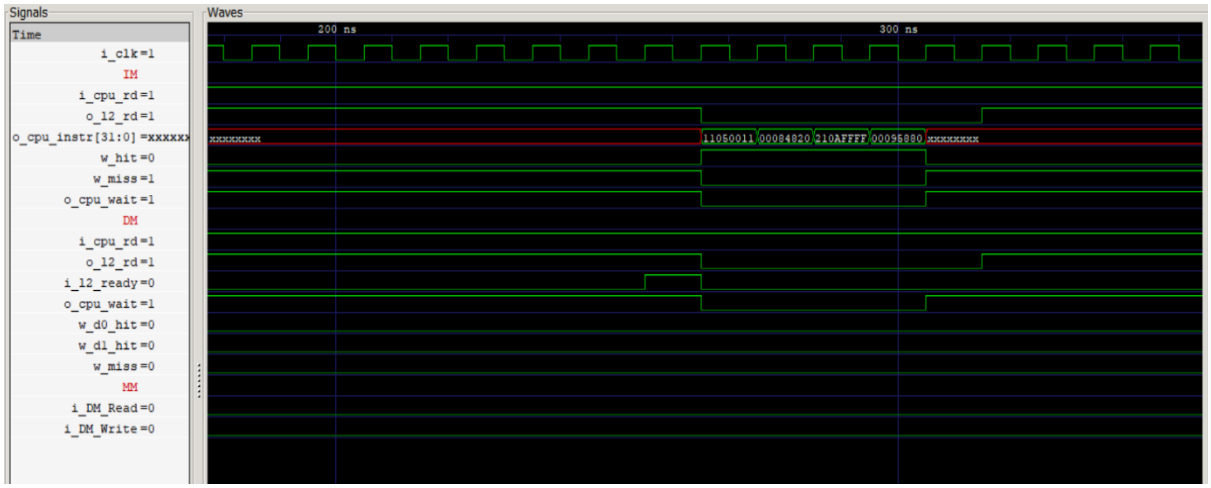
<실험 내용>

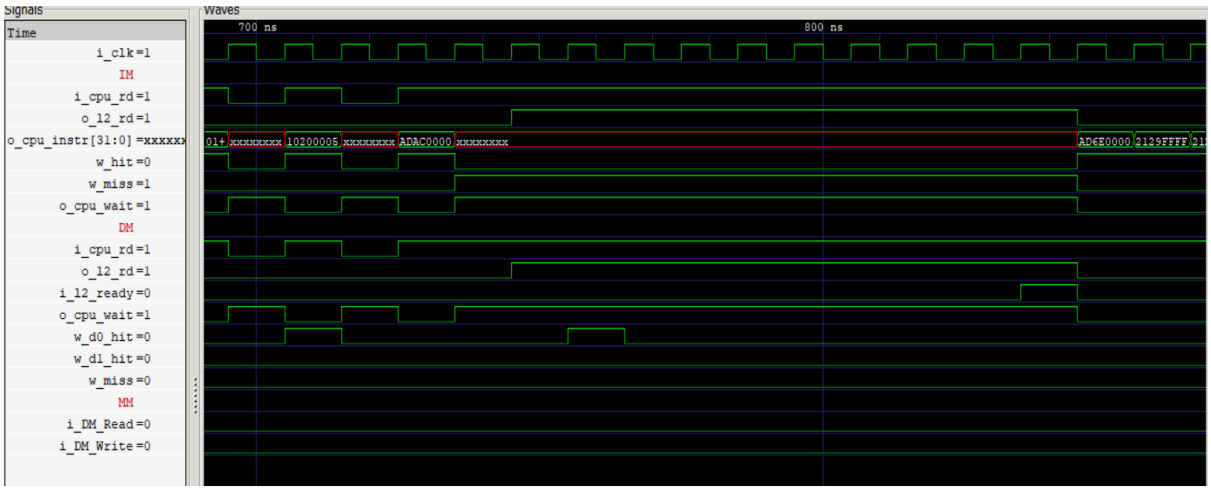
정렬 프로그램과 Benchmarks 프로그램에 각각 적합한 cache를 찾고, 각각의 프로그램의 적합한 cache가 왜 다른 건지 프로그램을 분석하여 비교합니다. 아래 testbench를 통해 비교할 bubble sort와 random sort의 알고리즘을 보면 bubble sort란 정렬 알고리즘 중 가장 기본적이고 간단한 알고리즘이며 버블 정렬은 두 인접한 원소를 검사하여 서로의 값을 교환하며 정렬하는 방법인데 오름차순 정렬의 경우 두 항목의 값을 비교하여 앞쪽 값이 더 크면 서로 위치를 교환하고, 내림차순의 경우 그 반대입니다. Random sort는 말 그대로 random하게 sort되는 것을 알 수 있으며 제공된 프로젝트 자료를 참고하면 bubble sort와 random sort를 비교할 수 있으며 각 testbench를 보면 다음과 같습니다. 바로 아래 내용은 Bubble sort입니다.





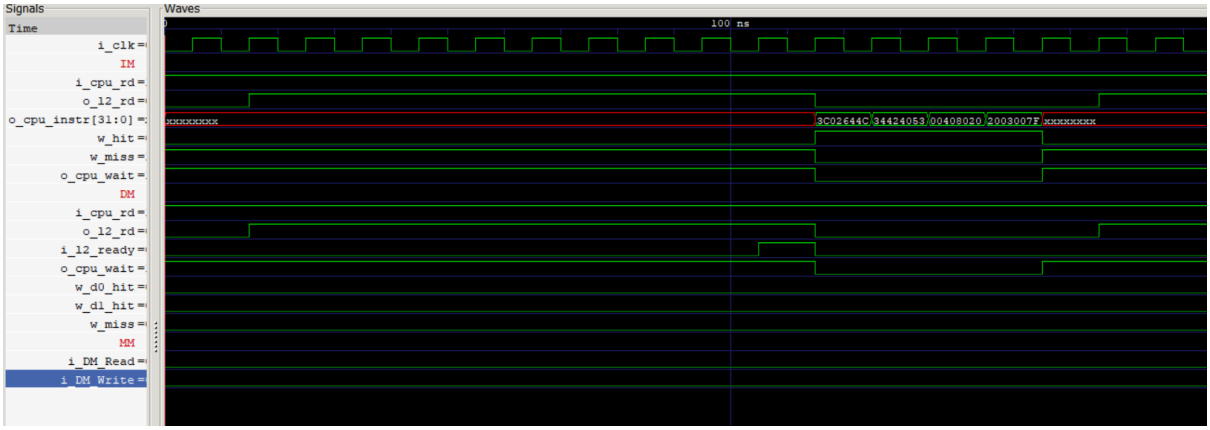
Data가 각각의 IM과 DM(cache)로 hit하면서 write된 것을 알 수 있습니다.

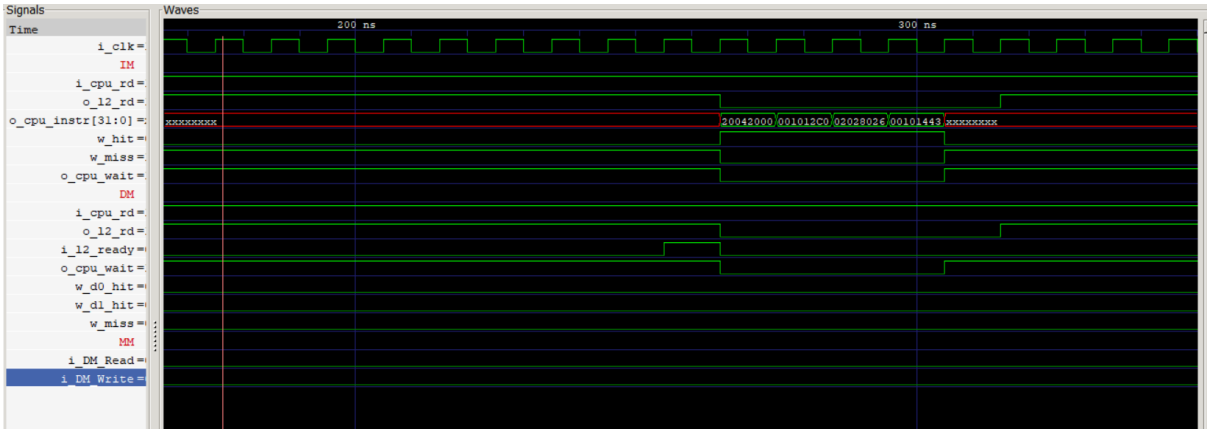
Main memory read가 진행된 것을 알 수 있습니다.



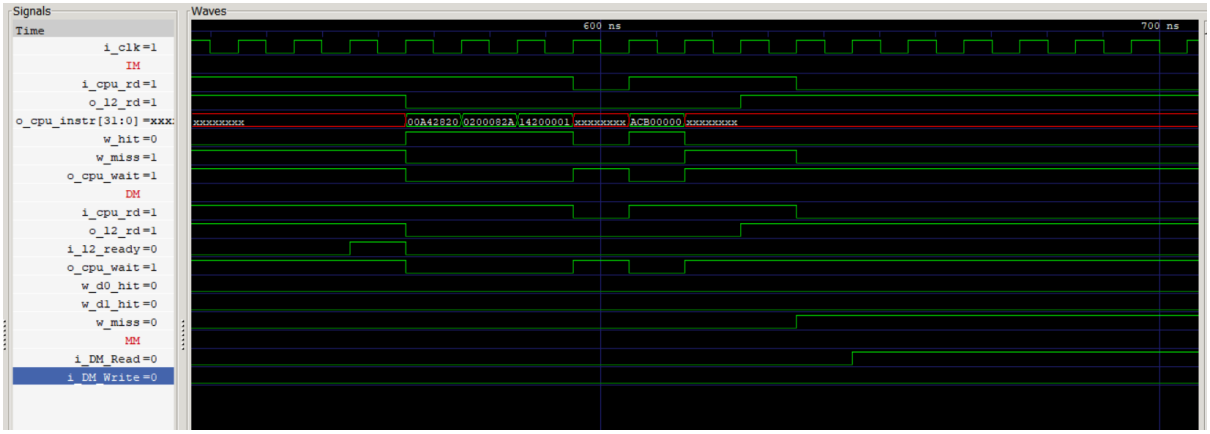
두 항목 간의 비교를 하여야 되므로 2개씩, 즉 2개씩 비교하므로 그에 따른 cache write를 진행하는 것을 알 수 있습니다.

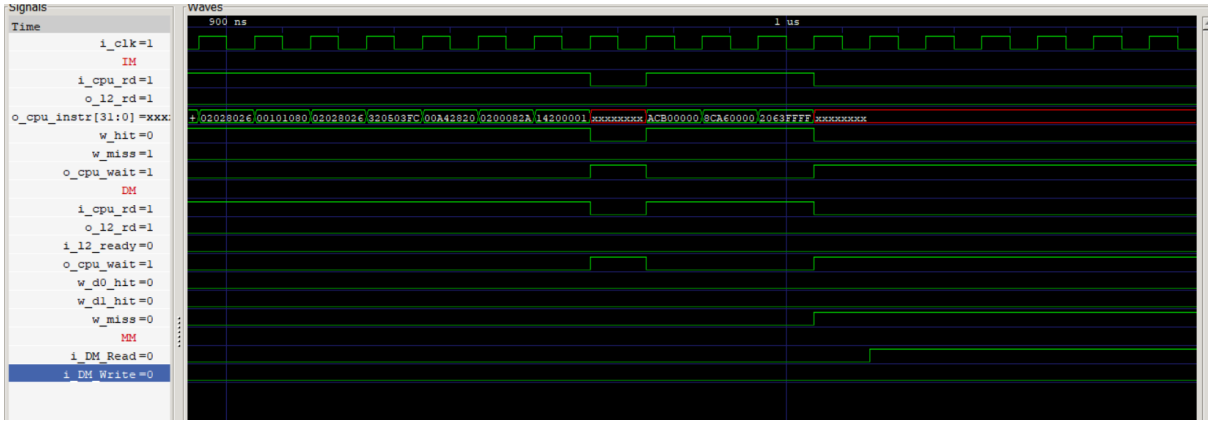
아래 random sort의 testbench를 보면





위의 bubble sort와 동일하게 처음에 cache에 write하는 과정은 동일하게 진행됩니다.

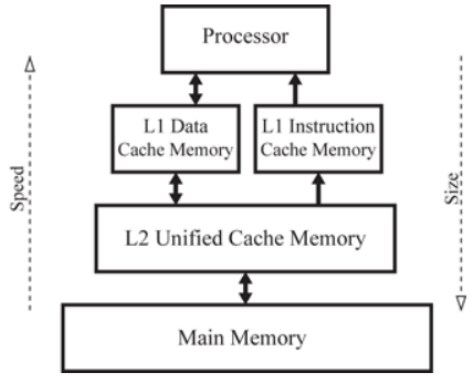




bubble sort에서는 2개씩 비교하는 과정이 있을 때는 하나씩 띄어서 instruction을 write했었는데 random sort에서는 그 또한 random하게 write하는 과정을 거치는 것을 알 수 있습니다.

<검증 전략, 분석 및 결과>

Cache의 기본 hierarchy를 보면



L1 cache는 instruction cache와 data cache로 separate 할 수 있고, L2 cache는 unified cache memory는 unified한 구조인 것을 참고 하여 아래 내용을 simulation할 수 있습니다.

◆ Unified cache / Separate cache

위의 경우에 해당하는 AMAT식은 다음과 같습니다.

AMAT = %instr x (instr hit time + instr miss rate x instr miss penalty) +
%data x (data hit time + data miss rate x data miss penalty)

아래 simulation의 과정의 예시입니다. I1을 unified cache로 작성한 것입니다.

```
-cache:il1 il1:64:16:1:l

-cache:dl1 none
-cache:il2 none
-cache:dl2 none
-tlb:itlb none
-tlb:dtlb none
```

```
sim: ** simulation statistics **
sim_num_insn            119392269 # total number of instructions executed
sim_num_refs             44164172 # total number of loads and stores executed
sim_elapsed_time                7 # total simulation time in seconds
sim_inst_rate        17056038.4286 # simulation speed (in insts/sec)
il1.accesses            119392269 # total number of accesses
il1.hits                 80660601 # total number of hits
il1.misses               38731668 # total number of misses
il1.replacements         38731604 # total number of replacements
il1.writebacks                 0 # total number of writebacks
il1.invalidations              0 # total number of invalidations
il1.miss_rate             0.3244 # miss rate (i.e., misses/ref)
il1.repl_rate             0.3244 # replacement rate (i.e., repls/ref)
il1.wb_rate               0.0000 # writeback rate (i.e., wrbks/ref)
il1.inv_rate              0.0000 # invalidation rate (i.e., invs/ref)
ld_text_base           0x00400000 # program text (code) segment base
ld_text_size              2166768 # program text (code) size in bytes
ld_data_base           0x10000000 # program initialized data segment base
ld data size               264644 # program init'ed `.data' and uninit'ed
```

```
sim: ** simulation statistics **
sim_num_insn              29241771 # total number of instructions executed
sim_num_refs               8043255 # total number of loads and stores executed
sim_elapsed_time                 2 # total simulation time in seconds
sim_inst_rate         14620885.5000 # simulation speed (in insts/sec)
il1.accesses              29241771 # total number of accesses
il1.hits                  21681208 # total number of hits
il1.misses                 7560563 # total number of misses
il1.replacements           7560531 # total number of replacements
il1.writebacks                   0 # total number of writebacks
il1.invalidations                0 # total number of invalidations
il1.miss_rate               0.2586 # miss rate (i.e., misses/ref)
il1.repl_rate               0.2586 # replacement rate (i.e., repls/ref)
il1.wb_rate                 0.0000 # writeback rate (i.e., wrbks/ref)
il1.inv_rate                0.0000 # invalidation rate (i.e., invs/ref)
dl1.accesses                8146520 # total number of accesses
dl1.hits                    6051951 # total number of hits
dl1.misses                  2094569 # total number of misses
dl1.replacements            2094537 # total number of replacements
dl1.writebacks               461897 # total number of writebacks
dl1.invalidations                0 # total number of invalidations
dl1.miss_rate               0.2571 # miss rate (i.e., misses/ref)
dl1.repl_rate               0.2571 # replacement rate (i.e., repls/ref)
dl1.wb_rate                 0.0567 # writeback rate (i.e., wrbks/ref)
dl1.inv_rate                0.0000 # invalidation rate (i.e., invs/ref)
ul2.accesses               10117029 # total number of accesses
```

I1을 separate한 cache로 작성한 것입니다. Data cache와 instruction cache로 작성한 것입니다.

```
-cache:dl1        dl1:32:16:1:l
-cache:dl2                  none #
-cache:il1        il1:32:16:1:l
none}
-cache:il2                  none #
dl2|none}
```

```
sim: ** simulation statistics **
sim_num_insn            119392269 # total number of instructions executed
sim_num_refs             44164172 # total number of loads and stores executed
sim_elapsed_time                7 # total simulation time in seconds
sim_inst_rate        17056038.4286 # simulation speed (in insts/sec)
il1.accesses            119392269 # total number of accesses
il1.hits                 73761455 # total number of hits
il1.misses               45630814 # total number of misses
il1.replacements         45630782 # total number of replacements
il1.writebacks                 0 # total number of writebacks
il1.invalidations              0 # total number of invalidations
il1.miss_rate             0.3822 # miss rate (i.e., misses/ref)
il1.repl_rate             0.3822 # replacement rate (i.e., repls/ref)
il1.wb_rate               0.0000 # writeback rate (i.e., wrbks/ref)
il1.inv_rate              0.0000 # invalidation rate (i.e., invs/ref)
dl1.accesses              44513362 # total number of accesses
dl1.hits                  34150595 # total number of hits
dl1.misses                10362767 # total number of misses
dl1.replacements          10362735 # total number of replacements
dl1.writebacks             4581715 # total number of writebacks
dl1.invalidations                0 # total number of invalidations
dl1.miss_rate             0.2328 # miss rate (i.e., misses/ref)
dl1.repl_rate             0.2328 # replacement rate (i.e., repls/ref)
dl1.wb_rate               0.1029 # writeback rate (i.e., wrbks/ref)
dl1.inv_rate              0.0000 # invalidation rate (i.e., invs/ref)
ld_text_base           0x00400000 # program text (code) segment base
ld_text_size              2166768 # program text (code) size in bytes
ld_data_base           0x10000000 # program initialized data segment base
```

```
sim_num_refs               8043255 # total number of loads and stores executed
sim_elapsed_time                 2 # total simulation time in seconds
sim_inst_rate         14620885.5000 # simulation speed (in insts/sec)
il1.accesses              29241771 # total number of accesses
il1.hits                  21681208 # total number of hits
il1.misses                 7560563 # total number of misses
il1.replacements           7560531 # total number of replacements
il1.writebacks                   0 # total number of writebacks
il1.invalidations                0 # total number of invalidations
il1.miss_rate               0.2586 # miss rate (i.e., misses/ref)
il1.repl_rate               0.2586 # replacement rate (i.e., repls/ref)
il1.wb_rate                 0.0000 # writeback rate (i.e., wrbks/ref)
il1.inv_rate                0.0000 # invalidation rate (i.e., invs/ref)
dl1.accesses                8146520 # total number of accesses
dl1.hits                    6051951 # total number of hits
dl1.misses                  2094569 # total number of misses
dl1.replacements            2094537 # total number of replacements
dl1.writebacks               461897 # total number of writebacks
dl1.invalidations                0 # total number of invalidations
dl1.miss_rate               0.2571 # miss rate (i.e., misses/ref)
dl1.repl_rate               0.2571 # replacement rate (i.e., repls/ref)
dl1.wb_rate                 0.0567 # writeback rate (i.e., wrbks/ref)
dl1.inv_rate                0.0000 # invalidation rate (i.e., invs/ref)
ul2.accesses               10117029 # total number of accesses
ul2.hits                    9832183 # total number of hits
ul2.misses                   284846 # total number of misses
ul2.replacements             284590 # total number of replacements
ul2.writebacks                36822 # total number of writebacks
ul2.invalidations                0 # total number of invalidations
```

<traces>

# of Sets	Unified cache Miss rate	Unified cache AMAT	Split cache		Split cache AMAT
			Inst. Miss rate	Data Miss rate	
64	0.32440683	7.10523	0.38219237	0.2328055	7.20026989
128	0.26866009	6.07218	0.32440683	0.17308457	7.13519851
256	0.23193162	6.05378	0.26866116	0.11305403	6.08496235
512	0.16395908	6.02688	0.23193162	0.07642519	7.05962383

실습강의 자료를 참고하여 작성한 표입니다. Instruction miss rate가 data miss rate보다는 크며 split cache가 비교적 amat가 큰 것으로 판단 했습니다.

위의 조건에서는 testbench끼리의 비교도 가능했는데 내용은 다음과 같습니다.

```
sim: ** simulation statistics **
sim_num_insn              119392269 #
sim_num_refs               44164172 #
sim_elapsed_time                  7 #
sim_inst_rate          17056038.4286
il1.accesses              119392269 #
il1.hits                   73761455 #
il1.misses                 45630814 #
il1.replacements           45630782 #
il1.writebacks                    0 #
il1.invalidations                 0 #
il1.miss_rate                0.3822 #
il1.repl_rate                0.3822 #
il1.wb_rate                  0.0000 #
il1.inv_rate                 0.0000 #
dl1.accesses               44513362 #
dl1.hits                   34150595 #
dl1.misses                 10362767 #
dl1.replacements           10362735 #
dl1.writebacks              4581715 #
dl1.invalidations                 0 #
dl1.miss_rate                0.2328 #
dl1.repl_rate                0.2328 #
dl1.wb_rate                  0.1029 #
dl1.inv_rate                 0.0000 #
ld_text_base           0x00400000 #
ld_text_size               2166768 #
ld_data_base           0x10000000 #
```

Plain T

```
sim_num_refs               8043255 #
sim_elapsed_time                 2 #
sim_inst_rate          14620885.5000
il1.accesses              29241771 #
il1.hits                  21681208 #
il1.misses                 7560563 #
il1.replacements           7560531 #
il1.writebacks                   0 #
il1.invalidations                0 #
il1.miss_rate               0.2586 #
il1.repl_rate               0.2586 #
il1.wb_rate                 0.0000 #
il1.inv_rate                0.0000 #
dl1.accesses               8146520 #
dl1.hits                   6051951 #
dl1.misses                 2094569 #
dl1.replacements           2094537 #
dl1.writebacks              461897 #
dl1.invalidations                0 #
dl1.miss_rate               0.2571 #
dl1.repl_rate               0.2571 #
dl1.wb_rate                 0.0567 #
dl1.inv_rate                0.0000 #
ul2.accesses              10117029 #
ul2.hits                   9832183 #
ul2.misses                  284846 #
ul2.replacements            284590 #
ul2.writebacks               36822 #
ul2.invalidations                0 #
```

Plain T

◆ L1 cache size / L2 cache size

왼쪽은 cc1이고 오른쪽은 ijpeg으로 64 split cache size에 해당합니다.

```
sim: ** simulation statistics **
sim_num_insn              119392269
sim_num_refs               44164172
sim_elapsed_time                  7
sim_inst_rate          17056038.4286
il1.accesses              119392269
il1.hits                   80660601
il1.misses                 38731668
il1.replacements           38731604
il1.writebacks                    0
il1.invalidations                 0
il1.miss_rate                0.3244
il1.repl_rate                0.3244
il1.wb_rate                  0.0000
il1.inv_rate                 0.0000
dl1.accesses               44513362
dl1.hits                   36808786
dl1.misses                  7704576
dl1.replacements            7704512
dl1.writebacks              3428266
dl1.invalidations                 0
dl1.miss_rate                0.1731
dl1.repl_rate                0.1731
dl1.wb_rate                  0.0770
dl1.inv_rate                 0.0000
ld_text_base            0x00400000
ld_text_size               2166768
ld_data_base            0x10000000
```

```
sim: ** simulation statistics **
sim_num_insn               29241771
sim_num_refs                8043255
sim_elapsed_time                  2
sim_inst_rate          14620885.5000
il1.accesses               29241771
il1.hits                   21681208
il1.misses                  7560563
il1.replacements            7560531
il1.writebacks                    0
il1.invalidations                 0
il1.miss_rate                0.2586
il1.repl_rate                0.2586
il1.wb_rate                  0.0000
il1.inv_rate                 0.0000
dl1.accesses                8146520
dl1.hits                    6051951
dl1.misses                  2094569
dl1.replacements            2094537
dl1.writebacks               461897
dl1.invalidations                 0
dl1.miss_rate                0.2571
dl1.repl_rate                0.2571
dl1.wb_rate                  0.0567
dl1.inv_rate                 0.0000
ul2.accesses                10117029
ul2.hits                     9832183
ul2.misses                    284846
ul2.replacements              284590
ul2.writebacks                 36822
```

왼쪽은 cc1이고 오른쪽은 ijpeg으로 128 split cache size에 해당합니다.

```
sim: ** simulation statistics **
sim_num_insn              119392269 #
sim_num_refs               44164172 #
sim_elapsed_time                  7 #
sim_inst_rate          17056038.4286
il1.accesses              119392269 #
il1.hits                   91701427 #
il1.misses                 27690842 #
il1.replacements           27690586 #
il1.writebacks                    0 #
il1.invalidations                 0 #
il1.miss_rate                0.2319 #
il1.repl_rate                0.2319 #
il1.wb_rate                  0.0000 #
il1.inv_rate                 0.0000 #
dl1.accesses               44513362 #
dl1.hits                   41111420 #
dl1.misses                  3401942 #
dl1.replacements            3401686 #
dl1.writebacks              1331578 #
dl1.invalidations                 0 #
dl1.miss_rate                0.0764 #
dl1.repl_rate                0.0764 #
dl1.wb_rate                  0.0299 #
dl1.inv_rate                 0.0000 #
ld_text_base            0x00400000 #
ld_text_size               2166768 #
ld_data_base            0x10000000 #
ld_data_size                264644 #
in bytes
ld_stack_base           0x7fffc000 #
stack)
```

```
sim: ** simulation statistics **
sim_num_insn               29241771 #
sim_num_refs                8043255 #
sim_elapsed_time                  2 #
sim_inst_rate          14620885.5000
il1.accesses               29241771 #
il1.hits                   21681208 #
il1.misses                  7560563 #
il1.replacements            7560531 #
il1.writebacks                    0 #
il1.invalidations                 0 #
il1.miss_rate                0.2586 #
il1.repl_rate                0.2586 #
il1.wb_rate                  0.0000 #
il1.inv_rate                 0.0000 #
dl1.accesses                8146520 #
dl1.hits                    6051951 #
dl1.misses                  2094569 #
dl1.replacements            2094537 #
dl1.writebacks               461897 #
dl1.invalidations                 0 #
dl1.miss_rate                0.2571 #
dl1.repl_rate                0.2571 #
dl1.wb_rate                  0.0567 #
dl1.inv_rate                 0.0000 #
ul2.accesses                10117029 #
ul2.hits                     9832183 #
ul2.misses                    284846 #
ul2.replacements              284590 #
ul2.writebacks                 36822 #
```

왼쪽은 cc1이고 오른쪽은 ijpeg으로 512 split cache size에 해당합니다.

L1,L2cache로 hierarchy를 나누어 작성한 것입니다.

L1I/L1D/L2U	Inst.Miss rate	Data.Miss rate	Unified Cache Miss rate	AMAT
8/8/1024	0.4572	0.2571	0.2603	0.2751325
16/16/512	0.12494437	0.30213173	0.0281551	0.27183286
32/32/256	0.38219237	0.23280055	0.0281551	0.20026988
64/64/128	0.32440683	0.17308457	0.0281551	0.13519851
128/128/0	0.26866116	0.11305403		0.08496

cache사이즈가 클수록 miss rate, AMAT모두 낮아지는 것을 확인할 수 있었습니다.

◆ Large block size / Small block size

Block size가 커질수록 Miss rate와 AMAT 모두 감소하는 것을 알 수 있습니다.

```
sim: ** simulation statistics **
sim_num_insn              119392269 # total number of instructions executed
sim_num_refs               44164172 # total number of loads and stores executed
sim_elapsed_time                  6 # total simulation time in seconds
sim_inst_rate          19898711.5000 # simulation speed (in insts/sec)
il1.accesses              119392269 # total number of accesses
il1.hits                   99816822 # total number of hits
il1.misses                 19575447 # total number of misses
il1.replacements           19574935 # total number of replacements
il1.writebacks                    0 # total number of writebacks
il1.invalidations                 0 # total number of invalidations
il1.miss_rate                0.1640 # miss rate (i.e., misses/ref)
il1.repl_rate                0.1640 # replacement rate (i.e., repls/ref)
il1.wb_rate                  0.0000 # writeback rate (i.e., wrbks/ref)
il1.inv_rate                 0.0000 # invalidation rate (i.e., invs/ref)
ld_text_base              0x00400000 # program text (code) segment base
ld_text_size                 2166768 # program text (code) size in bytes
ld_data_base              0x10000000 # program initialized data segment base
ld_data_size                  264644 # program init'ed `.data' and uninit'ed `.bss' size
in bytes
ld_stack_base             0x7fffc000 # program stack segment base (highest address in
stack)
ld_stack_size                 16384 # program initial stack size
ld_prog_entry             0x00400140 # program entry point (initial PC)
ld_environ_base           0x7fff8000 # program environment base address address
ld_target_big_endian              0 # target executable endian-ness, non-zero if big
endian
mem.page_count                  806 # total number of pages allocated
mem.page_mem                   3224k # total size of memory pages allocated
mem.ptab_misses                 816 # total first level page table misses
mem.ptab_accesses          579990118 # total page table accesses
mem.ptab_miss_rate            0.0000 # first level page table miss rate
```

Block size	Unified cache Miss rate	AMAT
16	0.1640	1.22306084
64	0.0322	1.03430942
128	0.0136	1.01399238
256	0.0067	1.00679015
512	0.0042	1.00423521

◆ Direct-mapped / Set-Associative

associative way가 늘어날수록 miss-rate와 AMAT가 감소하는 것을 알 수 있으며,

Set의 개수가 늘어날수록 miss-rate와 AMAT가 감소하는 것을 알 수 있습니다.

```
sim: ** simulation statistics **
sim_num_insn              119392269 # total number of instructions executed
sim_num_refs               44164172 # total number of loads and stores executed
sim_elapsed_time                 7 # total simulation time in seconds
sim_inst_rate          17056038.4286 # simulation speed (in insts/sec)
il1.accesses              119392269 # total number of accesses
il1.hits                   80660601 # total number of hits
il1.misses                 38731668 # total number of misses
il1.replacements           38731604 # total number of replacements
il1.writebacks                    0 # total number of writebacks
il1.invalidations                 0 # total number of invalidations
il1.miss_rate                0.3244 # miss rate (i.e., misses/ref)
il1.repl_rate                0.3244 # replacement rate (i.e., repls/ref)
il1.wb_rate                  0.0000 # writeback rate (i.e., wrbks/ref)
il1.inv_rate                 0.0000 # invalidation rate (i.e., invs/ref)
ld_text_base              0x00400000 # program text (code) segment base
ld_text_size                 2166768 # program text (code) size in bytes
ld_data_base              0x10000000 # program initialized data segment base
ld_data_size                  264644 # program init'ed `.data' and uninit'ed `.bss' size
in bytes
ld_stack_base             0x7fffc000 # program stack segment base (highest address in
stack)
ld_stack_size                 16384 # program initial stack size
ld_prog_entry             0x00400140 # program entry point (initial PC)
ld_environ_base           0x7fff8000 # program environment base address address
ld_target_big_endian              0 # target executable endian-ness, non-zero if big
endian
mem.page_count                  806 # total number of pages allocated
mem.page_mem                   3224k # total size of memory pages allocated
mem.ptab_misses                 816 # total first level page table misses
mem.ptab_accesses          579990118 # total page table accesses
mem.ptab_miss_rate            0.0000 # first level page table miss rate
```

# of Sets	Split Cache Miss rate / AMAT							
	1-way		2-way		4-way		8-way	
64	0.3244	1.585	0.2640	1.410	0.2055	1.300	0.1348	1.174
128	0.2689	1.439	0.2041	1.298	0.1363	1.1941	0.2319	1.1739
256	0.2319	1.363	0.1506	1.199	0.0740	1.084	0.0328	1.0657
512	0.1640	1.223	0.0874	1.183	0.0351	1.114	0.0191	1.019
1024	0.1190	1.149	0.0523	1.058	0.0196	1.020	0.0084	1.017
2048	0.0929	1.084	0.0265	1.0299	0.0092	1.0094	0.0022	1.002

<문제점 및 고찰>

miss rate가 작으려면 여러 조건들에 해당할 때 miss rate와 block size를 키운다는 것은 special locality를 고려하는 것이라고 볼 수 있는데 이때 큰 cache가 좋음. associative는 way가 많아질수록 하드웨어 cost가 증가한다는 것을 알 수 있습니다. 작은 cache일 때 효과는 점점 줄어들고 하드웨어 리소스는 커지는 것을 알 수 있습니다. associativity가 작으면 LRU방식을, 크면 Random방식을 주로 사용합니다.

그리고 프로젝트 스펙에 나와있는 benchmark가 어떤 조건에서는 둘 중하나만 작성 되어있고 또 어떤 조건에서는 그에 대한 파일이 없다고 하여서 제대로 수행해 보지는 못했습니다.