

# AN\_PN7462AU\_IAR

## Integrating PN7462AU into IAR IDE

Rev. 0.5 — 29 June 2016

Application note

### Document information

Info	Content
<b>Keywords</b>	PN7462AU IAR Integration
<b>Abstract</b>	Integrating PN7462AU Into IAR + Demo of TypeA106 Reader Mode
<b>Author</b>	Purnank H Ghumalia



## Revision history

Rev	Date	Description
0.5	2016.06.29	Download to EEPROM Functionality Added
0.4	2016.03.09	PN7362AU Added
0.3	2015.12.14	Variants Added
0.2	2015.10.19	With FW Download
0.1	2015.10.12	Initial Revision

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## Contact information

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## 1. Introduction

This document covers steps needed to integrate and develop PN7462AU into IAR IDE.

This document does not cover differences between IAR IDE and LPCXpresso. This document is also not authored to explain the features of IAR IDE in depth. Kindly look at IAR IDE Manual for more information data.

### 1.1 Pre Requisites

It is assumed that the following items are available with the developer:

- **MOST Important:**
  - o JLink\_V510f (<https://www.segger.com/>) or above is required to be installed on the developer's PC.
  - o JLink DLLs for IAR should have been updated during the installation of JLink\_V510f or above.
- IAR IDE
- PN7462AU Source Package for Customer
- phExRfPCDA.zip
  - o Example with for PCD Type A 106
- LPC Link 2 / Seggar J-Link Debugger
  - o The debugger
- LPCScript (See <https://www.lpcware.com/lpcscript>)
  - o Optional: To emulate LPC Link 2 as J-Link
- Administrative Privileges
  - o To update IAR with PN7462AU Configuration

### 1.2 Important Topics

- Delete files in C:\Program Files (x86)\IAR Systems\Embedded Workbench 7.4\arm\config\devices\NXP\PN73xxxx and C:\Program Files (x86)\IAR Systems\Embedded Workbench 7.4\arm\config\devices\NXP\PN74xxxx. These files are and should no longer be referred to. IDE Refers to Files in C:\Program Files (x86)\IAR Systems\Embedded Workbench 7.4\arm\config\devices\NXP\Other\PN73xxxx and C:\Program Files (x86)\IAR Systems\Embedded Workbench 7.4\arm\config\devices\NXP\Other\PN74xxxx
- As per the convention followed in all the corresponding FW Examples, the Debug build may do Printf(s)/logging on debug console, and Release build would never do/employ to Printf(s)/logging on debug console. When Printf(s) are used, debugger is required to be connected to the board. Without the debugger, firmware would not continue execution whenever a Printf is connected.

- Ensure that For “Debugger → J-Link/J-Trace → Setup” Ensure “Halt after bootloader” is selected (See Fig 7 on page 11)

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## 2. Configure LPC Link 2

If you already have Seggar J-Link, you can skip this section.

Follow the steps in “LPCScript User Guide”.

In short, the steps are:

- Open(Disconnect) JP1 & Close(connect) JP2
- Connect LPC Link 2 to USB Interface
- Run `<LPCScript Install Dir>\scripts\program_JLINK`
- Disconnect USB
- Close JP1 & Open JP2
- Connect USB to LPC Link 2. Now the LPC Link 2 should behave as J-Link.

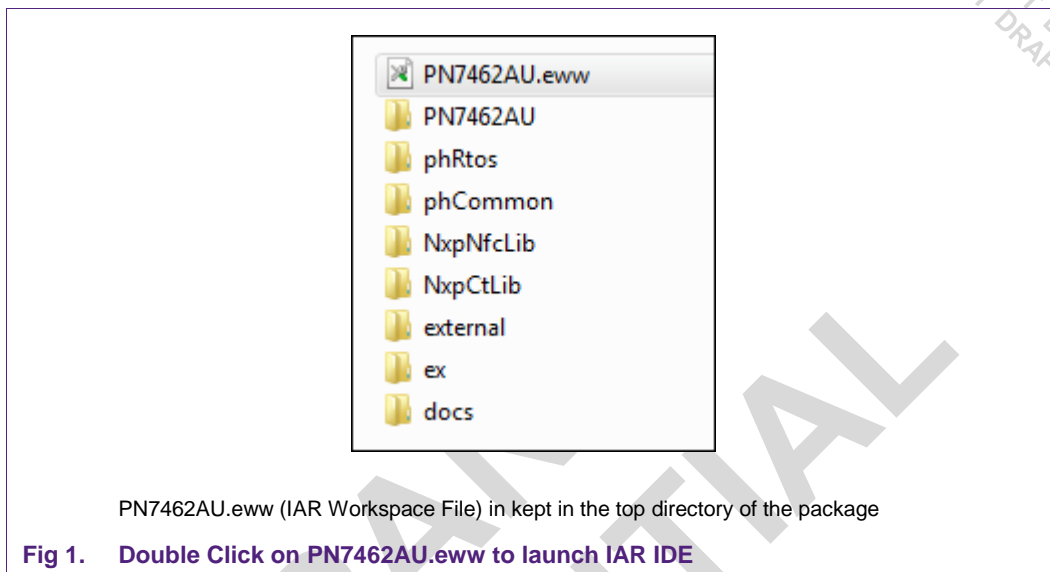
In case of any complication, please refer to “LPCScript User Guide” and “LPC-Link2 Debug Probe Firmware Programming”

### 3. Setting Up IAR for PN7462

The following files/patch is required to be applied/added to IAR IDE in "C:\Program Files (x86)\IAR Systems\Embedded Workbench 7.4\arm\config"

- debugger\NXP\PN7360AU-C3-00.ddf
- debugger\NXP\PN7362AU-C3-00.ddf
- debugger\NXP\PN73xxAU.svd
- debugger\NXP\PN7462AU-C3-00.ddf
- debugger\NXP\PN74xxAU.svd
- debugger\NXP\PN7xxxxx.ProbeScript
- devices\NXP\Other\PN73xxxx\PN7360AU-C3-00.i79
- devices\NXP\Other\PN73xxxx\PN7360AU-C3-00.menu
- devices\NXP\Other\PN73xxxx\PN7362AU-C3-00.i79
- devices\NXP\Other\PN73xxxx\PN7362AU-C3-00.menu
- devices\NXP\Other\PN74xxxx\PN7462AU-C3-00.i79
- devices\NXP\Other\PN74xxxx\PN7462AU-C3-00.menu
- flashloader\NXP\EepromPN7xxxxx\_3\_5k.flash
- flashloader\NXP\FlashPN7xxxxx.out
- flashloader\NXP\FlashPN7xxxxx\_158k.board
- flashloader\NXP\FlashPN7xxxxx\_158k.flash
- flashloader\NXP\FlashPN7xxxxx\_80k.board
- flashloader\NXP\FlashPN7xxxxx\_80k.flash
- linker\NXP\PN7xxxxx\_158k.icf
- linker\NXP\PN7xxxxx\_80k.icf

## 4. Importing / Building Project



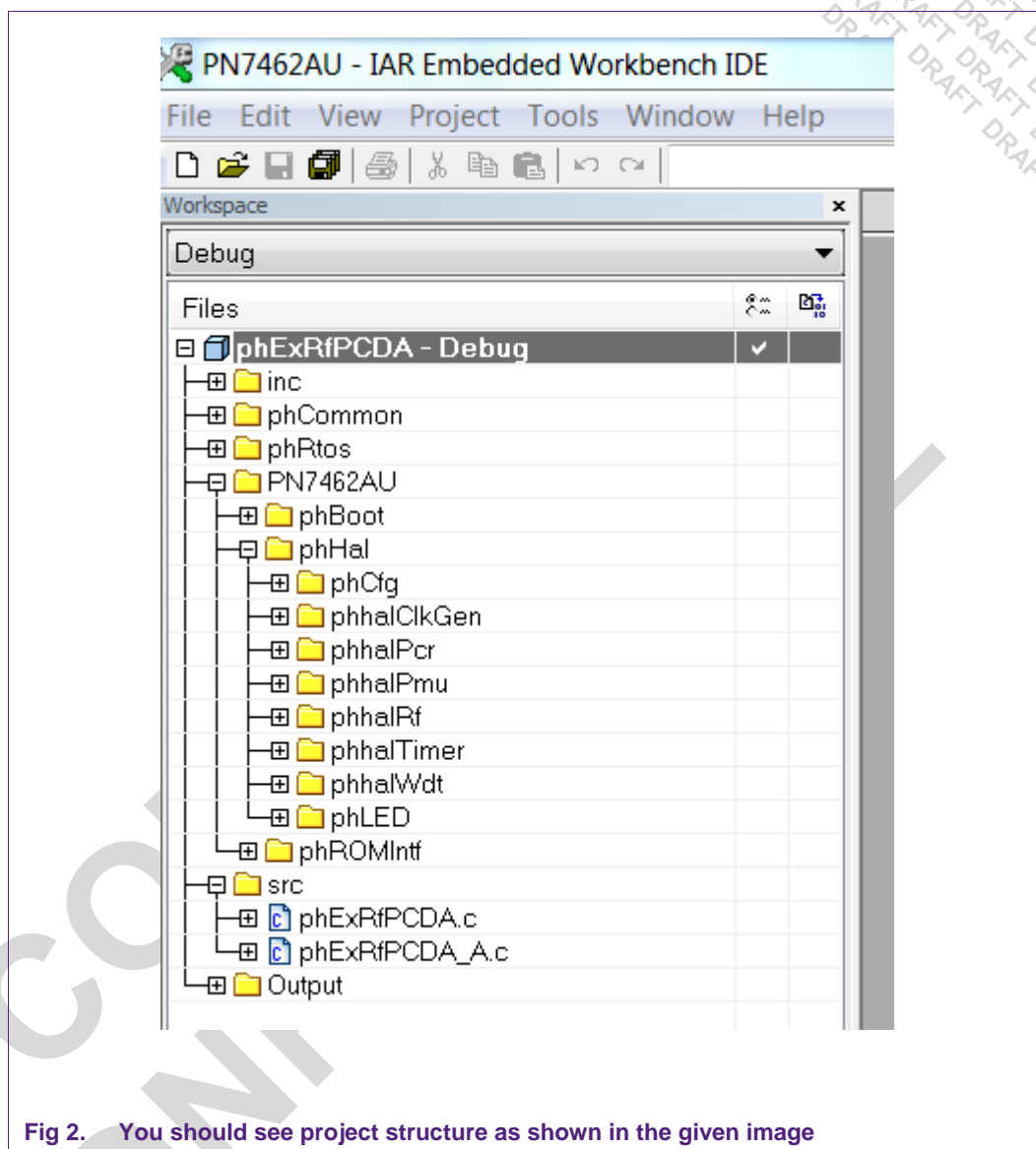
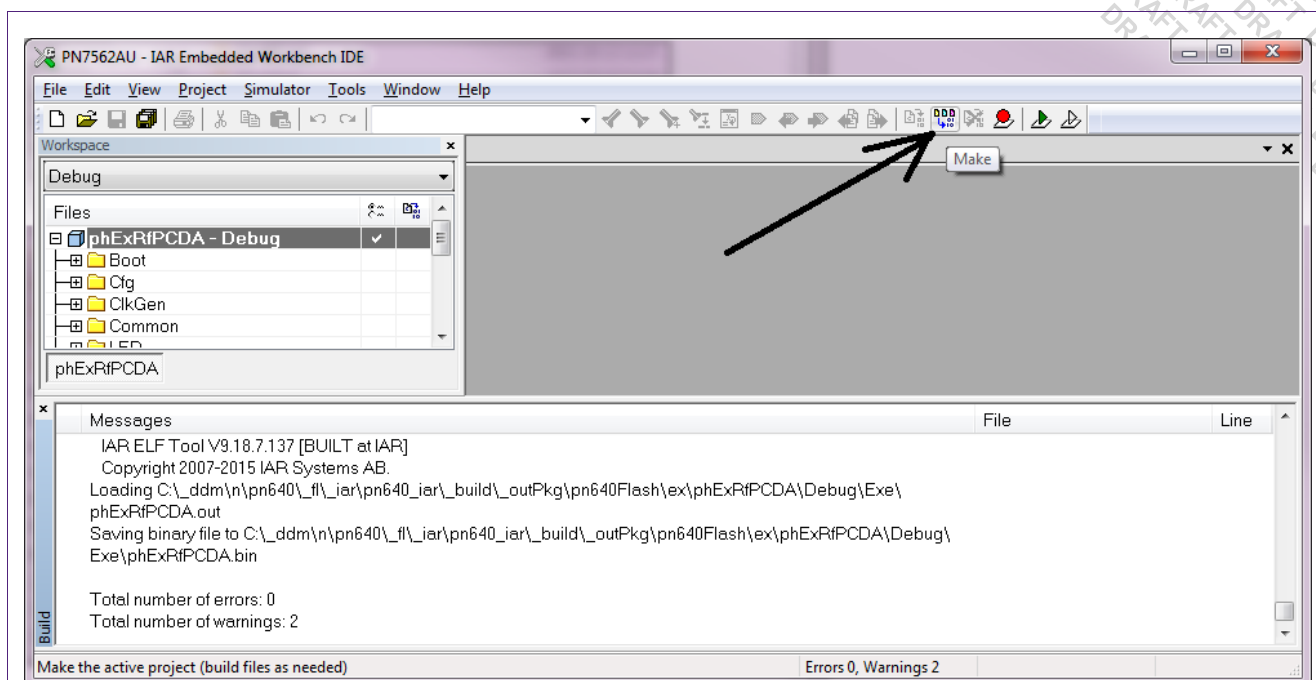


Fig 2. You should see project structure as shown in the given image



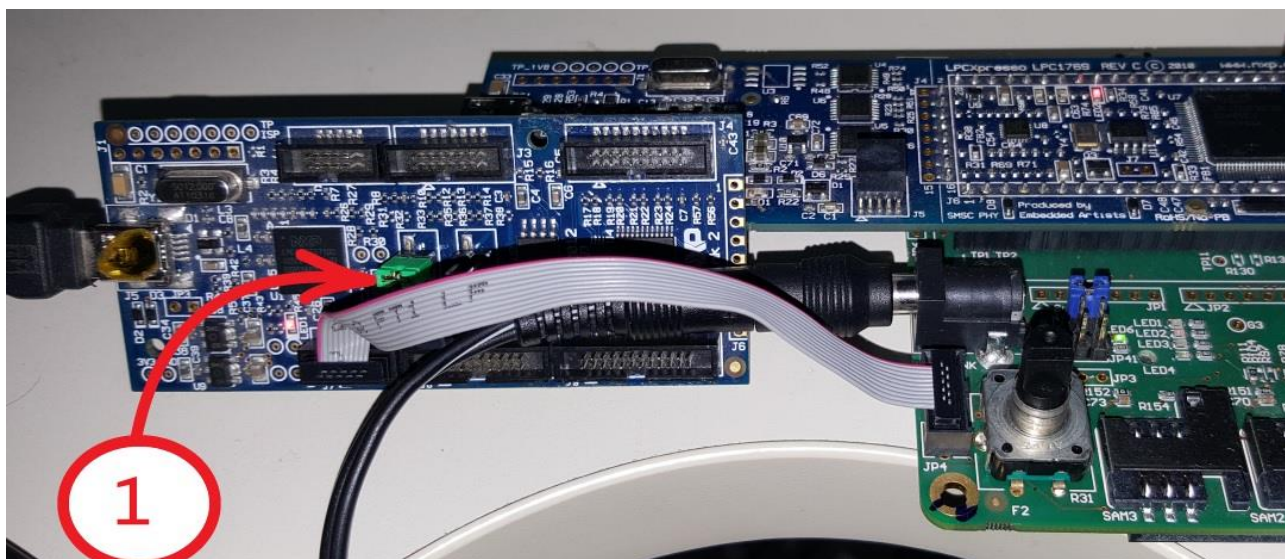


- (1) Make Button
- (2) "F7" Will build Current Configuration (Debug in this case)
- (3) "F8" Will trigger Batch Build (Debug + Release)
- (4) ^D will build and download the image

**Fig 3. Build the Project**

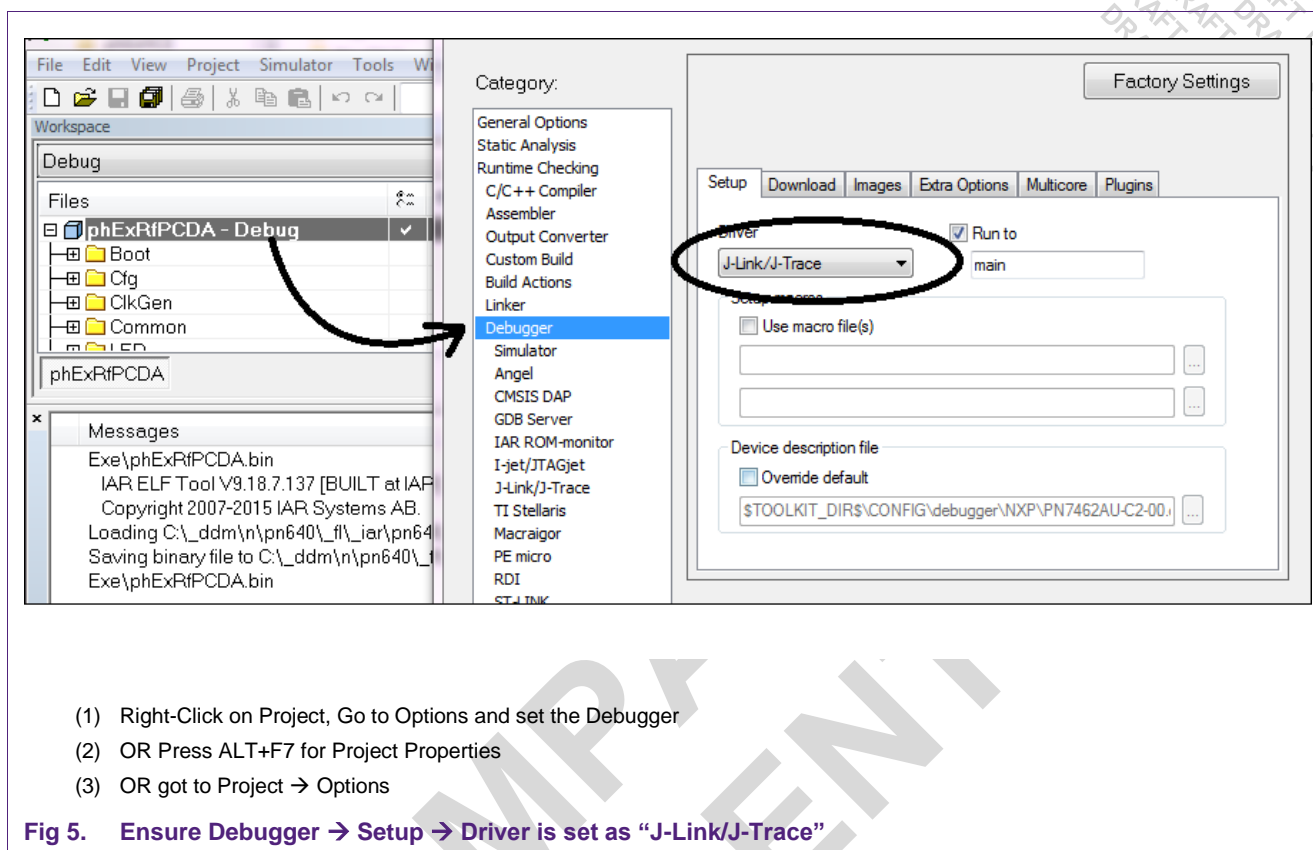
## 5. Debugging the Project

Ensure, LPCLink2-Configured as J-Link, or J-Link is connected to the Debugger.

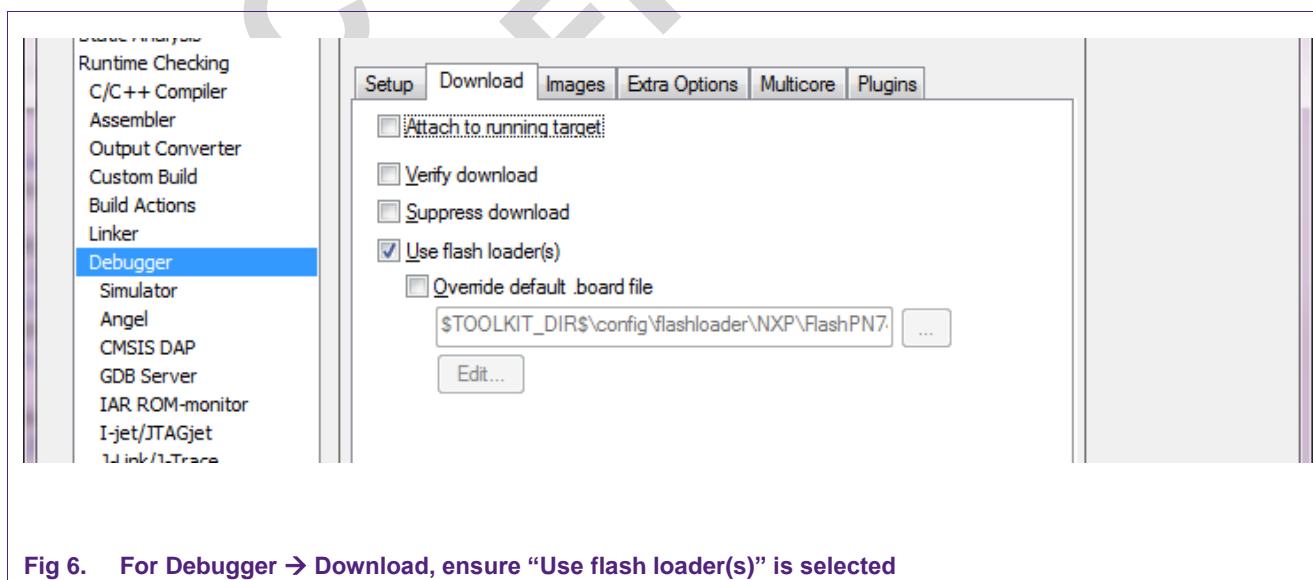


(1) When JP1 is connected and J-Link Firmware is downloaded to LPC Link 2, it would behave as a J-Link

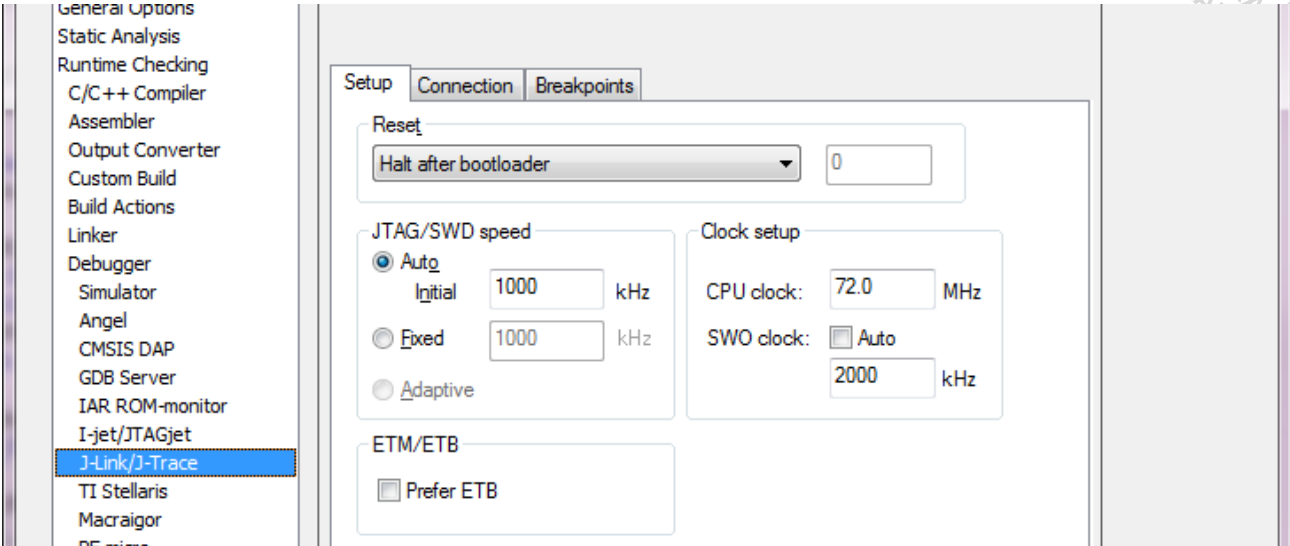
**Fig 4. Physical connection of LPCLink2 Debugger**



**Fig 5. Ensure Debugger → Setup → Driver is set as “J-Link/J-Trace”**



**Fig 6. For Debugger → Download, ensure “Use flash loader(s)” is selected**



(1) Ensure “Halt after bootloader” is selected for J-Link/J-Trace Configuration

Fig 7. For “Debugger → J-Link/J-Trace → Setup” Ensure “Halt after bootloader” is selected

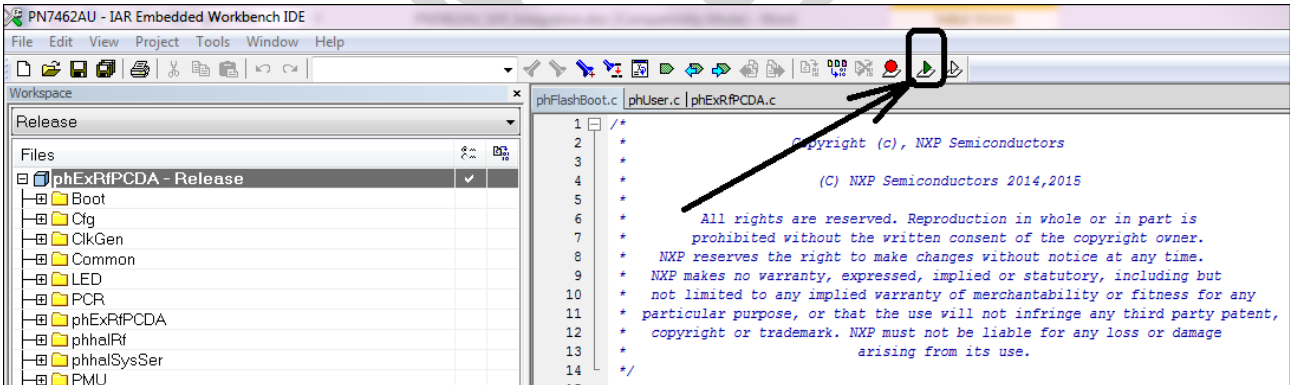


Fig 8. Press “Download and Debug” to Build + Download the Firmware

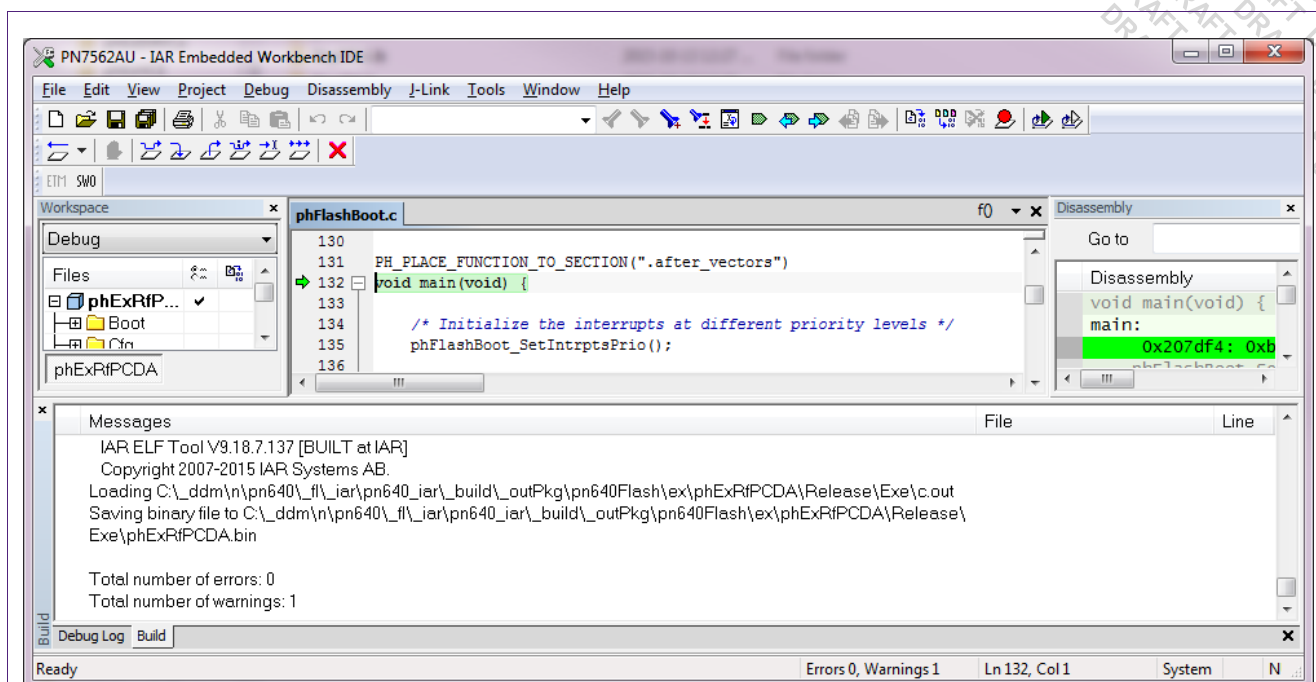
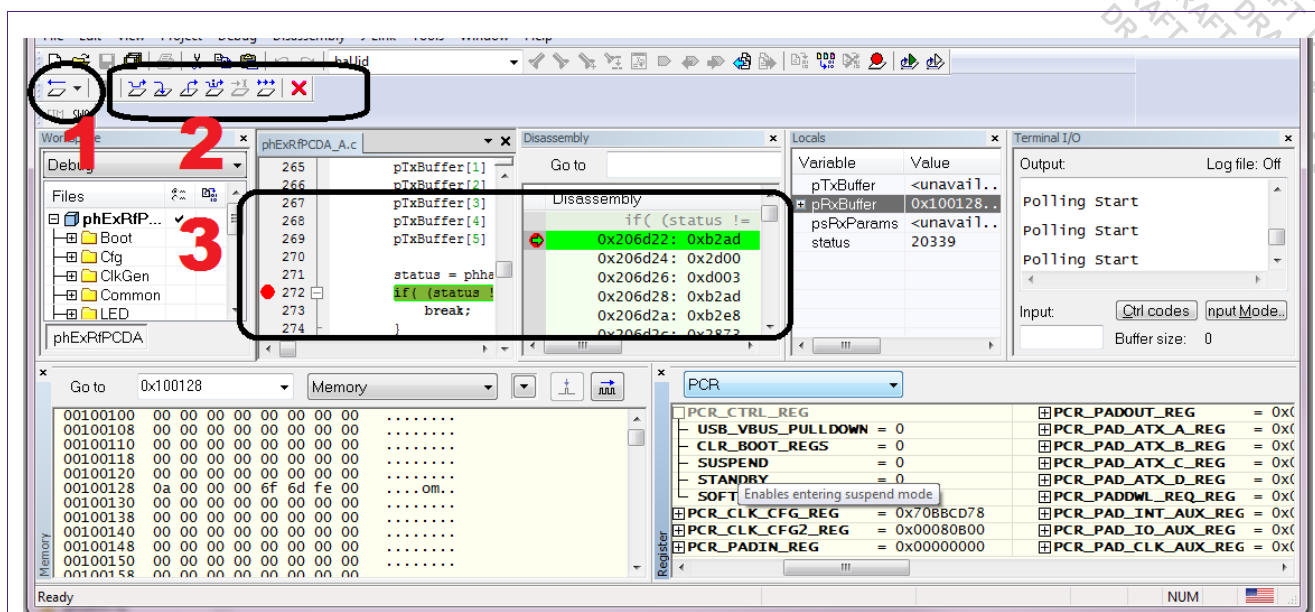


Fig 9. Debug View



- (1) Reset
- (2) Step Into / Step Out / etc.
- (3) Breakpoints

Other Aspects shown in the image:

- o Local Variables
- o Terminal IO / Debugger Printfs
- o Memory View
- o Register view (In the image, PCR Registers, with Documentation)

**Fig 10. Debugger View**

## 6. References

Table 1. Referenced Documents

File	Location
LPCScript User Guide	C:\nxp\LPCScript\docs
LPC-Link2 Debug Probe Firmware Programming	C:\nxp\LPCScript\docs
UM10883 PN7462AU Customer board_AXIS.pdf	Contact CAS



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