AN3703

Integrating PN7462AU into IAR IDE

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Document information

Info	Content
Keywords	PN7462AU IAR Integration
Abstract	Integrating PN7462AU Into IAR + Demo of TypeA106 Reader Mode
Author	Purnank H Ghumalia

Revision history

Rev	Date	Description
0.4	20160309	PN7362AU Added
0.3	20151214	Variants Added
0.2	20151019	With FW Download
0.1	20151012	Initial Revision

Contact information

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1. Introduction

This document covers steps needed to integrate and developer PN7462AU into IAR IDE.

This document does not cover differences between IAR IDE and LPCXpresso. This document is also not authored to explain the features of IAR IDE in depth. Kindly look at IAR IDE Manual for more information data.

1.1 Pre Requisites

It is assumed that the following items are available with the developer:

- **MOST Important:**
    - JLink_V510f (https://www.segger.com/) or above is required to be installed on the developer's PC.
    - JLink DLLs for IAR should have been updated during the installation of JLink_V510f or above.
- IAR IDE
- PN7462AU Source Package for Customer
- phExRfPCDA.zip
    - Example with for PCD Type A 106
- LPC Link 2 / Seggar J-Link Debugger
    - The debugger
- LPCScrypt (See https://www.lpcware.com/lpcscrypt)
    - Optional: To emulate LPC Link 2 as J-Link
- Administrative Privileges
    - To update IAR with PN7462AU Configuration

1.2 Important Topics

- As per the convention followed in all the corresponding FW Examples, the Debug build may do Printf(s)/logging on debug console, and Release build would never do/employ to Printf(s)/logging on debug console. When Printf(s) are used, debugger is required to be connected to the board. Without the debugger, firmware would not continue execution whenever a Printf is connected.
- Ensure that For "Debugger → J-Link/J-Trace → Setup" Ensure "Halt after bootloader" is selected (See Fig 7 on page 10)

2. Configure LPC Link 2

If you already have Seggar J-Link, you can skip this section.

Follow the steps in “LPCScrypt User Guide”.

In short, the steps are:

- Open(Disconnect) JP1 & Close(connect) JP2
- Connect LPC Link 2 to USB Interface
- Run `<LPCScrypt Install Dir>\scripts\program_JLINK`
- Disconnect USB
- Close JP1 & Open JP2
- Connect USB to LPC Link 2. Now the LPC Link 2 should behave as J-Link.

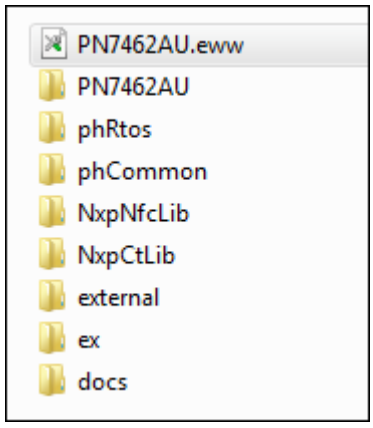
In case of any complication, please refer to “LPCScrypt User Guide” and “LPC-Link2 Debug Probe Firmware Programming”

3. Setting Up IAR for PN7462

The following files/patch is required to be applied/added to IAR IDE in "C:\Program Files (x86)\IAR Systems\Embedded Workbench 7.3\arm\config"

- config\debugger\NXP\PN7360AU-C3-00.ddf
- config\debugger\NXP\PN7362AU-C3-00.ddf
- config\debugger\NXP\PN73xxAU.svd
- config\debugger\NXP\PN7462AU-C3-00.ddf
- config\debugger\NXP\PN74xxAU.svd
- config\debugger\NXP\PN7xxxxx.ProbeScript
- config\devices\NXP\PN73xxxx\PN7360AU-C3-00.i79
- config\devices\NXP\PN73xxxx\PN7360AU-C3-00.menu
- config\devices\NXP\PN73xxxx\PN7362AU-C3-00.i79
- config\devices\NXP\PN73xxxx\PN7362AU-C3-00.menu
- config\devices\NXP\PN74xxxx\PN7462AU-C3-00.i79
- config\devices\NXP\PN74xxxx\PN7462AU-C3-00.menu
- config\flashloader\NXP\FlashPN7xxxxx.out
- config\flashloader\NXP\FlashPN7xxxxx_158k.board
- config\flashloader\NXP\FlashPN7xxxxx_158k.flash
- config\flashloader\NXP\FlashPN7xxxxx_80k.board
- config\flashloader\NXP\FlashPN7xxxxx_80k.flash
- config\linker\NXP\PN7xxxxx_158k.icf
- config\linker\NXP\PN7xxxxx_80k.icf

4. Importing / Building Project



PN7462AU.eww (IAR Workspace File) in kept in the top directory of the package

Fig 1. Double Click on PN7462AU.eww to launch IAR IDE

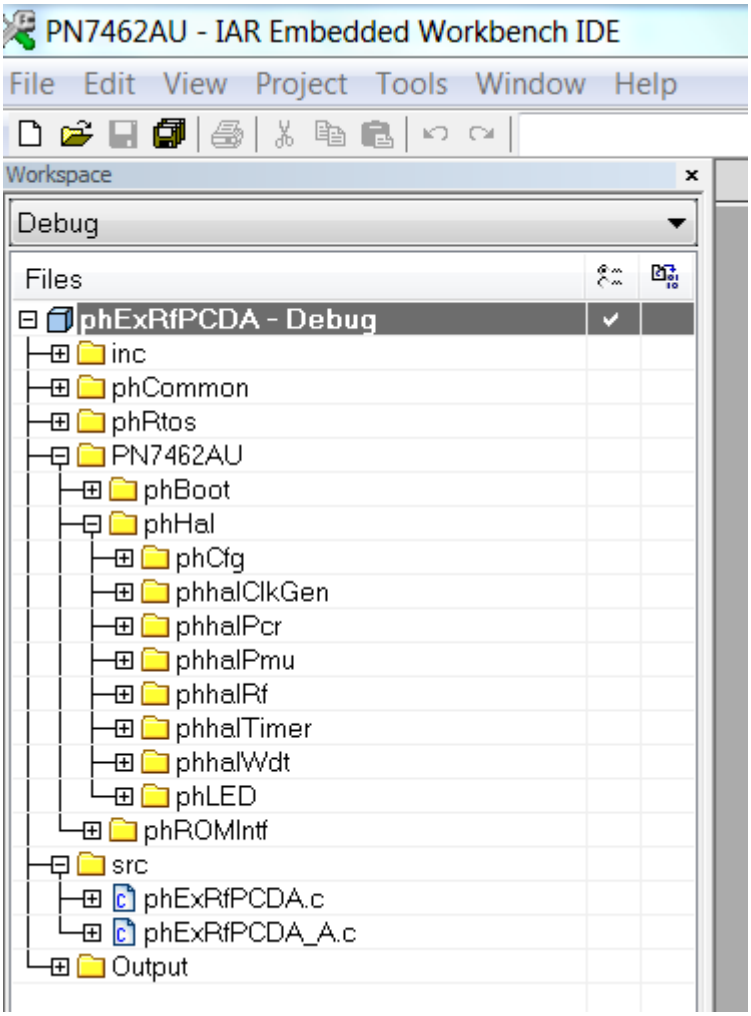
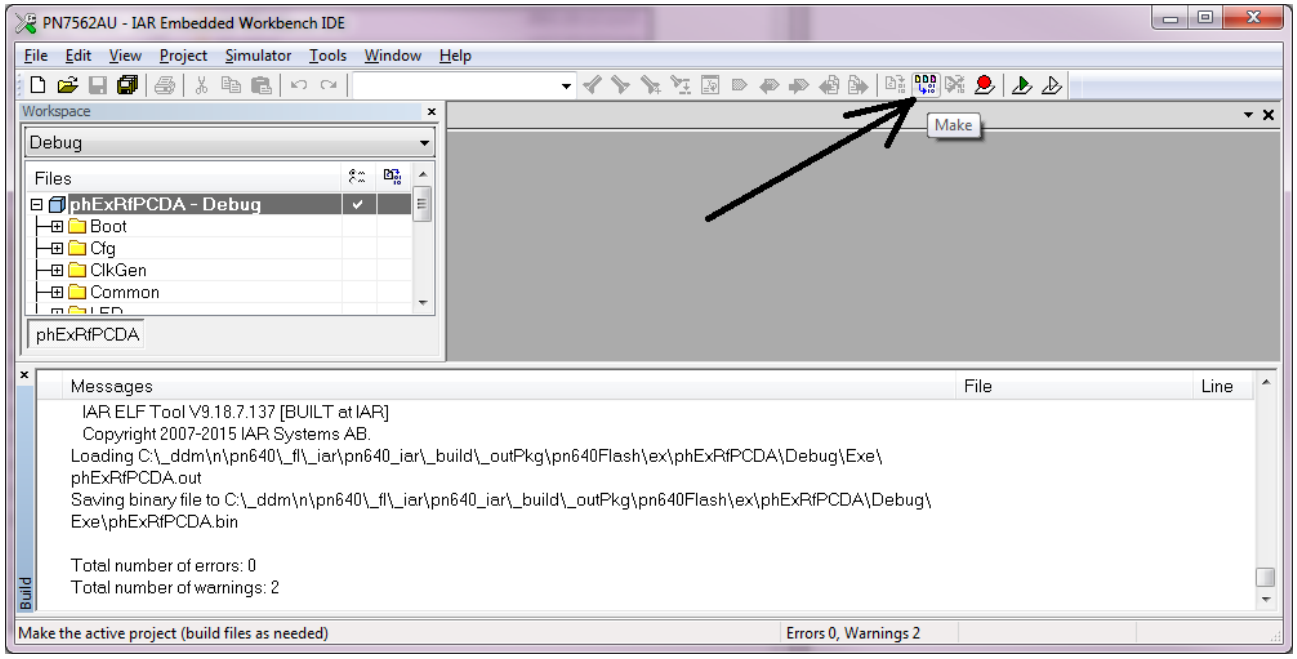


Fig 2. You should see project structure as shown in the given image



(1) Make Button

(2) “F7” Will build Current Configuration (Debug in this case)

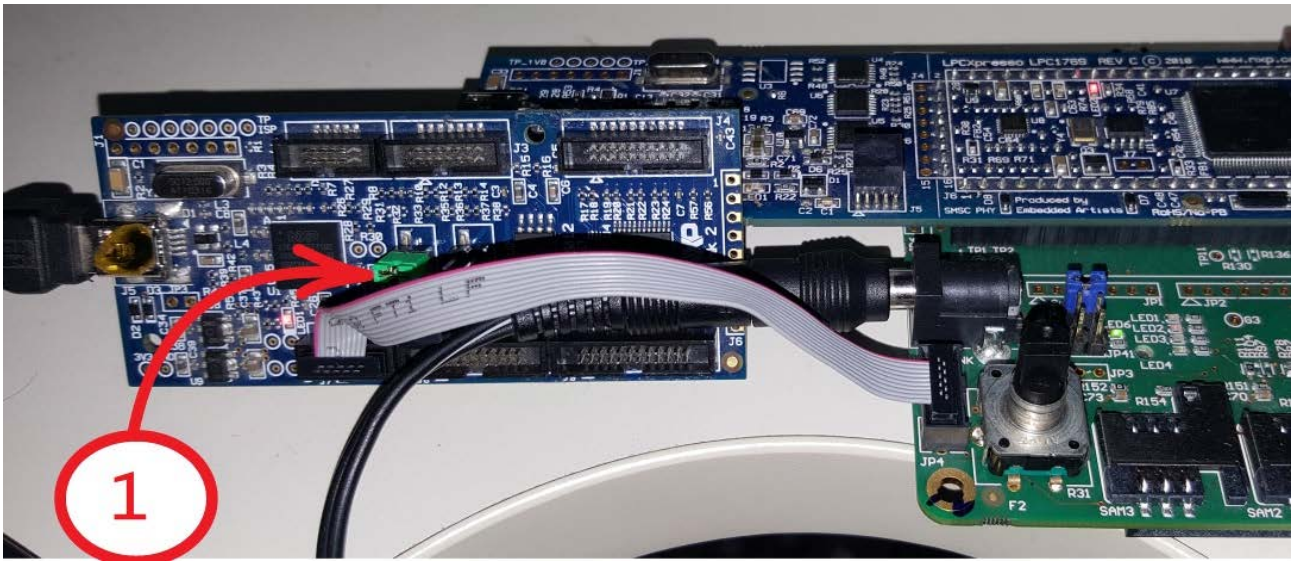
(3) “F8” Will trigger Batch Build (Debug + Release)

(4) ^D will build and download the image

Fig 3. Build the Project

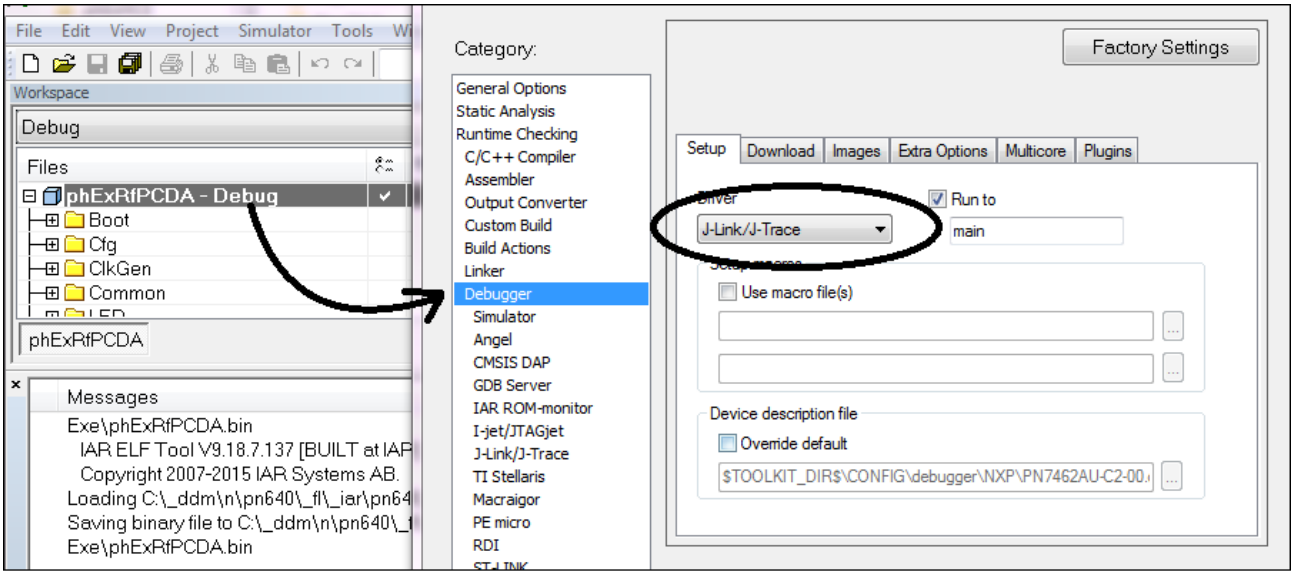
5. Debugging the Project

Ensure, LPCLink2-Configured as J-Link, or J-Link is connected to the Debugger.



(1) When JP1 is connected and J-Link Firmware is downloaded to LPC Link 2, it would behave as a J-Link

Fig 4. Physical connection of LPCLink2 Debugger



(1) Right-Click on Project, Go to Options and set the Debugger

(2) OR Press ALT+F7 for Project Properties

(3) OR got to Project → Options

Fig 5. Ensure Debugger → Setup → Driver is set as "J-Link/J-Trace"

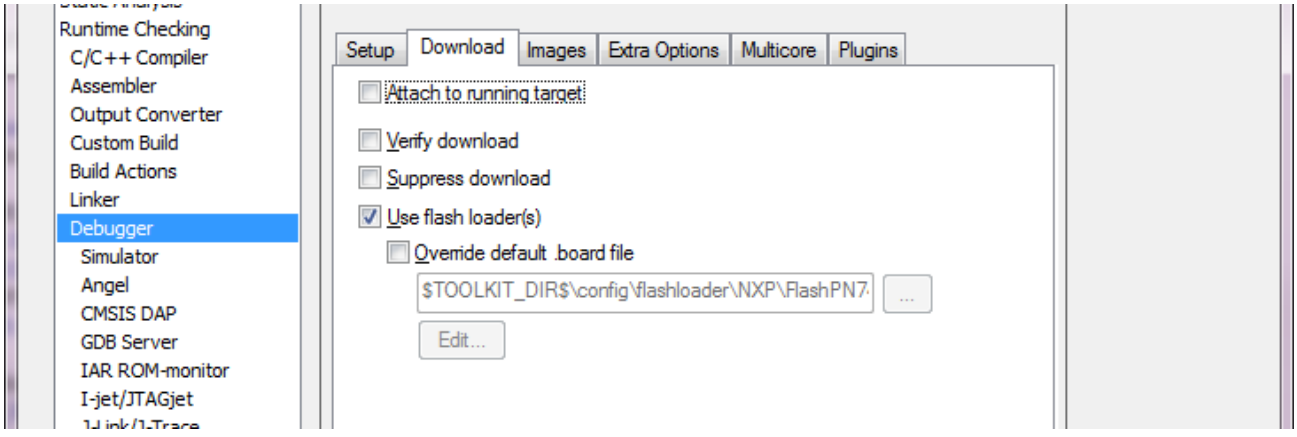
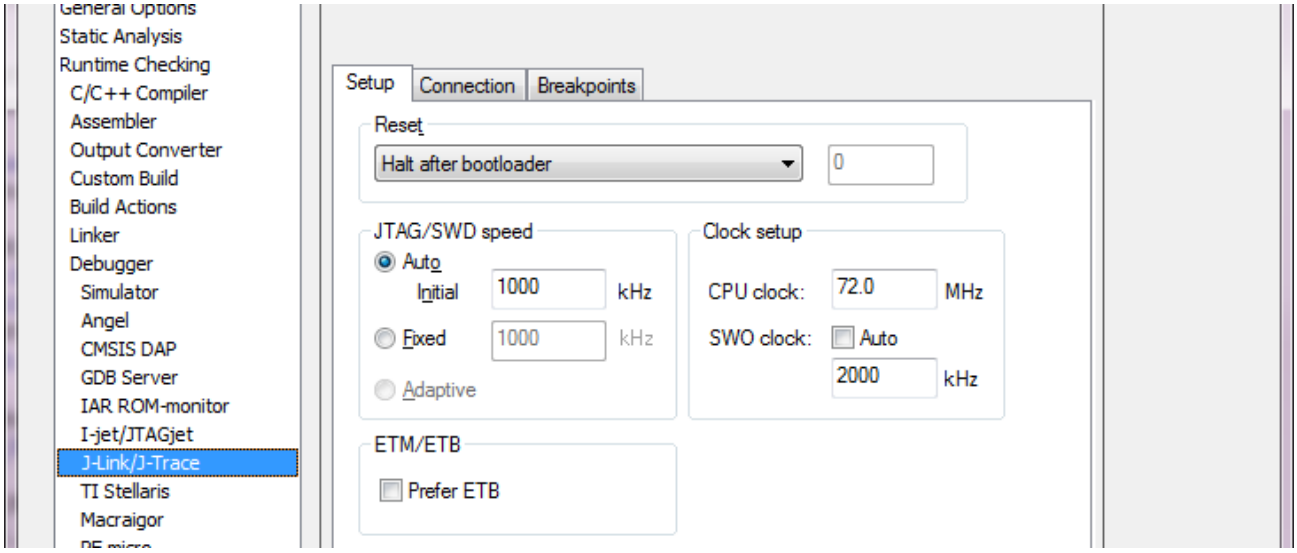


Fig 6. For Debugger → Download, ensure "Use flash loader(s)" is selected



(1) Ensure “Halt after bootloader” is selected for J-Link/J-Trace Configuration

Fig 7. For “Debugger → J-Link/J-Trace → Setup” Ensure “Halt after bootloader” is selected

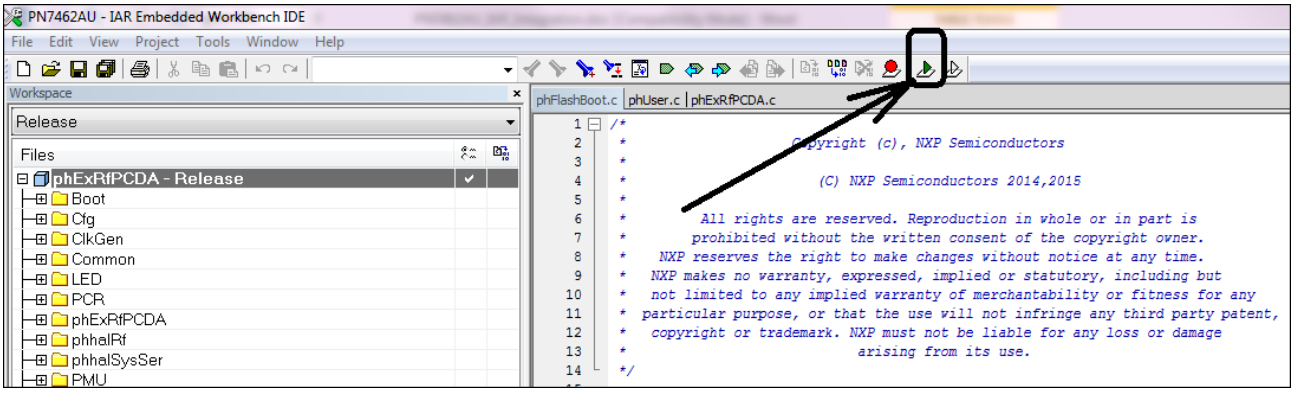


Fig 8. Press “Download and Debug” to Build + Download the Firmware

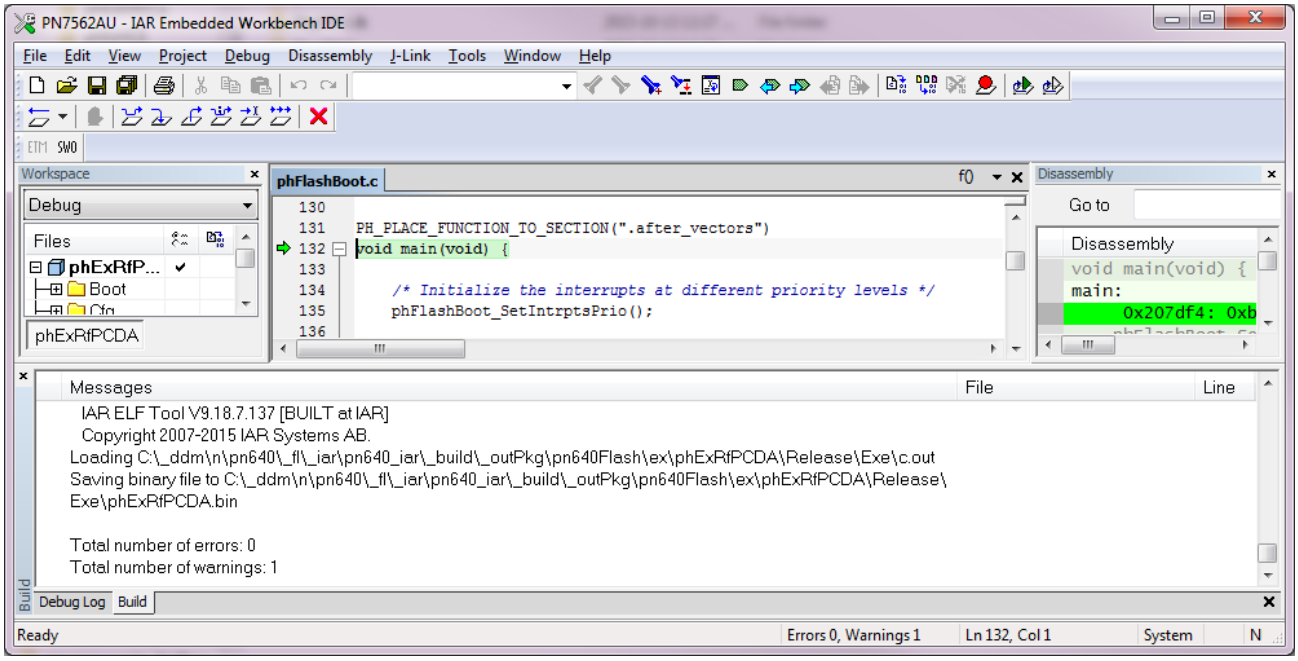
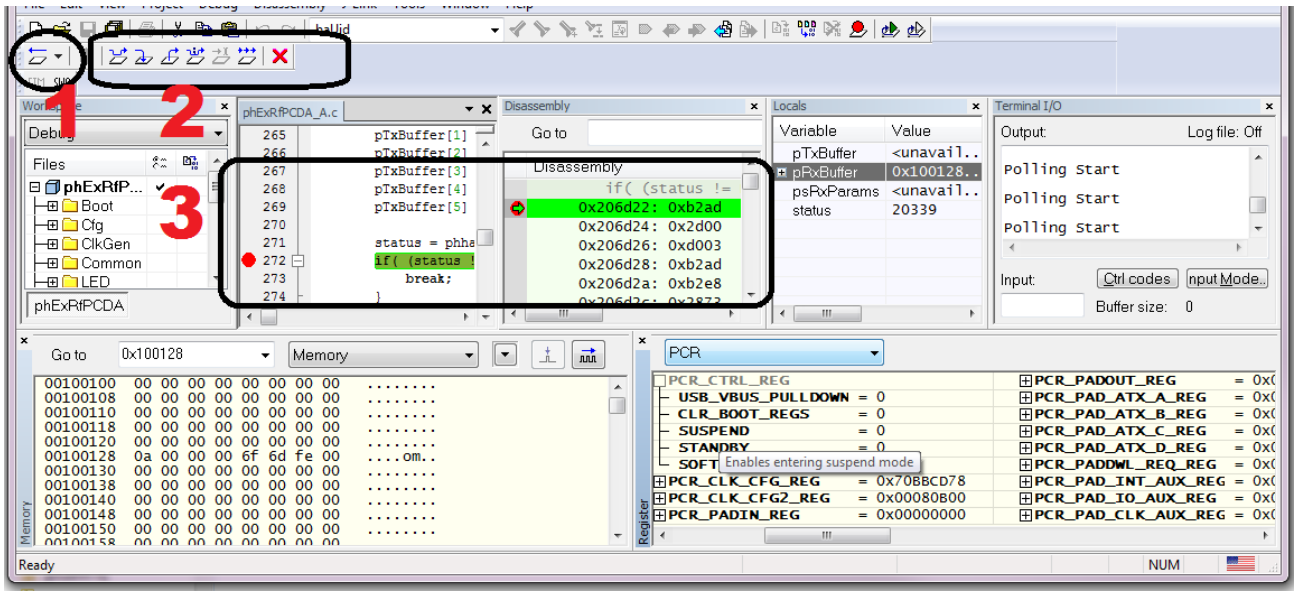


Fig 9. Debug View



(1) Reset

(2) Step Into / Step Out / etc.

(3) Breakpoints

Other Aspects shown in the image:

- Local Variables
- Terminal IO / Debugger Printfs
- Memory View
- Register view (In the image, PCR Registers, with Documentation)

Fig 10. Debugger View

6. References

Table 1. Referenced Documents

File	Location
LPCScrypt User Guide	C:\nxp\LPCScrypt\docs
LPC-Link2 Debug Probe Firmware Programming	C:\nxp\LPCScrypt\docs
UM10883 PN7462AU Customer board_AXIS.pdf	Contact CAS

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