AN11868

PN74xxxx and PN73xxxx - Integration with SWD based downloaders

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Application note
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Document information

Info	Content
Keywords	PN7462AU, PN74xxxx, PN73xxxx, SWD downloaders integration
Abstract	❑ This document outlines steps needed for integration of SWD based programmers with the PN74xxxx and PN73xxxx Family ❑ PN74xxxx & PN73xxxx are Cortex M0 based NFC controllers with SWD Interface ❑ This document also covers the variants of the PN74xxxx and PN73xxxx Family

Revision history

Rev	Date	Description
1.0	20160803	First release

Contact information

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1. Introduction

This document outlines steps needed for integration of SWD Based programmers with the PN74xxxx and PN73xxxx Family

PN74xxxx & PN73xxxx are Cortex M0 based NFC and Smart Card* controller with SWD Interface. See [PN7462AUDataSheet] for more information.

This document also covers the derivatives of the PN74xxxx and PN73xxxx Family.

Note: [*] PN73xxxx family of derivatives do not support Contact Interface.

1.1 Applicable Derivatives

This document is applicable to the following derivatives

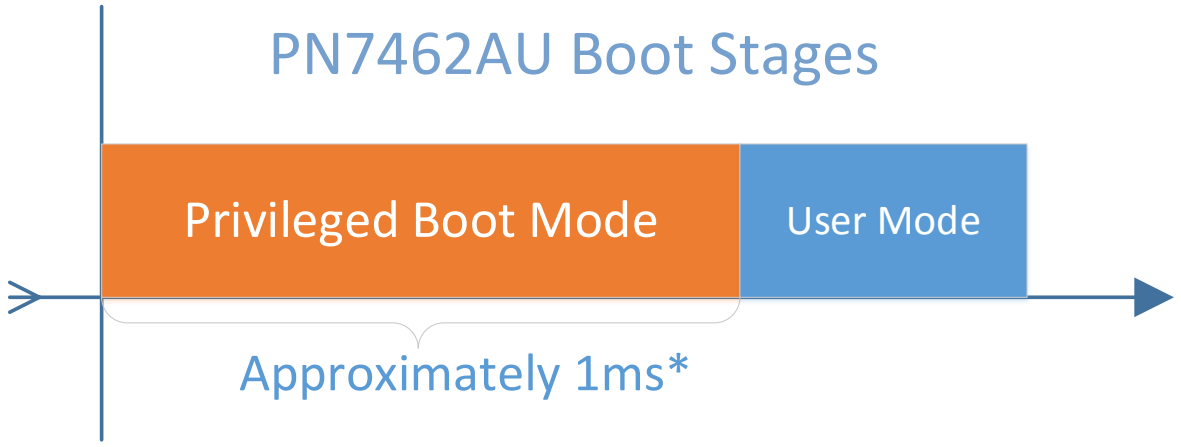
Table 1. Derivatives applicable for this document

Product Family	IC / Variant Name	Flash Size	EEPROM Size
PN74xxxx	PN7462AU-C3-00	158k	3.5k
PN73xxxx	PN7362AU-C3-00	158k	3.5k
	PN7360AU-C3-00	80k	3.5k

2. PN74xxxx & PN73xxxx – Boot Flow

PN74xxxx & PN73xxxx family of ICs have the following

- During “Privileged Boot Mode”, access to SWD is forbidden.
- Any access will reset the chip. (And, would keep on resetting the CHIP)
- Vector Catch Reset cannot be used, because that will halt IC in “Privileged Boot Mode” and eventually reset the CHIP, thereby disconnecting the Debugger
- See 2.1 How to halt debugger after Reset below



(1) The boot up time is approximately 1ms and the time would vary bases on various other parameters which are not described in this document.

Fig 1. Boot flow for PN74xxxx & PN73xxxx and its family of ICs

2.1 How to halt debugger after Reset

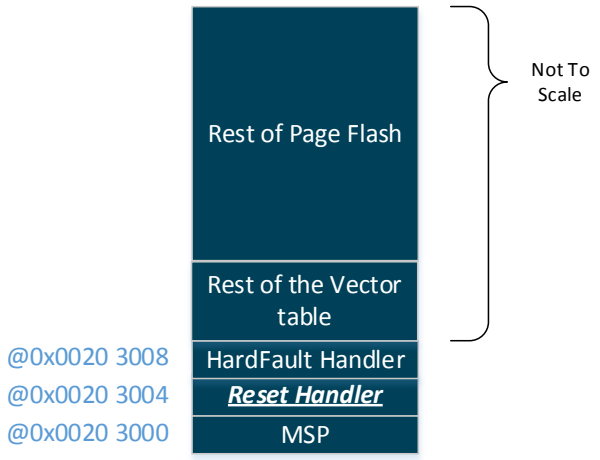


Fig 2. Reference vector table + Flash region for PN7462AU

- Read "`ResetHandler` address" from Vector table (`@0x203004`)
- Set initial breakpoint at `ResetHandler`
  - Address of `ResetHandler` read from `0x203004`. Note: Breakpoint is not set at `0x203004`. Breakpoint is set at address pointed by `0x203004`
- Turn off reset vector catch
  - clear "`bit [0], VC_CORERESET`, of the Debug Exception and Monitor Control
- Reset the part

3. Memory Map

- PN74xxxx & PN73xxxx Family has many derivatives with different IP Features and User accessible PageFlash Region.
- For the perspective of Programming over SWD, the only differentiating aspects is the PageFlash Size
- Table below demonstrate the Memory Map for different derivatives
- Product Derivatives to be support for SWD Based download are
  - PN7462AU-C3-00
  - PN7362AU-C3-00
  - PN7360AU-C3-00

Table 2. Derivatives, Memory Sizes and addresses

Variant Name	Variant Size	Memory Name	Start	Size(Hex)	Size(Int)	End
<ALL>	<ALL>	RAM	0x100020	0x2EE0	12000	0x102EFF
<ALL>	<ALL>	EEPROM	0x201200	0x0E00	3584	0x201FFF
PN7462AU-C3-00	158k	Flash	0x203000	0x27800	161792	0x22A7FF
PN7362AU-C3-00	158k	Flash	0x203000	0x27800	161792	0x22A7FF
PN7360AU-C3-00	80k	Flash	0x203000	0x14000	81920	0x216FFF

4. Pinning Diagram and Packaging Information

- See [UM10858] for Pinning Information and Packaging Information
- Pinning is same for all the derivatives

5. Reference implementation for programming

C Source code is provided with this package. Tool vendor can use the APIs provided to program the EEPROM or Flash region of the IP. For the most basic implementation, appropriate calls to these three APIs is enough. The APIs in SW Package provided together with this package is appropriately documented for advanced use cases.

```
void phCommon_WaitInit (E_COMMON_CPUSPEED_20MHZ);
phStatus_t phRomHal_Flash_WriteBuffer(
    uint8_t  *pBuffer, /**< [in,read] pointer to buffer containing data to be written to PAGEFLASH */
    uint8_t  *pFlash,  /**< [in,write] Valid address of a byte in the PAGEFLASH. Given address must be 4byte aligned. */
    uint32_t  bytes_to_write); /**< [in] number of bytes to be written. Must be Non zero, multiple of 4. */
phStatus_t phRomHal_Eeprom_WriteBuffer(
    uint8_t  *pBuffer, /**< [in,read] pointer to buffer containing data to be written to EEPROM */
    uint8_t  *pEeprom, /**< [in,write] pointer to EEPROM buffer where data will be copied */
    uint16_t  bytes_to_write); /**< [in] number of bytes to be written */
```

Fig 3. Basic APIs for programming EEPROM and Flash

5.1 Reference Integration

This flow chart shows simple integration/usage of NXP APIs for flash programmers

Note: The flow is over simplified for the sake of understanding

If needed, more APIs are also provided within the NXP's reference implementation

Please see "[flashcode.zip]"

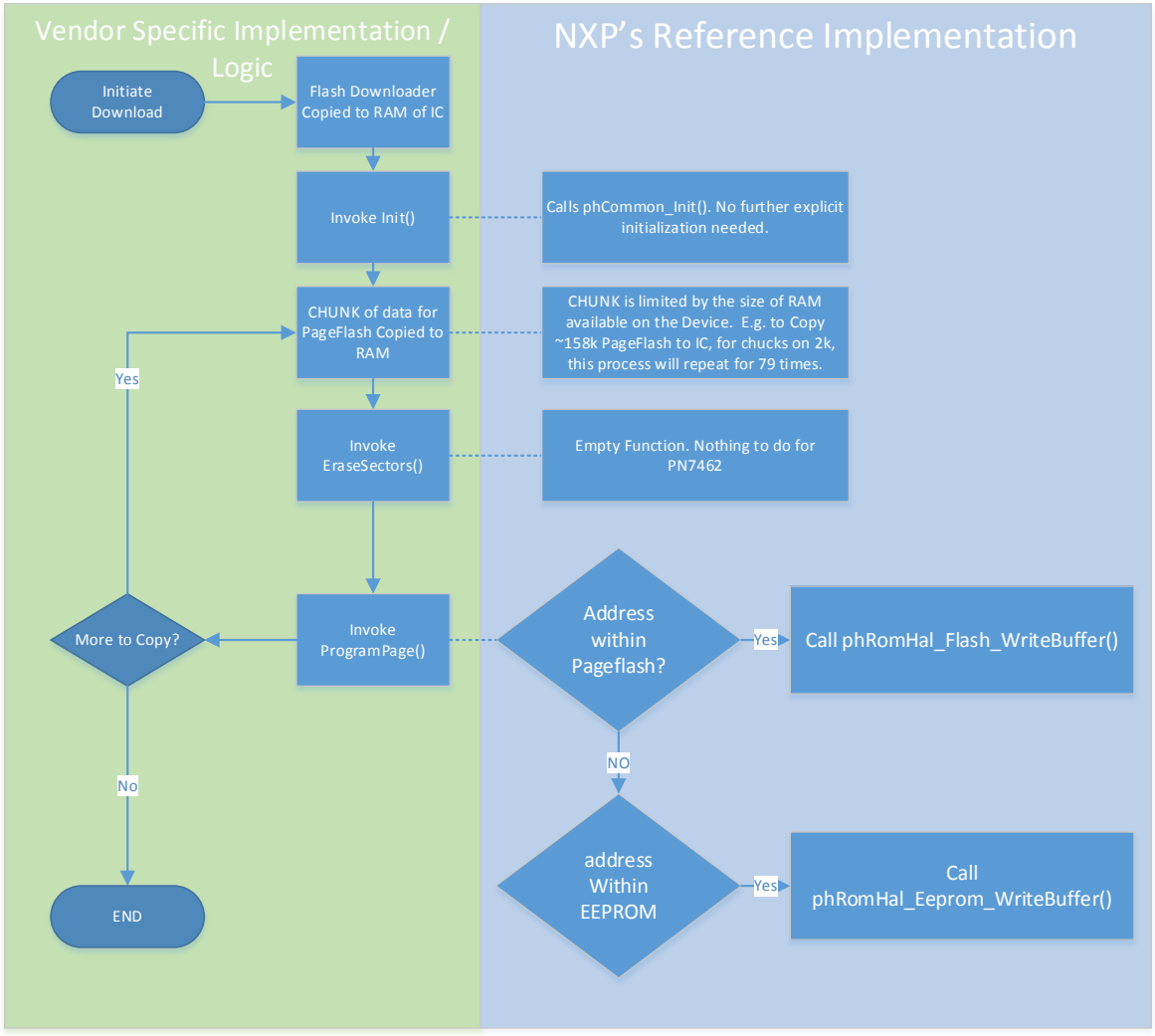


Fig 4. Common flow used during programming of Controller

5.2 Reference Implementation: Program Page

```
#include "phCommon.h"
#include "phRomHal_Flash.h"
#include "phRomHal_Eeprom.h"

/* Program Page in Flash Memory
 *    Parameter:      adr:  Page Start Address
 *                    sz:   Page Size
 *                    buf:  Page Data
 *    Return Value:   0 - OK,  1 - Failed */
int ProgramPage (unsigned long adr, unsigned long sz, unsigned char *buf) {
    phStatus_t phstat;
    int istat = 1 ; /* By default failure */

    if ( WITHIN_PAGEFLASH(adr)) {
        phstat = phRomHal_Flash_WriteBuffer((uint8_t *)buf, (uint8_t *)adr, sz);
        if ( PH_STATUS_SUCCESS == phstat ) {
            istat = 0; /* success */
        }
    }
    else if ( WITHIN_EEPROM(adr)) {
        phstat = phRomHal_Eeprom_WriteBuffer((uint8_t *)buf, (uint8_t *)adr, sz);
        if ( PH_STATUS_SUCCESS == phstat ) {
            istat = 0; /* success */
        }
    }
    else {
        istat = 1; /* failure */
    }
    return istat;
}
```

Fig 5. Sample API for Flash Programming

5.3 Supplied source code

Table 3. Description of files in flashcode.zip

File	Purpose
inc\phRomHal_Flash.h	APIs to write to PAGE FLASH
inc\phRomHal_Eeprom.h	APIs to write to EEPROM
inc\phCommon.h	APIs for Common code base
inc\ph_Status.h	Status code for APIs
inc\id_nfc_pn640_apb_if_reg.h	Internal header files for IP Register access
inc\id_reg_ro_rw.h	
inc\ph_Registers.h	
inc\ph_Config.h	Header files for portability across all the toolchains
inc\ph_Datatypes.h	
inc\ph_DefaultConfig.h	
src\phCommon.c	Implementation for writing to EEPROM, PAGE FLASH
src\phRomHal_Eeprom.c	
src\phRomHal_Flash.c	

5.4 Supplied Binary Files

- Along with this package, set of different PageFlash and EEPROM Binaries are provided
  - They are linked to each other. Mis-match would not glow the corresponding LEDs
- Two sets for each IC.
- These binaries can be used to run small acceptance test to confirm that the download is successful
- If corresponding EEPROM + PageFlash binaries are downloaded successfully, LED blinking pattern will be seen.
  - E.g. for `PN7360AU_YellowLED`, when downloaded successfully on PN7360AU IC, the pattern will toggle between
    - **Yellow**: **ON**, Blue Red Green: OFF
    - Yellow: OFF, **Blue Red Green**: **ON**
- ***DO NOT DOWNLOAD WRONG BINARY ON WRONG VARIANT***
- PAGE Flash and EEPROM Binaries
  - `PN7360AU_GreenLED`
  - `PN7360AU_YellowLED`
  - `PN7362AU_GreenLED`
  - `PN7362AU_RedLED`
  - `PN7462AU_BlueLED`
  - `PN7462AU_YellowLED`
- Each Folder contains
  - `EEPROM_*` ➔ Binary for EEPROM
  - `PAGEFLASH_*` ➔ Binary for PAGE FLASH

6. References

Table 4. References

This document refers to the following items

ID	Description
[PN7462AUDataSheet]	PN7462AU Datasheet
[UM10858]	PN7462AU HW User Manual
[ReferenceProductionBinaries.zip]	EEPROM and PageFlash Binaries that can be used to verify the Programmers
[flashcode.zip]	Portable code to be integrated into vendor downloader for programming/writing PageFlash and EEPROM of PN7462AU

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