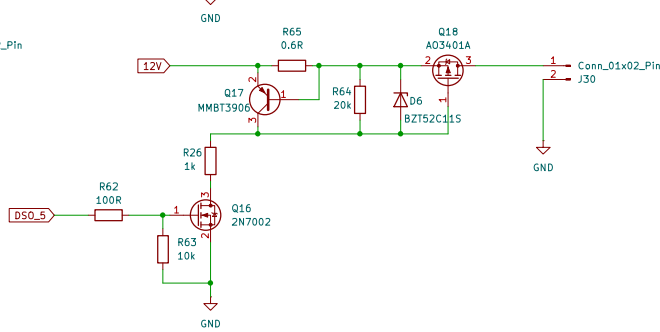
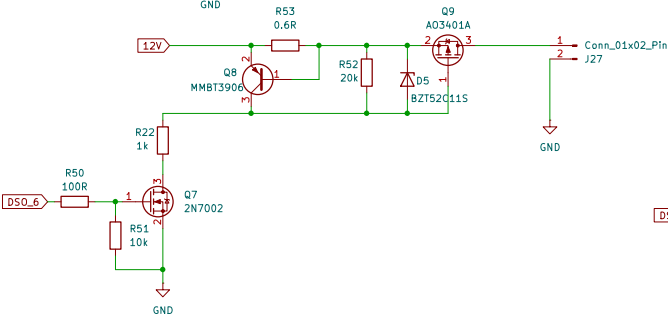
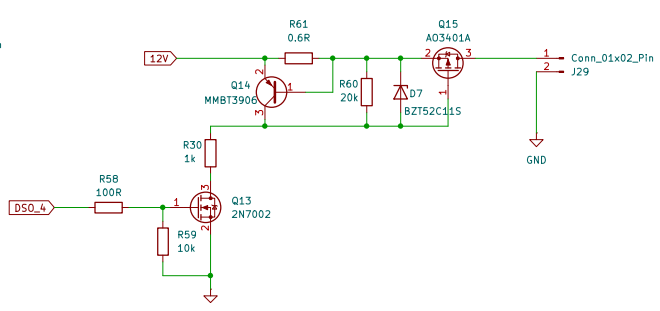
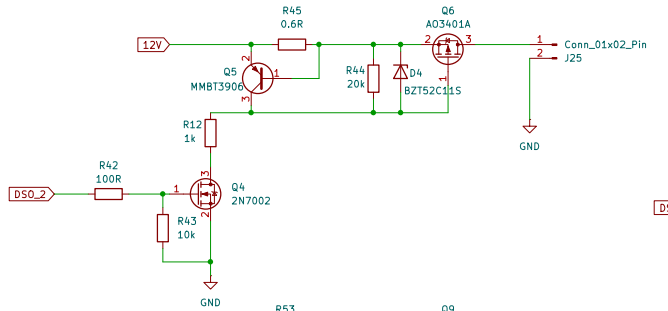
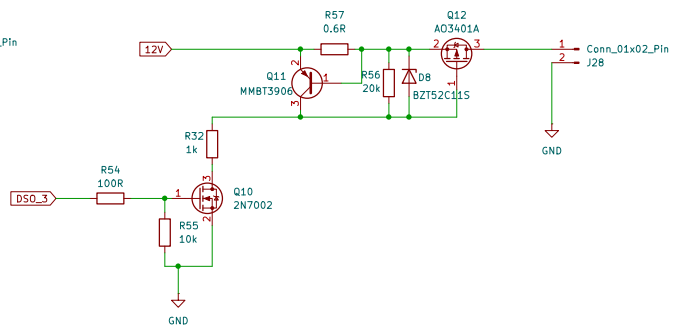
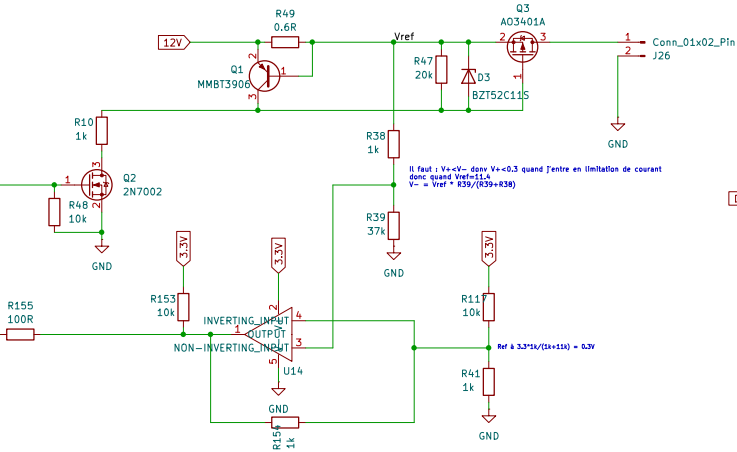
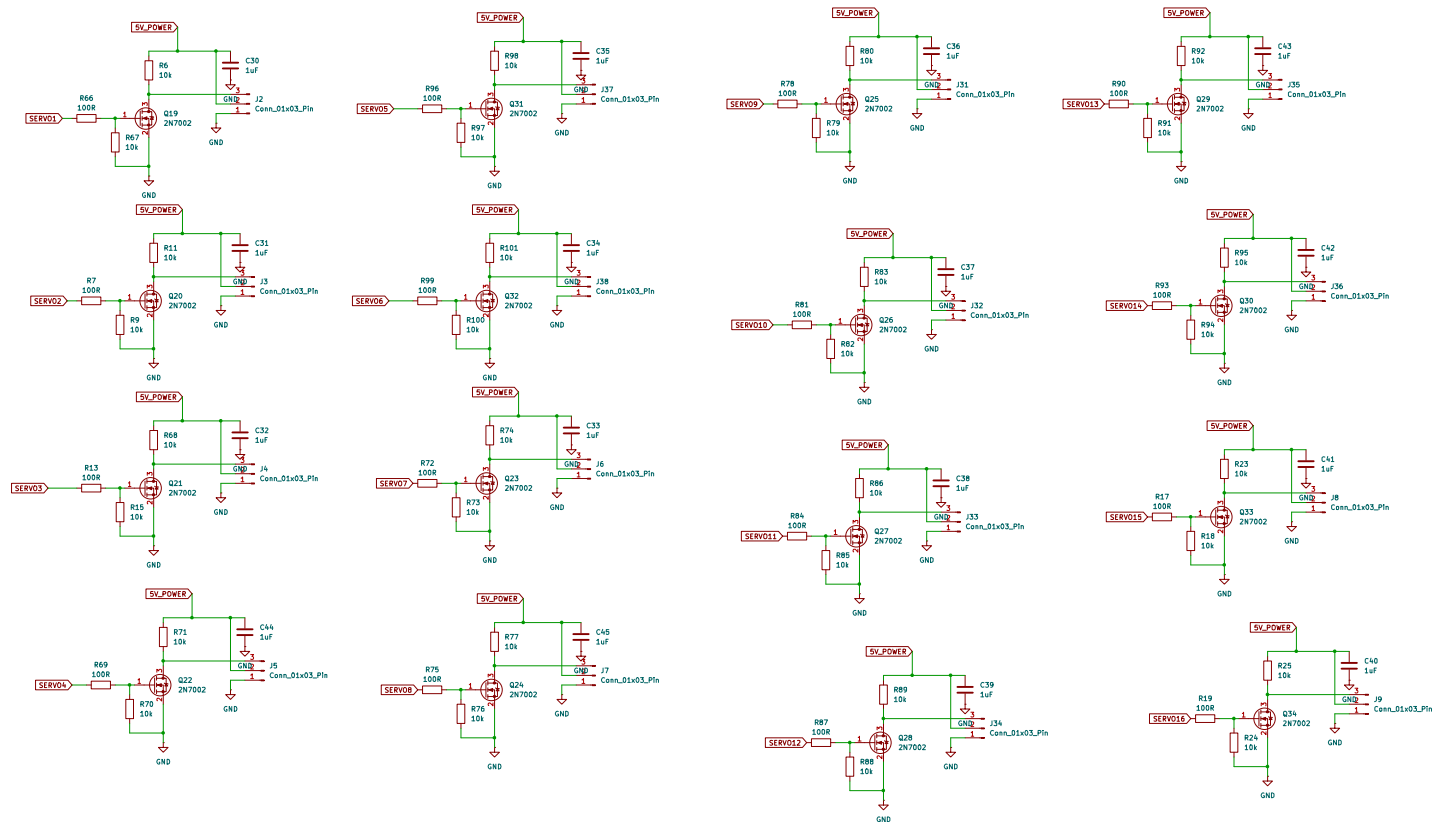
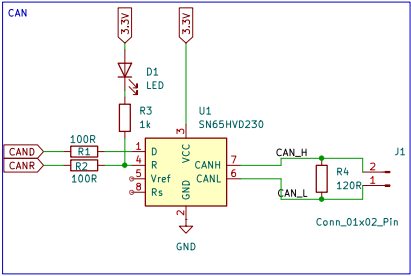


DSO - 1A max





The schematic diagram illustrates the input stage of the encoder, featuring three channels (A, B, and X) for the SN74LV1T34DCK (U3, U4, U7, U8, U9, U10, U11, U12, U13). Each channel consists of an inverter (Y) and a pull-up resistor (R5, R8, R14, R16, R20, R21, R28, R40) connected to a 5V supply. The input signals (QE1_1_A, QE1_1_B, QE1_1_X, QE1_2_A, QE1_2_B, QE1_2_X, QE1_3_A, QE1_3_B, QE1_3_X) are connected to the input pins (4) of the inverters. The output pins (2) of the inverters are connected to the corresponding pins (1, 2, 3, 4, 5) of the J17 and J40 connectors. Each inverter is also connected to a 3.3V supply (C1, C2, C23, C24, C25, C26, C27, C28, C29) and a 100nF decoupling capacitor. The ground pins (3) of the inverters are connected to GND.



AX12

