CSC 225 – Computer Architecture/Assembly Language

Assignment #1 - 50 Points

1. Provide a step-by-step description of the sequence of operations that must take place within the MIPS architecture. Then research two other architectures, of your choice, and list the sequence of operations.

   The MIPS architecture begins with the control unit sending a control signal is sent to a register file address, specified by the program counter, and fetches instructions from it to load into the instruction register. The program counter is incremented by four. Then, Rs and Rt, of the instructions, obtain the 32-bit source operands, which are routed to the ALU for calculations based on the Op-Code. Finally, the result is sent to a register file, specified by the Rd code in the IR. The process begins again with the next control signal.

   The SPARC architecture starts with an instruction fetch and the PC being incremented. The arithmetic instructions are executed by the ALU and the branch target address is computed, along with the memory address. Memory is accessed in the specified address point and the read/write process in memory commences and the write results are stored into a register or registers.

   In the Von Neumann architecture, the address of the PC is loaded into the memory address register and the PC is incremented by 1. The instructions in the MAR is loaded into the memory data register, which is used to send it to the current instruction register. The instructions are decoded in the CIR and executed and the cycle starts again with the incremented address of the PC.

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2. Using MIPS, and the other two architectures you have selected, provide a step-by-step description of the sequence of operations that must take place, with the processor, to fetch and execute the “store word” instruction. If there are no “store word” instructions for the two you have selected, indicate, “None” and why.

   In MIPS, an value is fetched from memory and loaded into the register file and stored from the base address to the effective address.

   The fetch and execute of the “store word” instruction in SPARC copies a value from a register and puts it into memory. The more significant word is stored in the effective address, while the less significant word is stored in the effective address plus four in the memory. The destination field is always set to zero.
   In the Von Neumann architecture, a value is stored into memory through a “write” signal to memory with the address of the MAR.