Classwork - 09

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1. Does the code has a control hazard? Yes

```
     CBZ X1, L2
L1: ADD X0, X1, X2
L2: SUB X3, X4, X5
```

How can it be resolved?

```
     CBZ X1, L1
L1: SUB X3, X4, X5
L2: ADD X0, X1, X2
```

2. For each code sequence below, state whether the code sequence must stall, can avoid stalls using only forwarding, or can execute without stalling or forwarding.

a) Yes Sequence 1 has a data dependency for X0, but can avoid a stall by forwarding.

```
i1: LDUR  X0, [X0, #0]
i2: ADD   X1, X0, X0
```

b) Yes, in i1 & i3. Forwarding avoids a stall.

```
i1: ADD   X1, X0, X0
i2: ADDI  X2, X0, #5
i3: ADDI  X4, X1, #5
```

c) No Dependencies or stalls.

```
i1: ADDI  X1, X0, #1
i2: ADDI  X2, X0, #2
i3: ADDI  X3, X0, #3
i4: ADDI  X4, X0, #4
i5: ADDI  X5, X0, #5
```

3. In this exercise, we examine how pipelining affects the clock cycle time of the processor. Problems in this exercise assume that individual stages of the Datapath have the following latencies:

IF	ID	EX	MEM	WB
250 ps	350 ps	150 ps	300 ps	200 ps

Also, assume that instructions executed by the processor are broken down as follows:

ALU/Logic	Jump/Branch	LDUR	STUR
45%	20%	20%	15%

a) What is the clock cycle time in a pipelined and non-pipelined processor? Non Pipeline = 1250 ps / Pipelined => Highest Latency = 350 ps

b) What is the total latency of an LDUR instruction in a pipelined and non-pipelined processor? Non Pipeline = 1250 ps / Pipelined => 1250 * 0.2 = 250 ps

c) Assuming there are no stalls or hazards, what is the utilization of the data memory? Data memory is utilized by LDUR & STUR. Utilization = 35% of the clock cycle.

d) Assuming there are no stalls or hazards, what is the utilization of the write-register port of the "Registers" unit?

ALU & LDUR use the write-register port. Utilization = 45% + 20% = 65%.

4. Assume that X1 is initialized to 11 and X2 is initialized to 22. Suppose you executed the code below on a version of the pipeline that does not handle data hazards (i.e., the programmer is responsible for addressing data hazards by inserting NOP instructions where necessary). What would the final values of registers X3 and X4 before and after the hazards are addressed?

```
ADDI X1, X2, #5
        =22 + 5
        =27
```

```
        =22 + 5
        =27
```

```
ADD X3, X1, X2
       =11 + 22
       =33
```

```
       =27 + 22
       =49
```

```
ADDI X4, X1, #15
        =11 +15
        =26
```

```
        =27 +15
        =42
```