Name:

Sample Test 1 -CS2400 - **SOLUTION**

1. Load and store instructions use ___**D**___ instruction format type .
2. R15 register is used as ___Program Counter__ in ARM.
3. __**MI**___ is the suffix used to check if it's a negative number in Arm instructions.
4. A bench mark program in computer A takes 20s to run, and in computer B it takes 10s. Computer _**B**___ is fastest by ___**2**____.

5. A program runs in 100 seconds. Multiply operations are responsible for 30 of those seconds. If extensive designer effort is applied such that multiply operations are made to run 2 times faster, what is the program's new execution time?

   Execution time after improvement= $\frac{\text{Execution time affected by improvement}}{Amount\ of\ improvement}$ + Execution time unaffected

   = 30 /2 +70 = 85 sec

6. If R2 has 500, R3 has 10, and memory locations 500, 504, and 508 have 20, 40, 10 respectively, what do those locations have after the following instruction?

```
ADDI   R3, R3,#2
STR    R3, [R2, #4]
```

   20 12 10

7. Assume that the flags are all initialized to 0 and instructions are sequential. For every instruction separately write the value in the destination register and the flags:

```
ADDS r2,r2,#32              r2 = #32 or 0x20 , NCZV =0000
MOV  r4,r2,LSL #1           r4 =#64  or 0x40 , NCZV =0000
TEQ  r4,#64                 NCZV = 0010
BIC  r4,r4,#0xF5            r4=0   ,NCZV=0010
```

8. Load 2 integer values in registers R1 and R2 respectively. Write a program to add the numbers if R1>R2 and subtract R1 from R2 if R2>R1 .

Commented [RR1]: **(See slide # 19 in S2_Instruction_02 Material)**

Commented [RR2]: Error in QP

```
        EXPORT __main
__main
        LDR r0,=6
        LDR r1,=4
        CMP r0, r1
        ADDGT  r3, r0, r1
        SUBLT  r3, r1, r0

        END
```

9. Write an ARM assembly program to swap two numbers in registers R0 and R1 without using a third register.

```
        EXPORT __main
__main

        LDR r0,=6
        LDR r1,=4
        EOR r0,r0,r1
        EOR r1,r0,r1
        EOR r0,r0,r1

        END
```

10. Write the register values after each instruction in the below code.

```
MOV r0, #0x11        r0 = 0x11
LSL r1, r0, #1       r1 = 0x22
LSL r2, r1, #1       r2 = 0x44
```

11. Assume R0 holds the value 0000000000101000. What is the value of R8 after the following instructions?

```
    CMP R0,#0
    BGE els
    B DONE
els
    ORR R8,R0,#2              R8=0x2A 0r 101010₂
DONE
```

12. Translate the following loop into C (or pseudo code). Assume that the C-level integer **"i" is** held in register R3, R2 holds the C-level integer called **"result"**, and R0 holds the base address of the integer in memory.

```
LOOP
     LDR R1,[R0,#0]
    ADD R2,R2, R1
    ADD R0,R0,#4
     ADD R3,R3,#1
    CMP R3,#50
    BLE  LOOP
```

```
do{
result += MemArray[i];
i ++;
}while(i < =50);
```

13. Implement the following high level code in ARM assembly language. Assume that the labels represent memory locations. Also write code to allocate memory for the given labels:

(a)
```
int c = 0;
while (c < count)
{
 c++;
}
```

```
        EXPORT __main
__main

        LDR R4,=c
         LDR R1, [R4]
loop1
         CMP R1, #3
        BEQ exit
        ADD R1, R1, #1
        B loop1
exit

c  DCD  0
        END
```

(b)

(c)
```
if (cost < givenValue)
{
  display = cost * 2;
}
else
{
  display= cost * 2 + surcharge;
}
```

Initialize:

```
cost:10
givenValue:12
surcharge:3
display:0
```

```
        EXPORT __main
__main
        LDR R4, =cost
        LDR R5, [R4]     ; cost in R5
        LDR R4, =givenValue
        LDR R1, [R4]     ; givenValue in R1
        LDR R4, =surcharge
        LDR R2, [R4]     ; surcharge in R2
        LDR R4, =display
        LDR R3, [R4]     ; display in R3
        CMP R5, R1
        MOVLS R3, R5, LSL #1
        BHI  else1
        B stop
else1
        ADD R3, R3, R2
```

```
stop

cost        DCD 10
givenValue  DCD 12
surcharge   DCD 3
display     DCD 0
    END
```

14. A program runs in 10 seconds on computer A, which has a 2 GHz clock. A computer designer builds a computer B, which will run the same program in 5 seconds. The increase in clock rate will affect the rest of the CPU design, causing computer B to require 1.5 times as many clock cycles as computer A for this program. What clock rate should be set for the best design?
    Write the equation used for the test.
    Clock Rate = Clock Cycles / CPU Time.

    6 GHz

15. Consider the following performance measurements for a program:

Measurement	Computer A	Computer B
Instruction count	12 billion	10 billion
Clock rate	4 GHz	5 GHz
CPI	1.0	1.2

    Which computer has the higher MIPS rating?
    Which computer is faster for that program?

a) MIPS(A)= $\frac{\text{Clock Rate}}{\text{CPI } X\ 10^6} = \frac{4\times 10^9}{1\ X\ 10^6} = 4000$

MIPS(B)= $\frac{\text{Clock Rate}}{\text{CPI } X\ 10^6} = \frac{5\times 10^9}{1.2\ X\ 10^6} = 4167.67$

Higher MIPS for B

b) CPU Time (A) = $\frac{Instruction\ Count \times CPI}{Clock\ Rate} = \frac{12 \times 10^9 \times 1}{4 \times 10^9} = 3\ Sec$

CPU Time (B)= $\frac{Instruction\ Count \times CPI}{Clock\ Rate} = \frac{10 \times 10^9 \times 1.2}{5 \times 10^9} = 2.4\ Sec$

B is faster