Christopher Welch

4. Suppose we have a memory and a direct-mapped cache with the following characteristics. Memory addresses are 16 bits, The cache has 8 rows (i.e., 8 cache lines) , Each cache row (line) holds 16 bytes of data .

a. In the spaces below, indicate how the 16 address bits are allocated to the offset, index, and tag parts of the address used to reference the cache:

___10_____ tag bits ____3____ index bits ____3____ offset bits.

Below is a sequence of four binary memory addresses in the order they are used to reference memory. Assume that the cache is initially empty. For each reference, write down the tag and index bits and write either it is a hit or miss.

Memory Address	Tag	Index	Hit Miss
0010110110110011	0010110110	110	M
0000011011111100	0000011011	111	M
0010110110111000	0010110110	111	M
1010101010101011	1010101010	101	M

Tag Index Offset