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CS2400 Spring 2020

Homework 05

1. Here is a series of address references given as word addresses: 2, 3, 11, 16, 21, 13, 64, 48, 19, 11, 3, 22, 4, 27, 6 and 11. a. Assuming a Direct-mapped cache with 16 one-word blocks that is initially empty, label each reference in the list as a hit or a miss. b. Now assume that the cache is a 2-way set associative, one-word blocks, total 16-word capacity.

A) Direct-mapped 16 one-word blocks.	**B) 2-Way Set Associative 16 one-word blocks**
2. Miss	2. Miss
3. Miss	3. Miss
11. Miss	11. Miss
16. Miss	16. Miss
21. Miss	21. Miss
13. Miss	13. Miss
64. Miss	64. Miss
48. Miss	48. Miss
19. Miss	19. Miss
11. Hit	11. Hit
3. Miss	3. Miss
22. Miss	22. Miss
4. Miss	4. Miss
27. Miss	27. Miss
6. Miss	6. Miss
11. Miss	11. Miss

2. A computer is using a fully associative cache and has $\mathbf{2^{16}}$ bytes of memory and a cache of 64 blocks, where each block contains 32 bytes.
   (a) How many blocks of main memory are there? 64 x 32 = 2048 = 2^{11}
   (b) What will be the sizes of the tag, index, and **byte offset fields**?
   Tag = 11 Index = 0 Offset = 5
   16-11=5
   (c) To which cache set will the memory address 0xF8C9(hexadecimal) map?
   1 set because it is a fully associative cache.

3. A computer using a direct mapped cache has $\mathbf{2^{20}}$ Bytes of memory and a cache of 32 blocks, each block contains 16 Bytes.
   (a) How many blocks of main memory are there? $2^{20} - 2^4 =$ $\mathbf{2^{16}}$
   (b What will be the sizes of the tag, index, and **byte offset fields**? $2^{20} - 2^{16} = 2^4$ & $2^{16}-2^5 = 2^{11}$
   Tag = 11 Index = 5 Offset = 4

   (c) To which cache set will the memory address 0x0DB63 map?
   0x0DB63 => 1101101101100011 => **22nd Block**

4. Suppose we have a 4 GB memory that is **byte addressable**, and a 2 MB cache with 256 bytes per block.

(a) How many total lines are in the cache?

log(256)/log(2) = 8 $256 = 2^8$

4GB memory = 2^{32} Bytes $2^{32}/2^8 =$ **24 Blocks of Memory**

2MB cache = 2^{21} Bytes $2^{21}/2^8 = 2^{13}$ = **13 Blocks of Cache**

If the cache is direct-mapped, how many cache lines could a specific memory block be mapped to? **1**

(b) If the cache is direct-mapped, what would be the format (tag bits, index, offset bits) of the address?

Tag = 11 **Index = 13** **Offset = 8**