04/21/2020 , Questions Redo **CHRISTOPHER WELCH**

1. Given Control Signals are RegDst, ALUSrc, MemtoReg, RegWrite, MemRead, MemWrite, Branch, ALUOp0, ALUOp1 Which all control Signals will be set as '1' for the following different instructions.

Give answers for each instruction separately.

1) ADD R1, R2, R3 =
   RegDst
   RegWrite
   ALUOp1
2) LDR R4, [R5] ALUSrc
   RegWrite
   MemtoReg
   MemRead
3) STR R3, [R4] ALUSrc
   MemWrite
4) BEQ Label Branch
   ALUOp0
5) ADDI R3, R2, #3
   ALUSrc
   RegWrite
6) CBZ R1, Label
   Branch

2. Problems in this exercise refer to the following sequence of instructions and assume that it is executed on a five-stage Pipelined Datapath.

ADD X5, X2, X1
LDUR X3, [X5, #4]
LDUR X2, [X2, #0]
ORR X3, X5, X3
STUR X3, [X5, #0]

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2.1 Draw the pipeline execution diagram. Identify the hazards in the code, explain it.
2.2 Is it possible to modify the code to reduce hazards? Justify.
2.3 Show the ways in which you can reduce hazards in the pipeline without reordering the code.

Can do NOP also in 2.3

3. With the help of neat pipeline execution diagram show how bypassing is done for each of the below instructions to avoid data hazard if required.

3.1 ADD R1, R3, R2
SUB R2, R4, R1
3.2 ADD R1, R2, R3
LDUR R5, [R7, #0]
SUB R2, R1, R4

3.3 ADD R3, R2, R1
LDUR R4, [R3, #4]
SUB R8, R3, R1
ADDI R6, R4, #1
4. In a single cycle Datapath the processor fetches the following instruction word: 0x8B0C016A.
4.1 Write the corresponding instruction for the given HEX instruction word.
4.2 What are the outputs of the Read data 1 and Read data2 from the Register File.
4.3 What are the values of the ALU control unit's inputs for this instruction?
4.4 Show the values of inputs and outputs for al MUX during the execution of this instruction.
4.5 Give the values of all control signals for this instruction.
4.6 What is the new PC address after this instruction is executed?
4.1 ADD X10, X11, X12
4.2 Read data 1: X11 Read data 2: X12
4.3 00010
4.4 First MUX receives: Inst [20:16] for Rm. Second MUX receives Read Data 2 from reg file. Third MUX receives ALU result to write back. PCSrc MUX receives regular address incremented by 4(deasserted).
4.5 RegDst = 0, AluSrc = 0, MemtoReg = 0, RegWrite = 1, MemRead = 0, MemWrite = 0, Branch = 0, AluOp1 = 1, AluOp0 = 0
4.6 PC+4
5. Convert the given Instructions to 32-bit LEGv8 binary representation and its corresponding HEX format.
[Use the green card for opcode binary values]
a. LDUR X11, [X9, #4]
b. CBZ X2, 0x1100
c. SUB X8, X10, X2
a. 11111000010 000000100 00 01001 01011
F 8 4 0 4 1 2 B
b. 10110100 0000001000100000000 00010
B 4 0 2 2 0 0 2
c. 11001011000 00010 000000 01010 01000
C B 0 2 0 1 4 8