

# TPS22810, 2.7-18-V, 79-mΩ On-Resistance Load Switch With Thermal Protection

## 1 Features

- Integrated Single Channel Load Switch
- Ambient Operating Temperature:  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ 
  - SOT23-6 (DBV): 2-A Maximum Continuous Current<sup>1</sup>
  - WSON (DRV): 3-A Maximum Continuous Current<sup>1</sup>
- Input Voltage Range: 2.7 V to 18 V
- Absolute Maximum Input Voltage: 20 V
- On-Resistance ( $R_{\text{ON}}$ )
  - $R_{\text{ON}} = 79\text{ m}\Omega$  (typical) at  $V_{\text{IN}} = 12\text{ V}$
- Quiescent Current
  - $62\text{ }\mu\text{A}$  (typical) at  $V_{\text{IN}} = 12\text{ V}$
- Shutdown Current
  - $500\text{ nA}$  (typical) at  $V_{\text{IN}} = 12\text{ V}$
- Thermal Shutdown
- Undervoltage Lock-Out (UVLO)
- Adjustable Quick Output Discharge (QOD)
- Configurable Rise Time With CT Pin
- SOT23-6 Package
  - 2.9-mm  $\times$  2.8-mm, 0.95-mm Pitch, 1.45-mm Height (DBV)
- WSON Package
  - 2-mm  $\times$  2-mm, 0.65-mm Pitch, 0.75-mm Height (DRV)
- ESD Performance Tested per JESD 22
  - $\pm 2\text{-kV}$  HBM and  $\pm 1\text{-kV}$  CDM

(1) Thermal performance must be considered

## 2 Applications

- HD TV
- Industrial Systems
- Set Top Box
- Surveillance systems

## 3 Description

The TPS22810 is a single channel load switch with configurable rise time and with an integrated quick output discharge (QOD). In addition, the device features thermal shutdown to protect the device against high junction temperature. Because of this, safe operating area of the device is inherently ensured. The device contains an N-channel MOSFET that can operate over an input voltage range of 2.7 V to 18 V. SOT23-5 (DBV) package can support a maximum current of 2 A. WSON (DRV) package can support a maximum current of 3 A. The switch is controlled by an on and off input, which is capable of interfacing directly with low-voltage control signals.

The configurable rise time of the device greatly reduces inrush current caused by large bulk load capacitances, thereby reducing or eliminating power supply droop. Undervoltage lock-out is used to turn off the device if the  $V_{\text{IN}}$  voltage drops below a threshold value, ensuring that the downstream circuitry is not damaged by being supplied by a voltage lower than intended. The configurable QOD pin controls the fall time of the device to allow design flexibility for power down.

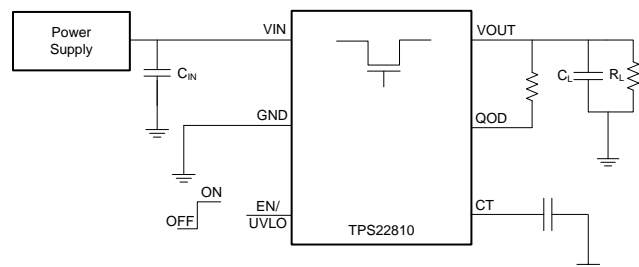
The TPS22810 is available in a leaded, SOT-23 package (DBV) which allows to visually inspect solder joints, as well as a WSON package (DRV). The device is characterized for operation over the free-air temperature range of  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ .

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22810	SOT-23 (6)	2.90 mm $\times$ 2.80 mm
	WSON (6)	2.00 mm $\times$ 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Simplified Schematic



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## 4 Revision History

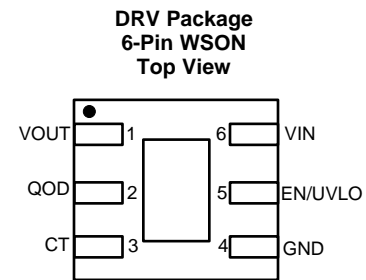
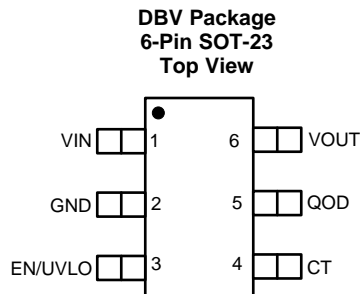
Changes from Revision A (December 2016) to Revision B	Page
• Added WSON (DRV) package .....	<b>1</b>
• Added WSON (DRV) current information in the <i>Features</i> , <i>Description</i> section and <i>Recommended Operating Conditions</i> table .....	<b>1</b>

Changes from Original (December 2016) to Revision A	Page
• Deleted $I_{MAX}$ and $I_{PLS}$ from the <i>Absolute Maximum Ratings</i> table .....	<b>4</b>
• Changed the Quiescent current MAX value From: 70 $\mu A$ To: 80 $\mu A$ in the <i>Electrical Characteristics</i> table .....	<b>5</b>
• Changed the Quiescent current MAX value for $V_{IN} = 2.7 V$ From: 60 $\mu A$ To: 70 $\mu A$ in the <i>Electrical Characteristics</i> table .....	<b>5</b>
• Changed the Shutdown current MAX value From: 2.25 $\mu A$ To: 2.3 $\mu A$ in the <i>Electrical Characteristics</i> table .....	<b>5</b>

## 5 Device Comparison Table

DEVICE	R <sub>ON</sub> at 12 V	Package	QUICK OUTPUT DISCHARGE	T <sub>A</sub>	MAXIMUM OUTPUT CURRENT	ENABLE
TPS22810	79 mΩ	DBV	Configurable	105°C	2 A	Active High
TPS22810	79 mΩ	DRV	Configurable	105°C	3 A	Active High

## 6 Pin Configuration and Functions



### Pin Functions

NAME	PIN NO,		I/O	DESCRIPTION
	SOT23	WSON		
CT	4	3	O	Switch slew rate control. Can be left floating
EN/UVLO	3	5	I	Active high switch control input and UVLO adjustment. Do not leave floating
GND	2	4	—	Device ground
QOD	5	2	O	Quick Output Discharge pin. This functionality can be enabled in one of three ways. <ul style="list-style-type: none"> <li>Placing an external resistor between VOUT and QOD</li> <li>Tying QOD directly to VOUT and using the internal resistor value (R<sub>PD</sub>)</li> <li>Disabling QOD by leaving pin floating</li> </ul> See the <a href="#">Quick Output Discharge (QOD)</a> for more information
VIN	1	6	I	Switch input. Place ceramic bypass capacitor(s) between this pin and GND
VOUT	6	1	O	Switch output

## 7 Specifications

### 7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup> <sup>(2)</sup>

		MIN	MAX	UNIT
V <sub>IN</sub>	Input voltage	−0.3	20	V
V <sub>OUT</sub>	Output voltage	−0.3	min(V <sub>IN</sub> + 0.3, 20)	V
V <sub>EN/UVLO</sub>	EN/UVLO voltage	−0.3	20	V
T <sub>J</sub>	Maximum junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

### 7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>IN</sub>	Input voltage	2.7	18	V
V <sub>EN/UVLO</sub>	EN/UVLO voltage	0	18	V
V <sub>OUT</sub>	Output voltage		V <sub>IN</sub>	V
I <sub>MAX</sub>	Maximum continuous switch current, T <sub>A</sub> = 65°C (DBV)		2	A
	Maximum continuous switch current, T <sub>A</sub> = 65°C (DRV)		3	
T <sub>A</sub>	Operating free-air temperature <sup>(1)</sup>	−40	105	°C
C <sub>IN</sub>	Input capacitor	1 <sup>(2)</sup>		μF

- (1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [T<sub>A(MAX)</sub>] is dependent on the maximum operating junction temperature [T<sub>J(MAX)</sub>], the maximum power dissipation of the device in the application [P<sub>D(MAX)</sub>], and the junction-to-ambient thermal resistance of the part/package in the application (θ<sub>JA</sub>), as given by the following equation: T<sub>A(MAX)</sub> = T<sub>J(MAX)</sub> − (θ<sub>JA</sub> × P<sub>D(MAX)</sub>).
- (2) See the [Detailed Description](#) section.

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS22810		UNIT
		DBV (SOT23)	DRV (WSON)	
		6 PINS	6 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	182	74.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	127.2	80.3	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	16.9	44.3	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	26.4	3.2	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	36.3	44.6	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

Unless otherwise noted, the specification in the following table applies over the following ambient operating temperature  $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ . Typical values are for  $T_A = 25^{\circ}\text{C}$ .

PARAMETER	TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$I_{Q, VIN}$ Quiescent current	$V = 18\text{ V}, I = 0\text{ A}$	$V_{IN} = 18\text{ V}$	$-40^{\circ}\text{C to } +85^{\circ}\text{C}$	62	80	$\mu\text{A}$
			$-40^{\circ}\text{C to } +105^{\circ}\text{C}$		85	
		$V_{IN} = 12\text{ V}$	$-40^{\circ}\text{C to } +85^{\circ}\text{C}$	62	80	
			$-40^{\circ}\text{C to } +105^{\circ}\text{C}$		85	
		$V_{IN} = 5\text{ V}$	$-40^{\circ}\text{C to } +85^{\circ}\text{C}$	59	80	
			$-40^{\circ}\text{C to } +105^{\circ}\text{C}$		85	
		$V_{IN} = 3.3\text{ V}$	$-40^{\circ}\text{C to } +85^{\circ}\text{C}$	53	80	
			$-40^{\circ}\text{C to } +105^{\circ}\text{C}$		85	
		$V_{IN} = 2.7\text{ V}$	$-40^{\circ}\text{C to } +85^{\circ}\text{C}$	49	70	
			$-40^{\circ}\text{C to } +105^{\circ}\text{C}$		85	
$I_{SD, VIN}$ Shutdown current	$V_{ON} = 0\text{ V}, V_{OUT} = 0\text{ V}$	$V_{IN} = 18\text{ V}$	$-40^{\circ}\text{C to } +85^{\circ}\text{C}$	0.5	2.3	$\mu\text{A}$
			$-40^{\circ}\text{C to } +105^{\circ}\text{C}$		3.8	
		$V_{IN} = 12\text{ V}$	$-40^{\circ}\text{C to } +85^{\circ}\text{C}$	0.5	2.3	
			$-40^{\circ}\text{C to } +105^{\circ}\text{C}$		3.8	
		$V_{IN} = 5\text{ V}$	$-40^{\circ}\text{C to } +85^{\circ}\text{C}$	0.5	2.3	
			$-40^{\circ}\text{C to } +105^{\circ}\text{C}$		3.8	
		$V_{IN} = 3.3\text{ V}$	$-40^{\circ}\text{C to } +85^{\circ}\text{C}$	0.5	2.3	
			$-40^{\circ}\text{C to } +105^{\circ}\text{C}$		3.8	
		$V_{IN} = 2.7\text{ V}$	$-40^{\circ}\text{C to } +85^{\circ}\text{C}$	0.5	2.3	
			$-40^{\circ}\text{C to } +105^{\circ}\text{C}$		3.8	
$I_{EN/UVLO}$ EN/UVLO pin input leakage current	$V_{IN} = 18\text{ V}, I_{OUT} = 0\text{ A}$	$-40^{\circ}\text{C to } +105^{\circ}\text{C}$			0.1	$\mu\text{A}$
$V_{UVR}$ VIN UVLO threshold, rising		$-40^{\circ}\text{C to } +105^{\circ}\text{C}$	2	2.54	2.62	V
$V_{UVhyst}$ VIN UVLO hysteresis		$-40^{\circ}\text{C to } +105^{\circ}\text{C}$		5%		
$V_{ENR}$ EN threshold voltage, rising		$-40^{\circ}\text{C to } +105^{\circ}\text{C}$	1.13	1.23	1.3	V
$V_{ENF}$ EN threshold voltage, falling		$-40^{\circ}\text{C to } +105^{\circ}\text{C}$	1.08	1.13	1.18	V
$V_{SHUTF}$ EN threshold voltage for low IQ shutdown		$-40^{\circ}\text{C to } +105^{\circ}\text{C}$	0.5	0.75	0.9	V

## Electrical Characteristics (continued)

Unless otherwise noted, the specification in the following table applies over the following ambient operating temperature  $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ . Typical values are for  $T_A = 25^{\circ}\text{C}$ .

PARAMETER	TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$R_{ON}$ On-resistance	$V_{IN} = 18\text{ V}$ , $I_{OUT} = -200\text{ mA}$	$25^{\circ}\text{C}$		79	86	$\text{m}\Omega$
		$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			105	
		$-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$			115	
	$V_{IN} = 12\text{ V}$ , $I_{OUT} = -200\text{ mA}$	$25^{\circ}\text{C}$		79	86	
		$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			105	
		$-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$			115	
	$V_{IN} = 9\text{ V}$ , $I_{OUT} = -200\text{ mA}$	$25^{\circ}\text{C}$		79	86	
		$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			105	
		$-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$			115	
	$V_{IN} = 5\text{ V}$ , $I_{OUT} = -200\text{ mA}$	$25^{\circ}\text{C}$		79	86	
		$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			105	
		$-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$			115	
	$V_{IN} = 3.3\text{ V}$ , $I_{OUT} = -200\text{ mA}$	$25^{\circ}\text{C}$		83	92	
		$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			115	
		$-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$			125	
	$V_{IN} = 2.7\text{ V}$ , $I_{OUT} = -200\text{ mA}$	$25^{\circ}\text{C}$		86	95	
		$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			120	
		$-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$			130	
$R_{PD}$ Output pull down resistance	$V_{IN} = V_{OUT} = 18\text{ V}$ , $V_{EN/UVLO} = 0\text{ V}$	$-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$		290	350	$\Omega$
	$V_{IN} = V_{OUT} = 12\text{ V}$ , $V_{EN/UVLO} = 0\text{ V}$	$-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$		265	350	
	$V_{IN} = V_{OUT} = 5\text{ V}$ , $V_{EN/UVLO} = 0\text{ V}$	$-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$		250	400	
TS Thermal shutdown	Threshold, $V_{IN} = 18\text{ V}$	$-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$		160		$^{\circ}\text{C}$
TSHDN Hyst Thermal shutdown hysteresis	TSD hysteresis, $V_{IN} = 18\text{ V}$	$-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$		30		$^{\circ}\text{C}$

## 7.6 Switching Characteristics

Refer to the timing test circuit in [Figure 16](#) (unless otherwise noted) for references to external components used for the test condition in the switching characteristics table. Switching characteristics shown below are only valid for the power-up sequence where VIN is already in steady state condition before the EN/UVLO pin is asserted high.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>IN</sub> = 18 V, V <sub>EN/UVLO</sub> = 5 V, T <sub>A</sub> = 25 °C (unless otherwise noted)						
t <sub>ON</sub>	Turnon time	R <sub>L</sub> = 10 Ω, C <sub>IN</sub> = 1 μF, C <sub>L</sub> = 0.1 μF, CT = 2200 pF		520		μs
t <sub>OFF</sub>	Turnoff time	R <sub>L</sub> = 10 Ω, C <sub>IN</sub> = 1 μF, C <sub>L</sub> = 0.1 μF, CT = 2200 pF		3.3		
t <sub>R</sub>	V <sub>OUT</sub> rise time	R <sub>L</sub> = 10 Ω, C <sub>IN</sub> = 1 μF, C <sub>L</sub> = 0.1 μF, CT = 2200 pF		700		
t <sub>F</sub>	V <sub>OUT</sub> fall time	R <sub>L</sub> = 10 Ω, C <sub>IN</sub> = 1 μF, C <sub>L</sub> = 0.1 μF, CT = 2200 pF		2		
t <sub>D</sub>	Delay time	R <sub>L</sub> = 10 Ω, C <sub>IN</sub> = 1 μF, C <sub>L</sub> = 0.1 μF, CT = 2200 pF		180		
V <sub>IN</sub> = 12 V, V <sub>EN/UVLO</sub> = 5 V, T <sub>A</sub> = 25 °C (unless otherwise noted)						
t <sub>ON</sub>	Turnon time	R <sub>L</sub> = 10 Ω, C <sub>IN</sub> = 1 μF, C <sub>L</sub> = 0.1 μF, CT = 2200 pF		380		μs
t <sub>OFF</sub>	Turnoff time	R <sub>L</sub> = 10 Ω, C <sub>IN</sub> = 1 μF, C <sub>L</sub> = 0.1 μF, CT = 2200 pF		3.3		
t <sub>R</sub>	V <sub>OUT</sub> rise time	R <sub>L</sub> = 10 Ω, C <sub>IN</sub> = 1 μF, C <sub>L</sub> = 0.1 μF, CT = 2200 pF		460		
t <sub>F</sub>	V <sub>OUT</sub> fall time	R <sub>L</sub> = 10 Ω, C <sub>IN</sub> = 1 μF, C <sub>L</sub> = 0.1 μF, CT = 2200 pF		2		
t <sub>D</sub>	ON delay time	R <sub>L</sub> = 10 Ω, C <sub>IN</sub> = 1 μF, C <sub>L</sub> = 0.1 μF, CT = 2200 pF		150		
V <sub>IN</sub> = 3.3 V, V <sub>EN/UVLO</sub> = 5 V, T <sub>A</sub> = 25 °C (unless otherwise noted)						
t <sub>ON</sub>	Turnon time	R <sub>L</sub> = 10 Ω, C <sub>IN</sub> = 1 μF, C <sub>L</sub> = 0.1 μF, CT = 2200 pF		185		μs
t <sub>OFF</sub>	Turnoff time	R <sub>L</sub> = 10 Ω, C <sub>IN</sub> = 1 μF, C <sub>L</sub> = 0.1 μF, CT = 2200 pF		3.3		
t <sub>R</sub>	V <sub>OUT</sub> rise time	R <sub>L</sub> = 10 Ω, C <sub>IN</sub> = 1 μF, C <sub>L</sub> = 0.1 μF, CT = 2200 pF		120		
t <sub>F</sub>	V <sub>OUT</sub> fall time	R <sub>L</sub> = 10 Ω, C <sub>IN</sub> = 1 μF, C <sub>L</sub> = 0.1 μF, CT = 2200 pF		2		
t <sub>D</sub>	ON delay time	R <sub>L</sub> = 10 Ω, C <sub>IN</sub> = 1 μF, C <sub>L</sub> = 0.1 μF, CT = 2200 pF		130		

## 7.7 Typical DC Characteristics

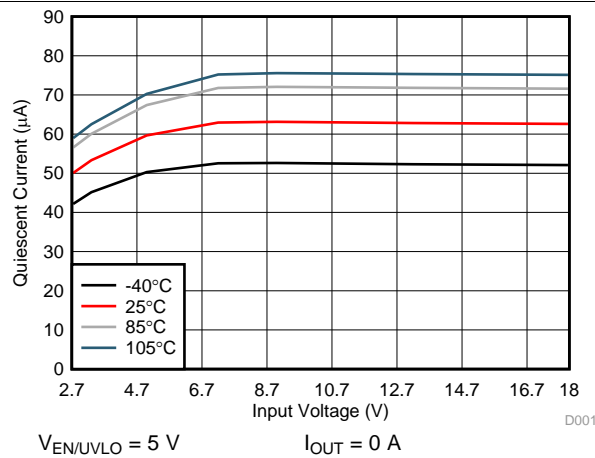


Figure 1. Quiescent Current vs Input Voltage

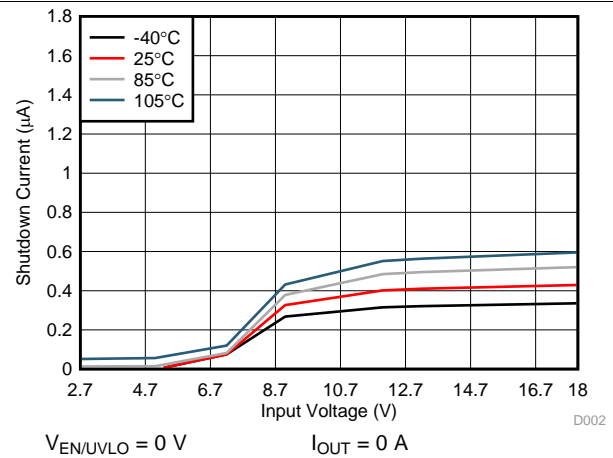


Figure 2. Shutdown Current vs Input Voltage

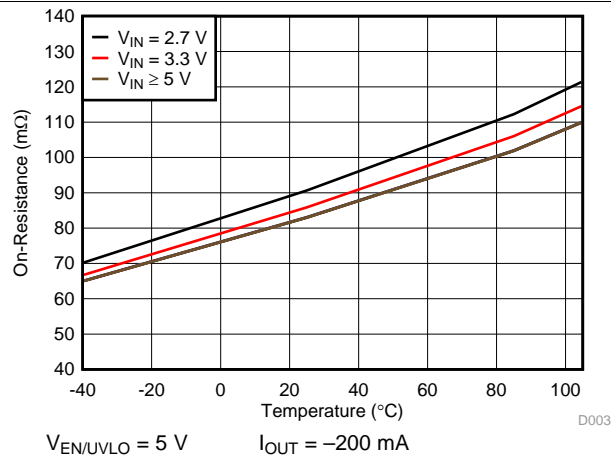


Figure 3. On-Resistance vs Temperature

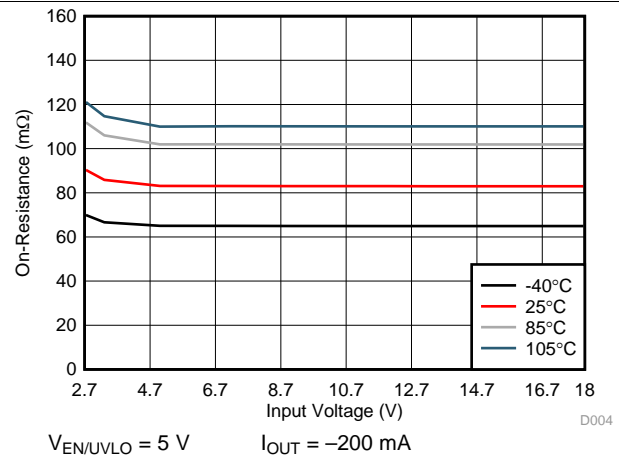


Figure 4. On-Resistance vs Input Voltage

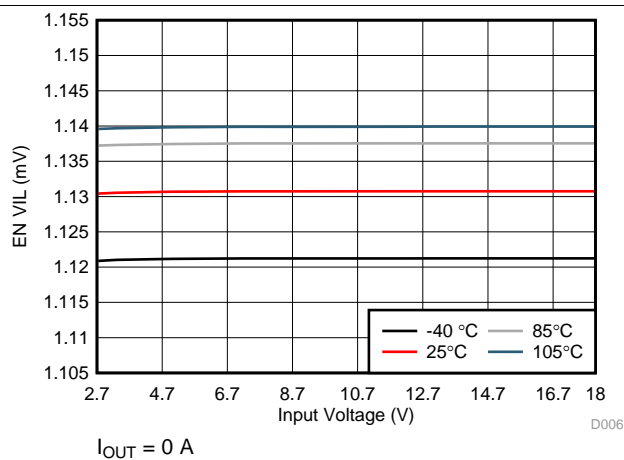


Figure 5. EN VIL vs Input Voltage

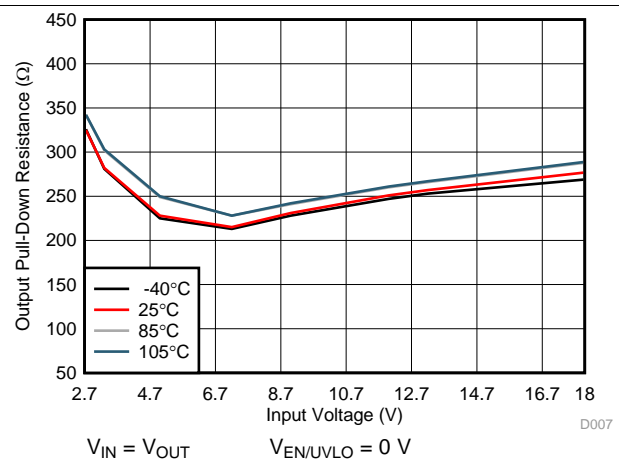
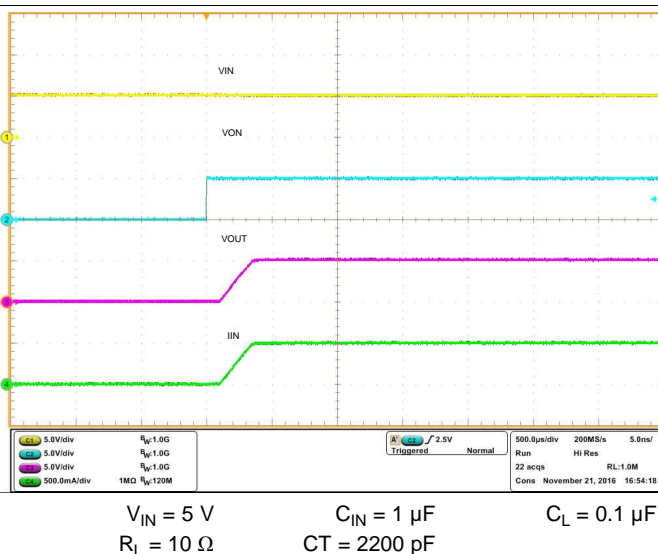
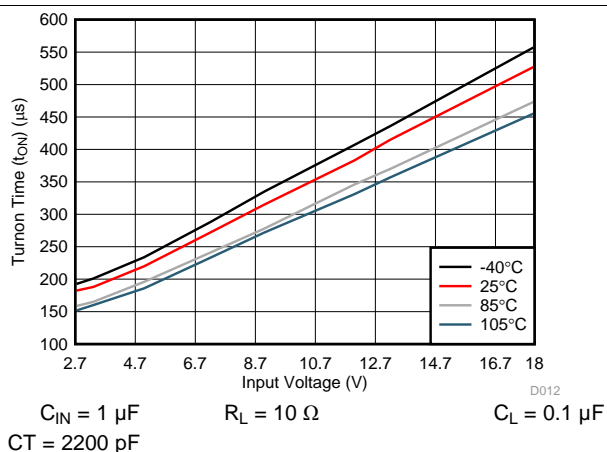
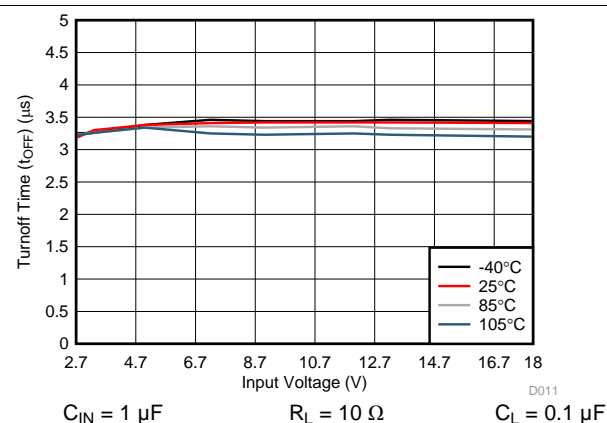
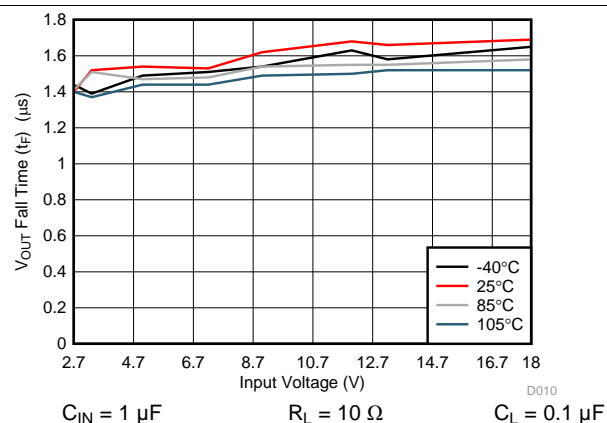
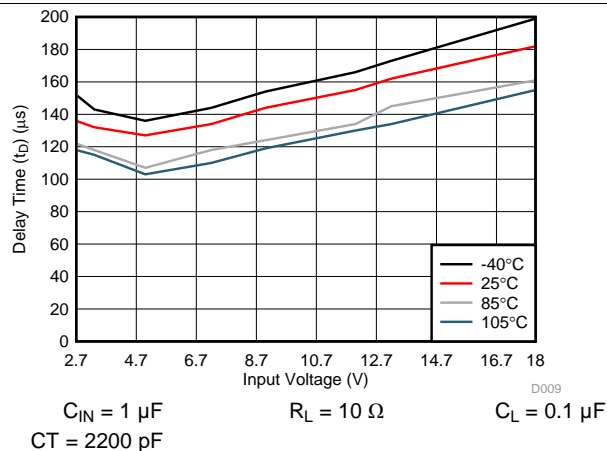
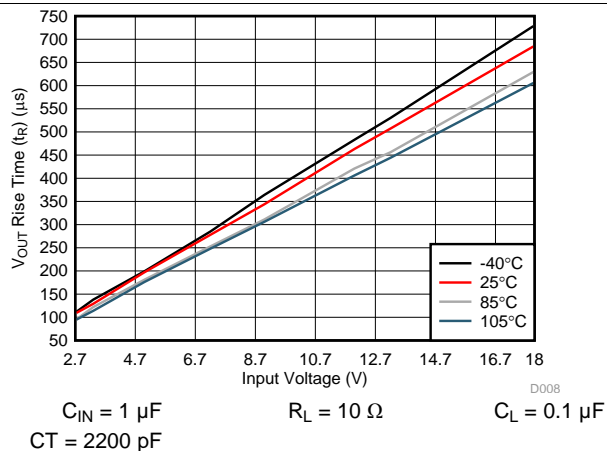


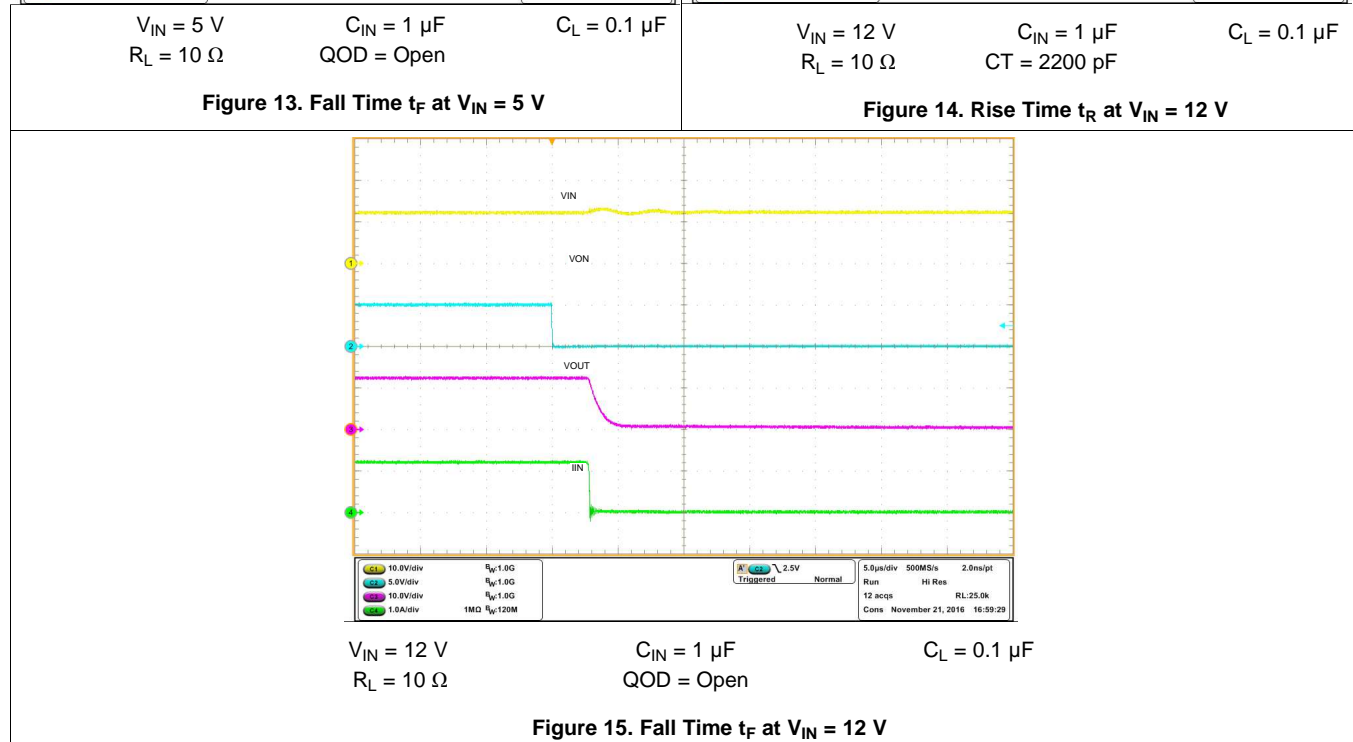
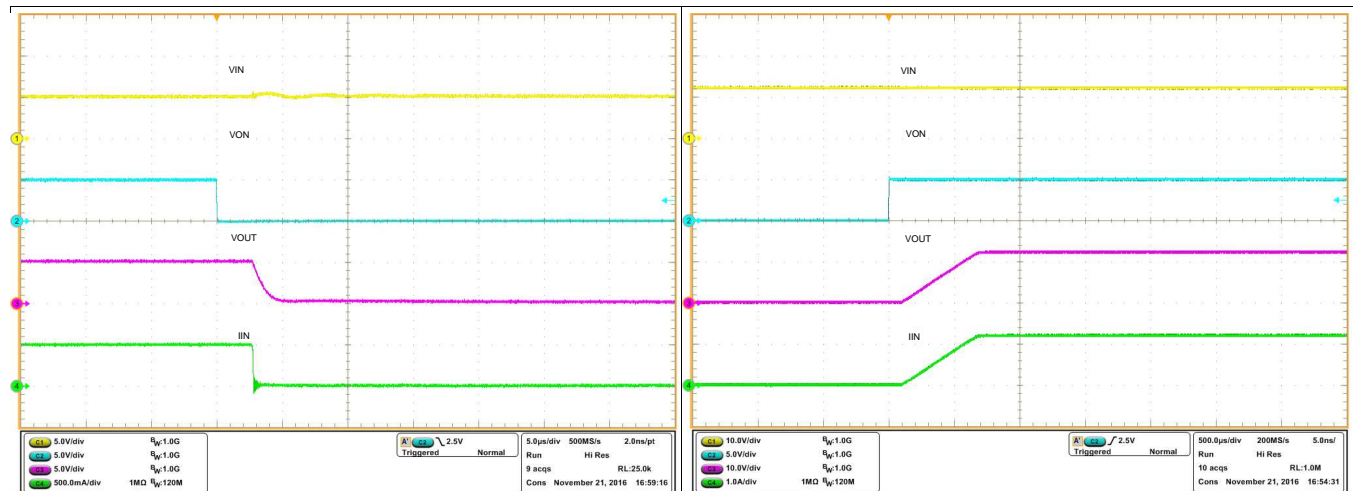
Figure 6. Output Pull-Down Resistance vs Input Voltage



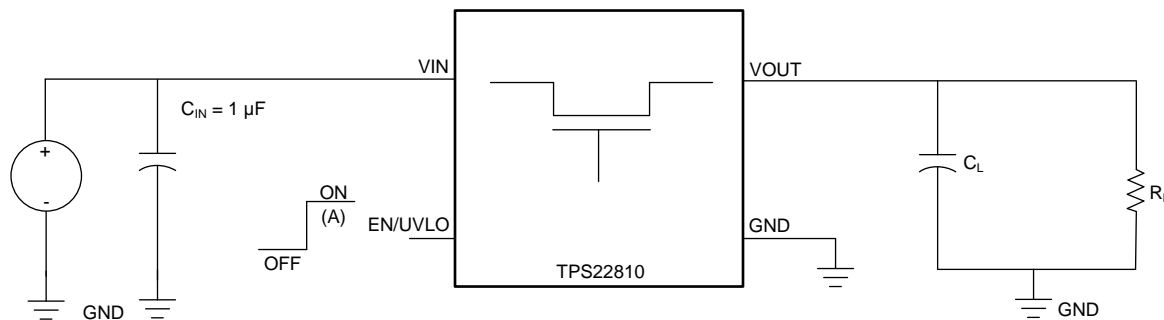
## 7.8 Typical AC Characteristics



## Typical AC Characteristics (continued)

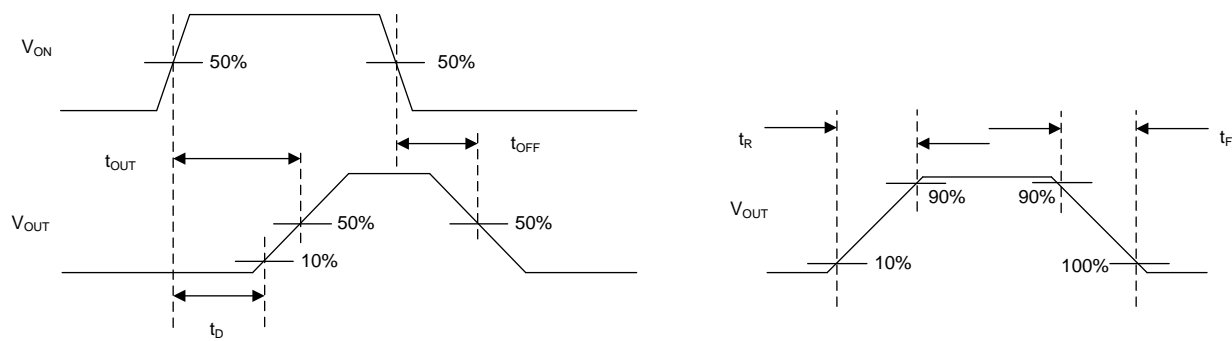


## 8 Parameter Measurement Information



A. Rise and fall times of the control signal are 100 ns

**Figure 16. Test Circuit**



**Figure 17. Timing Waveforms**

## 9 Detailed Description

### 9.1 Overview

The TPS22810 is a 6-pin, 2.7-18-V load switch with thermal protection in two separate package options. To reduce voltage drop for low voltage and high current rails, the device implements a low resistance N-channel MOSFET which reduces the drop out voltage across the device.

The device starts its operation by monitoring the VIN bus. When VIN exceeds the undervoltage-lockout threshold (VUVR), the device samples the EN/UVLO pin. A high level on this pin enables the internal MOSFET. As VIN rises, the internal MOSFET of the device starts conducting and allow current to flow from VIN to VOUT. When EN/UVLO is held low (below VENF), internal MOSFET is turned off.

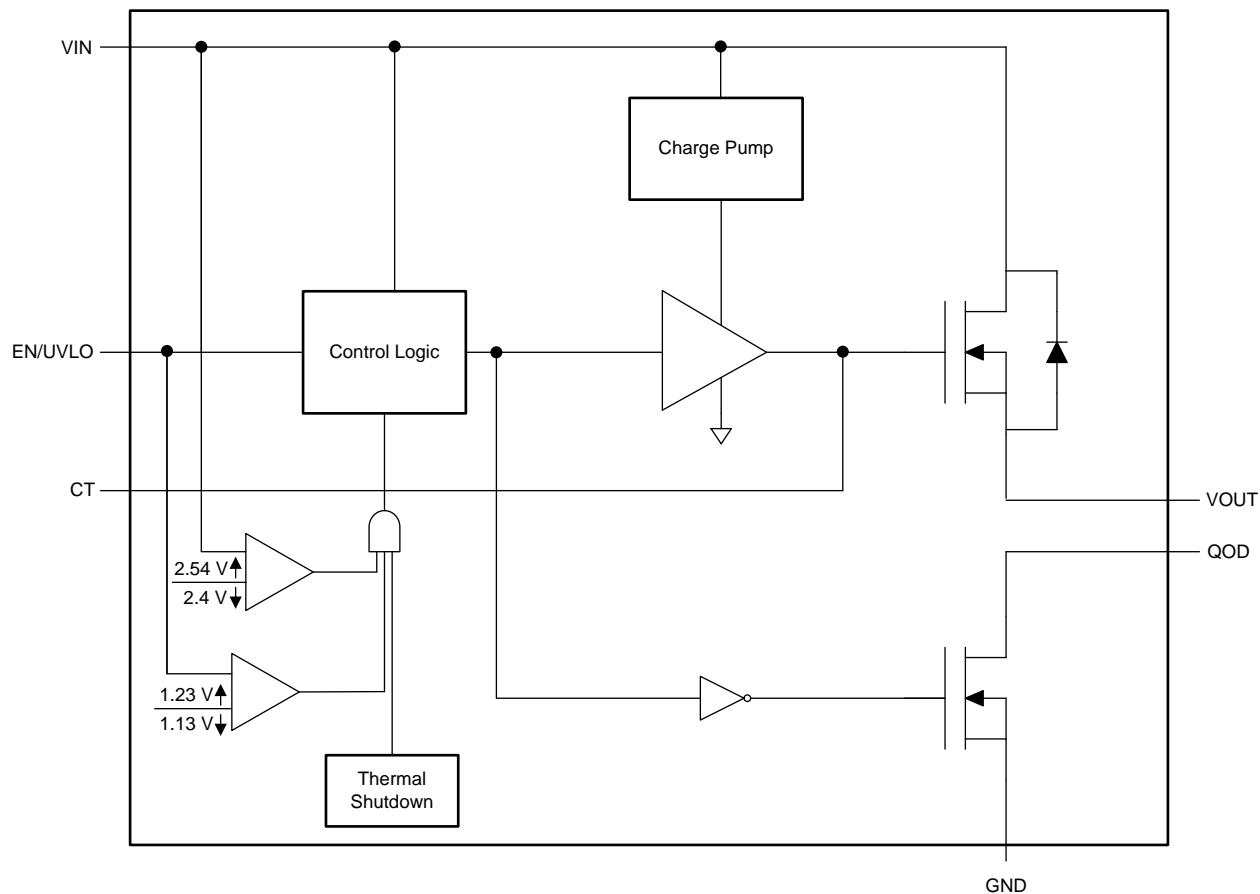
A voltage  $V(EN/UVLO) < V(ENF)$  on this pin turns off the internal FET, thus disconnecting VIN from VOUT, while voltage below  $V(SHUTF)$  takes the device into shutdown mode, with IQ less than 1  $\mu A$  to ensure minimal power loss.

The device has a configurable slew rate which helps reduce or eliminate power supply droop because of large inrush currents. The device also features an internal RPD resistor, which discharges VOUT once the switch is disabled.

During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, driver, charge pump, and output discharge FET eliminates the need for any external components which reduces solution size and bill of materials (BOM) count.

The device also features a QOD pin, which allows the configuration of the discharge rate of VOUT once the switch is disabled.

The device has a thermal protection feature. Due to this device protects itself against thermal damage due to over-temperature and over-current conditions. Safe Operating Area (SoA) requirements are thus inherently met without any special design consideration by the board designer.



## Feature Description (continued)

- QOD pin is unused and left floating. Using this method, there is no quick output discharge functionality, and the output remains floating after the switch is disabled.

Note that during thermal shutdown, the QOD functionality is not available. The device does not discharge the load as RPD does not become engaged.

The fall times of the device depend on many factors including the total resistance of the QOD,  $V_{IN}$ , and the output capacitance. When QOD is connected to VOUT, the fall time changes over  $V_{IN}$  as the internal  $R_{PD}$  varies over  $V_{IN}$ . To calculate the approximate fall time of  $V_{OUT}$  for a given  $R_{QOD}$ , use Equation 2 and Table 1.

$$V_{CAP} = V_{IN} \times e^{-t/\tau}$$

where

- $V_{CAP}$  is the voltage across the capacitor (V)
- $t$  is the time since power supply removal (s)
- $\tau$  is the time constant equal to  $R_{QOD} \times C_L$

(2)

The fall times' dependency on  $V_{IN}$  becomes minimal as the QOD value increases with additional external resistance. See Table 1 for QOD fall times.

**Table 1. QOD Fall Times**

$V_{IN}$ (V)	FALL TIME ( $\mu$ s) 90% - 10%, $C_{IN} = 1 \mu$ F, $I_{OUT} = 0$ A, $V_{IN} = 0$ V, ON = 0 V <sup>(1)</sup>					
	$T_A = 25^\circ\text{C}$			$T_A = 85^\circ\text{C}$		
	$C_L = 1 \mu$ F	$C_L = 10 \mu$ F	$C_L = 100 \mu$ F	$C_L = 1 \mu$ F	$C_L = 10 \mu$ F	$C_L = 100 \mu$ F
18	470	4700	47000	470	4700	47000
12	450	4500	45000	450	4500	45000
9	440	4400	44000	440	4400	44000
5	500	5000	50000	480	4800	48000
3.3	600	6000	60000	570	5700	57000

(1) TYPICAL VALUES WITH QOD SHORTED TO VOUT

### 9.3.2.1 QOD when System Power is Removed

The adjustable QOD can be used to control the power down sequencing of a system even when the system power supply is removed. When the power is removed, the input capacitor,  $C_{IN}$ , discharges at  $V_{IN}$ . Past the set UVLO level, the pull-down resistance RPD becomes disabled and the output no longer becomes discharged. If there is still remaining charge on the output capacitor, this results in longer fall times. Care must be taken such that  $C_{IN}$  is large enough to meet the device UVLO settings.

### 9.3.2.2 Internal QOD Considerations

Special considerations must be taken when using the internal  $R_{PD}$  by shorting the QOD pin to the VOUT pin. The internal  $R_{PD}$  is a pulldown resistance designed to quickly discharge a load after the switch has been disabled. Care must be used to ensure that excessive current does not flow through  $R_{PD}$  during discharge so that the maximum  $T_J$  of  $125^\circ\text{C}$  is not exceeded. When using only the internal  $R_{PD}$  to discharge a load, the total capacitive load must not exceed 200  $\mu$ F. Otherwise, an external resistor,  $R_{EXT}$ , must be used to ensure the amount of current flowing through  $R_{PD}$  is properly limited and the maximum  $T_J$  is not exceeded. To ensure the device is not damaged, the remaining charge from  $C_L$  needs to decay naturally through the internal QOD resistance and must not be driven.

### 9.3.3 EN/UVLO

As an input pin, EN/UVLO controls the ON and OFF state of the internal MOSFET. In its high state, the internal MOSFET is enabled. A low on this pin turns off the internal MOSFET. High and Low levels are specified in the parametric table of the datasheet

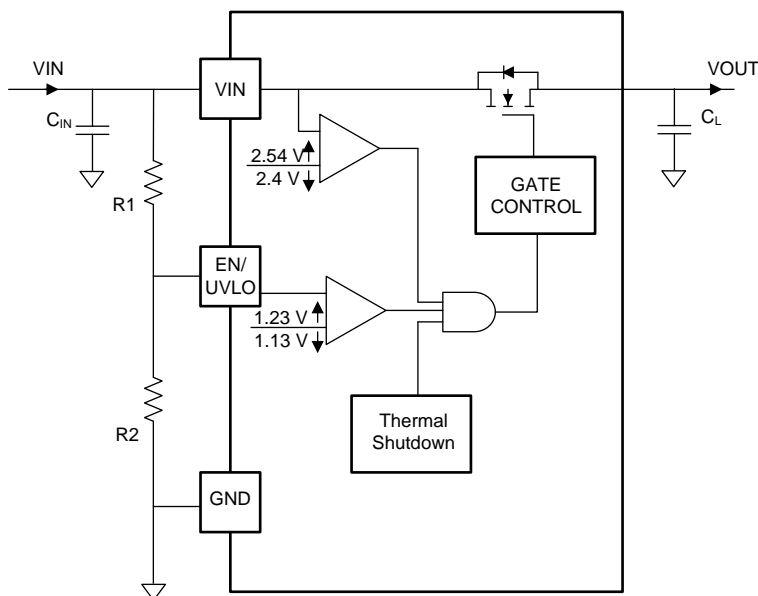
A voltage  $V(\text{EN/UVLO} < V(\text{ENF}))$  on this pin turns off the internal FET, thus disconnecting  $V_{IN}$  from VOUT, while voltage below  $V(\text{SHUTF})$  takes the device into shutdown mode, with  $I_Q$  less than 1  $\mu$ A to ensure minimal power loss.

The EN/UVLO pin can be directly driven by a 1.8 V, 3.3 V or 5 V general purpose output pin.

The internal de-glitch delay on EN/UVLO falling edge is intentionally kept low (2.5  $\mu$ s typical) for quick detection of power failure. For applications where a higher de-glitch delay on EN/UVLO is desired, or when the supply is particularly noisy, it is recommended to use an external bypass capacitor from EN/UVLO to GND.

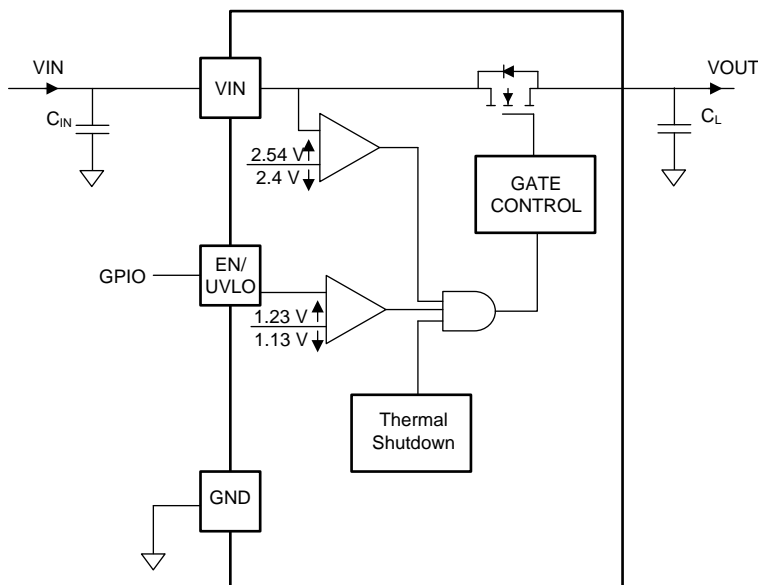
The undervoltage lock out can be programmed by using an external resistor divider from supply VIN terminal to EN/UVLO terminal to GND as shown in Figure 18. When an undervoltage or input power fail event is detected, the internal FET is quickly turned off. If the Under-Voltage Lock-Out function is not needed, the EN/UVLO terminal must be connected to the VIN terminal. EN/UVLO terminal must not be left floating.

The device also implements internal undervoltage-lockout (UVLO) circuitry on the VIN terminal. The device disables when the VIN terminal voltage falls below internal UVLO Threshold V(UVF). The internal UVLO threshold has a hysteresis of 125 mV (5% of V(UVR)). See Figure 19 and Figure 20.



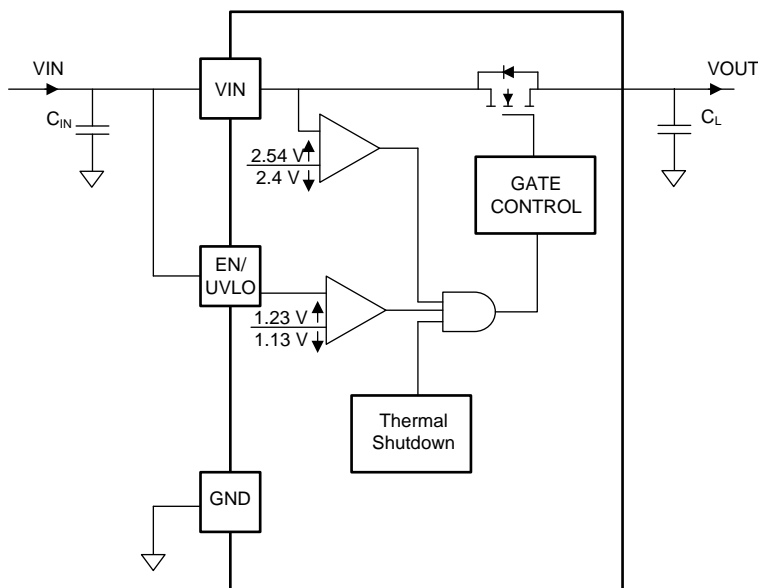
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**Figure 18. Configuring UVLO with External Resistor Network**



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**Figure 19. Using 1.8 V/3.3 V GPIO Signal Directly from Processor**



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**Figure 20. Default UVLO Threshold V(UVR) Using No Additional External Components**

### 9.3.4 Adjustable Rise Time (CT)

A capacitor to GND on the CT pin sets the slew rate. The voltage on the CT pin can be as high as 2.5 V. An approximate formula for the relationship between CT and slew rate is shown in [Equation 3](#). This equation accounts for 10% to 90% measurement on VOUT and does NOT apply for CT < 1 nF.

Use [Table 2](#) to determine rise times for when CT ≥ 1 nF.

$$SR = 46.62 / C_t$$

where

- SR is the slew rate (in V/μs)



- CT is the the capacitance value on the CT pin (in pF)
- The units for the constant a are  $\mu\text{s}/\text{V}$ . The units for the constant b are  $\mu\text{s}/(\text{V} \times \text{pF})$ . (3)

Rise time can be calculated by multiplying the input voltage by the slew rate. [Table 2](#) contains rise time values measured on a typical device. Rise times shown below are only valid for the power-up sequence where VIN is already in steady state condition before the EN/UVLO pin is asserted high.

**Table 2. Rise Time Table**

CT (pF)	RISE TIME ( $\mu\text{s}$ ) 10% - 90%, $C_L = 0.1 \mu\text{F}$ , $C_{IN} = 1 \mu\text{F}$ , $R_L = 10 \Omega$				
	VIN = 18 V	VIN = 12 V	VIN = 9 V	VIN = 5 V	VIN = 3.3 V
0	115	91	78	60	98
470	136	94	80	63	98
1000	310	209	158	91	102
2200	688	464	345	198	135
4700	1430	957	704	397	265
10000	3115	2085	1540	864	550
27000	8230	5460	4010	2245	1430

### 9.3.5 Thermal Shutdown

The switch disables when the junction temperature ( $T_J$ ) rises above the thermal shutdown threshold,  $T_{SD}$ . The switch re-enables once the temperature drops below the  $T_{SD} - T_{SD,HYS}$  value.

## 9.4 Device Functional Modes

The features of the TPS22810 depend on the operating mode. [Table 3](#) summarizes the Device Functional Modes.

**Table 3. Function Table**

EN/UVLO	Device State
L	Disabled
H	Enabled

## 10 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available in the product page of this device on [www.ti.com](http://www.ti.com) (See the [Device Support](#) section for more information).

#### 10.1.1 ON and OFF Control

The EN/UVLO pin controls the state of the switch. Asserting EN/UVLO high enables the switch. EN/UVLO is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The EN/UVLO pin is compatible with standard GPIO logic thresholds. It can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

#### 10.1.2 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor, a capacitor needs to be placed between VIN and GND. A 1- $\mu$ F ceramic capacitor,  $C_{IN}$ , placed close to the pins, is usually sufficient. Higher values of  $C_{IN}$  can be used to further reduce the voltage drop during high current applications. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

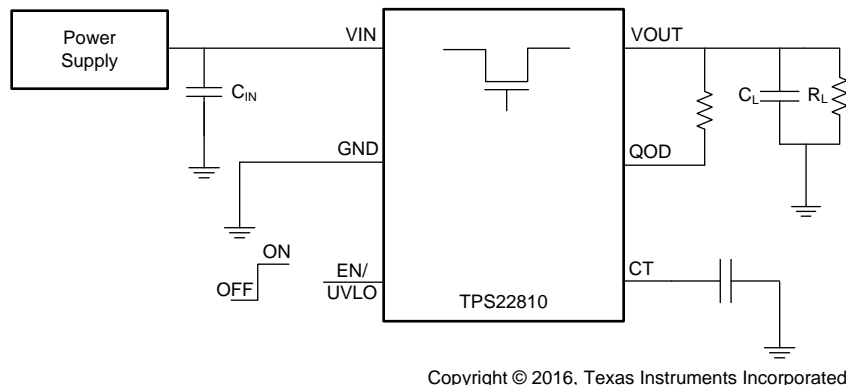
#### 10.1.3 Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, a  $C_{IN}$  greater than  $C_L$  is highly recommended. A  $C_L$  greater than  $C_{IN}$  can cause VOUT to exceed VIN when the system supply is removed. This can result in current flow through the body diode from VOUT to VIN. A  $C_{IN}$  to  $C_L$  ratio of 10 to 1 is recommended for minimizing VIN dip caused by inrush currents during startup; however, a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) can cause slightly more VIN dip upon turnon due to inrush currents.

This can be mitigated by increasing the capacitance on the CT pin for a longer rise time.

### 10.2 Typical Application

This typical application demonstrates how the TPS22810 can be used to power downstream modules.



**Figure 21. Typical Application Schematic**

## Typical Application (continued)

### 10.2.1 Design Requirements

For this design example, use the values listed in [Table 4](#) as the design parameters:

**Table 4. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
$V_{IN}$	12 V
Load current	2 A
$C_L$	22 $\mu$ F
Desired fall time	20 ms
Maximum acceptable inrush current	400 mA

### 10.2.2 Detailed Design Procedure

#### 10.2.2.1 Shutdown Sequencing During Unexpected Power Loss

Using the adjustable Quick Output Discharge function of the TPS22810, adding a load switch to each power rail can be used to manage the power down sequencing in the event of an unexpected power loss (that is battery removal). To determine the QOD values for each load switch, first confirm the power down order of the device you wish to power sequence. Be sure to check if there are voltage or timing margins that must be maintained during power down. Next, consult [Table 1](#) to determine appropriate  $C_L$  and  $R_{QOD}$  values for each power rail's load switch so that the load switches' fall times correspond to the order in which they need to be powered down. In the above example, we must have this power rail's fall time to be 4 ms. Using [Equation 2](#), we can determine the appropriate  $R_{QOD}$  to achieve our desired fall time.

Since fall times are measured from 90% of  $V_{OUT}$  to 10% of  $V_{OUT}$ , using [Equation 2](#), we get [Equation 4](#) and [Equation 5](#).

$$1.2V = 10.8V \times e^{-(20ms)/(R_{QOD} \times (22\mu F))} \quad (4)$$

$$R_{QOD} = 413.7 \, \Omega \quad (5)$$

Consulting [Figure 6](#),  $R_{PD}$  at  $V_{IN} = 12$  V is approximately 250  $\Omega$ . Using [Equation 1](#), the required external QOD resistance can be calculated as shown in [Equation 6](#) and [Equation 7](#).

$$413.7 \, \Omega = 250 \, \Omega + R_{EXT} \quad (6)$$

$$R_{EXT} = 163.7 \, \Omega \quad (7)$$

[Figure 22](#) through [Figure 25](#) are scope shots demonstrating an example of the QOD functionality when power is removed from the device (both ON and VIN are disconnected simultaneously). In the scope shots, the  $V_{IN} = 12$  V and correspond to when  $R_{QOD} = 1000 \, \Omega$ ,  $R_{QOD} = 500 \, \Omega$ , and QOD = VOUT with two values of  $C_L = 10 \, \mu$ F and 22  $\mu$ F.

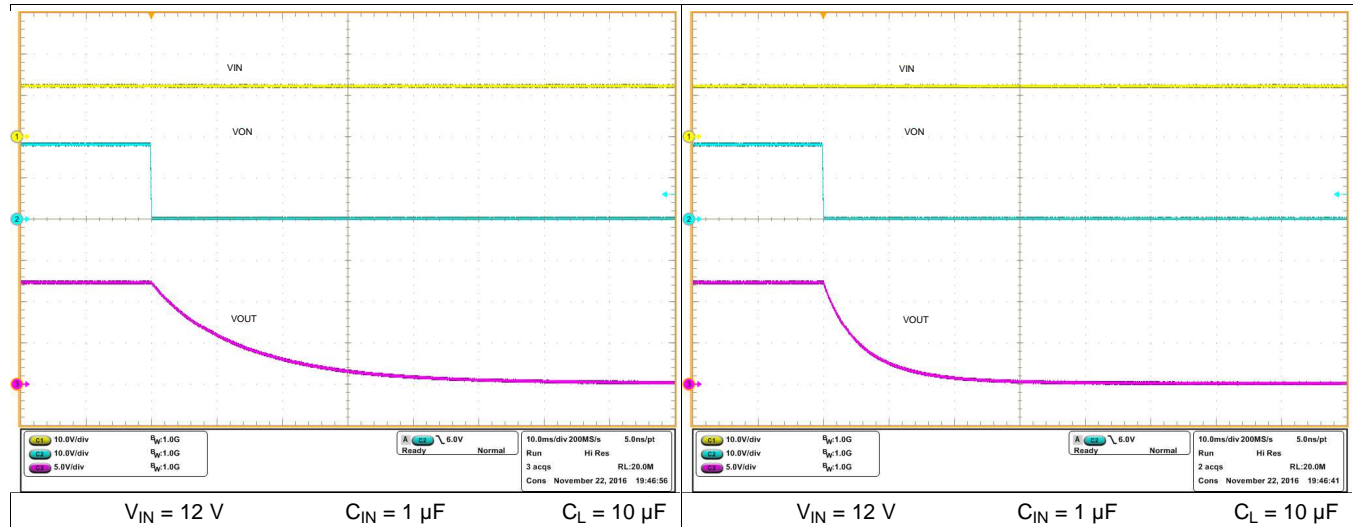


Figure 22. Fall Time  $t_F$  at  $V_{IN} = 12\text{ V}$ ,  $R_{QOD} = 1000\text{ }\Omega$

Figure 23. Fall Time  $t_F$  at  $V_{IN} = 12\text{ V}$ ,  $R_{QOD} = 500\text{ }\Omega$

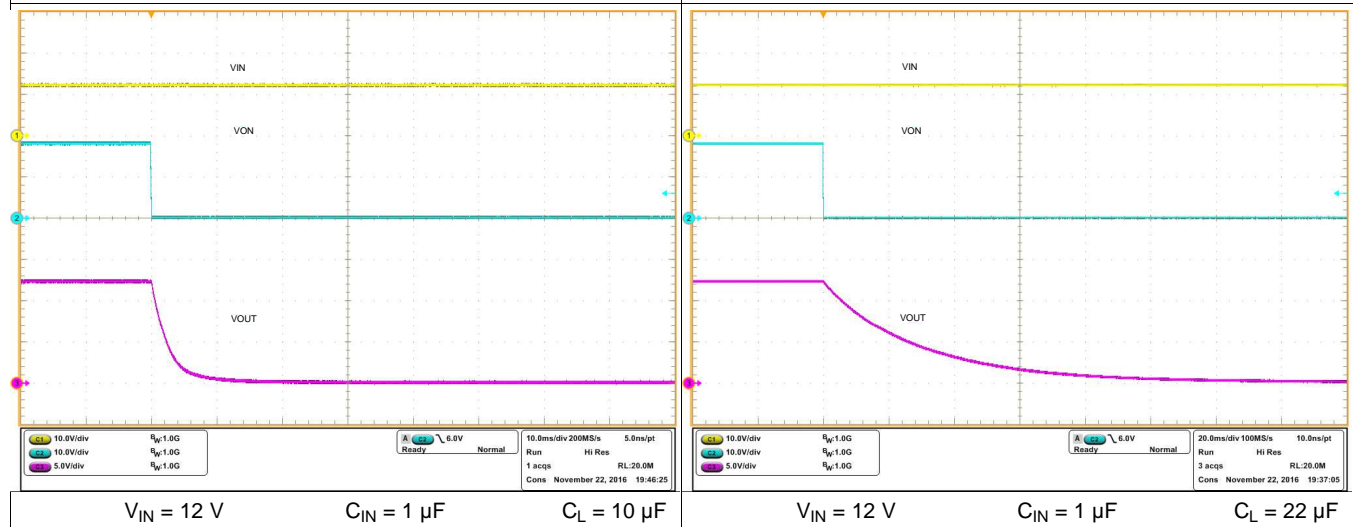
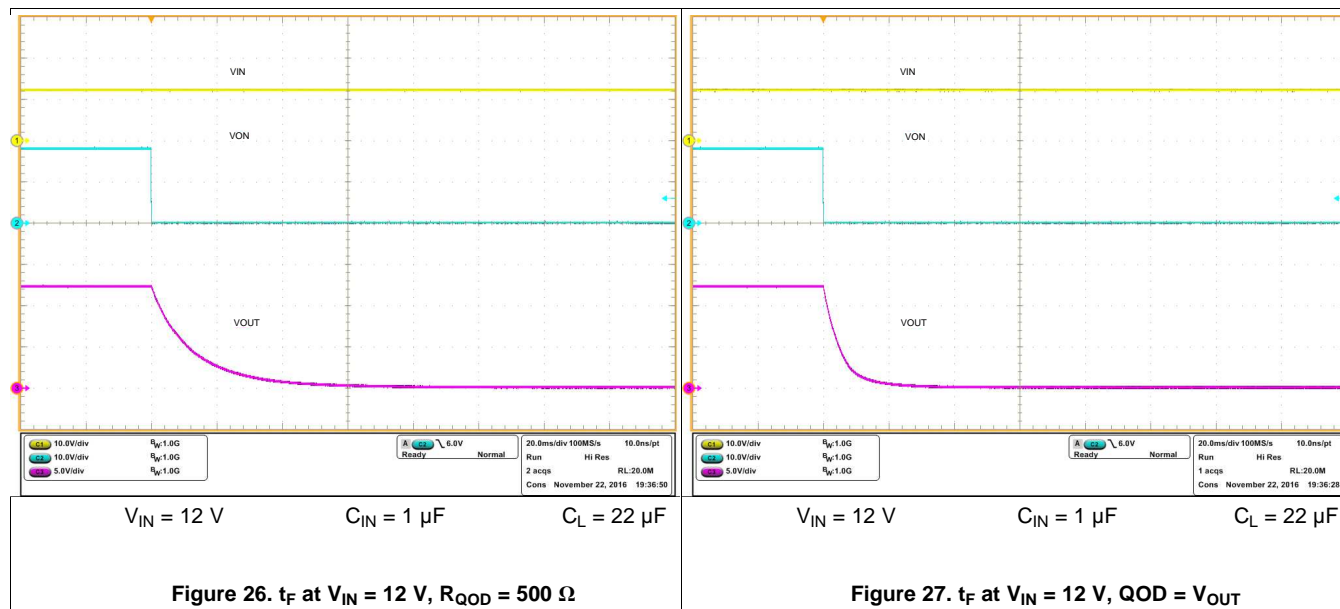


Figure 24.  $t_F$  at  $V_{IN} = 12\text{ V}$ ,  $QOD = V_{OUT}$

Figure 25.  $t_F$  at  $V_{IN} = 12\text{ V}$ ,  $R_{QOD} = 1000\text{ }\Omega$



### 10.2.2.2 VIN to VOUT Voltage Drop

The VIN to VOUT voltage drop in the device is determined by the  $R_{ON}$  of the device and the load current. The  $R_{ON}$  of the device depends upon the VIN conditions of the device. Refer to the  $R_{ON}$  specification of the device in the [Electrical Characteristics](#) table of this datasheet. Once the  $R_{ON}$  of the device is determined based upon the VIN conditions, use [Equation 8](#) to calculate the VIN to VOUT voltage drop.

$$\Delta V = I_{LOAD} \times R_{ON}$$

where

- $\Delta V$  is the voltage drop from VIN to VOUT
- $I_{LOAD}$  is the load current
- $R_{ON}$  is the On-resistance of the device for a specific  $V_{IN}$

(8)

An appropriate  $I_{LOAD}$  must be chosen such that the  $I_{MAX}$  specification of the device is not violated.

### 10.2.2.3 Inrush Current

To determine how much inrush current is caused by the  $C_L$  capacitor, use [Equation 9](#).

$$I_{INRUSH} = C_L \times \frac{dV_{OUT}}{dt}$$

where

- $I_{INRUSH}$  is the amount of inrush caused by  $C_L$
- $C_L$  is the capacitance on VOUT
- $dt$  is the Output Voltage rise time during the ramp up of VOUT when the device is enabled
- $dV_{OUT}$  is the change in  $V_{OUT}$  during the ramp up of VOUT when the device is enabled

(9)

The appropriate rise time can be calculated using the design requirements and the inrush current equation. As we calculate the rise time (measured from 10% to 90% of  $V_{OUT}$ ), we account for this in our  $dV_{OUT}$  parameter (80% of  $V_{OUT} = 9.6\text{ V}$ ) as shown in [Equation 10](#) and [Equation 11](#).

$$400\text{ mA} = 22\ \mu\text{F} \times 9.6\text{ V}/dt \quad (10)$$

$$dt = 528\ \mu\text{s} \quad (11)$$

To ensure an inrush current of less than 400 mA, choose a CT value that yields a rise time of more than 528  $\mu\text{s}$ . Consulting [Table 2](#) at  $V_{IN} = 12\text{ V}$ , CT = 4700 pF provides a typical rise time of 957  $\mu\text{s}$ . Using this rise time and voltage into [Equation 9](#), yields [Equation 12](#) and [Equation 13](#).

$$I_{Inrush} = 22\ \mu\text{F} \times 9.6\text{ V}/957\ \mu\text{s} \quad (12)$$

$$I_{Inrush} = 220\text{ mA} \quad (13)$$

## TPS22810

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An appropriate  $C_L$  value must be placed on VOUT such that the  $I_{MAX}$  and  $I_{PLS}$  specifications of the device are not violated.

### 10.2.3 Application Curves

See the oscilloscope captures below for an example of how the CT capacitor can be used to reduce inrush current for  $V_{IN} = 12\text{ V}$ . See the [Adjustable Rise Time \(CT\)](#) section for rise times for corresponding CT values.

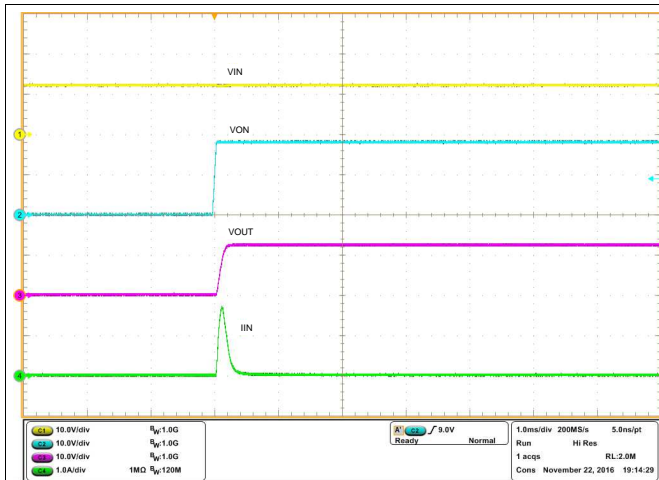


Figure 28. TPS22810 Inrush Current With  $C_L = 22\text{ }\mu\text{F}$ ,  $C_T = 0\text{ pF}$

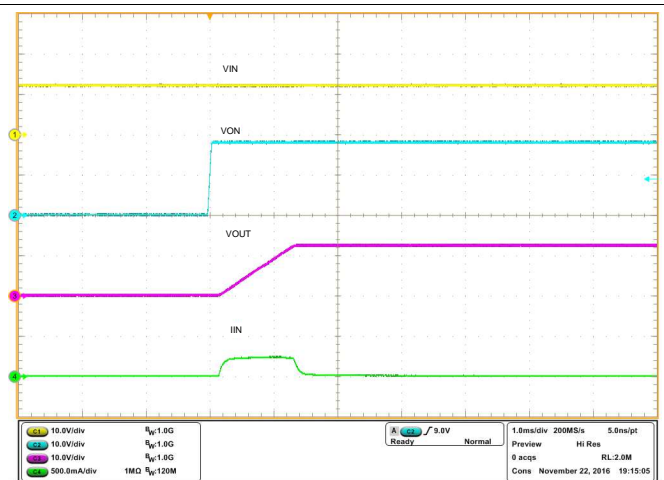


Figure 29. TPS22810 Inrush Current with  $C_L = 22\text{ }\mu\text{F}$ ,  $C_T = 4700\text{ pF}$

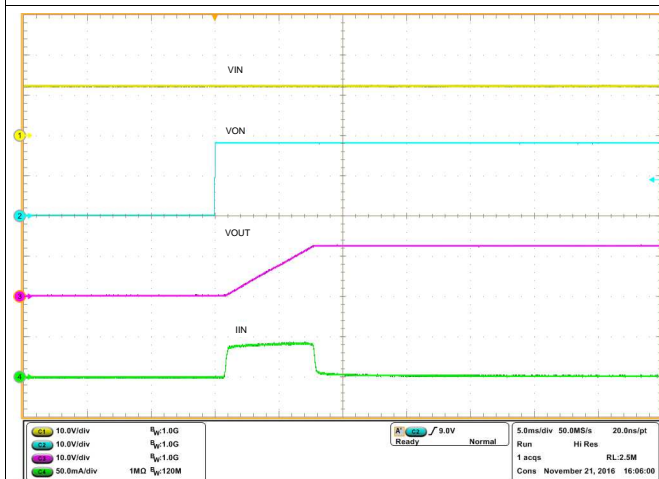


Figure 30. TPS22810 Inrush Current With  $C_L = 22\text{ }\mu\text{F}$ ,  $C_T = 27000\text{ pF}$

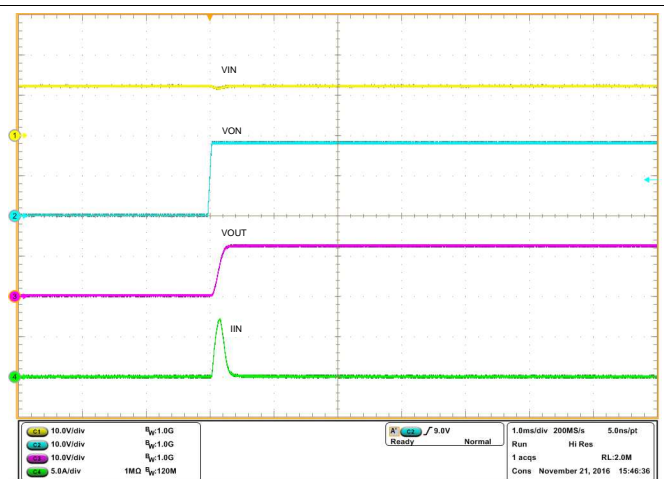
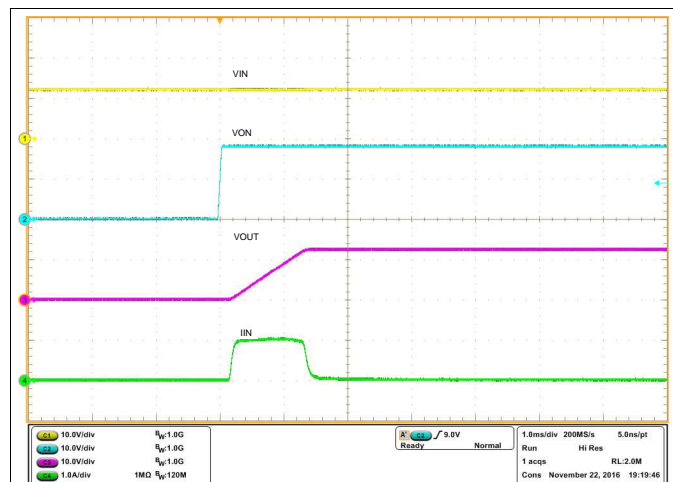
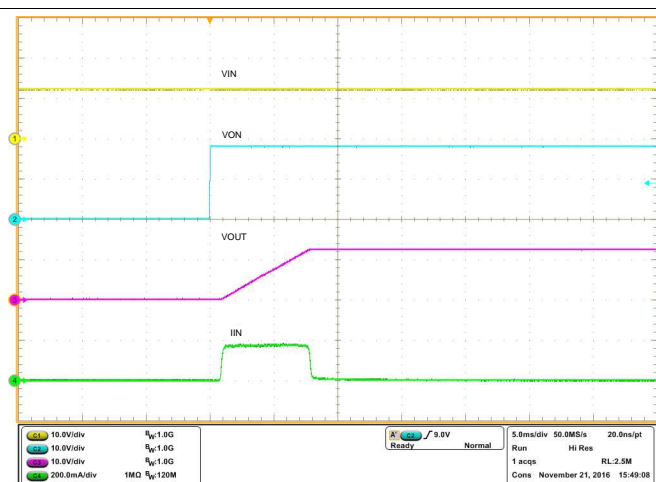


Figure 31. TPS22810 Inrush Current With  $C_L = 100\text{ }\mu\text{F}$ ,  $C_T = 0\text{ pF}$



**Figure 32. TPS22810 Inrush Current  
With  $C_L = 100 \mu\text{F}$ ,  $C_T = 4700 \text{ pF}$**



**Figure 33. TPS22810 Inrush Current  
With  $C_L = 100 \mu\text{F}$ ,  $C_T = 27000 \text{ pF}$**

## 11 Power Supply Recommendations

The device is designed to operate from a  $V_{IN}$  range of 2.7 V to 18 V. This supply must be well regulated and placed as close to the device terminal as possible with the recommended 1- $\mu\text{F}$  bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 1  $\mu\text{F}$  may be sufficient.

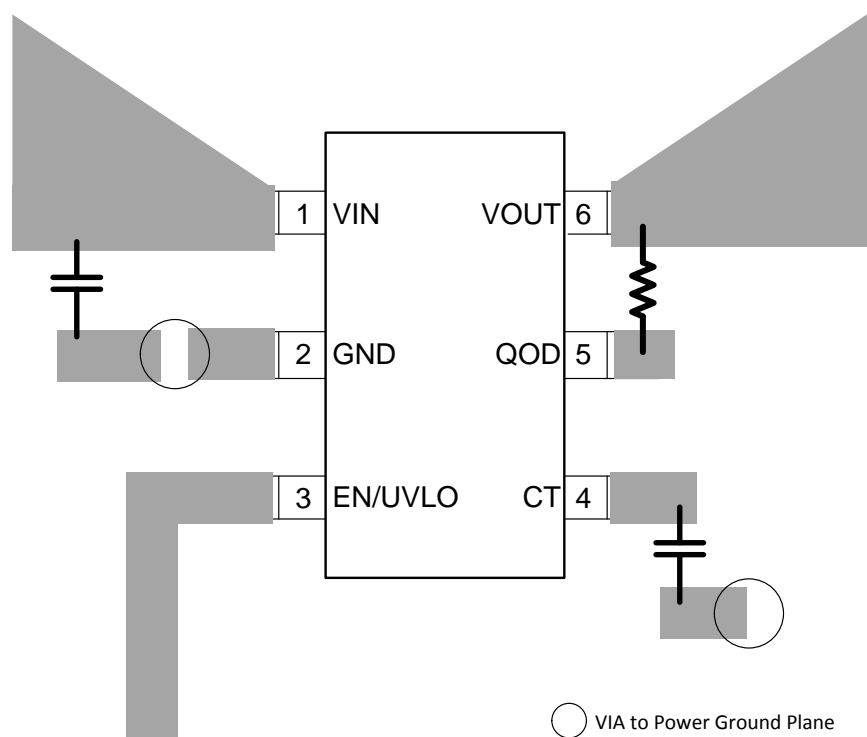
The TPS22810 operates regardless of power sequencing order. The order in which voltages are applied to  $V_{IN}$  and ON does not damage the device as long as the voltages do not exceed the absolute maximum operating conditions.

## 12 Layout

### 12.1 Layout Guidelines

1. VIN and VOUT traces must be as short and wide as possible to accommodate for high current.
2. The VIN pin must be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1-μF ceramic with X5R or X7R dielectric. This capacitor must be placed as close to the device pins as possible.

### 12.2 Layout Example



**Figure 34. Recommended Board Layout**

### 12.3 Thermal Considerations

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

The maximum IC junction temperature must be restricted to 150°C under normal operating conditions. To calculate the maximum allowable dissipation,  $P_{D(max)}$  for a given output current and ambient temperature, use [Equation 14](#).

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where

- $P_{D(MAX)}$  is the maximum allowable power dissipation
- $T_{J(MAX)}$  is the maximum allowable junction temperature (150°C for the TPS22810)
- $T_A$  is the ambient temperature of the device
- $\theta_{JA}$  is the junction to air thermal impedance. Refer to the [Thermal Information](#) table. This parameter is highly dependent upon board layout. (14)



## 13 Device and Documentation Support

### 13.1 Device Support

#### 13.1.1 Developmental Support

For the TPS22810 PSpice Transient Model, see [TPS22810 PSpice Transient Model](#)

### 13.2 Documentation Support

#### 13.2.1 Related Documentation

For related documentation see the following:

- [TPS22810 Load Switch Evaluation Module](#)
- [Selecting a Load Switch to Replace a Discrete Solution](#)
- [Timing of Load Switches](#)

### 13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on [ti.com](http://ti.com). In the upper right-hand corner, click the *Alert me* button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

### 13.4 Community Resources

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### 13.5 Trademarks

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### 13.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 13.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22810DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	19HF	<a href="#">Samples</a>
TPS22810DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	19HF	<a href="#">Samples</a>
TPS22810DRVVR	ACTIVE	WSO	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	1CRH	<a href="#">Samples</a>
TPS22810DRVVT	ACTIVE	WSO	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	1CRH	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

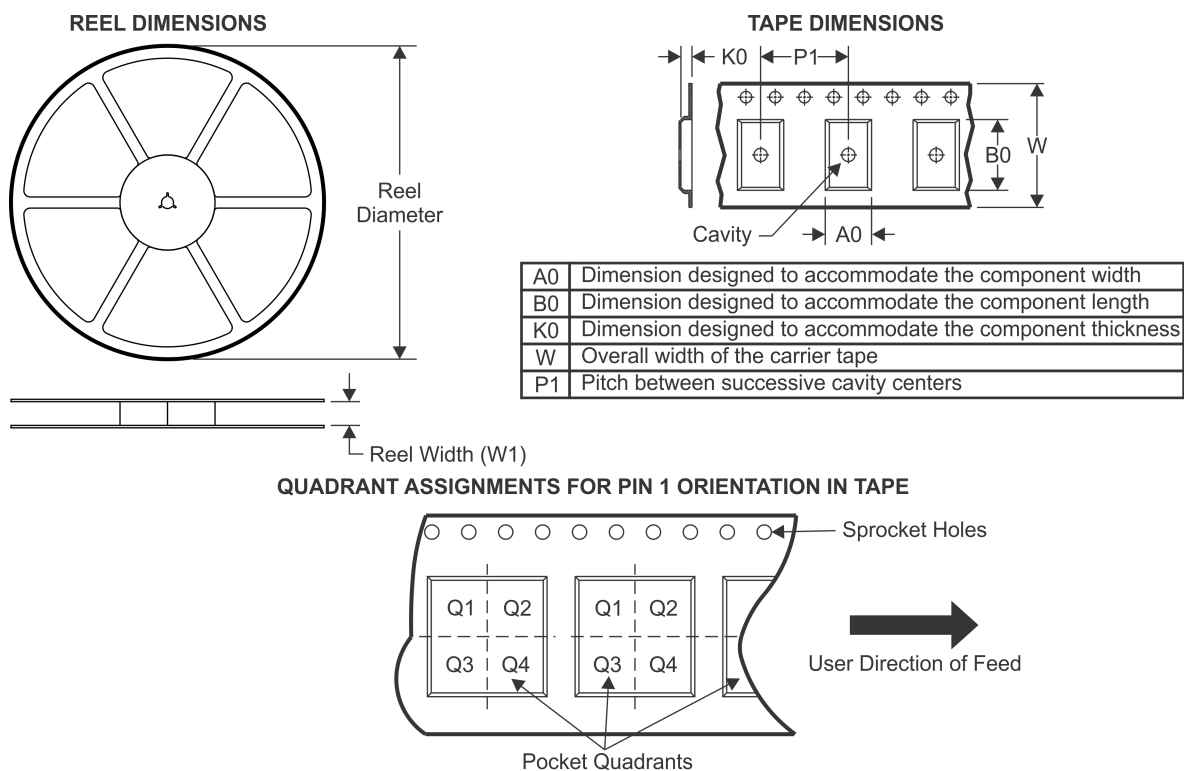
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22810DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS22810DBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS22810DRVR	WSO	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22810DRV	WSO	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

## TAPE AND REEL BOX DIMENSIONS

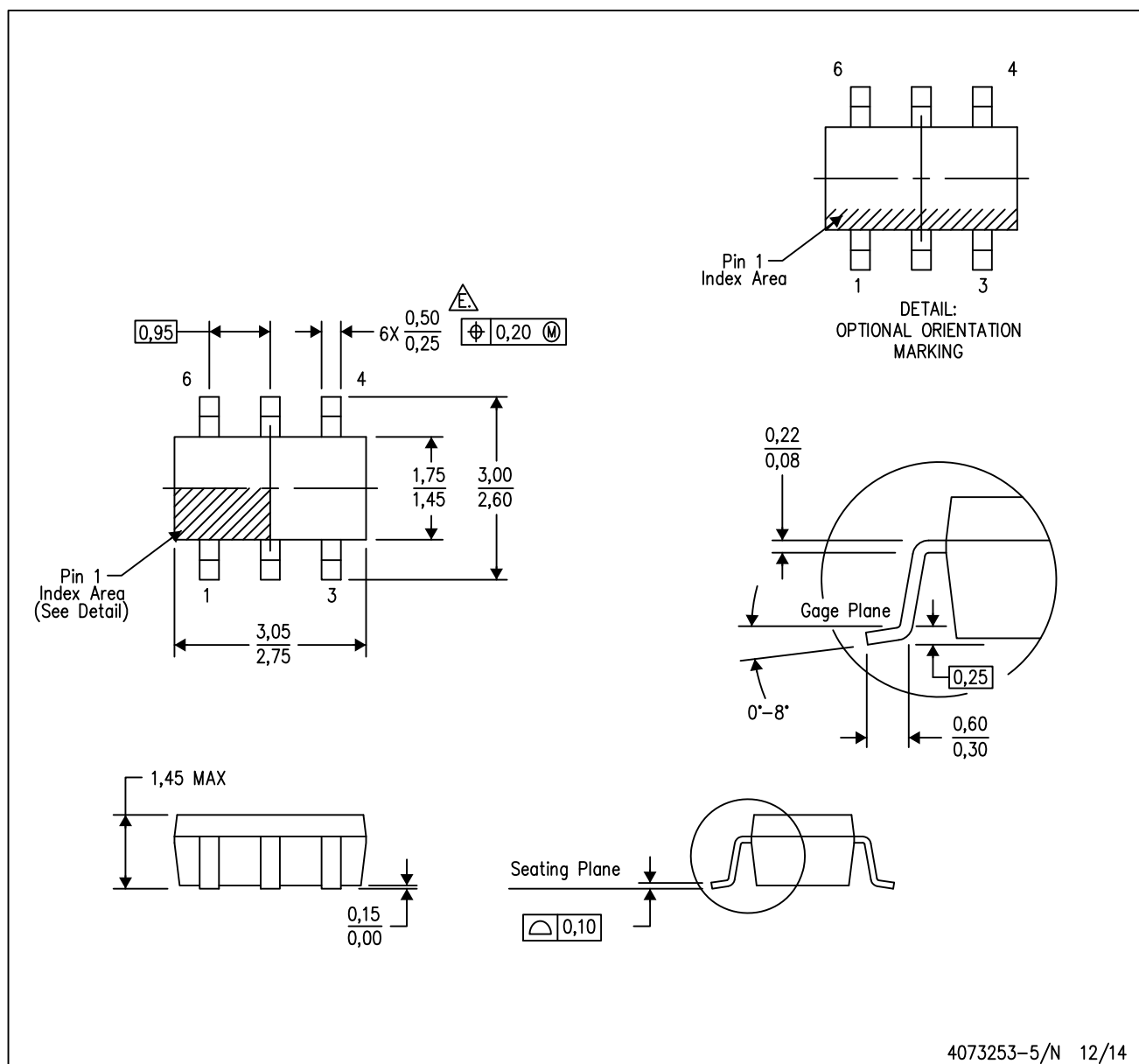


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22810DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS22810DBVT	SOT-23	DBV	6	250	210.0	185.0	35.0
TPS22810DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS22810DRVT	WSON	DRV	6	250	210.0	185.0	35.0

DBV (R-PDSO-G6)

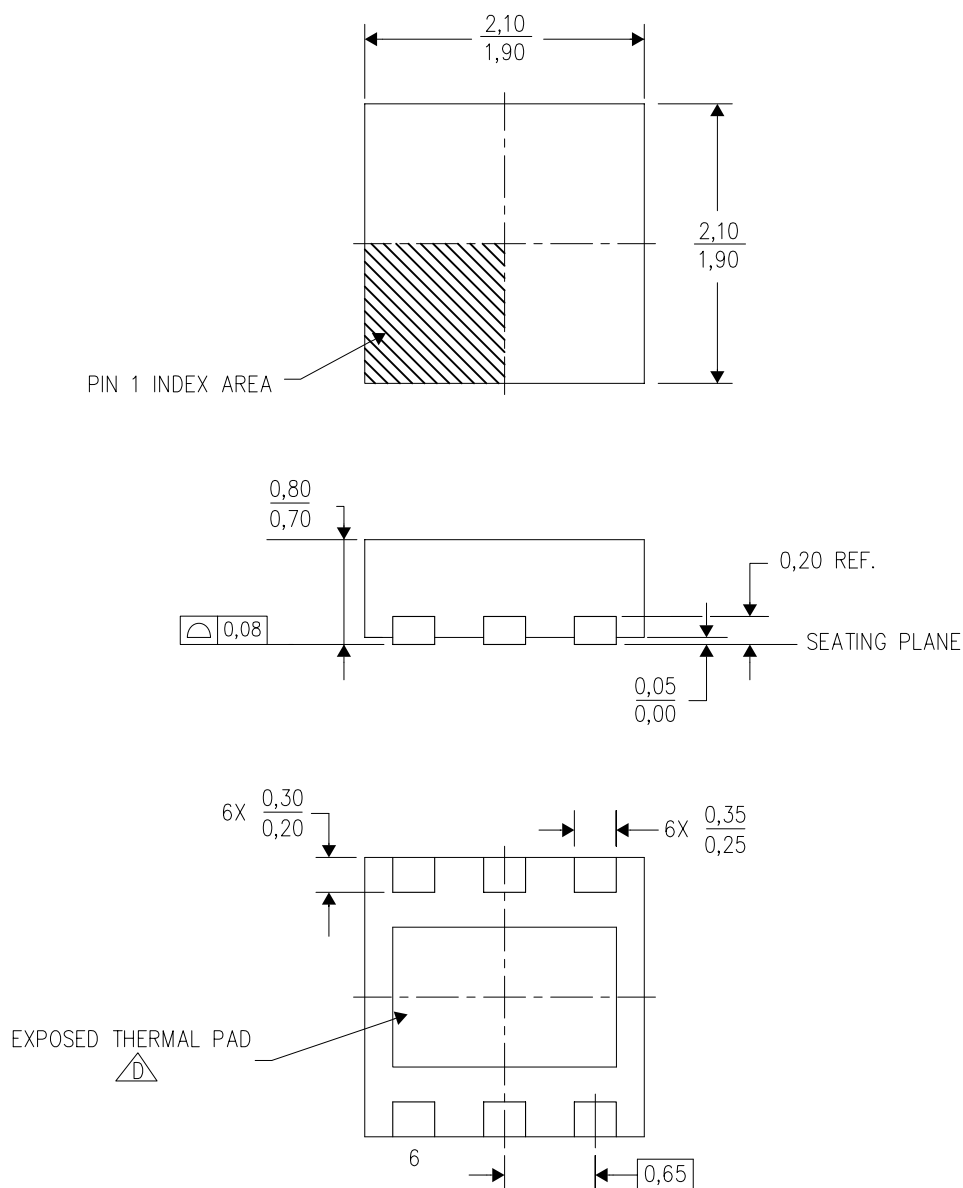
PLASTIC SMALL-OUTLINE PACKAGE




- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
  - E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DRV (S-PWSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



4206925/E 10/10

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Small Outline No-Lead (SON) package configuration.
  -  D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.



## THERMAL PAD MECHANICAL DATA

DRV (S-PWSON-N6)

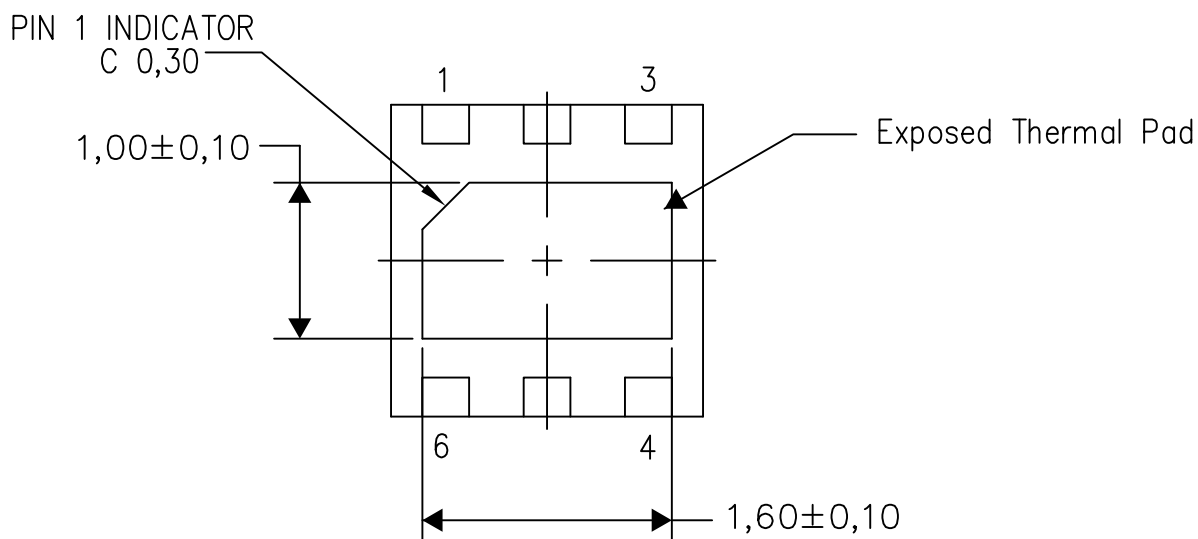
PLASTIC SMALL OUTLINE NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

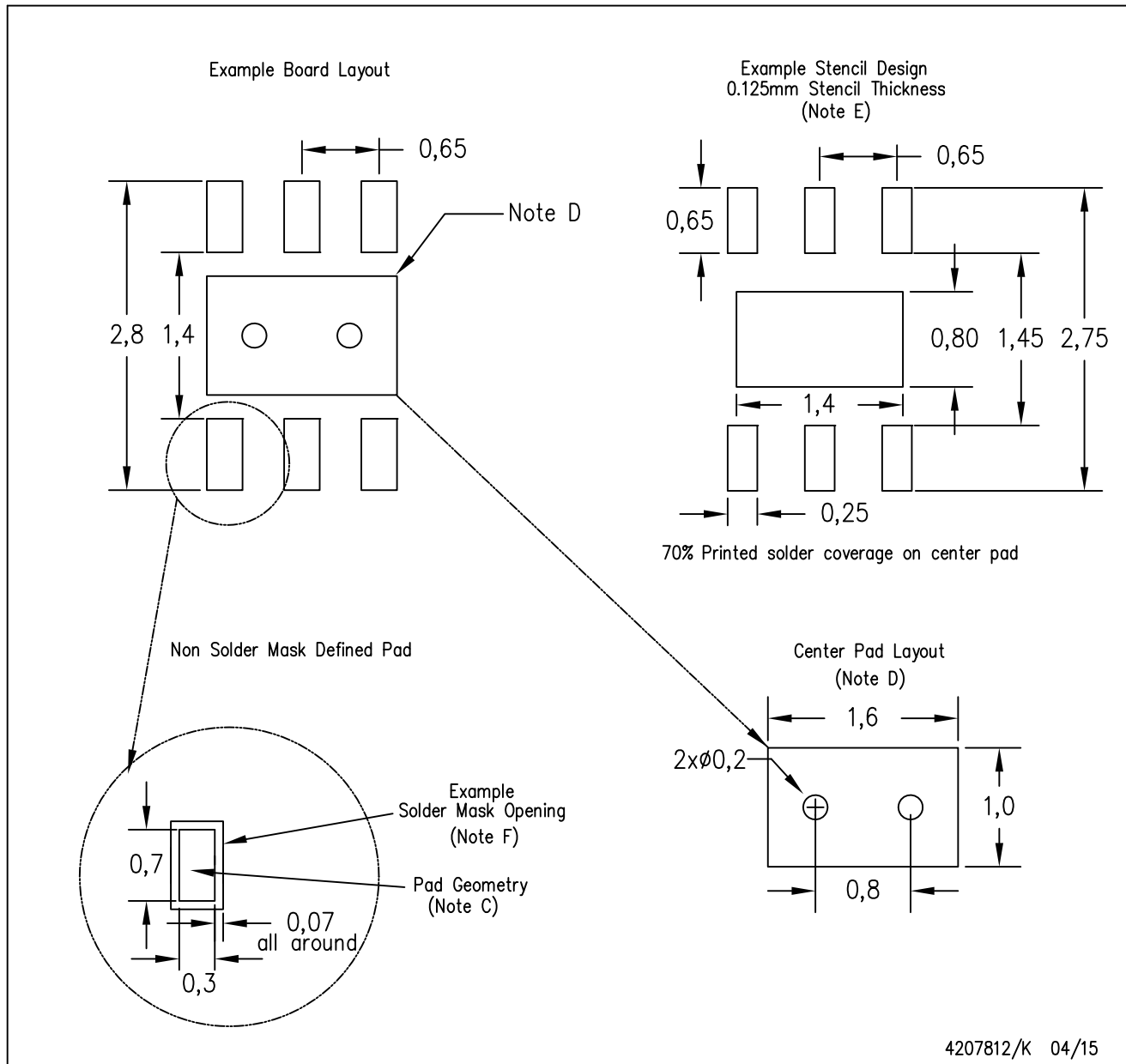
Exposed Thermal Pad Dimensions

4206926/Q 04/15

NOTE: All linear dimensions are in millimeters

DRV (S-PWSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for solder mask tolerances.

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