Radio Frequency Integrated Circuits and Systems Laboratory
-RFICS Lab-

Integrated Circuits Design For Communications

DESIGN OF DIFFERENTIAL AMPLIFIER WITH MOS LOAD

-MINIPROJECT 1-

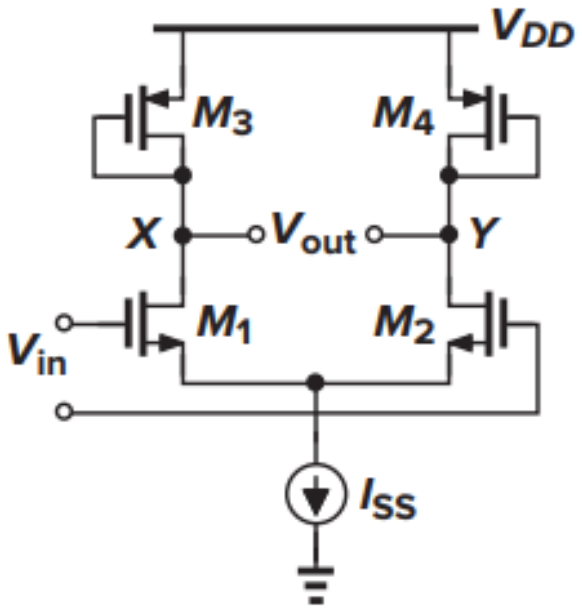
Student: Le Truong Quoc

Summary

❑ **Work plan for this week**

	Works	Results	Progress
1	Design of Differential pair with diode-connected	100%	Finish
2	Design of Differential pair with PMOS source follower	100%	Finish

Experiment 1



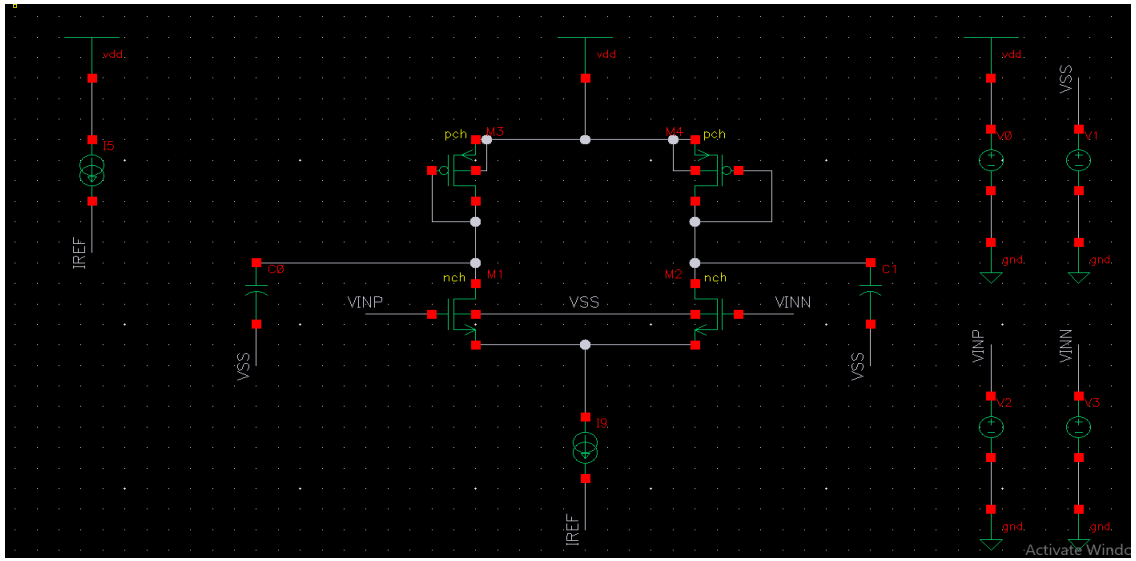
Differential pair with diode-connected

SPECIFICATIONS	
Voltage Supply	1.2 V
GAIN	7dB
Unity Gain Bandwidth	130MHz
Power Consumption	<0.15mW
Output Voltage	>450mV
Load Capacitance (C_L)	1pF

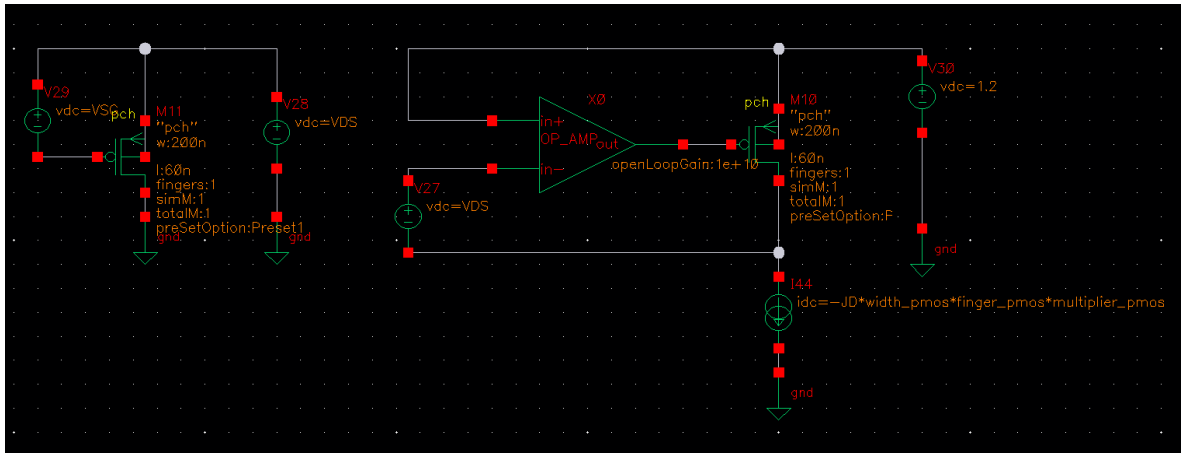
Requirements:

- Design of differential pair with diode-connected with the specifications as shown in the table above by gmid methodology.
- Replace the source current by the current mirrors.
- What can you do to achieve higher gain or bandwidth, and what are the trade-offs in this scenario?
- Compare this structure to the differential pair with current source loads.

Instruction



The testbench of differential pair with diode-connected loads



The gmid testbench for PMOS

- Use the gmid testbench as the previous lab for design.
- Consider related expressions (gain, unity gain bandwidth,…) and build them into the ADEL gmid testbench to choose the parameters of a transistor for achieve the specifications. (Refer to Chapter 4 – 6 in AICD_Lectures).
- *Note that: the transistor can operate in the region 3 of this design (not high frequency).*

Your report must be shown:

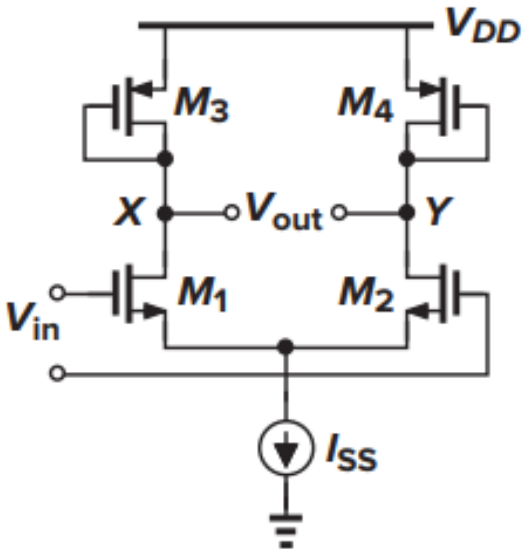
- **Your design flow and the outcomes of the simulation (comments & review).**
- **How do you choose the parameters (V_{DS}, V_{bias}, I_d, length, width,…) for design? Why?**

Experiment 1

The design flow of this problem is as follows:

First, we can calculate the ranges for V_{SD}, V_{SG}, V_{DS}, V_{GS}. From these, we can determine the corresponding values based on the parameters provided in the table, which will be presented in the next slide.

1. Using the testbench of the PMOS, find the gm_p, $rout_p$ and find gm/id, JD versus V_{SG}. From that, determine the corresponding width.
2. From the values of gm_P and $rout_P$, write the function Av versus I_D and find the value of V_{GS} in testbench of the NMOS.
3. From the formula $\mathrm{GBW} = \frac{gm_N}{2\pi C_L}$ we can find gm_N. We can plot gm/id and J_D versus V_{GS} to determine the width.
4. Calculate the V_{IN_DC} of the circuit and apply the values of the NMOS and PMOS to the circuit. Plotting the gain.



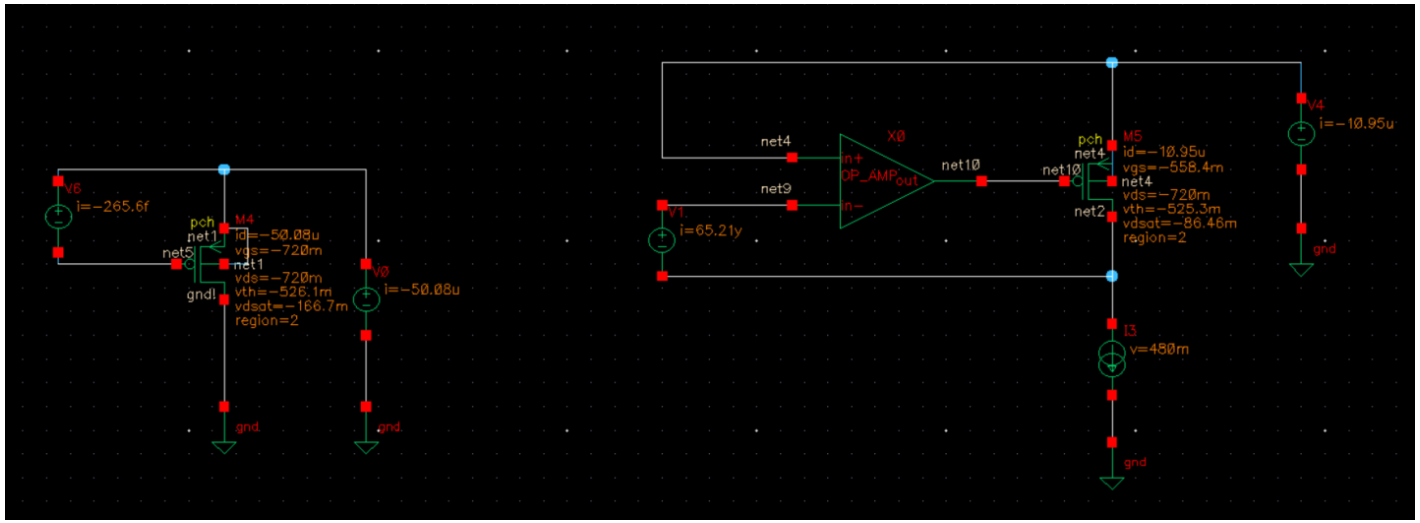
Differential pair with diode-connected

Experiment 1

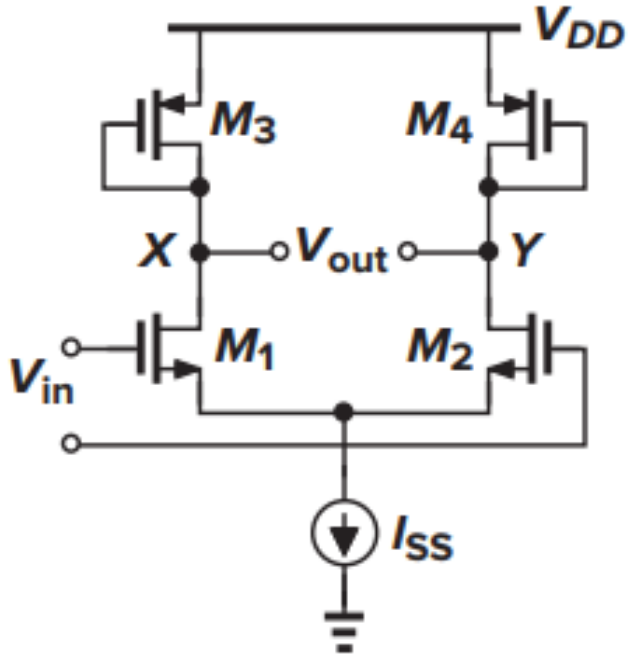
Based on the parameters in the table:

We have $P < 0.15\,mW \Rightarrow P/U < 0.15/U \Rightarrow I < 0.125\,mA \Rightarrow$ choose $I = 100\ \mu A$ (total current).

- $I_{D1} = I_{D2} = 50uA$
- $Vout > 450mV \Rightarrow V_{DD} - V_{SD} > 450mV \Rightarrow V_{SD} < 750mV$
- We choose $Vout = 480mV$, so $V_{SD} = V_{SG} = 720mV$

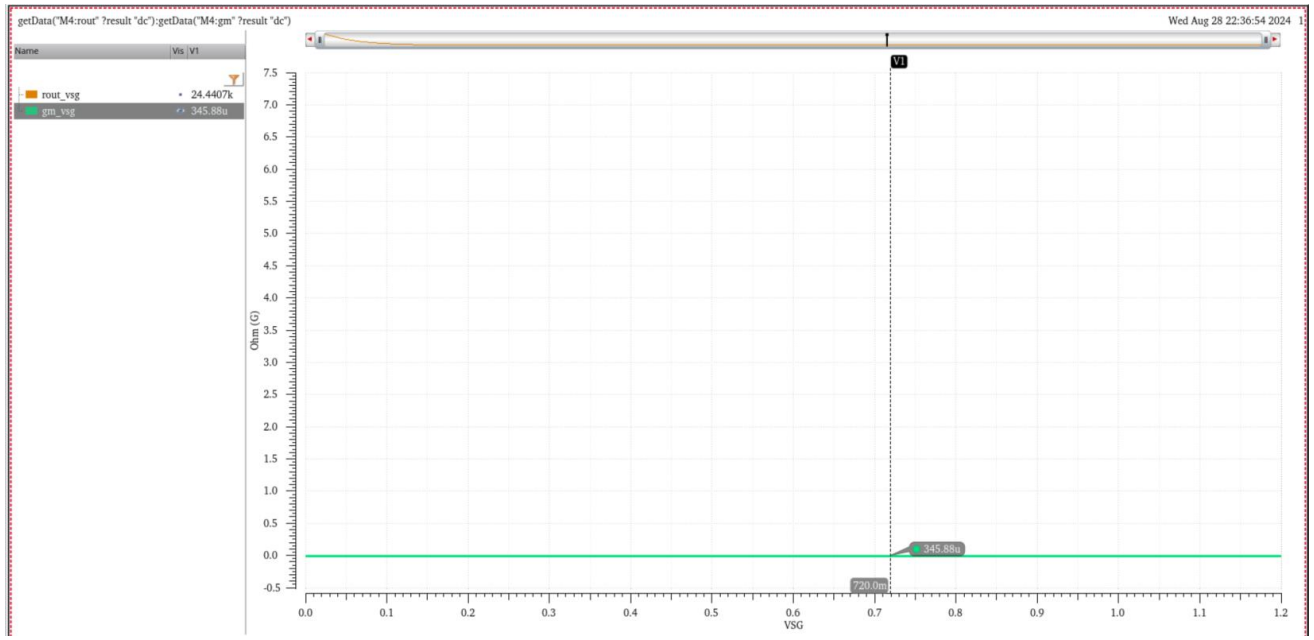


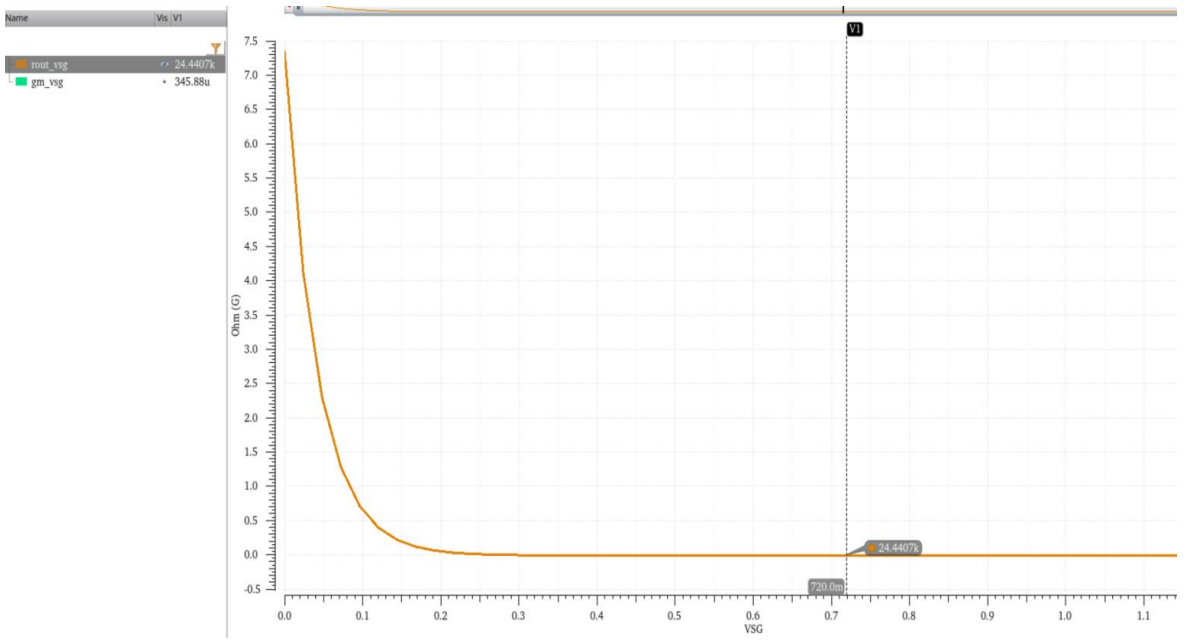
The gmid testbench for PMOS



Differential pair with diode-connected

Experiment 1

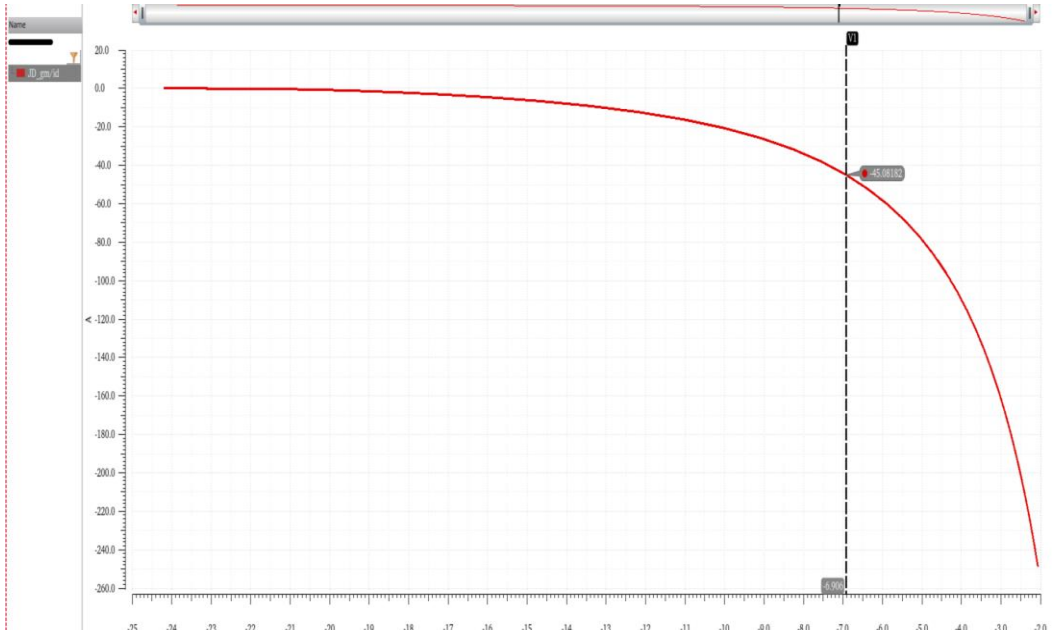


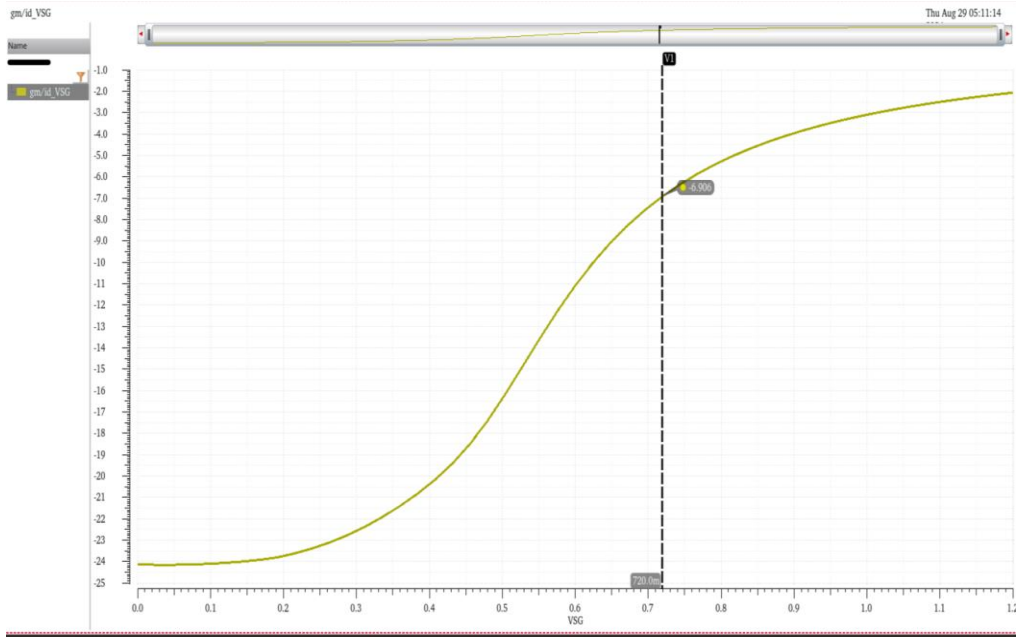


Based on the graph, we have $gm_p = 348.88u$, $rout_p = 24.44K$ as $V_{SG} = 720\text{mV}$

As increasing the length, V_{TH} will decrease, which reduces gm_p, increases $rout_p$, and can reduce the overall gain of the circuit. Since the length affects the V_{TH} of the PMOS, in this case, we fix the length at 60nm (same the values from the previous lab) , with V_{TH} approximately 526 mV.

Experiment 1



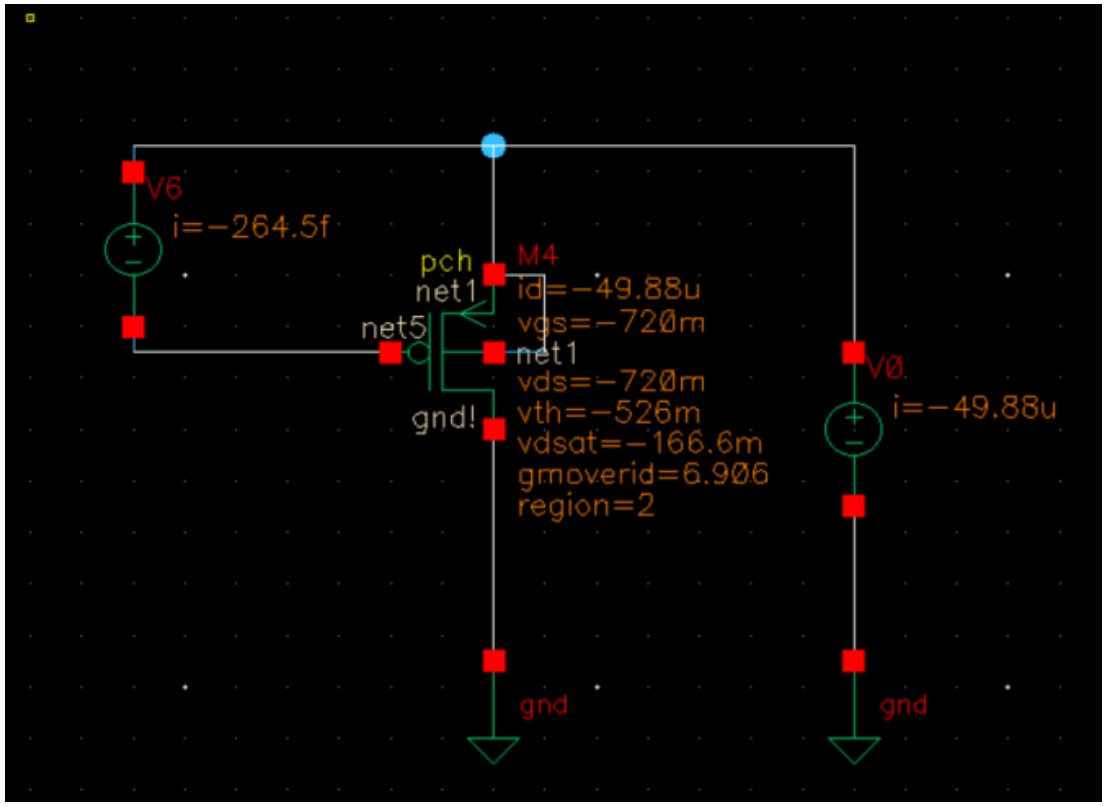


Based on the graph, we have gm/id= -6.906; $J_D = -45.08182$ as $V_{SG}= 720\text{mV}$

We need to keep $I_D = 50uA$ and find the value of to achieve the desired gain

Have: $J_D = \frac{I_D}{W} \Rightarrow \text{W} = \frac{I_D}{J_D} = \frac{50u}{45.08182} \approx 1.093u$

Experiment 1



DC Operating point check

With $V_{SD} = V_{SG} = 720mV,\ L = 60nm, W = 1.093u$. We found the $I_D \approx 50uA$ in the testbench.

Experiment 1

For NMOS transistors

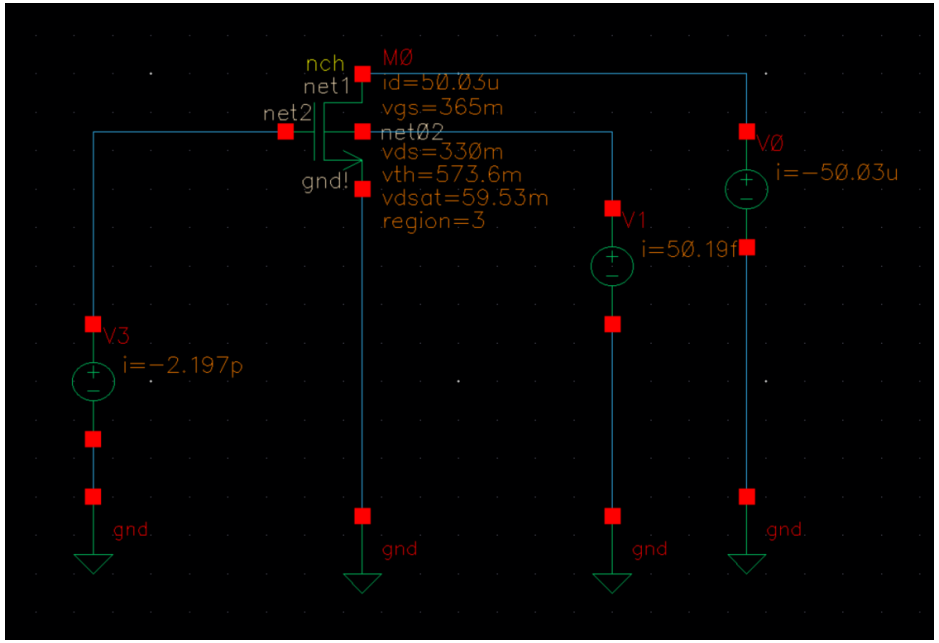
As the length increases, V_{TH} decreases. For NMOS, we should choose a smaller value to make it easier to adjust the width, because if the width is too large when the length is high, the gain decreases at high frequencies due to the increased parasitic capacitances.

We have:

$$\omega_p = [(r_{O1}||r_{O2})C_L]^{-1}$$
$$|A_0| = g_{m1}(r_{O1}||r_{O2})$$

Unity gain band-width: As circuit has dominant pole: GBW=ω_u

$$\omega_u = \sqrt{A_0^2 - 1}\omega_p$$
$$\approx A_0\omega_p$$



The gmid testbench for NMOS

We have Unity gain band-width =130MHz

$\text{GBW} = \frac{gm_N}{2\pi C_L} \leftrightarrow 130MHz = \frac{gm_N}{2\pi \times 1pF} \rightarrow gm_N = 8{,}168 \times 10^{-4}$ S (minimum value of NMOS)

Experiment 1

For NMOS transistors

We have: $gm_P = 345.88u; rout_P = 24.44K \Rightarrow \frac{1}{gm_P} // rout_P = 2585.34\Omega$

And:

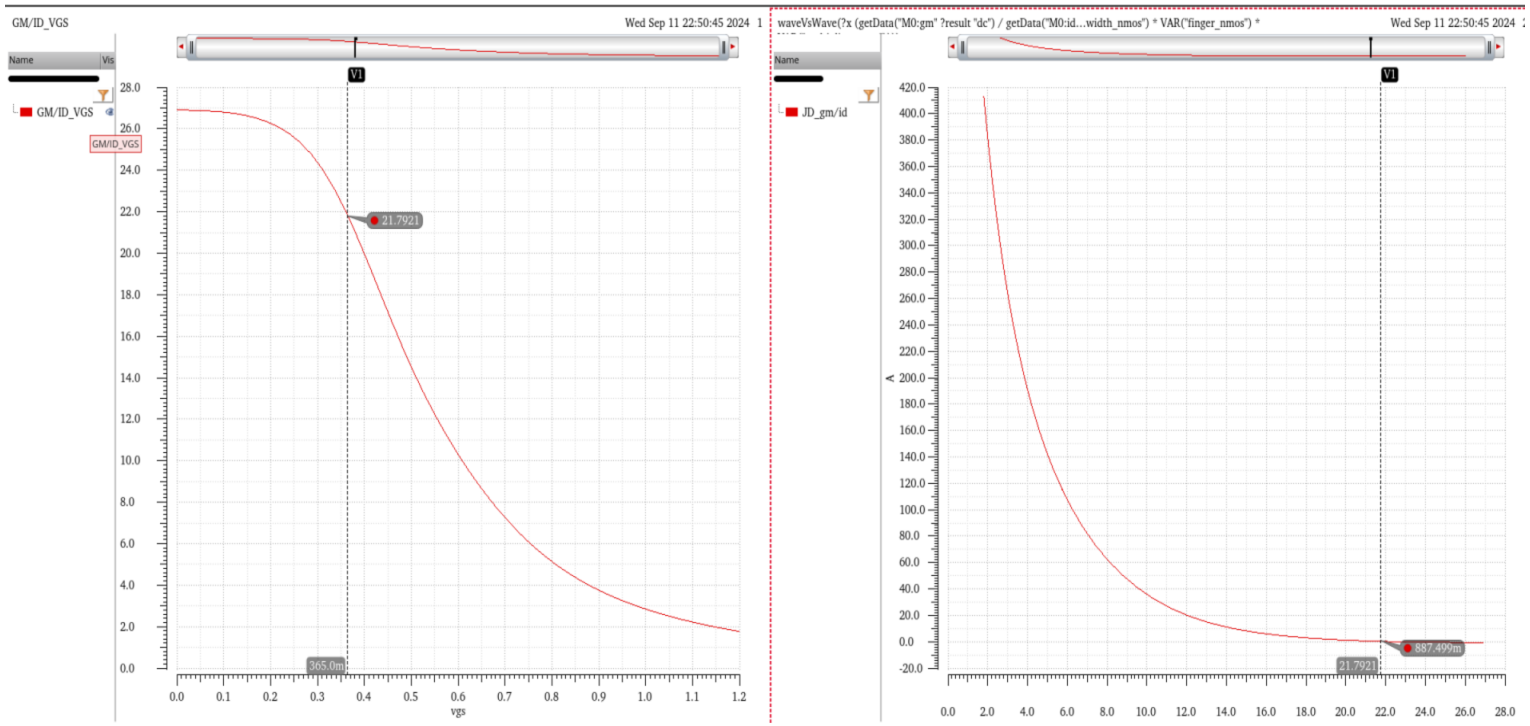
$$Av = -gm_N(\frac{1}{gm_P} // rout_P // rout_N)$$

$$Av@50uA = (gm@50uA)(RD//(ro@50uA))$$

We write the av function based on the values calculated at I_D = 50 µA, at Av = 7dB as $V_{GS} \approx 365mV$.

*Function: ((getData("M3:gm" ?result "dc") / getData("M3:id" ?result "dc")) * 5e-05)*((2585*getData("M3:rout" ?result "dc")*getData("M3:id" ?result "dc")/60u)/(2585+getData("M3:rout" ?result "dc")*getData("M3:id" ?result "dc")/50u))*

Experiment 1



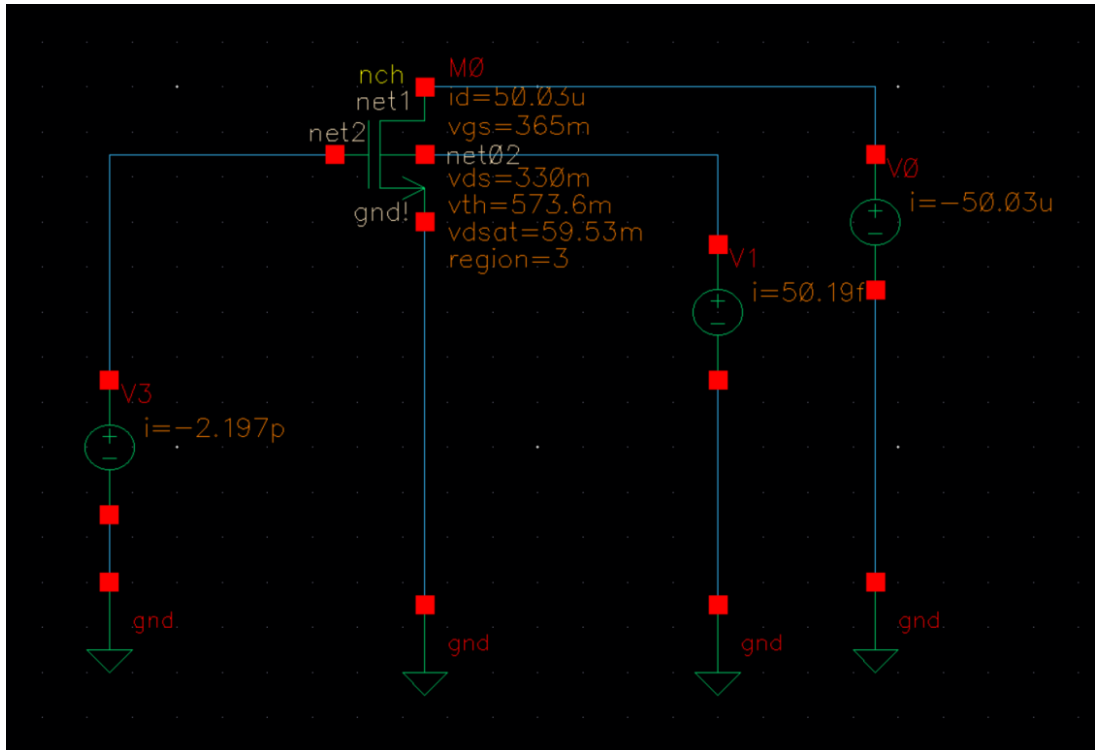
Graph of JD (left) and gm/id (right) versus Vgs

Based on the graph, we have gm/id= $21.7921\ S$; $J_D = 887.499m\ \ A/m$ as $V_{SG}= 365\ mV$.

We need to keep $I_D = 50uA$ and find the value of to achieve the desired gain.

Have: $J_D = \frac{I_D}{W} \Rightarrow \text{W} = \frac{I_D}{J_D} = \frac{50u}{887.499m} \approx 69.73u$

Experiment 1



DC Operating point check

	Name	
1	vsb	150m
2	finger_nmos	1
3	length_nmos	60n
4	multiplier_nmos	1
5	vds	330m
6	vgs	365m
7	width_nmos	71.3u

Design variables

We choose $V_{ISS} = 150mV$ (same in previous lab), bias voltage for NMOS

$$Vout = VDS + V_{ISS}\ ;$$

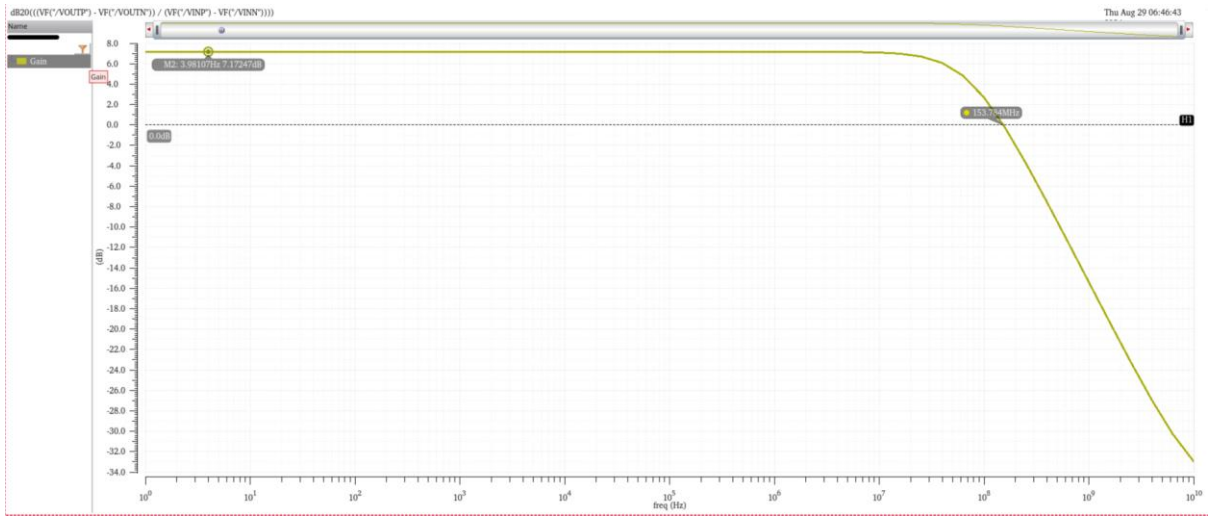
$$\Rightarrow VDS = Vout - V_{ISS} = 0.48 - 0.15 = 0.35mV$$

With these values, the NMOS operates in region 3 (which is still allowed in this project).

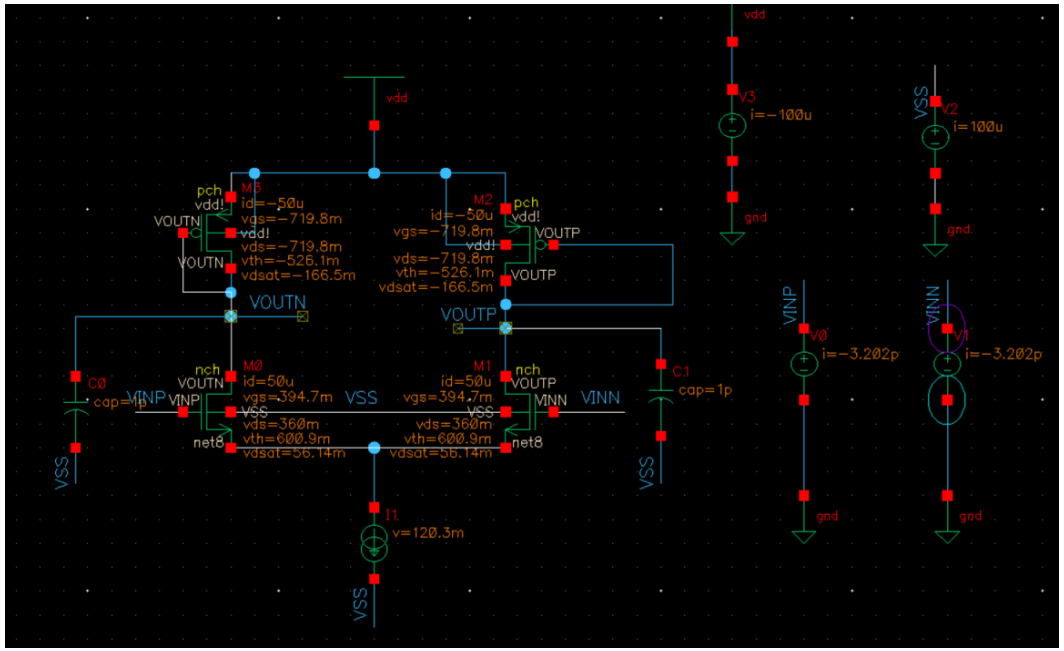
With $V_{DS} = 0.35mV;\ V_{GS} = 365mV,\ L = 60nm, W = 71.3u$.

We found the $I_D \approx 50uA$ in the testbench.

Experiment 1



Frequency response of *differential pair with diode-connected*



We observe that the gain achieved is quite high, with Av = 7.17 dB and the unity gain bandwidth is also quite high at around 153 MHz. This is quite good for our initial purpose. However, $V_{OUT} = 480mV$ still quite low, results in a relatively low headroom. The trade-off here is that while the gain and unity gain bandwidth are good, the headroom is low, and the width is quite high, leading to large $(W/L)_P$, $|V_{SG} - V_{THP}|$ decrease, large parasitic capacitance in high frequency.

We need to achieve a specific gain. We need to adjust V_{ISS} to modify the circuit's gain without changing the current I_D. The NMOS voltage bias is reduced from 150 mV to 120 mV

DC Operating point check

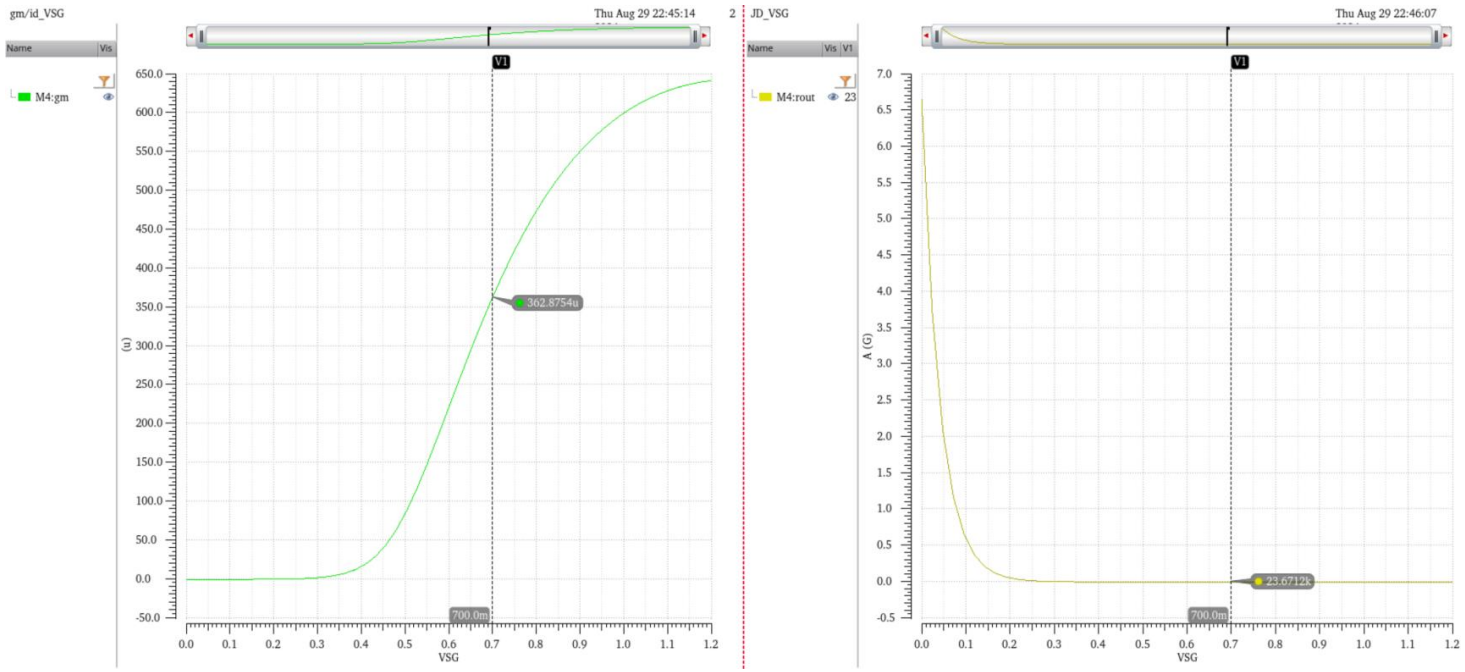
$$We\ have: V_{INP} = V_{INN} = V_{GS} + V_{ISS}$$
$$= 0.365 + 0.15 = 0.515mV$$

Design Variables

	Name	
1	length_nmos	60n
2	length_pmos	60n
3	width_nmos	71.3u
4	width_pmos	1.095u
5	VINN	515m
6	VINP	515m

Experiment 1

For PMOS transistors



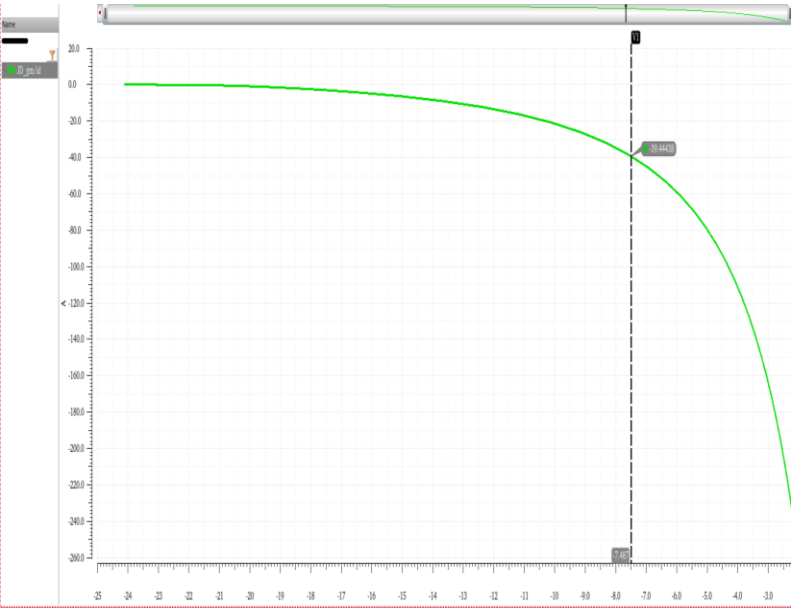
We also use the gm/ID methodology to continue finding the values for NMOS and PMOS as we did before

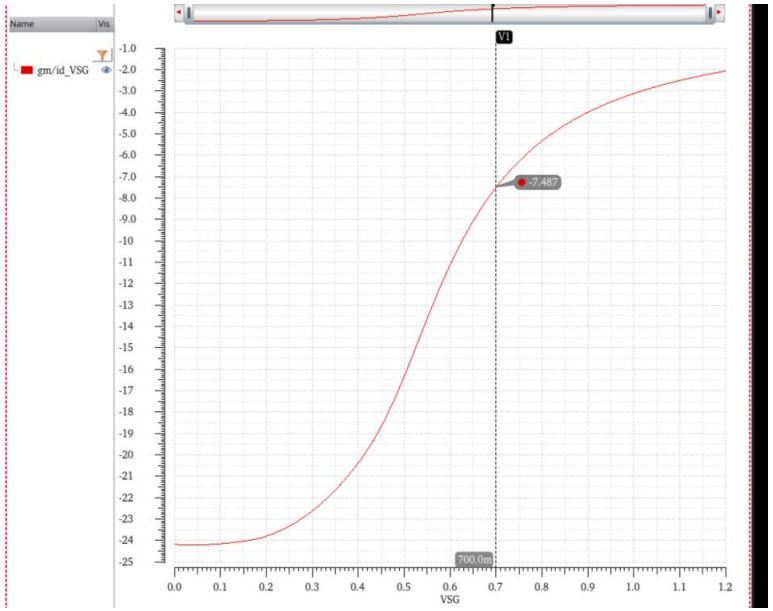
- $Vout > 450m \Rightarrow V_{DD} - V_{SD} > 450mV \Rightarrow V_{SD} < 750mV$
- We choose $Vout = 500mV$, so $V_{SD} = V_{SG} = 700mV$

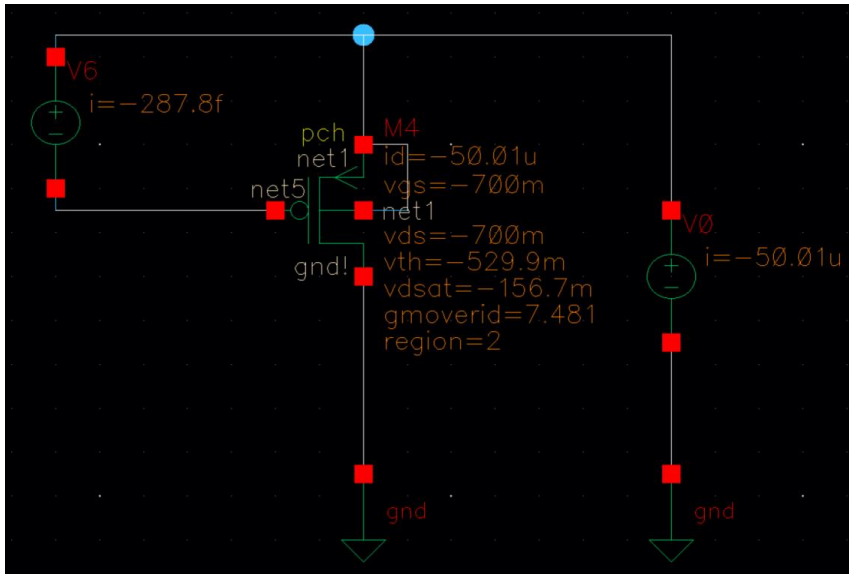
Based on the graph, we have $gm_p = 362.87u$, $rout_p = 23.67K$ as $V_{SG} = 700\text{mV}$

As increasing the length, V_{TH} will decrease, which reduces gm_p, increases $rout_p$, and can reduce the overall gain of the circuit. Since the length affects the V_{TH} of the PMOS, in this case, we fix the length at 60nm (same the values from the previous lab) , with V_{TH} approximately 530 mV.

Experiment 1







DC Operating point check

Based on the plot, we have gm/id= -7.487; $J_D = -39.4444$ as $V_{SG}= 700\text{mV}$

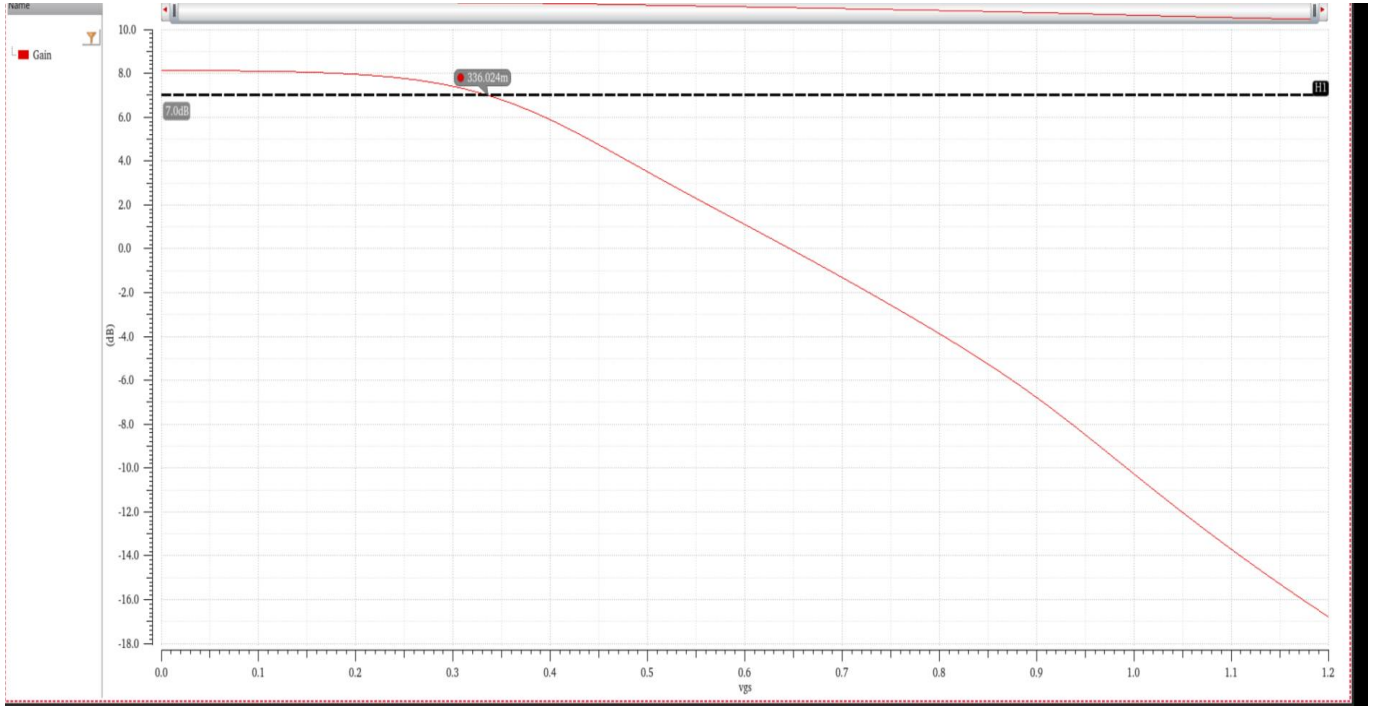
We need to keep $I_D = 50uA$ and find the value of to achieve the desired gain

Have: $J_D = \frac{I_D}{W} \Rightarrow \text{W} = \frac{I_D}{J_D} = \frac{50u}{39.4444} \approx 1.301u$

	Name	Value
1	VSD	700m
2	VSG	700m
3	finger_pmos	1
4	length_pmos	60n
5	multiplier_pmos	1
6	width_pmos	1.303u

Experiment 1

For NMOS transistors



We have: $gm_P = 362.87u; rout_P = 23.67K \Rightarrow \frac{1}{gm_P} // rout_P = 2468.41K$

And:

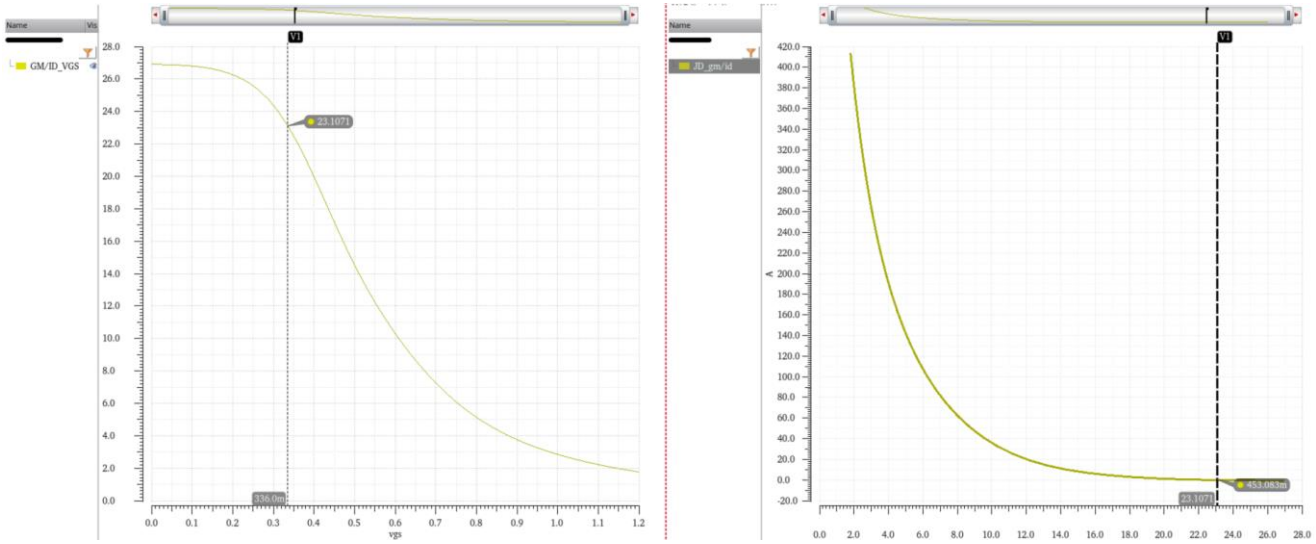
$$Av = -gm_N(\frac{1}{gm_P} // rout_P // rout_N)$$

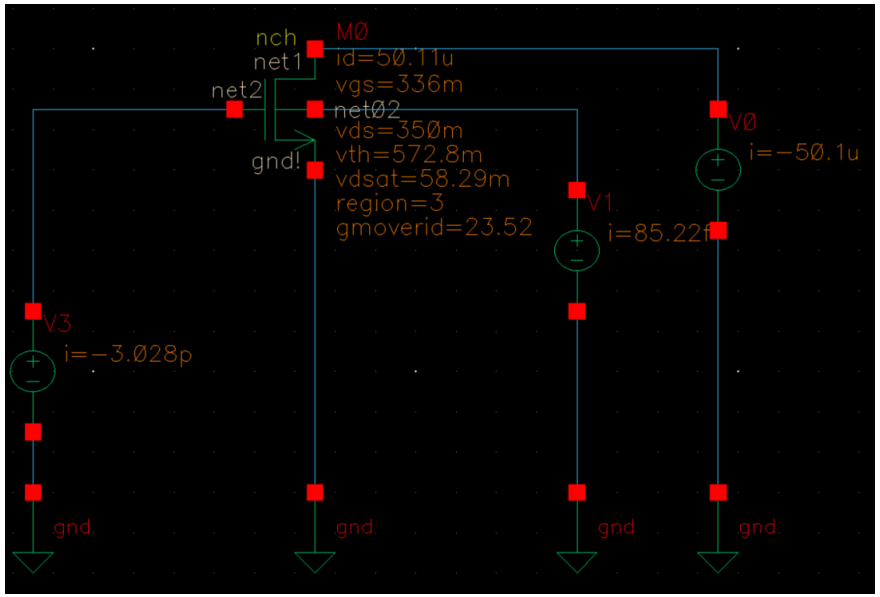
$$Av@50uA = (gm@50uA)(RD//(ro@50uA))$$

We write the av function based on the values calculated at I_D = 50 µA, at Av = 7dB as $V_{GS} \approx 336mV$.

*Function: ((getData("M3:gm" ?result "dc") / getData("M3:id" ?result "dc")) * 5e-05)*((2585*getData("M3:rout" ?result "dc")*getData("M3:id" ?result "dc")/60u)/(2585+getData("M3:rout" ?result "dc")*getData("M3:id" ?result "dc")/50u))*

Experiment 1





Based on the graph, we have gm/id= $231071\ S$; $J_D = 453.083m\ \ A/m$ as V_{GS}= $336\ mV$.

We need to keep $I_D = 50uA$ and find the value of to achieve the desired gain.

Have: $J_D = \frac{I_D}{W} \Rightarrow \text{W} = \frac{I_D}{J_D} = \frac{50u}{453.083m} \approx 133.3u$

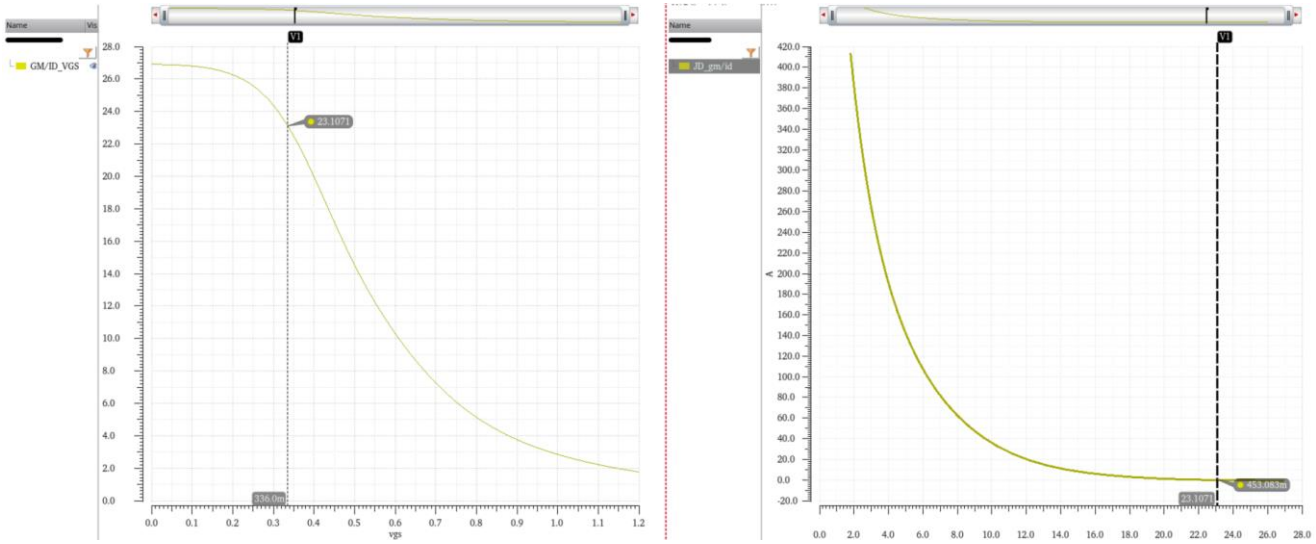
We use this plot to find the most accurate value for W when $I_D = 50u$

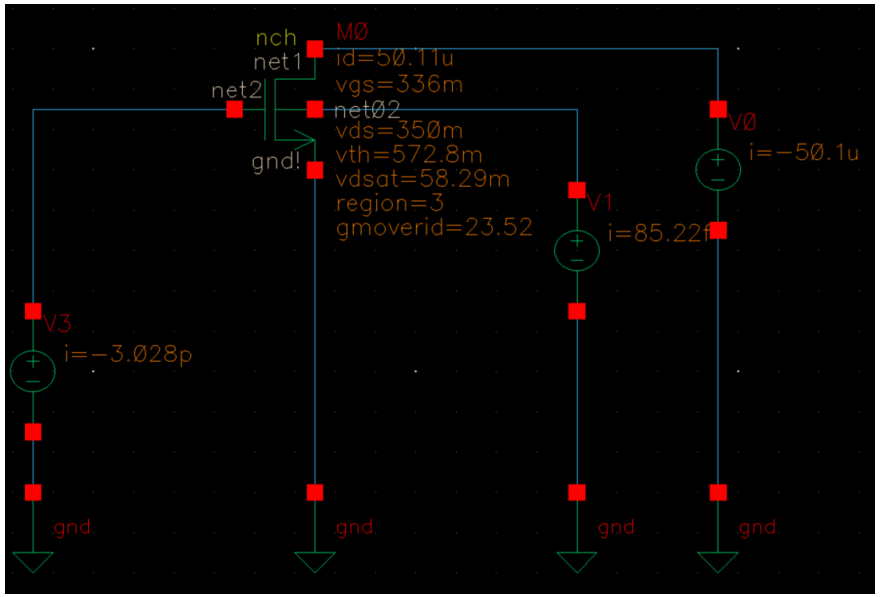
With these values, the NMOS operates in region 3 (which is still allowed in this project).

With $V_{DS} = 0.35mV$; $V_{GS} = 336mV$, $L = 60nm, W = 133.6u$. We found the $I_D \approx 50uA$ in the testbench

	Name	Value
1	finger_nmos	1
2	length_nmos	60n
3	multiplier_nmos	1
4	vds	350m
5	vgs	336m
6	vsb	150m
7	width_nmos	133.6u

Experiment 1





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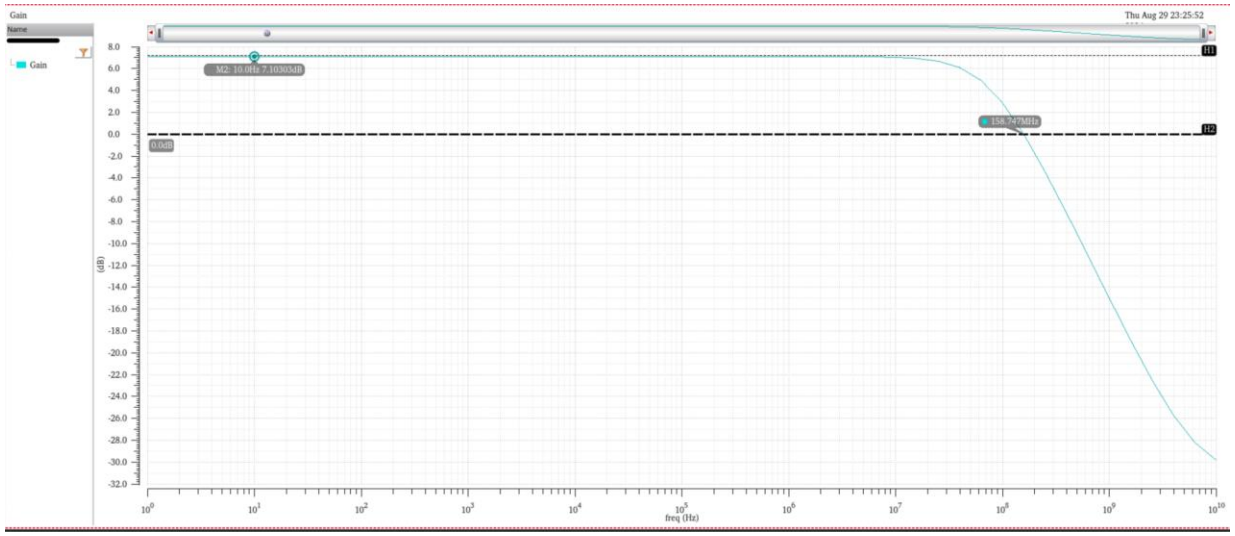
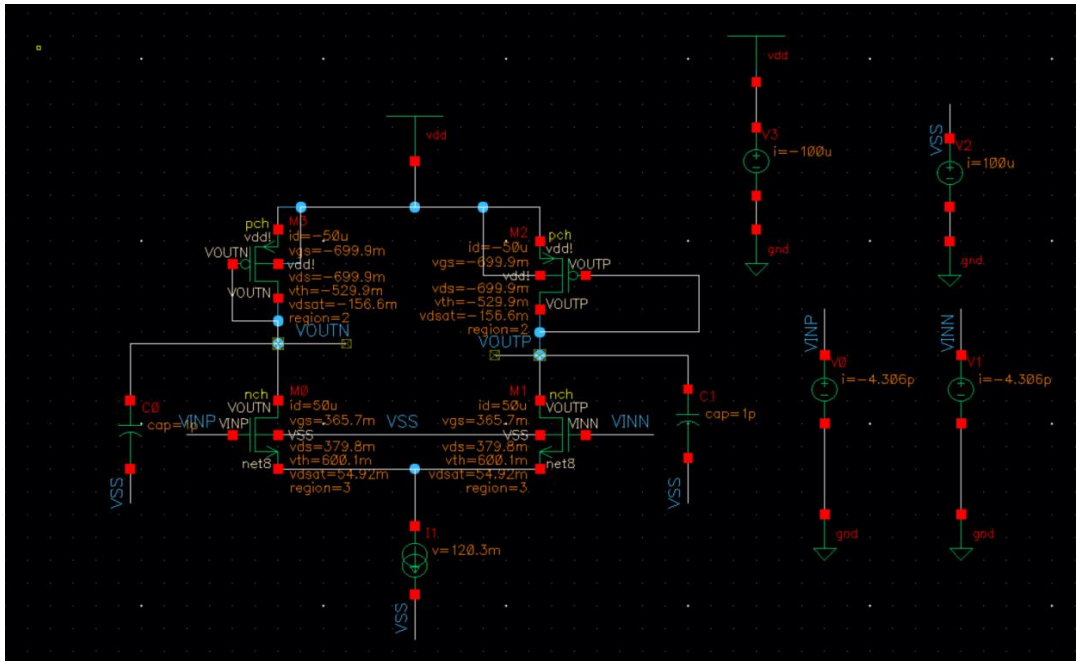
5	vgs	336m
6	vsb	150m
7	width_nmos	133.6u

Experiment 1



Frequency response of *differential pair with diode-connected*



DC Operating point check

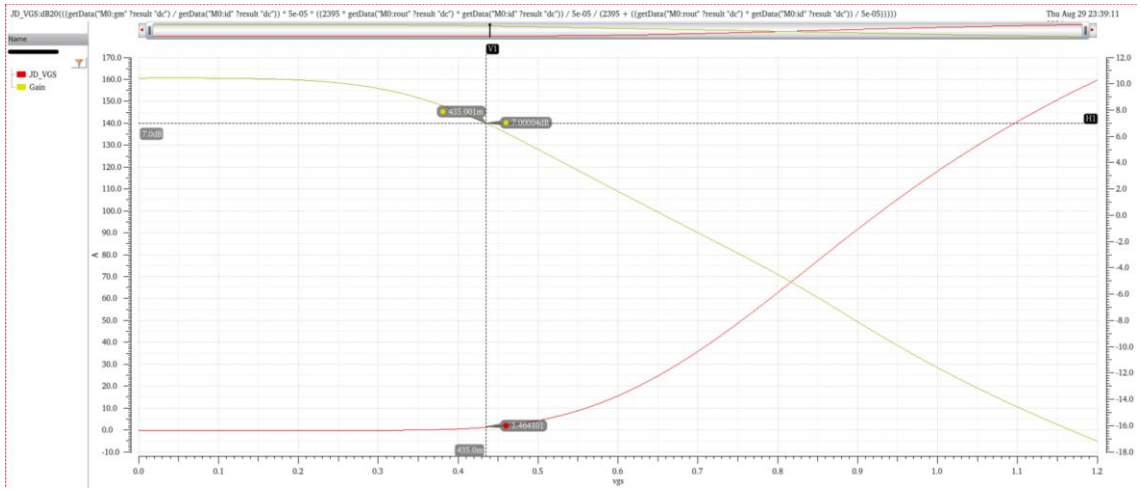
As reducing V_{ISS}, the gate-source voltage V_{GS} of the NMOS transistors will decrease. If V_{GS} decreases too much, it might fall below the threshold voltage V_{TH} of the NMOS, causing the transistors to operate in the subthreshold region. When V_{ISS} is reduced, you may need to adjust other circuit components to compensate for the reduced gmg m and changes in transistor sizing, which could increase parasitic capacitance and impact high-frequency performance However, here we choose V_{out} higher than the previous test so the headroom will be better.

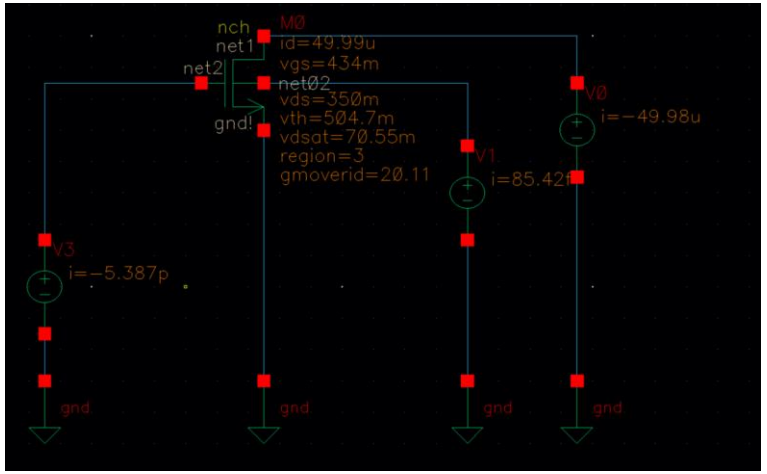
$$We\ have: V_{INP} = V_{INN} = V_{GS} + V_{ISS} = 0.336 + 0.15 = 0.486mV$$

	Name	Val
1	length_nmos	60n
2	length_pmos	60n
3	width_nmos	133.6u
4	width_pmos	1.303u
5	VINN	486m
6	VINP	486m

Experiment 1

Change length of NMOS





Design Variables

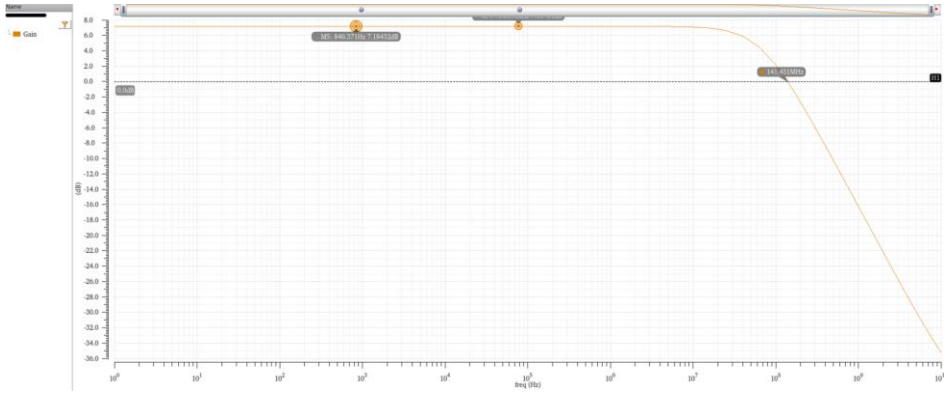
	Name	Value
1	finger_nmos	1
2	length_nmos	200n
3	multiplier_nmos	1
4	vds	350m
5	vgs	434m
6	vsb	150m
7	width_nmos	35.2u

DC Operating point check for NMOS

Based on the graph, we have $J_D = 1.4641$ as $\mathrm{Av} = 7\mathrm{dB}$

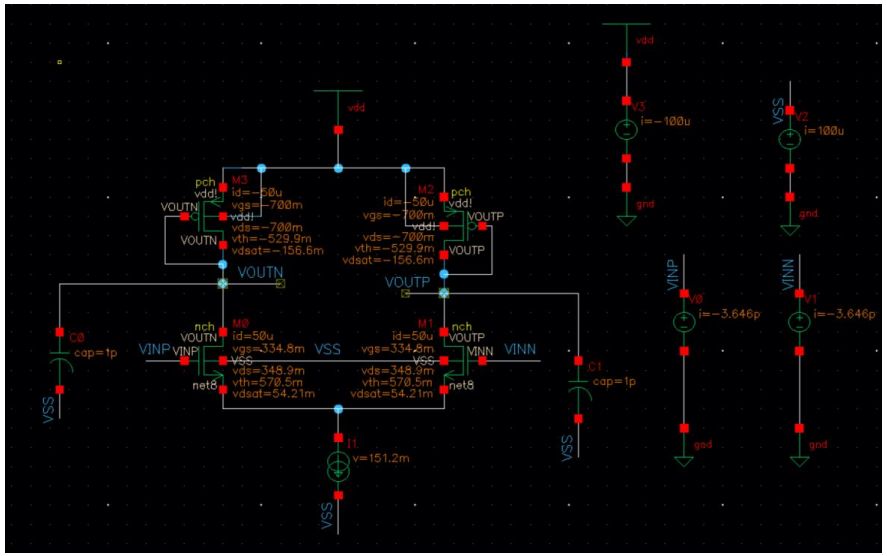
Have: $J_D = \frac{I_D}{W} \Rightarrow \mathrm{W} = \frac{I_D}{J_D} = \frac{50u}{1.4641} \approx 34.2uM$

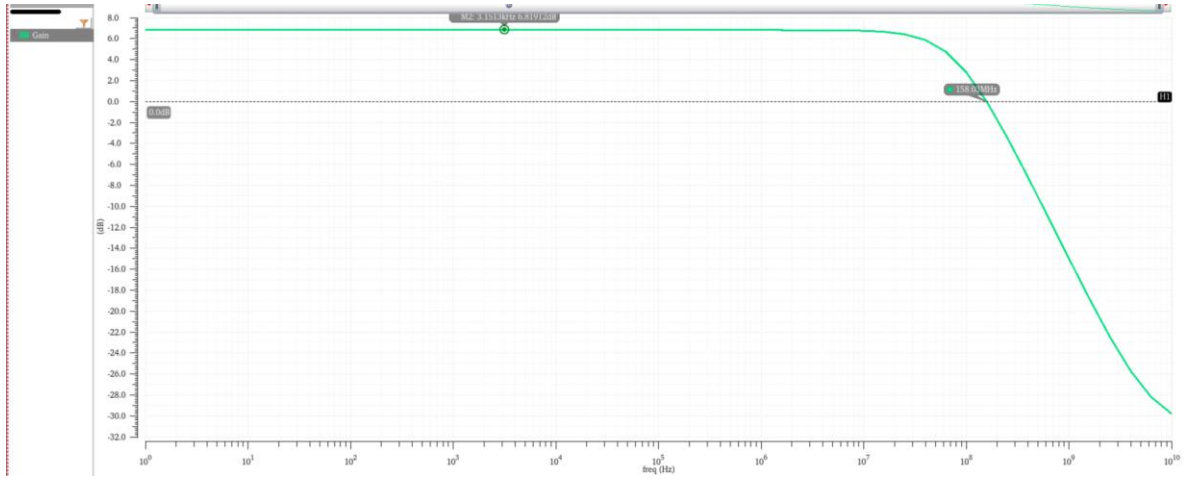
Enter the values into the NMOS testbench, then plot JD to find the width such that I_D in the testbench equals 50 µA. We find $\mathrm{W} = 35.2\mathrm{uM}$



- When increasing the length while keeping $I_D = 50uA$ (constant) , VGS must increase, which decreases the transconductance (gm) . Increasing the length leads to a decrease in λ and an increase in roN. When gm decreases and roN increases, the decrease in gm can significantly reduce the gain. Increasing the length also causes the intrinsic capacitances Cgd and Cdb to decrease, which increases the unity bandwidth.

Experiment 1





Frequency response of differential pair with diode-connected as finger splitted

As dividing a transistor, the total area remains the same, but the intrinsic capacitance of each finger is smaller. Although the intrinsic capacitance of each individual finger is smaller, the total capacitance of the entire transistor (when all fingers are combined) remains unchanged. Therefore, the unity bandwidth, which depends on the total intrinsic capacitance, does not change significantly. The transconductance of each smaller finger may be lower compared to a larger transistor. The gain decreases from 7.17 dB to 6.8 dB, corresponding to a reduction of approximately 0.37 dB. This reduction occurs because dividing the transistor into fingers can reduce the transconductance of the transistor due to changes in the configuration of the fingers.

Design Variables

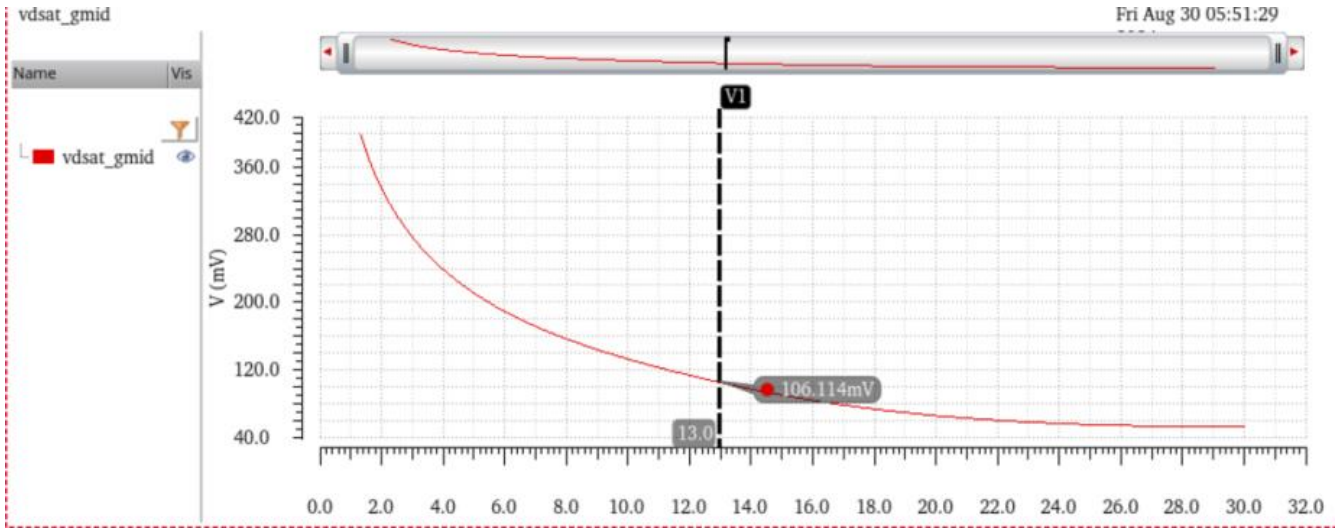
	Name	
1	finger_nmos	6
2	finger_pmos	1
3	length_nmos	60n
4	length_pmos	60n
5	width_nmos	22.3u
6	width_pmos	1.303u
7	VINN	486m
8	VINP	486m

DC Operating point check

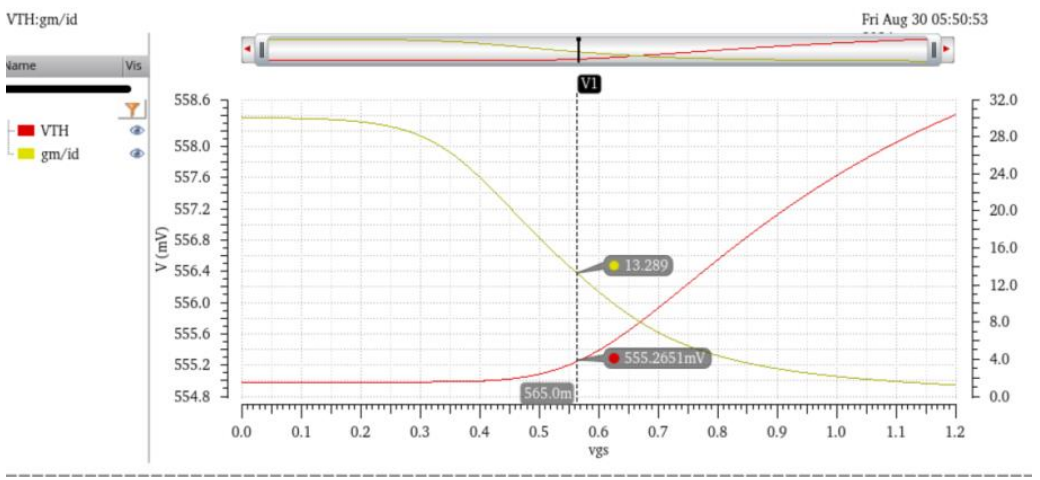
Experiment 1

Function:

- *JD (gm/id) nch: waveVsWave(?x (getData("M3:gm" ?result "dc") / getData("M3:id" ?result "dc")) ?y (getData("M3:id" ?result "dc") / (VAR("width_nch") * VAR("finger_nch"))))*
- *v("M2:vth" ?result "dc")*



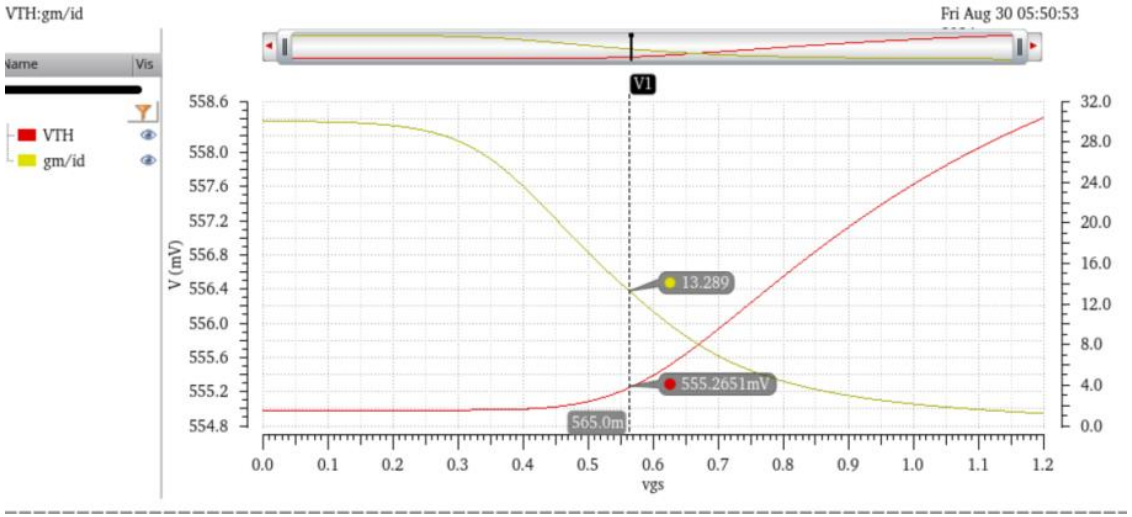
The plot of the Vov_gm/id with length = 1u

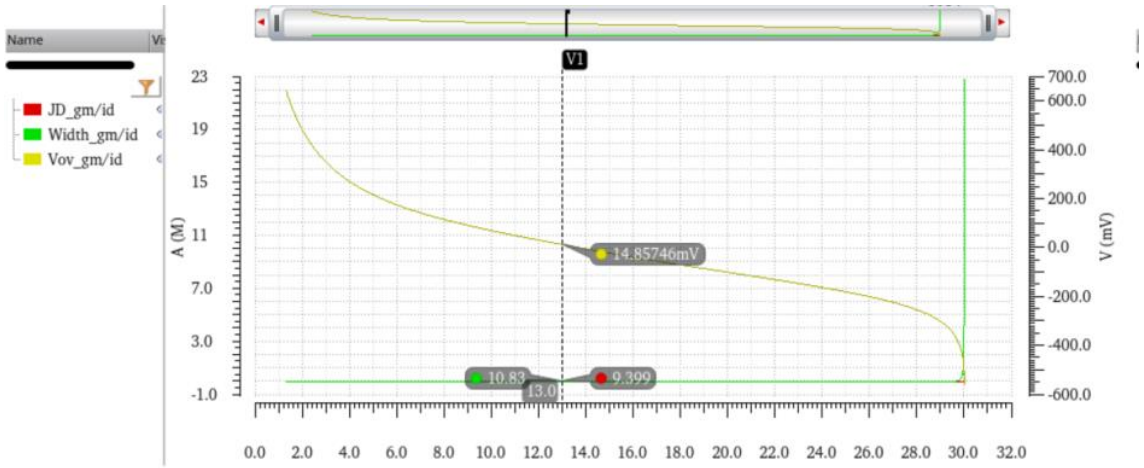


The plot of the VTH_VGS with length = 1u

At VGS2= 565mV, we know that VTH=555mV. With the value of VTH= 555mV we need to choose VGS2> 555mV. Besides, we obtain VDS2 = 120m V,so we need to choose gm/id with vdsat (overdrive voltage) < VDS2 (to ensure the NMOS operates in the saturation region)

Experiment 1

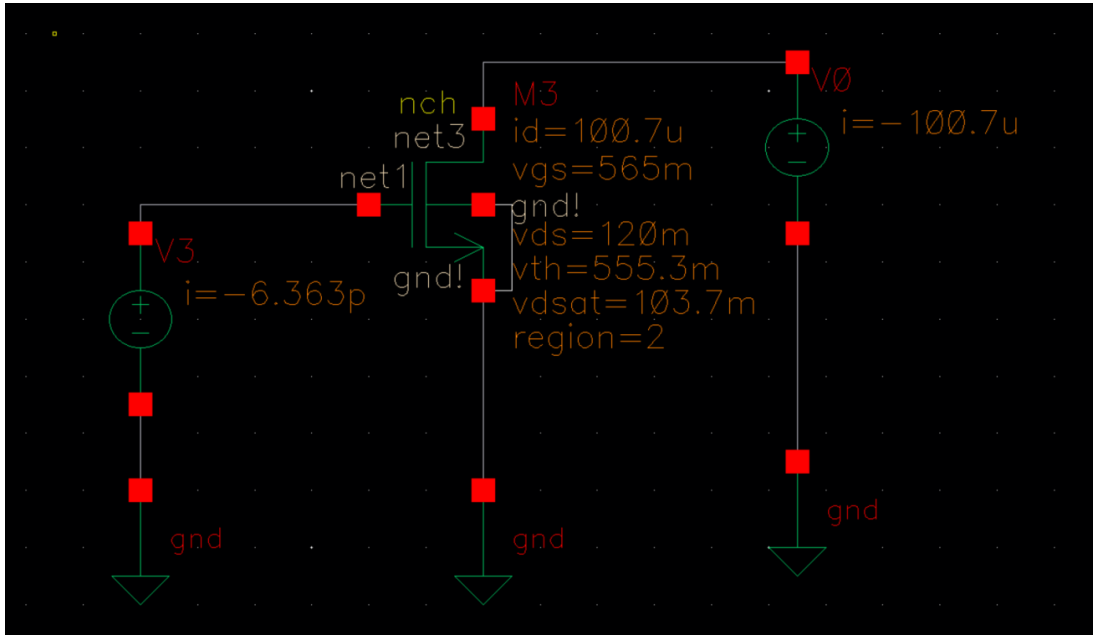




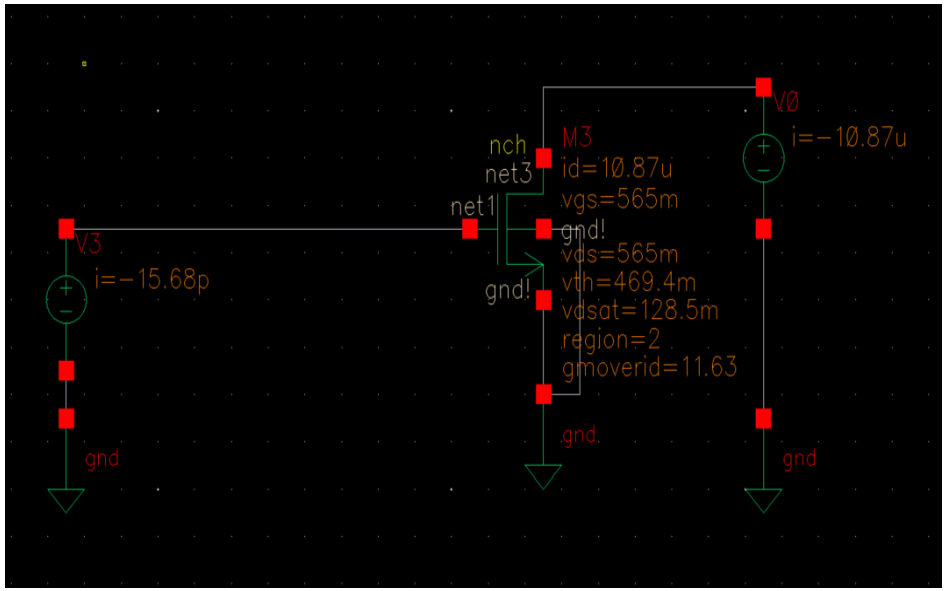
We choose VGS > VTH with VGS = 565mV and Vov>VGS2-VTH2. We obtain gm/id in the range of 10-14.

We choose gm/id =13. With this value, we find Width M1= 10.83um and JD = 9.399 on the plot

Experiment 1



DC operating points of M1 as ID =100uA



DC operating points of M2 as ID =10uA

Entering the value of design variables after chose by gmid methodology run DC analysis

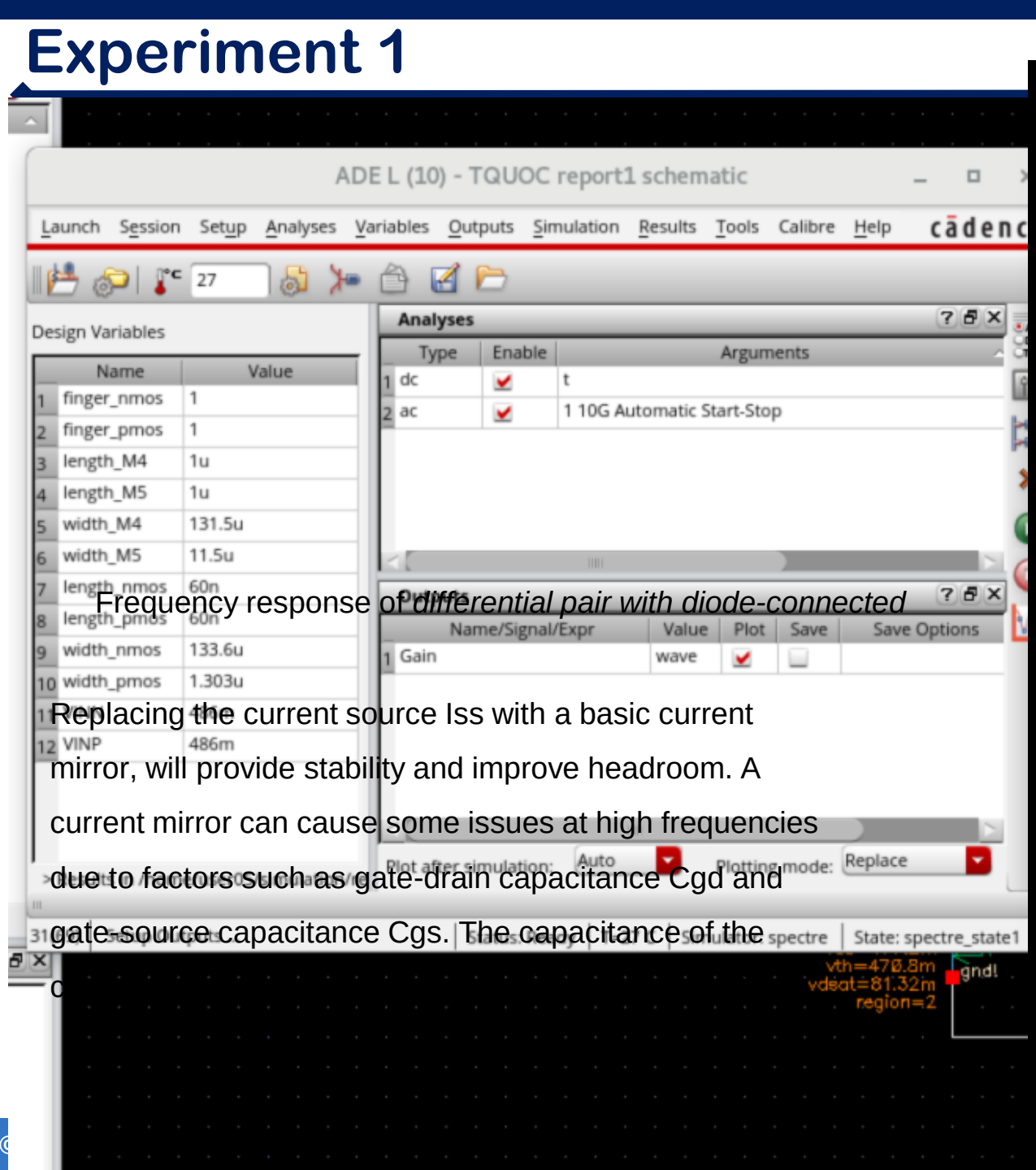
Observe the DC operating points, the drain current equal 100.7u.

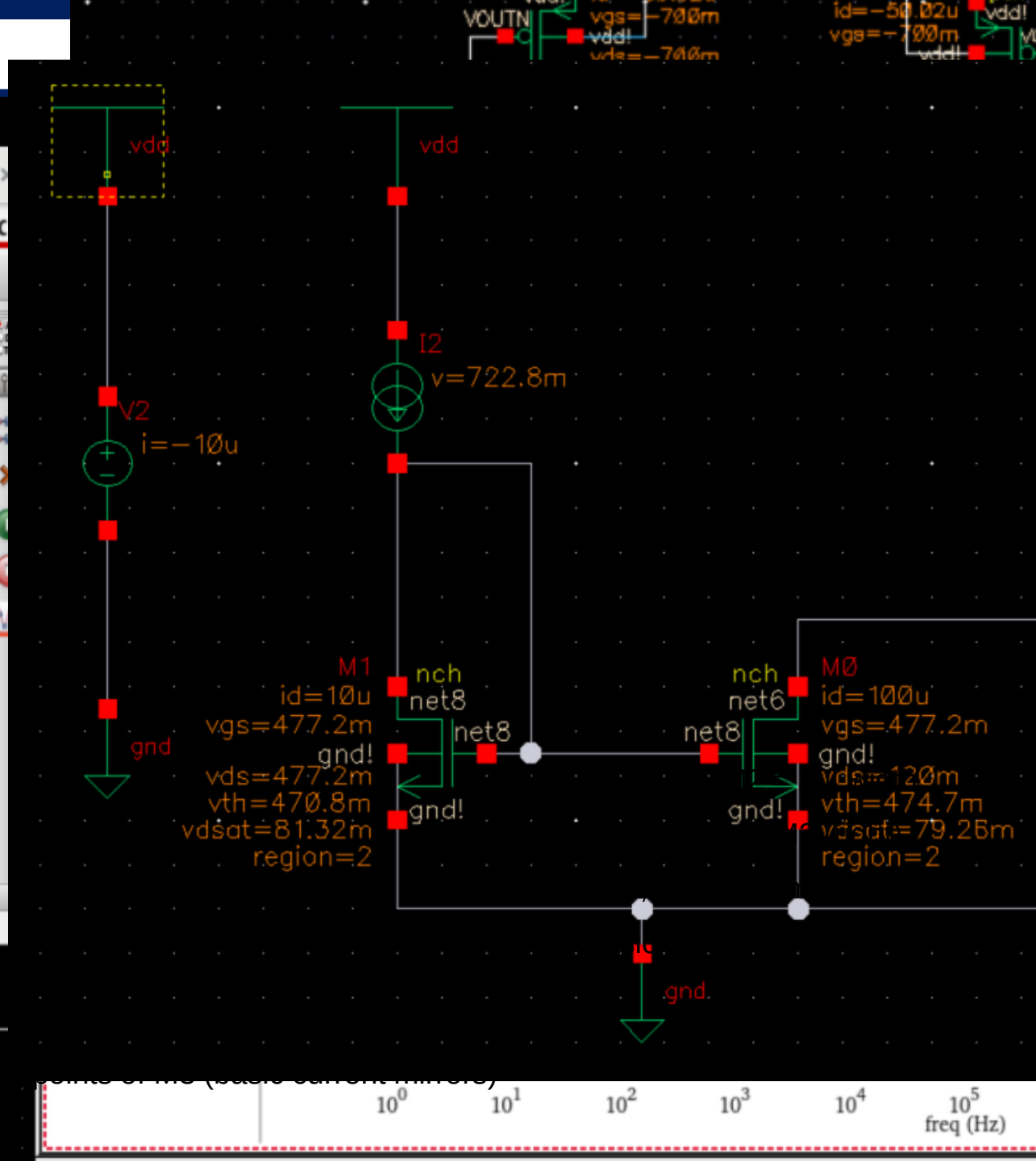
We need id =100uA. We slightly increase VGS to achieve the desired value

We design M1 of basic current mirrors with VDS1 = VGS1 = VGS2 = 565mV → Run DC operating points & observe drain current → gm/id, JD → Adjust width to the correct value.

Width M2 =11.5um

Experiment 1



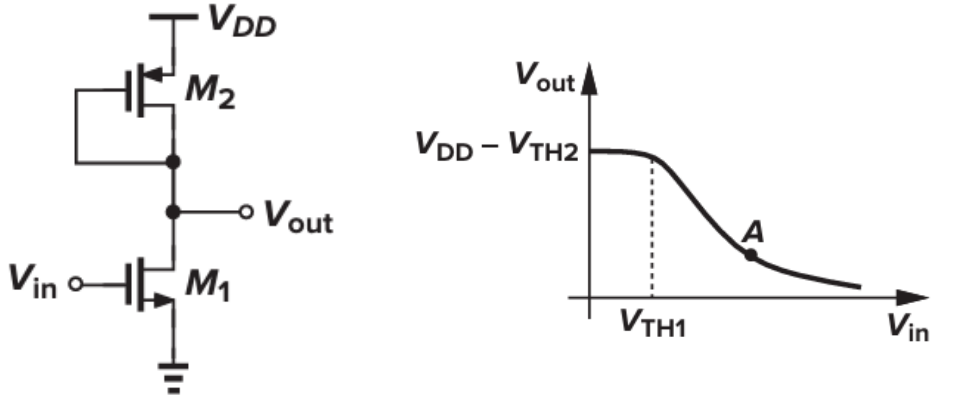


Frequency response of *differential pair with diode-connected*

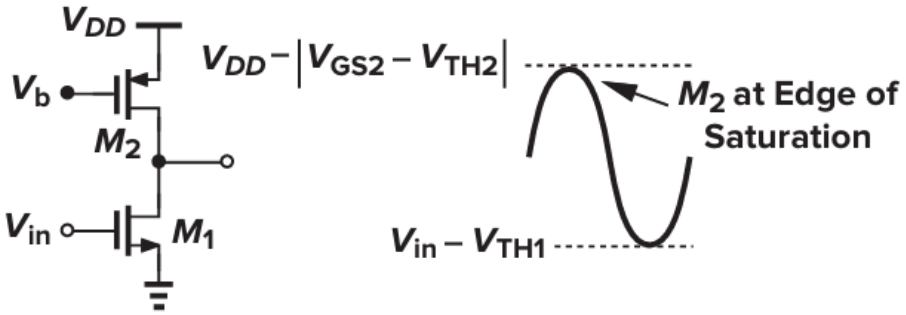
Replacing the current source Iss with a basic current mirror, will provide stability and improve headroom. A current mirror can cause some issues at high frequencies due to factors such as gate-drain capacitance Cgd and gate-source capacitance Cgs. The capacitance of the

Experiment 1

Compare this structure to the differential pair with current source loads.



Diode-Connected Load



Current Source Load

Diode-Connected Load: A higher gain with a diode-connected load will reduce the output bandwidth due to the requirements for overdrive voltage and the threshold voltage of the transistors. Diode-connected loads typically require lower headroom but can encounter issues when $Vout$ is low, as variations in $Vout$ directly affect the operation of the circuit. Larger overdrive voltages for transistors in a diode-connected load lead to limitations on the output swings.

Current Source Load: A circuit with a current source load can achieve higher gain due to the higher output impedance provided by the current source. The stability of the current and better adjustability contribute to increased gain of the circuit. A current source load can provide better and more stable headroom when Vout changes. This is because the current is more stable and less affected by fluctuations in the supply voltage. A circuit with a current source load offers higher gain but lower bandwidth.

Experiment 2

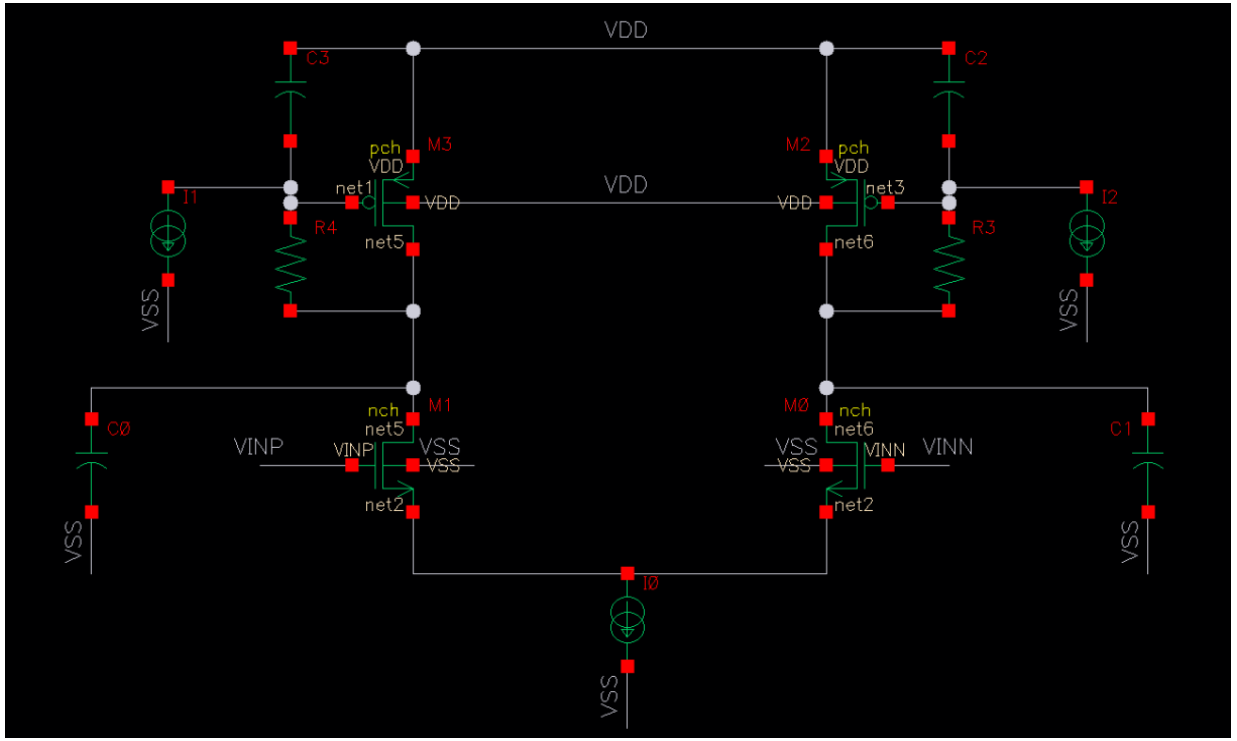


Fig.1 Differential pair with PMOS source follower

Keeping the same components size and value of the previous experiment, we reconfigure the architecture from PMOS diode-connected to a PMOS source follower to increase the bandwidth of our amplifier

Requirements:

-Find the suitable value for capacitor (C2 & C3), resistor (R3 & R4) and current source (I1 & I2) to achieve a greater UGBW, prove and explain your answer

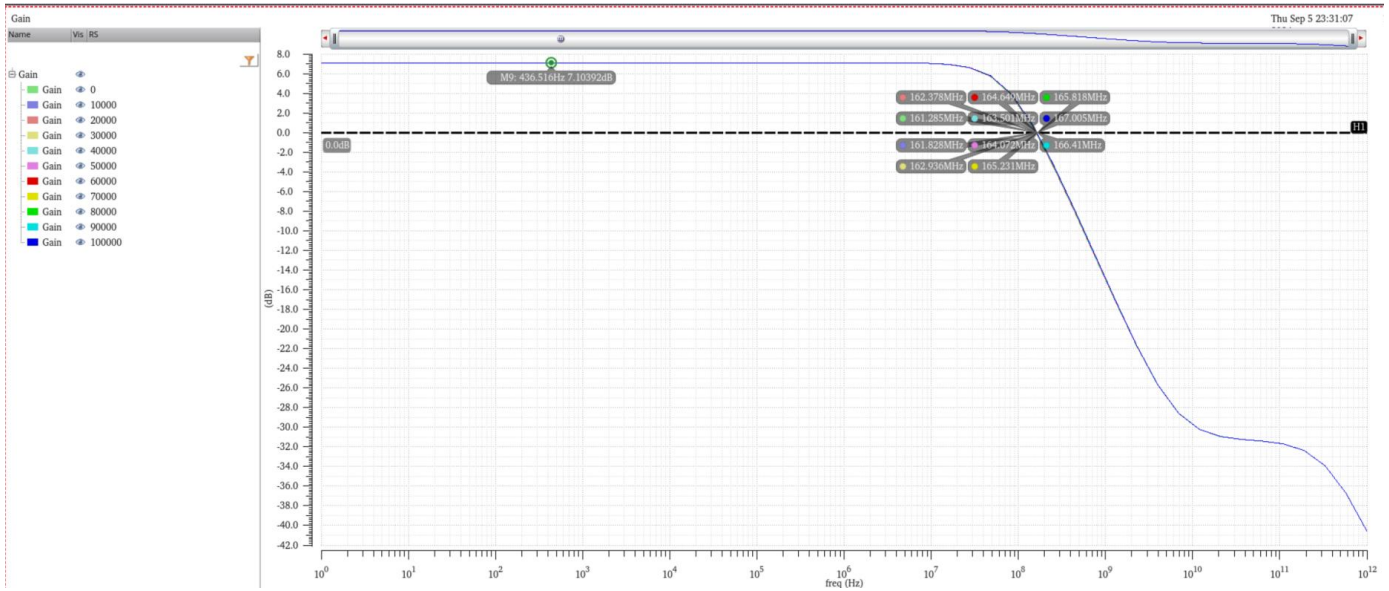
-What is the trade-off when achieve a wider UGBW

Note: you can refer this link https://www.seas.ucla.edu/brweb/papers/Journals/BR_SSCM_2_2020.pdf to achieve for the value above

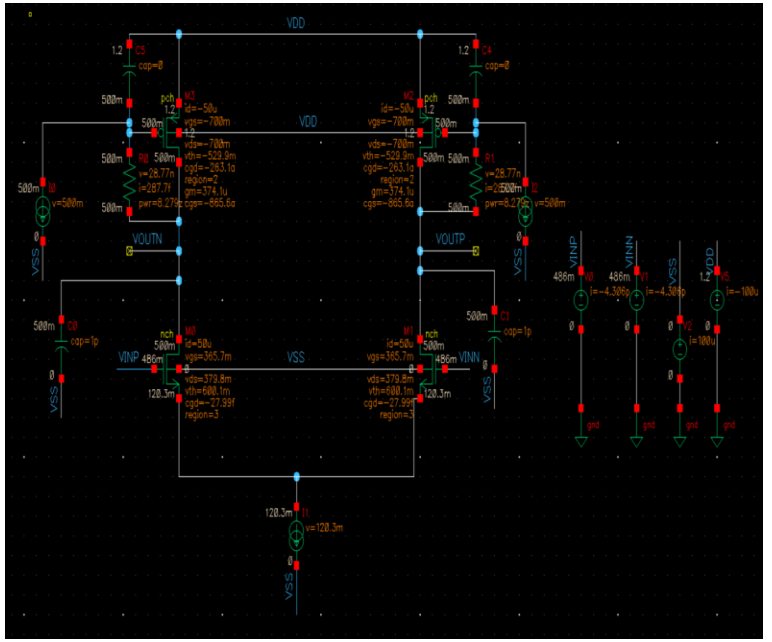
Experiment 2

- First, we run the parameter with the values of R searched for with the largest unity gain bandwidth, we choose R. Based on the formula with PMOS R1.I1 = VTH, which makes the gap not decrease too much.

$$I_1 R_1 = V_{TH} \Rightarrow I_1 = \frac{529.9m}{100K} = 5.299uA$$

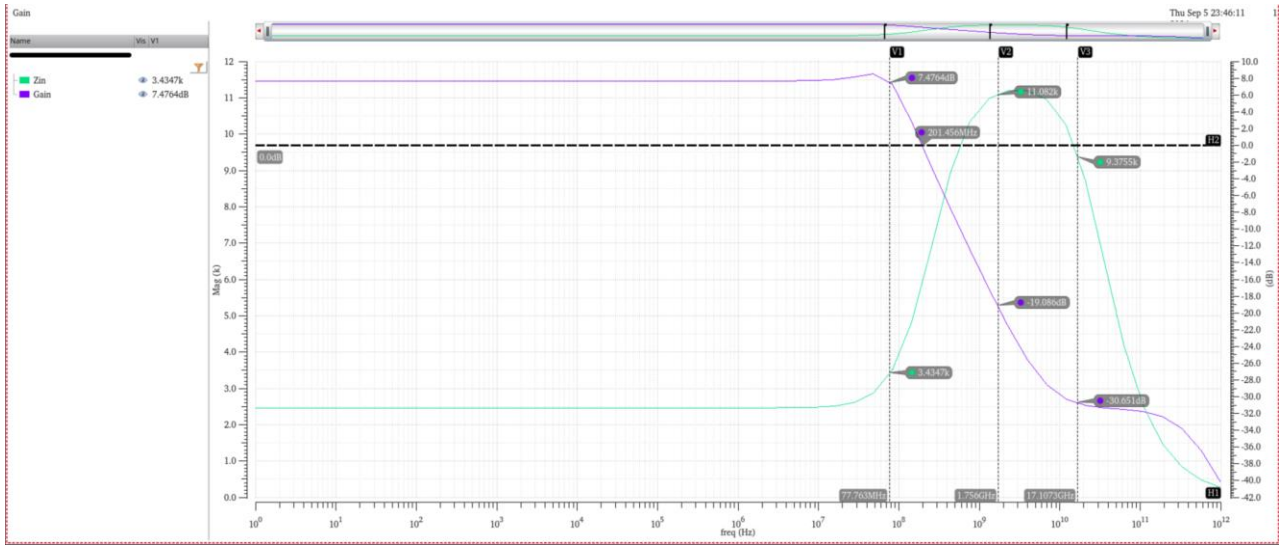


Frequency response of Differential pair with PMOS source follower



DC operating points

Experiment 2



As unity gain bandwidth $\approx 167MHz$=> $\frac{1}{2\pi R_1 C_0} = 167MHz \Rightarrow C_0 = 19.29f$

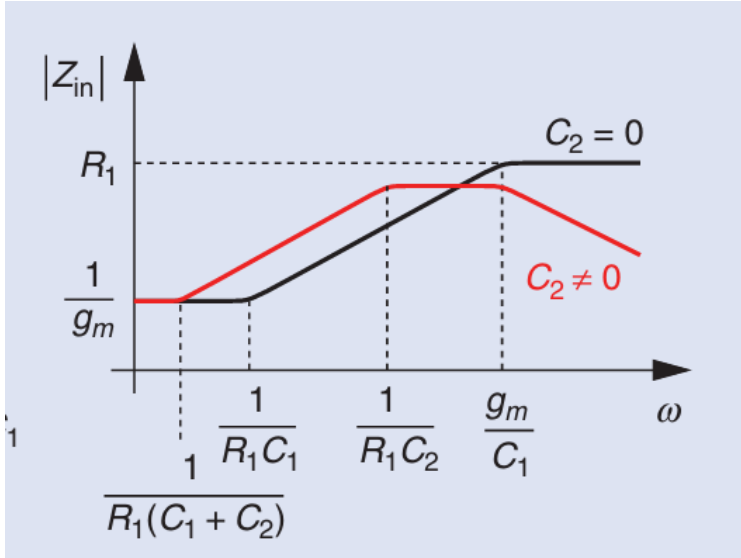
We have 2 poles and 1 zero point as shown, use the formula to find the points:

As $C_2 \neq 0; C_2 = Cgd; C_1 = C_{gs} + C_0$

$$f_z = \frac{1}{R1(C1 + C2) \times 2\pi} = \frac{1}{100K(19.29f + 865.6a + 263.1a) \times 2\pi} = 77.95MHz$$

$$f_{p1} = \frac{1}{R1C2 \times 2\pi} = \frac{1}{100K(263.1a) \times 2\pi} = 1.76GHz$$

$$f_{p2} = \frac{gm}{C1 \times 2\pi} = \frac{345u}{19.29f \times 2\pi} = 17.1GHz$$



Input impedance

We see on the plot of Av and Zin that the poles and zeros are quite similar to the theory. With Zin, when encountering a zero at low frequency, Zin will increase. Then, when encountering a pole at high frequency, Zin will decrease by an amount, and at very high frequency, Zin will decrease to a fairly low level.

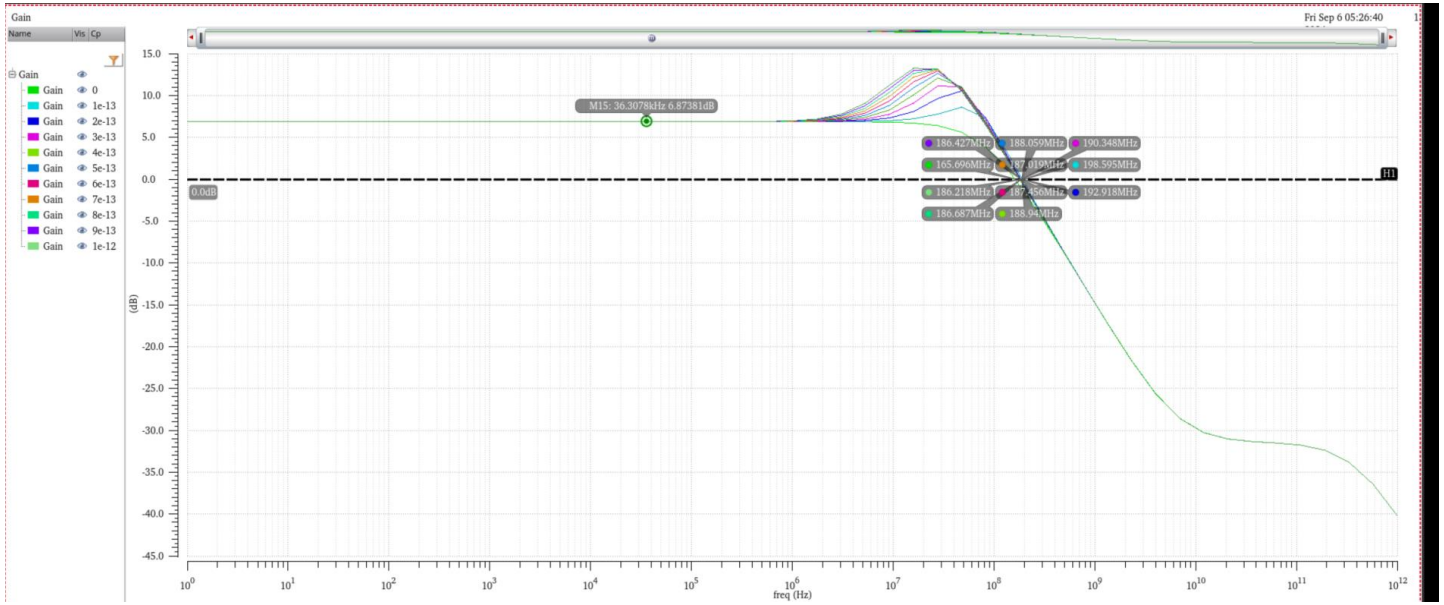
Experiment 2

In theory, the active conductor creates a shunt peaking phenomenon, with 1 capacitor and 1 resistor in parallel at the gate. The purpose is to prevent Av from being reduced too much, and to expand the band-width of the circuit.

At low frequencies, C1 is open so M1 is like a connected diode, at which time $Zin \approx \frac{1}{gm}$; at high frequencies Zin increases with frequency, if $\frac{1}{gm} \ll R_1 \Rightarrow Zin \approx R_1$

We also run parametric with values $C1 = 0 \rightarrow 1p$. It shows that at low frequencies, C1 does not affect the gain, however at high frequencies, the larger C1, the gain increase higher as meet zero of C1.

The larger the unity band-width, however, the gain decreases quite quickly.



Frequency response of *differential pair with diode-connected as C1 changes*

Thank you