ALU unit verification

Noah Woelki 05/10/2021

1 Introduction

To verify the functionality of the ALU unit, the VHDL code is tested using Verilog Simulation process. The implementation of the ALU consists of the entity and an architecture.

For verification a so called *testbench* is designed. The testbench creates a new unit of the ALU the *Unit under test (UUT)*.