Levi Masters

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**Homework 6**

Problem 1:

Consider the following sequence of memory accesses where each address is a byte address: 0, 1, 4, 3, 4, 15, 2, 15, 2, 10, 12, 2. Assume that the cash is direct-mapped, cash size is 4 bytes, and block size is one byte; Map addresses to cache blocks and indicate whether hit or miss.

0, 1, 4, 3, 4, 15, 2, 15, 2, 10, 12, 2.

0000 0001 0100 0011 0100 1111 0010 1111 0010 1010 1100 0010

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 Miss | |  | 1 Miss | |  | 4 Miss | |  | 3 Miss | |
| 00 | Mem(0) |  | 00 | Mem(0) |  | 01 | Mem(4) |  | 01 | Mem(4) |
|  |  |  | 00 | Mem(1) |  | 00 | Mem(1) |  | 00 | Mem(1) |
|  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  | 00 | Mem(3) |
|  |  |  |  |  |  |  |  |  |  |  |
| 4 Hit | |  | 15 Miss | |  | 2 Miss | |  | 15 Hit | |
| 01 | Mem(4) |  | 01 | Mem(4) |  | 01 | Mem(4) |  | 01 | Mem(4) |
| 00 | Mem(1) |  | 00 | Mem(1) |  | 00 | Mem(1) |  | 00 | Mem(1) |
|  |  |  |  |  |  | 00 | Mem(2) |  | 00 | Mem(2) |
| 00 | Mem(3) |  | 11 | Mem(15) |  | 00 | Mem(15) |  | 00 | Mem(15) |
|  |  |  |  |  |  |  |  |  |  |  |
| 2 Hit | |  | 10 Miss | |  | 12 Miss | |  | 2 Miss | |
| 01 | Mem(4) |  | 01 | Mem(4) |  | 11 | Mem(12) |  | 11 | Mem(12) |
| 00 | Mem(1) |  | 00 | Mem(1) |  | 00 | Mem(1) |  | 00 | Mem(1) |
| 00 | Mem(2) |  | 10 | Mem(10) |  | 10 | Mem(10) |  | 00 | Mem(2) |
| 00 | Mem(15) |  | 00 | Mem(15) |  | 00 | Mem(15) |  | 00 | Mem(15) |

Problem 2:

Consider the following sequence of memory accesses where each address is a byte address: 0, 1, 4, 3, 4, 15, 2, 15, 2, 10, 12, 2. Assume that the cash is direct-mapped, cash size is 4 bytes, and block size is two bytes; Map addresses to cache blocks and indicate whether hit or miss.

0, 1, 4, 3, 4, 15, 2, 15, 2, 10, 12, 2.

0000 0001 0100 0011 0100 1111 0010 1111 0010 1010 1100 0010

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 Miss | | |  | 1 Miss | | |  | 4 Miss | | |  | 3 Miss | | |
| 00 | Mem(1) | Mem(0) |  | 00 | Mem(1) | Mem(0) |  | 01 | Mem(5) | Mem(4) |  | 01 | Mem(5) | Mem(4) |
|  |  |  |  |  |  |  |  |  |  |  |  | 00 | Mem(3) | Mem(2) |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 4 Miss | | |  | 15 Miss | | |  | 2 Miss | | |  | 15 Miss | | |
| 01 | Mem(5) | Mem(4) |  | 01 | Mem(5) | Mem(4) |  | 01 | Mem(5) | Mem(4) |  | 01 | Mem(5) | Mem(4) |
| 00 | Mem(3) | Mem(2) |  | 11 | Mem(15) | Mem(14) |  | 00 | Mem(3) | Mem(2) |  | 11 | Mem(15) | Mem(14) |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 2 Miss | | |  | 10 Miss | | |  | 12 | | |  | 2 Miss | | |
| 01 | Mem(5) | Mem(4) |  | 01 | Mem(5) | Mem(4) |  | 11 | Mem(13) | Mem(12) |  | 11 | Mem(13) | Mem(12) |
| 00 | Mem(3) | Mem(2) |  | 10 | Mem(11) | Mem(10) |  | 10 | Mem(11) | Mem(10) |  | 00 | Mem(3) | Mem(2) |

Problem 3:

Consider a direct-mapped cache with 32 blocks

Cache is initially empty, Block size = 16 bytes

The following memory addresses (in hexadecimal) are referenced:

0x000002B4, 0x000002B8, 0x0000002BC, 0x000003E8, 0x000003EC, 0x000004F0, 0x000008F4, 0x0000008F8, 0x0000008FC.

Map addresses to cache blocks and indicate whether hit or miss.

|  |  |  |  |
| --- | --- | --- | --- |
| ADDRESS | IDX | TAG | H/M |
| 24B | 00 | 1 | MISS |
| 2B8 | 00 | 1 | HIT |
| 2BC | 01 | 1 | MISS |
| 2E8 | 1C | 2 | MISS |
| 2EC | 00 | 2 | MISS |
| 4F0 | 1C | 3 | MISS |
| 8F4 | 40 | 3 | MISS |
| 8F8 | 40 | 3 | HIT |
| 8FC | F0 | 3 | MISS |

Problem 4:

Below is a list of 32-bit memory address references (represented in decimal), each of them is a word addresses.

3, 180, 43, 2, 191, 88, 190, 14, 181, 44, 186, 253

For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with two-word blocks and a total size of 8 blocks. Also indicate whether hit or miss, assuming the cache is initially empty.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Address | Translation | tag | indx | LSB | H/M |
| 3 | 0000 0011 | 0000 | 001 | 1 | Miss |
| 108 | 1011 0100 | 1011 | 010 | 0 | Miss |
| 43 | 0010 1011 | 0010 | 101 | 1 | Miss |
| 2 | 0000 0010 | 0000 | 001 | 0 | Hit |
| 191 | 1011 1111 | 1011 | 111 | 1 | Miss |
| 88 | 0101 1000 | 0101 | 100 | 0 | Miss |
| 190 | 1011 1110 | 1011 | 111 | 0 | Hit |
| 14 | 0000 1110 | 0000 | 111 | 0 | Miss |
| 181 | 1011 0101 | 1011 | 010 | 1 | Hit |
| 44 | 0010 1100 | 0010 | 110 | 0 | Miss |
| 186 | 1011 1010 | 1011 | 101 | 0 | Miss |
| 253 | 1111 1101 | 1111 | 110 | 1 | Miss |