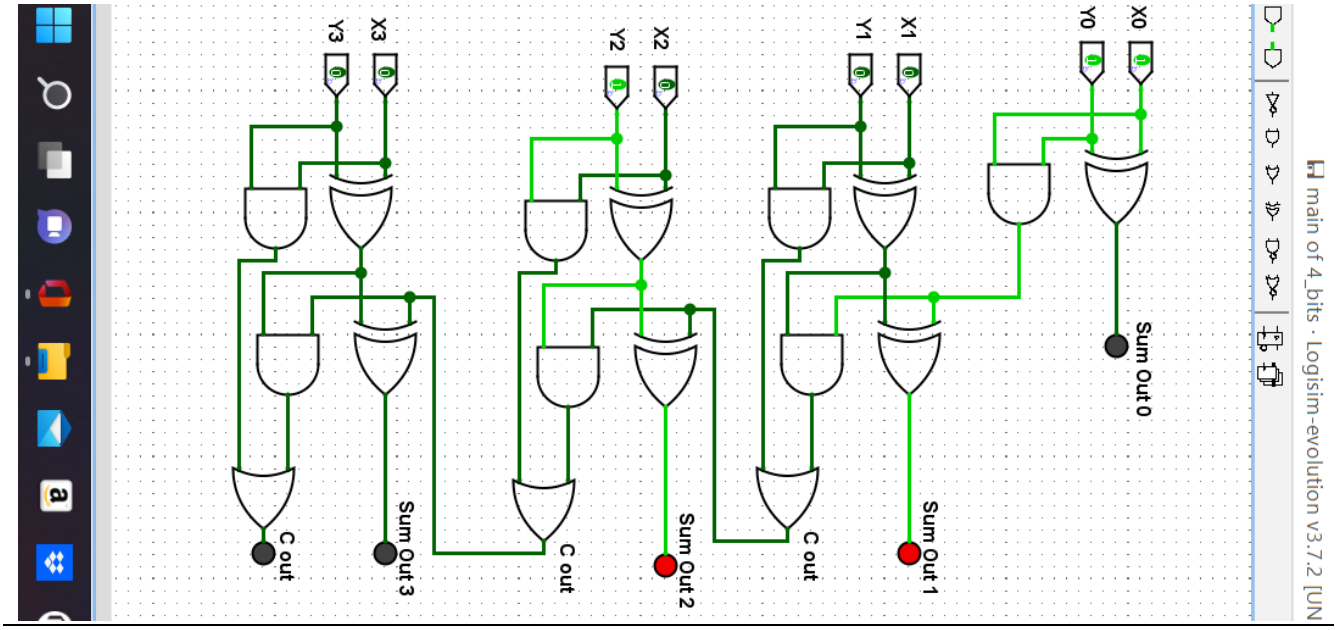
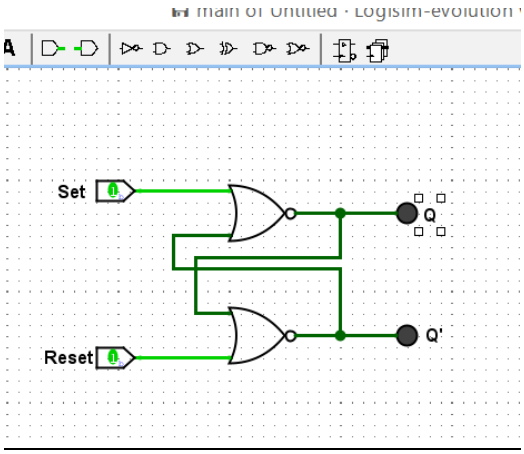
4 Bit Adder



Input X	Input Y	Output
0101	0000	0101
0101	0001	0110
0101	0010	0111
0101	0011	1000
0101	0100	1001
0101	0101	1010
0101	0110	1011
0101	0111	1100
0101	1000	1101
0101	1001	1110
0101	1010	1111
0101	1011	0000
0101	1100	0001
0101	1101	0010
0101	1110	0011
0101	1111	0100

R-S Flip-Flop



Set	Reset	Q	Q’
1	0	0	1
1	1	0	0
0	1	1	0
1	1	0	0

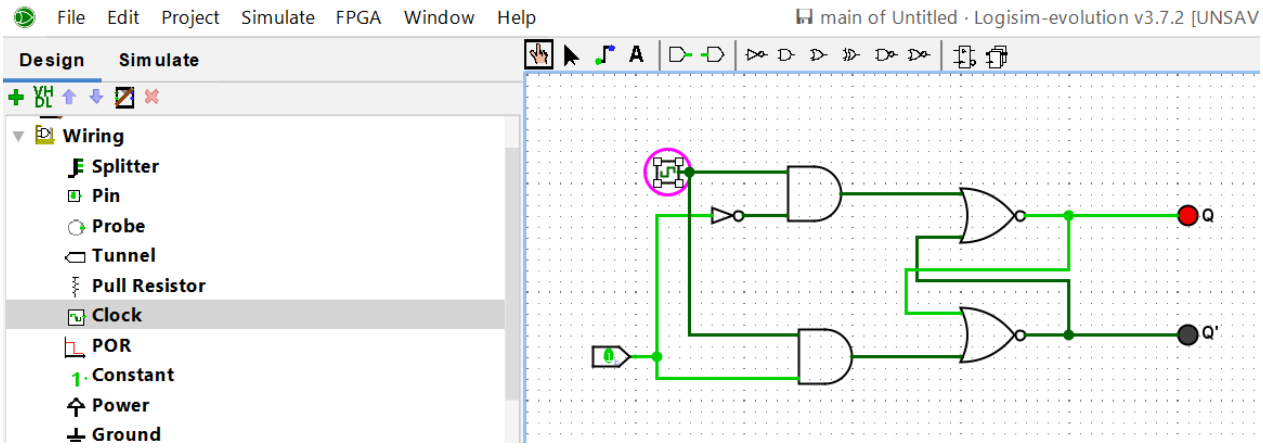
Describe in a sentence, the behaviour of the circuit when one of the inputs is 1 (but not both) and why this is useful for digital circuit design.

If Input Set is set to 1, the output (Q) goes low (0) and consequently, the other output (Q') goes high (1) and if Input Reset is set to high (1), the output Q' goes low (0).

What do you notice about the two times you set both inputs to 1. Briefly explain what is happening here and why this is an issue for digital circuit design?

There is no change in the output, all output goes low (Zero) since the outputs of an R-S Flip-Flops are always the negation of its inputs. Also, R-S Flip-Flop is asynchronous and there is no stability when it comes to getting the results of the two outputs simultaneously.

D Flip-Flop



Clock	Pin	Q	Q'
0	0	1	0
0	1	1	0
1	1	1	0
1	0	0	1

Briefly explain the behaviour of a D Flip Flop and how it is useful for digital circuit design.

The D Flip-Flop has only one input and according to the Logisim Experiment, when the clock is turn into an active mode, the output Q change to become the value same as input, D. D Flip-Flops are used in computer registers, memories, counters, and shift registers.

What is the role of the clock? How does it impact the changing of state of Q and Q'?

The clock helps to synchronise activity to ensure to stability and predictability within a circuit. As the clock is turned on in D Flip-Flop, The value of the output Q goes same as the input D and when it is off, the value of the output Q and Q' both remain as it is.

Why is it generally preferred over the R-S Flip Flop?

R-S Flip-Flops are not clocked. That is, they never work in synchrony, the output may take time and therefore promote instability within the output results. D Flip-Flops are better since the results are obtained instantaneously.