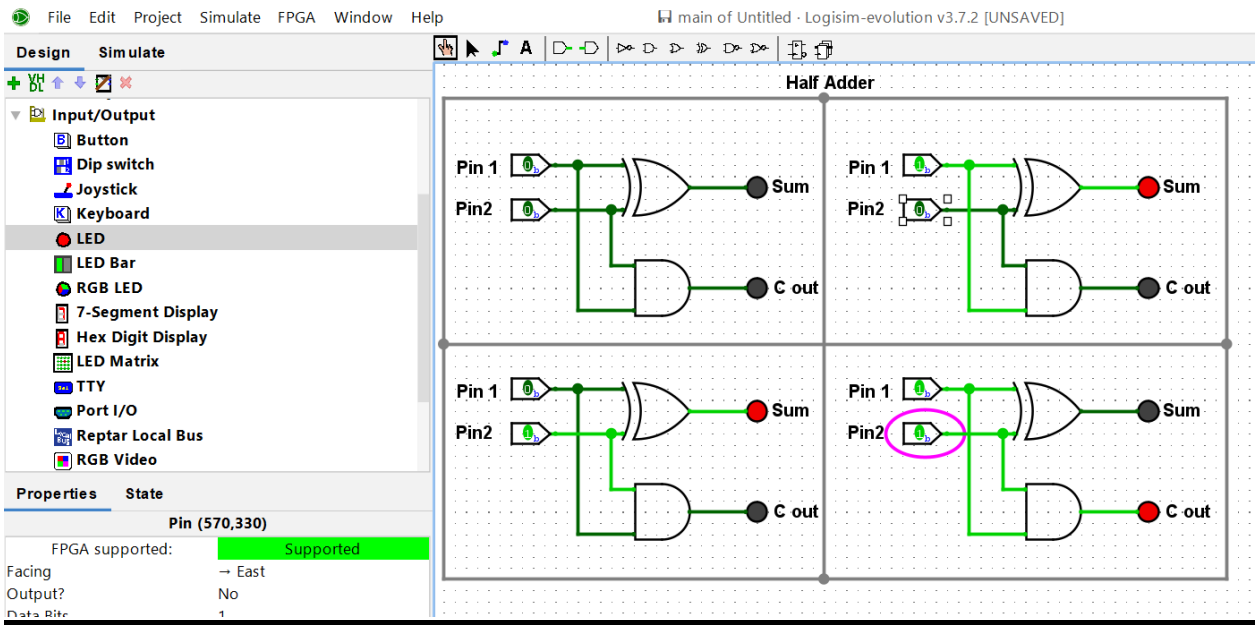
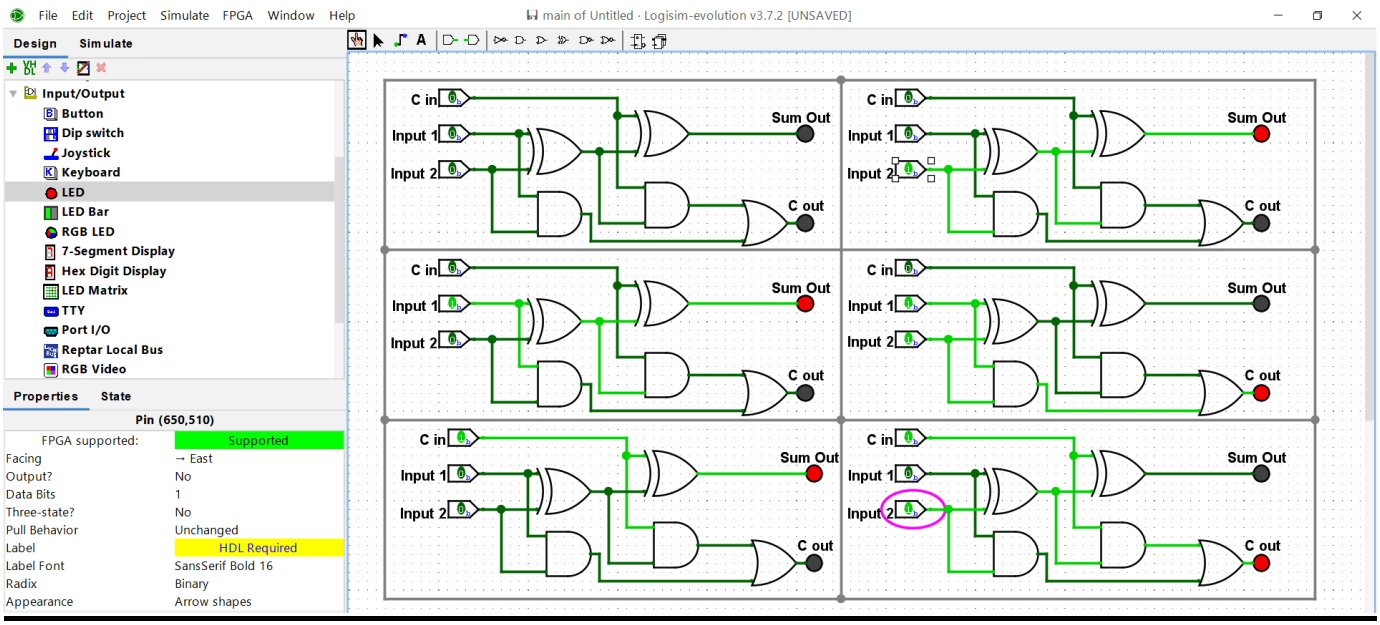
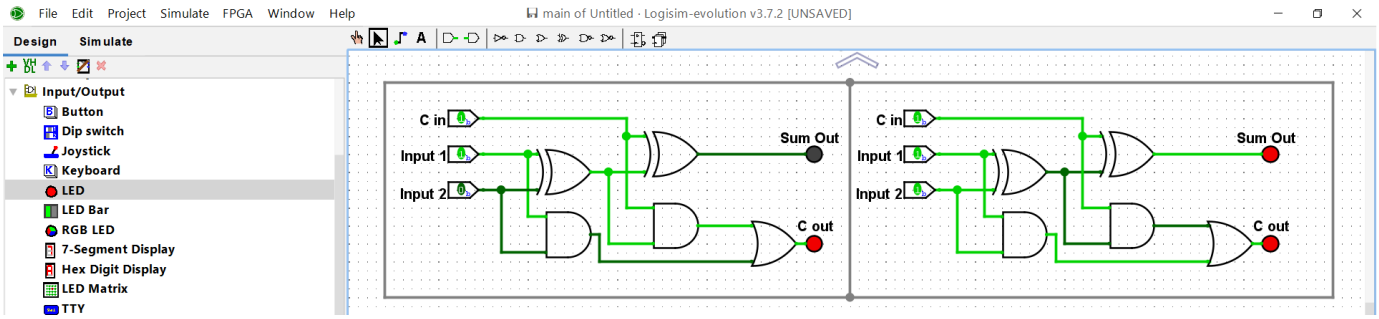
4. Half-Adder



Input 1	Input 2	Sum Output	Carry Output
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

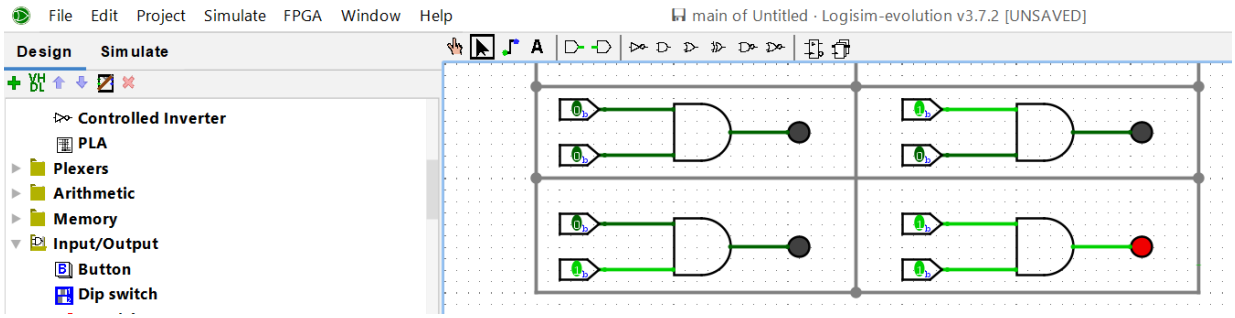
5. Full-Adder





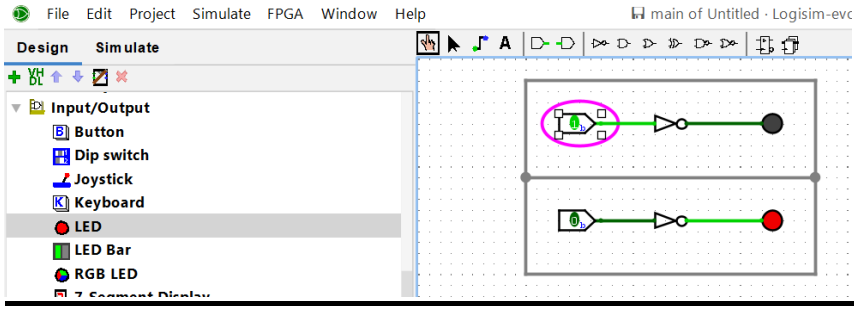
Input 1	Input 2	Carry Input	Sum Output	Carry Output
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

2. AND Gate



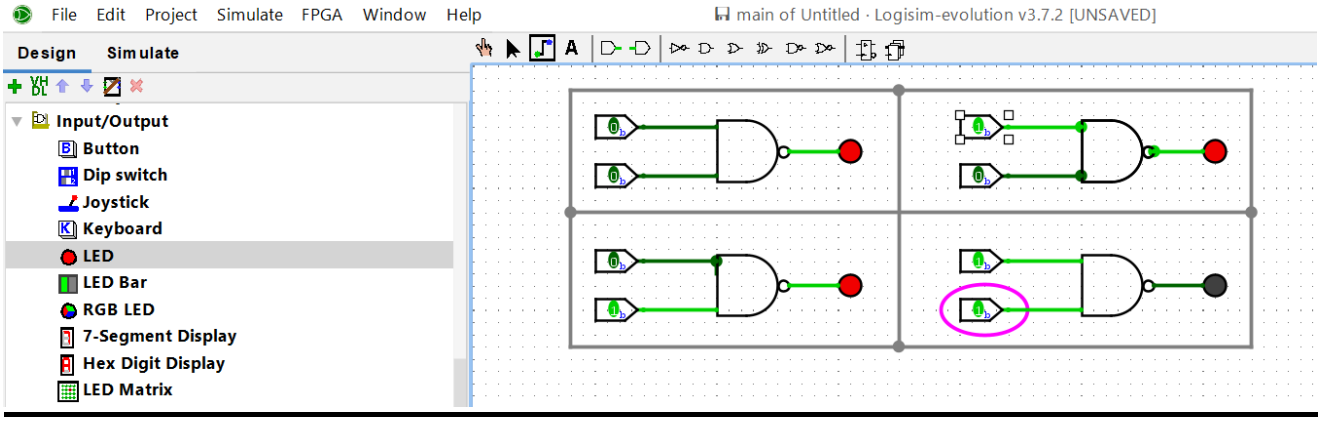
Pin 1	Pin 2	Output
0	0	0
1	0	0
0	1	0
1	1	1

1. NOT Gate



Pin	Output
1	0
0	1

3. NAND Gate



Pin 1	Pin 2	Output
0	0	1
1	0	1
0	1	1
1	1	0