Description:

The circuit overleaf implements a 4-bit version of the Register-file section of the datapath shown in Mano and Kime figure 7-9 (or 4th lecture, page 12), by using components designed in VHDL.

1. Design the VHDL components (Register, Decoder, and two Multiplexer 32 bit)   and interconnect them to build a register-file. The schematic shows only four registers. Your solution should implement 32 registers.
2. You should provide test benches and simulations   that prove the correctness of the following operations:
    a. Load your StudentID (HEX value) into the first of the 32 registers. Then load your StudentID - 1 (HEX value) into the 2nd register, your StudentID - 2 (HEX value) into the 3rd register... Please continue until all 32 registers have a value.
    b. Transfer the contents of any register to any other register, i.e. that it can execute the transfers R_i <- R_j, I,j=O,31 (show 10 examples)