BES2700H-6X/8X

Datasheet Rev. 1.1

Ultra-Low Power Bluetooth Audio Platform

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Revision History

The following table lists the technical content changes for all revisions.

Revision	Date	Description
1.0	July 2022	Initial release
1.1	August 2022	Updated the pin map

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1 General Description

BES2700H-6X/8X is an ultra-low power and highly integrated Bluetooth audio SoC, which features a high-performance dual-core STAR-MC1 CPU subsystem and a sensor hub subsystem. This combination dramatically reduces power consumption while enabling abundant application processing capabilities.

The platform integrates a dual-mode BT 5.3 subsystem to support BT classic and LE audio, and integrates a codec subsystem to support always-on voice assistants and audio applications. It also integrates a serial flash to support various software features and product customization.

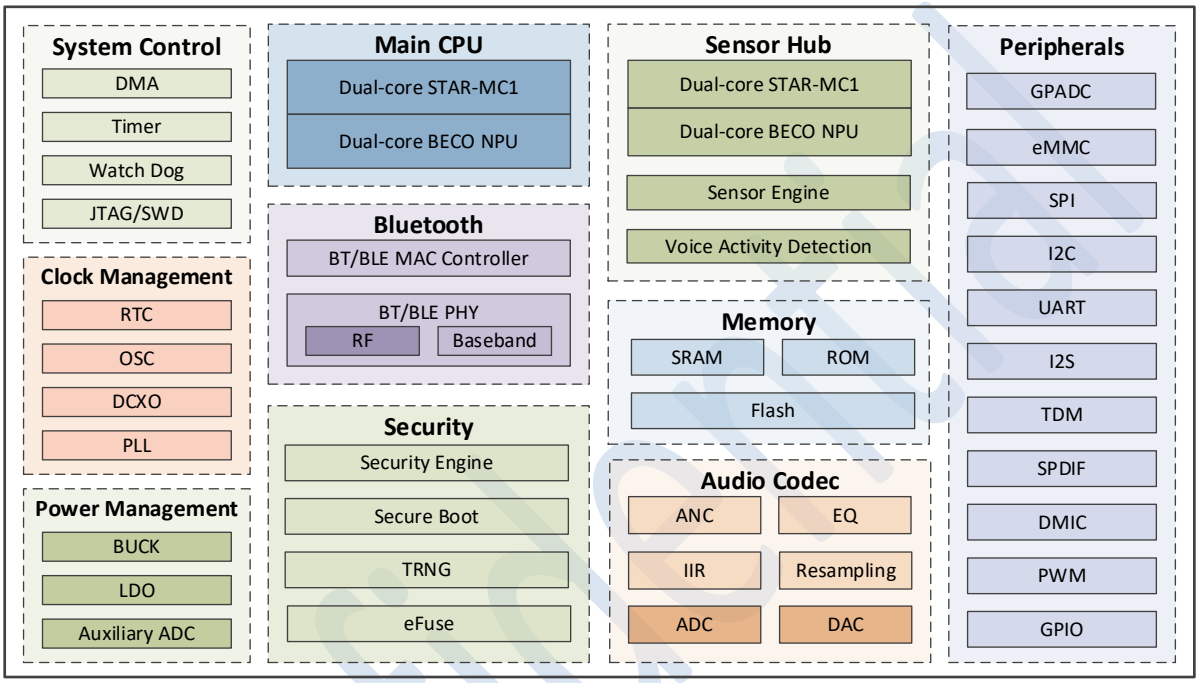


Figure 1-1 System Block Diagram

1.1 Applications

- Adaptive TWS ANC
- Adaptive ANC headphones
- High-end Bluetooth headsets
- Spatial audio
- BT boom boxes
- Bluetooth and LE audio portable speakers
- IoT platform

1.2 Features

CPU Subsystem

- Up to 208 MHz dual-core STAR-MC1 for application development
- Dual-core BECO NPU for advanced signal processing
- Shared 2.2 MB SRAM
- 96 KB boot ROM
- 4/8 MB flash in package
- Support OTA

Sensor Hub Subsystem

- Up to 96 MHz dual-core STAR-MC1 for the sensor hub
- Dual-core BECO NPU for advanced signal processing
- Sensor engine
  - Hardware engine for sensor data gathering
  - 32 KB buffer size
  - Support 2x SPI, 4x I2C
- 2x UART interfaces, 3 Mbps, with CTS/RTS
- 6x cap sensors

Bluetooth Subsystem

- Dual-mode BT 5.3 with LE audio
- Support multipoint connectivity
- Bluetooth transmit power:
  - BDR: up to 14 dBm
  - EDR: up to 11 dBm
  - BLE: up to 14 dBm
- Bluetooth receiver sensitivity:
  - BDR: -95.5 dBm
  - EDR: -94.5 dBm (π /4 DQPSK)
  - EDR: -88.5 dBm (8DPSK)
  - BLE: -100 dBm

Audio Features

- Adaptive hybrid ANC
- 2x audio DACs:
  - SNR: 110 dB
  - DNR: 109 dB
  - Sample rate: 8 kHz to 384 kHz
- 5x audio ADCs:
  - SNR: 103 dB
  - Sample rate: 8 kHz to 384 kHz
- 24-bit audio processing
- Support PDM/I2S digital mic input
- I2S/TDM: 32-bit, TDM supports 8-channel

PSAP (Personal Sound Amplify Product) Features

- 16 frequency bands configurable
- Delay < 0.65 ms
- Multi-knee DRC
- Environment noise suppression
- Support dual-microphone beam forming
- Howling suppression

ANC Features

- Wideband digital adaptive ANC
- Support AI voice
- Support low power voice activity detection
- Up to 45 dB attenuation at 200 Hz
- Over 1 kHz suppression range
- Input-to-output latency < 9 us

Peripheral Interfaces

- 2x Watchdogs, with reset and interrupt
- Up to 80 MHz QSPI interface for the flash
- 2x SPI interfaces, 48 MHz
- 6x I2C interfaces, 400 Kbps
- 2x I2S master interfaces
- 3x UART interfaces, 3 Mbps
- 4x GPADCs: 12-bit SAR ADCs
- 2x 32-bit timers
- 8x PWM out
- GPIOs:
  - 32x digital IOs, all could be used as GPIOs
  - Each IO supports interrupts

Security and Cryptography

- TRNG (True Random Number Generator)
- Cryptography engine with AES 256-bit, 3DES, SHA-512, aes-128/192/256 ecb/cbc/ctr/xts, md5, sha1/224/256/384/512, des/3des ecb/cbc
- 512-byte OTP (one-time programmable)

Clock Management

- 24 MHz crystal oscillator
- Internal 96 MHz RC oscillator
- Internal low-power LPO

- 2x PLLs for system clock and audio

PMU Features

- 3.1 V-5.5 V input for VBAT
- Internal temperature sensor
- 2x LDOs for peripherals: 1.8 V and 3.3 V, both are available in sleep mode
- DCXO with internal oscillator circuit, typical 24 MHz

Package

- 219-pin BGA (5.7 mm x 6.2 mm x 0.88 mm, 0.35 mm pitch)

2 Functional Description

2.1 CPU Subsystem

2.1.1 Overview

BES2700H-6X/8X is embedded with a multi-core STAR-MC1 processor to provide the best system performance with the lowest power consumption. High-throughput low-latency DMA reduces CPU loads and improves data transfer performance.

- Multi-core high-performance STAR-MC1 processor with float and HW DSP instruction
- Supports I-Cache and D-Cache
- Supports various memories in package
- High-performance multi-layer AMBA bus
- Clock frequency up to 208 MHz
- Secure boot support
- Watchdog Timer (WDT) for system crash recovery
- General-purpose Timers
- DMA for audio/voice data transfer

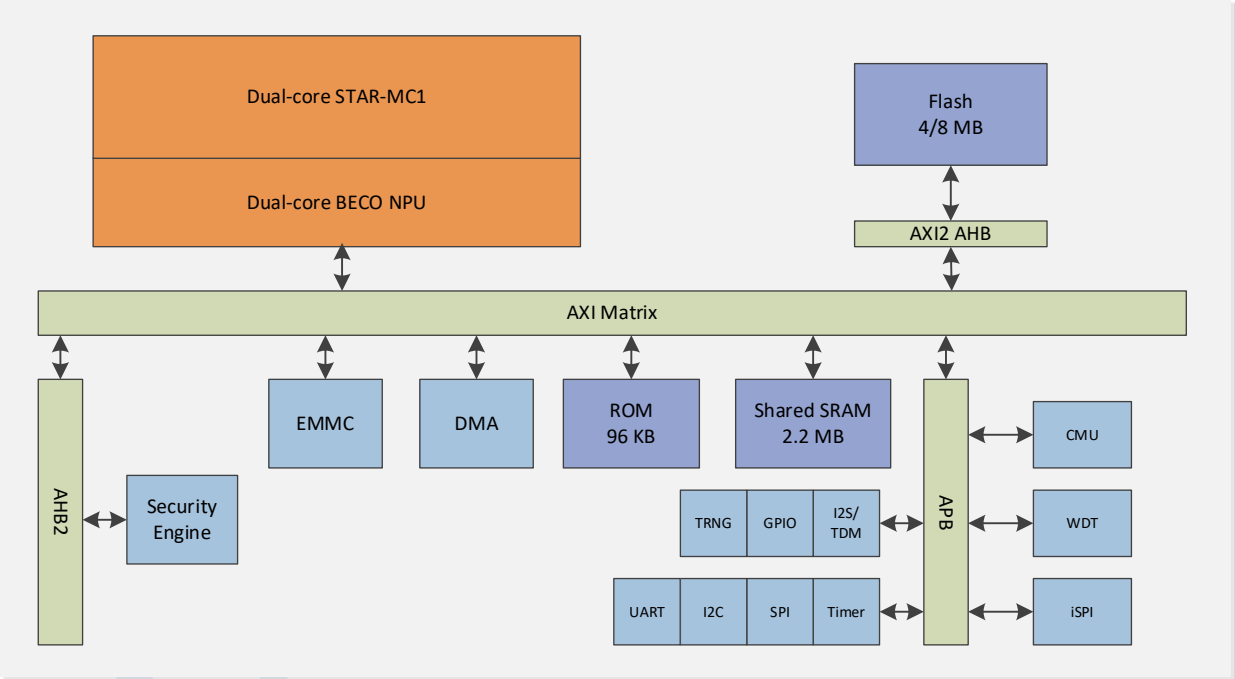


Figure 2-1 CPU Architecture

2.1.2 STAR-MC1 Processor

The STAR-MC1 processor is an embedded processor designed by Arm China, compatible with Cortex-M33. It is based on the latest Armv8-M architecture and can be used for microcontrollers or integrated SoCs. The STAR-MC1 processor is a lightweight real-time processor for IoT devices. It is optimized for the needs of IoT devices and can fully implement real-time control, digital signal processing, and safe operation of IoT devices. The STAR-MC1 processor occupies an extremely small area and features low power consumption.

The STAR-MC1 processor has the following features:

- Up to 208 MHz clock frequency with 1.5 DMIPS/MHz performance
- Harvard architecture
- 32-bit data/address
- Address below 0x2000_0000 uses code ports and address above 0x2000_0000 uses system ports
- Integrated DSP and SIMD instructions
- 32-bit hardware multiply-accumulate unit (MAC)
- Hardware divide instruction
- Single-precision floating point instructions
- Thumb-2 technology allows 16-bit instructions and 32-bit instructions to work together without any state switching overhead
- Arm eco-system, with CMSIS library and third-party libraries

2.1.3 BECO Coprocessor

The BECO coprocessor is designed for parallel multiply accumulate workloads in bus-limited systems. Beneficial algorithms are everything that can be reduced to a vector dot product, GeMM, or FIR filter structures.

The BECO coprocessor has the following features:

- Calculate up to 64 dot-products in parallel
- 64 accumulators can be stacked for 8x8, 8x16 or 16x16 bit multiplication
- Mixed sign vector input support
- Mixed bit-dept vector input support
- 8 general purpose 64 bit registers
- Accumulator with 11 bit head-room, allowing 1024 mixed signed/unsigned or 2048 element same sign accumulation
- Support multiply accumulate
  - (col-vector x row-vector) -> matrix
  - (vector x vector) -> vector and
  - Broadcast (scalar) x vector -> vector
- Special support for calculating (long) FIR filters
  - FIR mode need 8 cycles per tap
  - Using scalar broadcast mode. The FIR core calculates 16 output samples in parallel.
  - One and two channel interleaved input is supported.
- Performance: 16 MACC per cycle. 64 every 4 cycles in parallel with memory loads and ARM instructions.
- Multi-cycle instructions are decoupled from main program flow, allowing nearly 100% utilization of the MACC's.
- Output Scale/Pack module prepare 32 bit per cycle. Either packed 8 or 16 bit vectors or single 32 bit integer or float32.
- Output handle signed and unsigned saturation. Unsigned saturation is used for ReLU and Hard-Sigmoid. This allows changing of (data:unsigned x weights:signed) -> data:unsigned.
- Simple element rotation, Rubik, allow on-the-fly transpose of output matrix.

2.1.4 Memory

BES2700H-6X/8X supports internal and external memories.

- Embedded ROM 96 KB for critical constants and code
- Embedded SRAM 2.2 MB for critical data and code
- SIP serial flash 4/8 MB

2.2 Sensor Hub Subsystem

2.2.1 Overview

The sensor hub subsystem provides computability for RTOS, sensor data processing and user programs. The operating frequency is up to 96 MHz. High bandwidth modules are connected to the multi-layer AHB bus, such as CPU/DMA/memories; low bandwidth modules are connected to the APB bus, such as I2C/SPI.

The CPU core is STAR-MC1 with single-precision float and SIMD (Single Instruction Multiple Data) for DSP, and implemented with the BECO coprocessor. For more information about the features, see **2.1.2 STAR-MC1 PROCESSOR** and **2.1.3 BECO COPROCESSOR**. The sensor subsystem also includes a hardware I2C or SPI master engine, which can access sensors automatically with programmed command sequences.

The sensor hub subsystem supports SWD debugging.

2.2.2 Sensor Engine

The sensor engine is a flow controller working together with the I2C or SPI master to transfer data periodically between the external sensor data buffer and internal memory without CPU core interference. Thus, the CPU core can be clock gated to reduce power or used to process other primary data.

The sensor engine has the following features:

- Support 5 sensors in total
- Each sensor can use I2C or SPI to transfer data
- Two trigger modes: periodical timer or external interrupt

2.3 Bluetooth Subsystem

2.3.1 Overview

BES2700H-6X/8X offers a highly integrated Bluetooth subsystem. Only the minimum number of external components are required. The internal SRAM is 64 KB and ROM is 600 KB.

BES2700H-6X/8X is fully compliant with Bluetooth BT/BLE 5.3 dual-mode. It also supports the LE Audio CIS/CIG and BIS/BIG full feature set.

2.3.2 Bluetooth Radio

BES2700H-6X/8X has the following Bluetooth radio features:

- Integrated Bluetooth TX/RX switch
- Fully integrated RF synthesizer without any external component
- Bluetooth transmit power (configurable with a step size of 1 dB):
  - BDR: up to 14 dBm
  - EDR: up to 11 dBm

- BLE: up to 14 dBm

- Bluetooth receiver sensitivity:
  - BDR: -95.5 dBm
  - EDR: -94.5 dBm (π /4 DQPSK)
  - EDR: -88.5 dBm (8DPSK)
  - BLE: -100 dBm

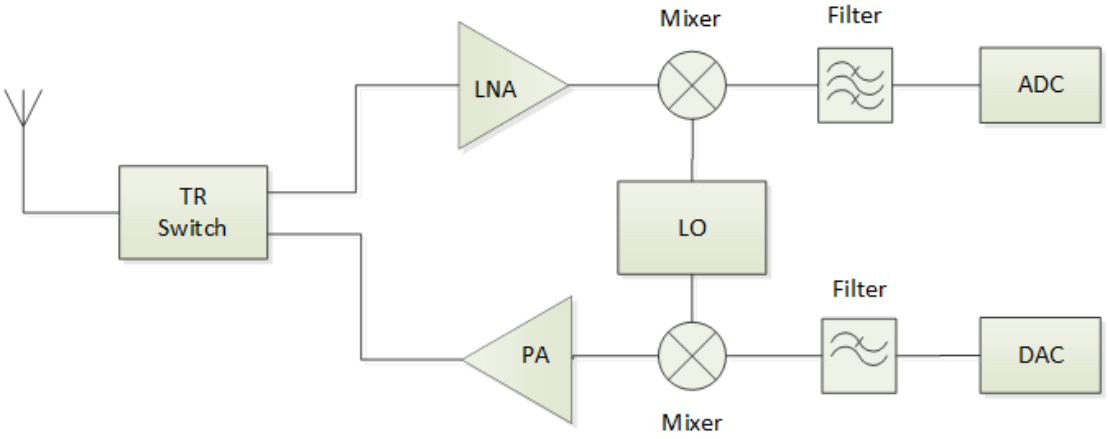


Figure 2-2 RF Architecture

2.3.3 Auxiliary Features

- Supports low power mode for power management
- Internal LPO for Bluetooth sniff mode

2.4 Audio Codec Subsystem

2.4.1 Overview

BES2700H-6X/8X integrates an audio codec subsystem, which consists of the following blocks:

- Stereo/dual-mono audio codec
- 5x 24-bit high-quality ADCs with sample rates from 8 kHz to 384 kHz
- 2x 32-bit high-quality DACs with sample rates from 8 kHz to 384 kHz
- 1x configurable I2S/TDM interface

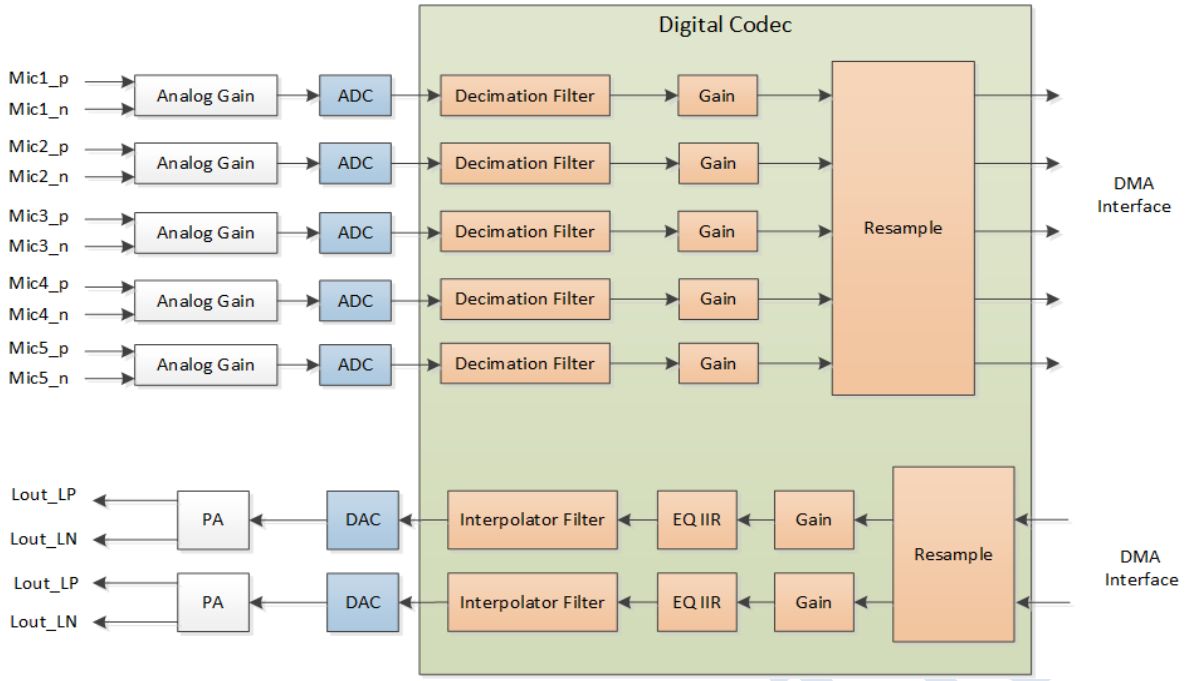


Figure 2-3 Audio Codec Diagram

2.4.2 ADC

BES2700H-6X/8X can accept both line level and microphone ac-couple inputs. Each analog input channel can be configured in diff-ended mode or single-ended mode. In single-ended mode, ac-couple the unused input pins to the ground.

Each ADC has a three-order Sigma-Delta converter. Each ADC is a separate channel with identical functionality. There are two gain stages for each channel, one of which is an analogue gain stage and the other is a digital gain stage.

The main ADC parameters are listed as follows:

- SNR: 103 dB
- THD+N: -90 dB
- Sample rate: 8 kHz to 384 kHz

For more information about the ADC parameters, see **3.3 AUDIO CODEC ELECTRICAL CHARACTERISTICS**.

2.4.3 DAC

Data can be routed to the output DAC paths from the serial ports, ADCs and digital microphones. Both DAC channels must have a source at the same sample rate. The analog output pins are capable of driving headphone or earpiece speakers. The analog output pins are biased at the CM voltage.

The main DAC parameters are listed as follows:

- SNR: 110 dB
- DNR: 109 dB
- THD+N: -96 dB
- Sample rate: 8 kHz to 384 kHz

For more information about the DAC parameters, see **3.3 AUDIO CODEC ELECTRICAL CHARACTERISTICS**.

2.5 Power Management

BES2700H-6X/8X integrates a Power Management Unit (PMU), which supports 3.1 V~5.5 V input from VBAT. The PMU includes multiple LDOs and DCDCs to achieve low power consumption, as well as an internal 32 KHz LPO for standby and sleep modes. Power-on reset control is supported.

BES2700H-6X/8X offers various low power features to reduce power consumption. The following modes are available: standby mode with 32 kHz clock, power-down mode for individual peripherals and processor sleep mode. In addition, BES2700H-6X/8X is also fabricated by using the advanced low leakage CMOS process in order to provide an ultra-low leakage solution.

BES2700H-6X/8X provides the following LDOs:

- LDO_VIO generates a 1.2 V~3.3 V supply rail for the sensor;
- LDO_VMEM generates a 1.2 V~2 V supply rail for the memory, GPIOs, and audio codec;
- LDO_VDCDC generates a 1.0 V~1.8 V supply rail for the analog blocks;
- LDO_CORE generates 0.3 V~1.3 V supply rail for the digital logics;
- LDO_VPA generates a 2.1 V~3.3 V supply rail for the RF PA;
- LDO_VUSB generates a 2.1 V~3.3 V supply rail for the USB;
- LDO_MIC generates a 1.5 V~3 V supply rail for the microphone.

BES2700H-6X/8X provides the following switch-mode DCDCs for low-power applications. The efficiency is high from light loads to heavy loads.

- BUCK 1 generates a 0.6~1.2 V supply rail for the digital core;
- BUCK 2 generates a 1.0~1.7 V supply rail for the analog blocks;
- BUCK 3 generates a 1.3~2.2 V supply rail for the memory, GPIOs, and audio codec.

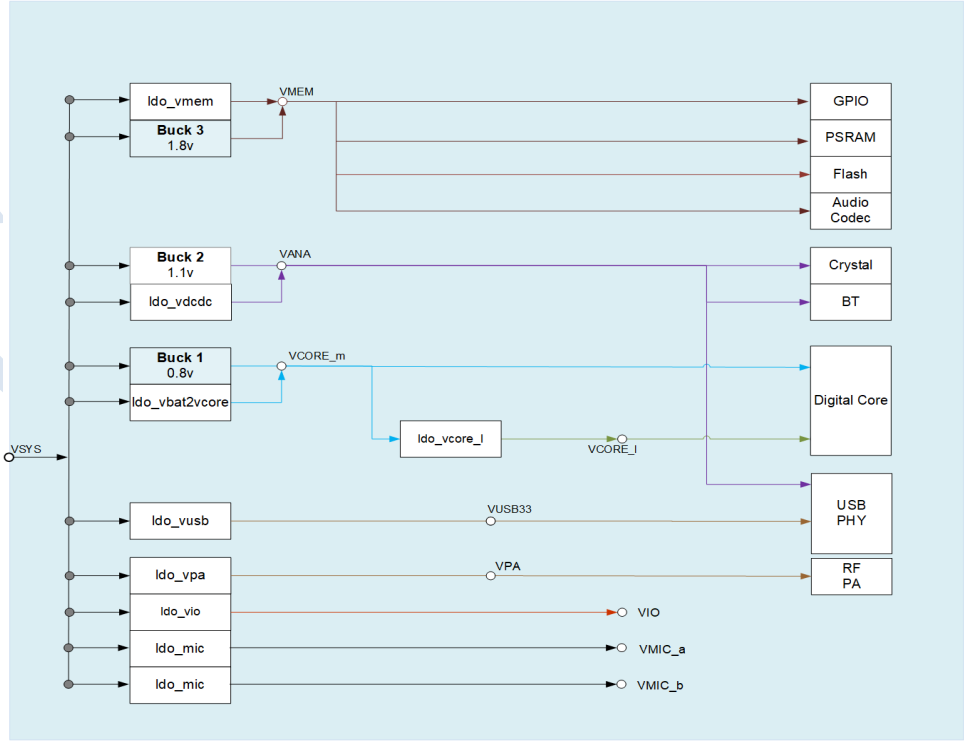


Figure 2-4 PMU Block

2.6 System Peripherals

2.6.1 Overview

BES2700H-6X/8X is embedded with rich peripheral blocks, and supports URAT downloading.

- Clock management unit (CMU) provides general control over the whole system
- UART with configurable baud rates
- I2C master/slave peripheral interfaces
- General Purpose Input Output (GPIO) with independent interruptions
- Pulse Width Modulation (PWM)
- Several timers: RTC timer, WDT, General-purpose Timer

2.6.2 Clock Management

BES2700H-6X/8X provides the clock management module to manage the clocks and system reset. The module supports the following features:

- Clock frequency division
- Selection and switch of clock sources
- Clock enable control
- Set and release of reset signals for other modules

2.6.3 UART

BES2700H-6X/8X provides independent UART interfaces, which support the following features:

- FIFO-based design. The FIFO trigger threshold can be configured.
- Support DMA to transfer data on the APB bus
- Support interrupts to report errors, such as overrun, underrun, RX timeout, etc.
- Programmable baud rate generator
- Standard asynchronous communication bits (start, stop and parity). These are added before transmission and removed upon reception.
- False start bit detection
- Line break generation and detection
- Programmable hardware flow control

2.6.4 I2C

BES2700H-6X/8X provides I2C interfaces, which support the following features:

- FIFO based design. The FIFO trigger threshold could be configured.
- Support DMA to transfer data on the APB bus
- Support interrupts or polled-mode operations
- Support bulk transmit mode
- Support interrupts to report events and errors, such as FIFO, RX overrun, TX underrun, TX abort, etc.
- Programmable I2C clock frequency
- Support the following speed modes:
- Standard mode (0 to 100 Kbps)
- Fast mode (up to 400 Kbps)
- Fast mode Plus (up to 1.4 Mbps)
- Support RESTART

- Support 7-bit or 10-bit addressing
- Support spike suppression for SDA

2.6.5 GPIO

BES2700H-6X/8X provides programmable GPIOs, which support the following features:

- Direction and outputs of the IOs can be programmed separately.
- Input data of the IOs can be read back through memory-mapped registers.
- Support interrupts. The interrupt feature can be programmed separately.
- Support optional debounce for interrupts

Multiple peripheral functions can be assigned to the GPIOS. For more information, see 4.2 GPIO PIN-MUX.

2.6.6 PWM

BES2700H-6X/8X has a PWM module. The PWM module supports multiple channels.

- Each of the PWM channels contains the following registers:
  - 16-bit initial value register (read/write)
  - 16-bit toggle register (read/write)
  - 16-bit PWM counter value register (read)
- A PWM configuration register is provided to implement the following functions:
  - Configure each PWM channel
  - Select the clock of each PWM channel
  - Change the phase of each PWM channel

2.6.7 Timers

BES2700H-6X/8X has a timer module, which consists of two programmable counters. They operate from the common timer clock, but have their own clock enable inputs. Each count rate is controlled by its individual clock enable and prescaler.

Each counter can operate in three timer modes:

- Free-running
  The counter operates continuously and wraps around to its maximum value each time it reaches zero.
- Periodic
  The counter operates continuously by reloading from the Load Register each time it reaches zero.
- One-shot
  The counter is loaded with a new value by writing to the Load Register. The counter decrements to zero and then halts until it is reprogrammed.

3 Electrical Characteristics

3.1 Electrical Characteristics

Table 3-1 Operating Conditions [a]

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply Voltage from battery or LDO		3.8		V
T_{amb}	Ambient Temperature	-20	27	+85	°C
V_{IL}	CMOS Low Level Input Voltage	0		$0.3*V_{IO}$ [b]	V
V_{IH}	CMOS High Level Input Voltage	$0.7*V_{IO}$		V_{IO}	V
V_{TH}	CMOS Threshold Voltage		$0.5*V_{IO}$		V

(a) Minimum input voltage of 3.1V is required in the recommended operation conditions.

(b) V_{IO}=1.8V

Table 3-2 Absolute Maximum Ratings [c]

Symbol	Description	Min.	Typ.	Max.	Unit
T_{amb}	Ambient Temperature	-30		+85	°C
I_{IN}	Input Current	-10		+10	mA
V_{IN}	Input Voltage	-0.3		V_{IO} [b]+0.3	V
V_{lna}	LNA Input Level			0	dBm
V_{BAT}	Supply Voltage			6 [a]	V

(a) Standard maximum input voltage is 6V.

(b) V_{IO}=1.8V

(c) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 3-3 Power Consumption [a]

Symbol	Description	Min.	Typ.	Max.	Unit
Power off	Soft power off mode	/	3	/	uA
Sleep mode 1	No BLE/BT connect	/	60	/	uA
BLE connect	Interval 1s	/	TBD	/	uA
BLE ADV	200ms interval	/	TBD	/	uA
BT connect	Sniffing interval 500ms	/	TBD	/	uA
BT play music	AAC 128kbps	/	TBD	/	mA
BT Phone call	Msbc 16k	/	TBD	/	mA
MP3 local play	128kbps MP3 EMMC play no speaker	/	TBD	/	mA

(a) The power consumption is in the DCDC mode and VBAT=3.8V

3.2 Bluetooth Radio Electrical Characteristics

Table 3-4 Receiver Characteristics - Basic Data Rate [a]

Symbol	Description	Min.	Typ.	Max.	Unit
Sensitivity with dirty transmit off@0.1% BER		/	-95.5	/	dBm
Sensitivity with dirty transmit on@0.1% BER		/	-94	/	dBm
Maximum received signal@0.1% BER		/	/	0(b)	dBm
C/I co-channel		/	8	11	dB
Adjacent channel selectivity C/I Adjacent channel selectivity C/I	F=F_0 + 1MHz	/	-10	-4	dB
	F=F_0 - 1MHz	/	-11	-4	dB
	F=F_0 - 2MHz	/	-47	-40	dB
	F=F_0 + 3MHz	/	-48	-40	dB
	F=F_0 - 3MHz	/	-49	-40	dB
	F=F_{image} (F_0 + 2MHz)	/	-36	-20	dB
Out-of-band blocking performance	30MHz–2000MHz	-10	-5	/	dBm
Out-of-band blocking performance Intermodulation	2000MHz–2400MHz	-27	-22	/	dBm
	2500MHz–3000MHz	-27	-22	/	dBm
	3000MHz–12.5GHz	-10	-5	/	dBm
		-39	-31	/	dBm
Spurious output level		/	-135	/	dBm/Hz
Sensitivity with dirty transmit off@0.1% BER		/	-96	/	dBm

(a) VBAT = 3.8 V Temp = 27°C

Table 3-5 Transmitter Characteristics - Basic Data Rate [a]

Parameter	Condition	Min.	Typ.	Max.	Unit
General specifications					
Maximum RF transmit power(d)		12.5	14	16	dBm
RF power control range		2	4	8	dB
20dB band width		/	0.9	1	MHz
Adjacent channel transmit power	F=F_0 + 1MHz	/	-19	/	dBm
	F=F_0 - 1MHz	/	-17	/	dBm
	F=F_0 + 2MHz	/	-48	-40	dBm
	F=F_0 - 2MHz	/	-47	-40	dBm
	F=F_0 + 3MHz	/	-50	-40	dBm
	F=F_0 - 3MHz	/	-50	-40	dBm
	F=F_0 + >3MHz	/	-55	-40	dBm
	F=F_0 - >3MHz	/	-55	-40	dBm
	F=F_0 - >3MHz	/	-55	-40	dBm
△f1avg Maximum modulation		140	160	180	kHz
△f2max Minimum modulation		120	145	180	kHz
△f2avg/△f1avg		0.80	0.88	/	/
ICFT		-75	0	+75	kHz
Drift rate		/	/	/	kHz/50us
Drift (1 slot packet)		-25	0	25	kHz
Drift (5 slot packet)		-40	0	40	kHz
Harmonic Spur(b)	3GHz~20GHz	/	-50	-30	dBm

Parameter	Condition	Min.	Typ.	Max.	Unit
harmonic spur(c)	3GHz~20GHz	/	-30	-15	dBm

(a) VBAT = 3.8 V Temp = 27°C

(b) With external π type matching network

(c) *Without external matching network*

Table 3-6 Receiver Characteristics - Enhanced Data Rate (a)

Parameter	Condition	Min.	Typ.	Max.	Unit
π/4 DQPSK					
Sensitivity with dirty transmit off@0.01% BER		/	-94.5	/	dBm
Sensitivity with dirty transmit on@0.01% BER		-96	-93.5	-93	dBm
Maximum received signal@0.1% BER		/	/	0(b)	dBm
C/I co-channel		/	10	13	dB
Adjacent channel selectivity C/I	$F=F_0+1MHz$	/	-12	0	dB
	$F=F_0-1MHz$	/	-14	0	dB
	$F=F_0-2MHz$	/	-47	-35	dB
	$F=F_0+3MHz$	/	-48	-40	dB
	$F=F_0-3MHz$	/	-48	-40	dB
Adjacent channel selectivity C/I	$F=F_{image}$ (F_0+2MHz)	/	-36	-10	dB
8DPSK					
Sensitivity with dirty transmit off@0.01% BER		/	-88.5	-85	dBm
Sensitivity with dirty transmit off@0.01% BER		/	-87	-85	dBm
Maximum received signal@0.1% BER		0(b)	/	/	dBm
C/I c-channel		/	18	21	dB
Adjacent channel selectivity C/I	$F=F_0+1MHz$	/	-7	5	dB
	$F=F_0-1MHz$	/	-7	5	dB
	$F=F_0-2MHz$	/	-36	-25	dB
	$F=F_0+3MHz$	/	-41	-30	dB
	$F=F_0-3MHz$	/	-42	-30	dB
Adjacent channel selectivity C/I	$F=F_{image}$ (F_0+2MHz)	/	-30	-5	dB

(a) VBAT = 3.8 V Temp = 27°C

Table 3-7 Transmitter Characteristics - Enhanced Data Rate (a)

Parameter	Condition	Min.	Typ.	Max.	Unit
Maximum RF transmit power(b)		9.5	11	13	dBm
Relative transmit control		/	-2	/	dB
π/4 DQPSK max w_0		-10	0	10	kHz
π/4 DQPSK max w_i		-75	0	75	kHz
π/4 DQPSK max $\|w_i + w_0\|$		-75	0	75	kHz
8DPSK max w_0		-10	0	10	kHz
8DPSK max w_i		-75	0	75	kHz
8DPSK max $\|w_i + w_0\|$		-75	0	75	kHz
	RMS DEVM	/	6	20	%

π/4 DQPSK modulation accuracy	99% DEVM	/	10	30	%
	Peak DEVM	/	13	35	%
8DPSK modulation accuracy	RMS DEVM	/	6	13	%
	99% DEVM	/	10	20	%
	Peak DEVM	/	13	25	%
In-band spurious emissions	$F=F_0$ + 1MHz	/	-32	-20	dBm
	$F=F_0$ - 1MHz	/	-32	-20	dBm
	$F=F_0$ + 2MHz	/	-28	-20	dBm
	$F=F_0$ - 2MHz	/	-28	-20	dBm
	$F=F_0$ + 3MHz	/	-32	-30	dBm
	$F=F_0$ - 3MHz	/	-32	-30	dBm
	$F=F_0$ +/- > 3MHz	/	/	-40	dBm
EDR differential phase encoding		/	99	100	%

(a) VBAT = 3.8 V Temp = 27°C

Table 3-8 Bluetooth LE Receiver Specifications

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency Range		2402		2480	MHz
Sensitivity with dirty transmit off	PER < 30.8%	/	-100	/	dBm
Sensitivity with dirty transmit on	PER < 30.8%	/	-99	/	dBm
Max. Usable Signal	PER < 30.8%	-5	/	0[(a)]	dBm
C/I Co-channel	Co-channel selectivity (PER <30.8%)	/	13		dB
C/I 1MHz	Adjacent channel selectivity (PER <30.8%)		-6		dB
C/I 2MHz	2nd adjacent channel selectivity (PER< 30.8%)	/	-23		dB
C/I ≧3MHz	3rd adjacent channel selectivity (PER < 30.8%)	/	-35		dB
C/I Image channel	Image channel selectivity (PER <30.8%)	/	-22		dB
C/I Image 1MH	1MHz adjacent to image channel selectivity (PER < 30.8%)	/	-30		dB
Inter-modulation			-36	/	dBm
Out-of-band Blocking	30MHz to 2000MHz		-10	/	dBm
	2001MHz to 2339MHz		-25	/	dBm
	2501MHz to 3000MHz		-25	/	dBm

Table 3-9 Bluetooth LE Transmitter Specifications

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency Range		2402		2480	MHz
Output Power[(a)]	At max power output level	12.5	14	16	dBm
Carrier Frequency Offset and Drift	Frequency offset	/	+/-3	/	kHz
	Frequency drift	/	+/-3	/	kHz

	Max. drift rate	/	+/-3	/	Hz/us
Modulation Characteristic	△f1avg	/	250	/	kHz
	△f2max (For at least 99% of all △f2max)	/	210	/	kHz
	△f2avg/△f1avg	/	0.8	/	Hz/Hz
In-band Spurious Emission	±2M offset	/	-48	/	dBm
	>±3MHz offset	/	-50	/	dBm

3.3 Audio Codec Electrical Characteristics

Table 3-10 Digital to Analogue Converter under 1.95V [b]

Parameter	Conditions				Min.	Typ.	Max.	Unit
Resolution					/	/	32	Bits
Output Sample Rate, F_{sample}					8	/	384	kHz
SNR[a]	f_{in}=1kHz	Vrms Output	**F_{sample}**	**Load**				
	B/W=20Hz~20kHz	0.95	48kHz	32Ω	/	110	/	dB
	A-Weighted	0.88	48kHz	16Ω	/	110	/	dB
SNR with DRE on	f_{in}=1kHz	Vrms Output	**F_{sample}**	**Load**				
	B/W=20Hz~20kHz	0.95	48kHz	32Ω	/	116	/	dB
	A-Weighted	0.88	48kHz	16Ω	/	116	/	dB
THD+N		Vrms Output	**F_{sample}**	**Load**				
	f_{in}=1kHz	0.95	48kHz	100kΩ	/	-96		dB
	B/W=20Hz~20kHz	0.95	48kHz	32Ω	/	-96		dB
		0.88	48kHz	16Ω	/	-96		dB
Digital Gain	Digital Gain Resolution = 1dB					/		dB
Analogue Gain	Analogue Gain Resolution = 1.5dB					/		dB
Output Voltage	600-Ohm loading				/	/		mV rms
Freq. Response	0.02-20kHz 30mW output				/	0.086	/	dB
Phase	1kHz sine wave				/	0.002	/	Deg
Pop Up Noise					/	<0.1	/	mV
Noise Floor with DRE on					/	1.6	/	uV rms
Noise Floor	Audio PA on A-WT				/	2.9	/	uV rms
DNR	A-Weight, 32Ω				/	109	/	dB

(a) SNR is the ratio of output level with a 1-kHz full-scale input, to the output level playing an all-zero signal, measured A-weighted over a 20-Hz to 20-kHz bandwidth.

(b) The BES2700H-6X/8X provides a digital noise gate function for each of the output signal paths. The noise gate ensures best noise performance when the signal path is idle. When the noise gate is enabled, and the applicable signal level is below the noise gate threshold, then the noise gate is activated, causing the signal path to be muted.

Table 3-11 Codec - Analogue to Digital Converter under 1.8V

Parameter	Conditions	Min.	Typ.	Max.	Unit
Resolution		/	/	24	Bits
Output Sample Rate, F_{sample}		8	/	384	kHz

Parameter	Conditions		Min.	Typ.	Max.	Unit
SNR	f_{in}=1kHz B/W=20Hz~20kHz	F_{sample}				
	A-Weighted 1Vrms Input	48kHz	/	103	/	dB
THD+N	f_{in}=1kHzB/W=20Hz~20kHz	F_{sample}				
	1Vrms Input	48kHz	/	-90	/	dB
Digital Gain	Digital Gain Resolution = 1dB		-30	/	30	dB
Analogue Gain	Analogue Gain Resolution = 3dB		-9	/	12	dB

3.4 BUCK Electrical Characteristics

Table 3-12 DCDC Characteristics [a]

Parameter	Conditions	Min.	Typ.	Max.	Unit
Input voltage		3.1	4	5.5	V
Output voltage1 (v_{core})			0.9		V
Output voltgae2 (V_{ana})			1.3		V
Output voltgae3 (V_{codec})			1.8		V
Max output current core		200			mA
Max output current ana		200			mA
Max output current codec		180			mA
Burst status current				20	uA
ULP status current				3.5	uA
Line regulation				1	%
Load regulation (dc)	1mA-100mA		0.06		mV/mA
Load regulation (step)	1mA-100mA		0.1		mV/mA
Switch frequency (V_{core})	Internal_freq<1:0>=10		1.68		MHz
Burst mode ripple			20	40	mV
Efficiency (burst mode)	I=10mA		85[a]		%
Leakage current	Power down		5		uA

(a) Efficiency depends on inductor

4 Pin Map & Application Schematic

4.1 Pin Description

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R
16	GND	PGND	VSYS	VSYS	PGND	LX_VCORE	GND	VCORE0P6	VMEM	GND	GND	GPIO_22	GND	VUSB	GND
15	RESET	GND	GND	LX_HPPA	LX_VANA	GND	VIO		VCORE0P8		GPIO_12	GPIO_23			USB_DP
14	PWRON	VCHG_R	GND		GND	GND	NC		ADC_VREF	GPIO_11	GPIO_10	GPIO_24	GND	GND	USB_DN
13	GND	GND	GND	GND	GND	GND	GND	GND	GND	GPIO_13	GPIO_20	GPIO_25	GPIO_26	GPIO_27	GPIO_17
12	VMEM	VANA_LDO	GND	GND	GND		NC	GND			GPIO_21	GND	GND	GPIO_15	GPIO_14
11	ADC0	VPA_3P3_LDO	GND	GND	GND	NC		NC	NC	GND			GPIO_16		GPIO_36
10	ADC3	ADC2	GND	GND	GND		NC	NC	GND	GND	GPIO_35	GPIO_37	GND	GND	GPIO_32
9	MIC4_N	ADC1	GND		GND	GND	GND	GND	GND	GPIO_34	GPIO_33	GPIO_30	GPIO_07	GND	GPIO_06
8	MIC4_P	GND	GND	GND		GND	GND	GND	GND	GND	GPIO_31		GPIO_04	GPIO_03	GND
7	GND	NC	GND	GND	GND	GND	GND	GND	GND		GPIO_05	GPIO_01	GND	GND	VPA_1V8
6	VMEM	VCODEC	REFN_TX	GND	GND	GND	GND	GND	GND	GND	GPIO_02	GND	VANA2	VPA_3V3	GND
5	VMIC1	GND	GND	GND		GND	GND	GND	GND	GND	GPIO_00	GND	GND	GND	BT_RF
4	VCODEC_HPPA	HP_RP	VMIC2	GND	SAR_VREFP	CAP_CHAN3		CAP_CHAN2	GND	GND	GND	GND	GND	GND	GND
3	HP_LN	HP_RN	GND	VCM_CAP	AVSS_REFN_ADC	GND	GND	CAP_CHAN0	CAP_CHAN5	GND	GND	GND	GND	GND	GND
2	HP_LP	GND	GND	MIC1_P	MIC1_N	AVSS_REFN		CAP_CHAN4	VCORE0P8	VCORE0P6	VANA_XTAL	GND	GND	GND	GND
1	GND	MIC2_P	MIC2_N	MIC3_P	MIC3_N	MIC5_P	MIC5_N	CAP_CHAN1	VOUT1P5	GND	XTAL_IN	XTAL_OUT	GND	VANA1	GND

Figure 4-1 Pinout Diagram

Table 4-1 Pin Description

Pin	No.	Type	Description
Clock signals			
XTAL_OUT	M1	Analog	24 MHz crystal oscillator output
XTAL_IN	L1	Analog	24 MHz crystal oscillator input
PMU			
VMEM	A6	Analog	1.2~2.7 V internal memory LDO with decap
VMEM	A12	Analog	1.2~2.7 V internal memory LDO with decap
VMEM	J16	Analog	1.2~2.7 V internal memory LDO with decap
VIO	G15	Analog	1.2~3.3 V GPIO LDO with decap
VANA_LDO	B12	Analog	1.0~1.8 V analog LDO with decap
VANA1	P1	Analog	1.0~1.8 V analog LDO with decap
VANA2	N6	Analog	1.0~1.8 V analog LDO with decap
VPA_3P3_LDO	B11	Analog	LDO output of RF PA
VPA_3V3	P6	Analog	3.3 V power supply of RF PA
VPA_1V8	R7	Analog	1.8 V power supply of RF PA
ADC_VREF	J14	Analog	LDO for GPADC function
VCODEC	B6	Analog	1.2~2 V codec LDO with decap
VCODEC_HPPA	A4	Analog	Audio PA power supply
VANA_XTAL	L2	Analog	24 MHz crystal power supply

Pin	No.	Type	Description
SAR_VREFP	E4	Analog	SAR ADC reference voltage
VSYS	C16	Analog	The system supply pin. The 4.7 uF capacitor must be connected as close as this pin to protect the charger system.
VSYS	D16	Analog	The system supply pin. The 4.7 uF capacitor must be connected as close as this pin to protect the charger system.
VCORE0P8	J15	Analog	0.8 V digital core LDO with decap
VCORE0P8	J2	Analog	0.8 V digital core LDO with decap
VCORE0P6	H16	Analog	0.6 V digital core LDO with decap
VCORE0P6	K2	Analog	0.6 V digital core LDO with decap
LX_HPPA	D15	Analog	DCDC switch port
LX_VANA	E15	Analog	DCDC switch port
LX_VCORE	F16	Analog	DCDC switch port
VUSB	P16	Analog	2.1~3.3 V USB LDO with decap
VOUT1P5	J1	Analog	Internal reference voltage output
PMU interface			
VCHG_R	B14	Analog	Vbus voltage detector
ADC0	A11	Analog	GPADC
ADC1	B9	Analog	GPADC
ADC2	B10	Analog	GPADC
ADC3	A10	Analog	GPADC
CAP_CHAN0	H3	Analog	Cap sensor channel
CAP_CHAN1	H1	Analog	Cap sensor channel
CAP_CHAN2	H4	Analog	Cap sensor channel
CAP_CHAN3	F4	Analog	Cap sensor channel
CAP_CHAN4	H2	Analog	Cap sensor channel
CAP_CHAN5	J3	Analog	Cap sensor channel
Digital interface			
PWRON	A14	I	Chip power on input, high level/ high pules(min 10ms) is active
RESET	A15	I	Chip reset pin, reset if high
GPIO_00	L5	I/O	GPIO
GPIO_01	M7	I/O	GPIO
GPIO_02	L6	I/O	GPIO
GPIO_03	P8	I/O	GPIO
GPIO_04	N8	I/O	GPIO
GPIO_05	L7	I/O	GPIO
GPIO_06	R9	I/O	GPIO
GPIO_07	N9	I/O	GPIO
GPIO_10	L14	I/O	GPIO
GPIO_11	K14	I/O	GPIO
GPIO_12	L15	I/O	GPIO
GPIO_13	K13	I/O	GPIO
GPIO_14	R12	I/O	GPIO

Pin	No.	Type	Description
GPIO_15	P12	I/O	GPIO
GPIO_16	N11	I/O	GPIO
GPIO_17	R13	I/O	GPIO
GPIO_20	L13	I/O	GPIO
GPIO_21	L12	I/O	GPIO
GPIO_22	M16	I/O	GPIO
GPIO_23	M15	I/O	GPIO
GPIO_24	M14	I/O	GPIO
GPIO_25	M13	I/O	GPIO
GPIO_26	N13	I/O	GPIO
GPIO_27	P13	I/O	GPIO
GPIO_30	M9	I/O	GPIO
GPIO_31	L8	I/O	GPIO
GPIO_32	R10	I/O	GPIO
GPIO_33	L9	I/O	GPIO
GPIO_34	K9	I/O	GPIO
GPIO_35	L10	I/O	GPIO
GPIO_36	R11	I/O	GPIO
GPIO_37	M10	I/O	GPIO
USB Interface			
USB_DN	R14	Analog	USB data minus
USB_DP	R15	Analog	USB data plus
Audio interface			
MIC1_N	E2	Analog	MIC 1 N port
MIC1_P	D2	Analog	MIC 1 P port
MIC2_N	C1	Analog	MIC 2 N port
MIC2_P	B1	Analog	MIC 2 P port
MIC3_N	E1	Analog	MIC 3 N port
MIC3_P	D1	Analog	MIC 3 P port
MIC4_N	A9	Analog	MIC 4 N port
MIC4_P	A8	Analog	MIC 4 P port
MIC5_N	G1	Analog	MIC 5 N port
MIC5_P	F1	Analog	MIC 5 P port
HP_LP	A2	Analog	Audio DAC output positive, left
HP_LN	A3	Analog	Audio DAC output negative, left
HP_RP	B4	Analog	Audio DAC output positive, right
HP_RN	B3	Analog	Audio DAC output negative, right
VMIC1	A5	Analog	MIC BIAS1 decap
VMIC2	C4	Analog	MIC BIAS2 decap
VCM_CAP	D3	Analog	Decoupling of audio reference
RF interface			
BT_RF	R5	Analog	Bluetooth transmitter output /receiver input

Pin	No.	Type	Description
Ground			
PGND	B16	Analog	PMU GND
PGND	E16	Analog	PMU GND
AVSS_REFN_ADC	E3	Analog	ADC reference GND
AVSS_REFN	F2	Analog	Audio reference GND
REFN_TX	C6	Analog	Codec TX reference GND
GND	A16	Analog	Chip GND
GND	A13	Analog	Chip GND
GND	A7	Analog	Chip GND
GND	A1	Analog	Chip GND
GND	B15	Analog	Chip GND
GND	B13	Analog	Chip GND
GND	B8	Analog	Chip GND
GND	B7	Analog	Chip GND
GND	B5	Analog	Chip GND
GND	B2	Analog	Chip GND
GND	C2	Analog	Chip GND
GND	C3	Analog	Chip GND
GND	C5	Analog	Chip GND
GND	C7	Analog	Chip GND
GND	C8	Analog	Chip GND
GND	C9	Analog	Chip GND
GND	C10	Analog	Chip GND
GND	C11	Analog	Chip GND
GND	C12	Analog	Chip GND
GND	C13	Analog	Chip GND
GND	C14	Analog	Chip GND
GND	C15	Analog	Chip GND
GND	D4	Analog	Chip GND
GND	D5	Analog	Chip GND
GND	D6	Analog	Chip GND
GND	D7	Analog	Chip GND
GND	D8	Analog	Chip GND
GND	D10	Analog	Chip GND
GND	D11	Analog	Chip GND
GND	D12	Analog	Chip GND
GND	D13	Analog	Chip GND
GND	E6	Analog	Chip GND
GND	E7	Analog	Chip GND
GND	E9	Analog	Chip GND
GND	E10	Analog	Chip GND
GND	E11	Analog	Chip GND

Pin	No.	Type	Description
GND	E12	Analog	Chip GND
GND	E13	Analog	Chip GND
GND	E14	Analog	Chip GND
GND	F3	Analog	Chip GND
GND	F5	Analog	Chip GND
GND	F6	Analog	Chip GND
GND	F7	Analog	Chip GND
GND	F8	Analog	Chip GND
GND	F9	Analog	Chip GND
GND	F13	Analog	Chip GND
GND	F14	Analog	Chip GND
GND	F15	Analog	Chip GND
GND	G3	Analog	Chip GND
GND	G5	Analog	Chip GND
GND	G6	Analog	Chip GND
GND	G7	Analog	Chip GND
GND	G8	Analog	Chip GND
GND	G9	Analog	Chip GND
GND	G13	Analog	Chip GND
GND	G16	Analog	Chip GND
GND	H5	Analog	Chip GND
GND	H6	Analog	Chip GND
GND	H7	Analog	Chip GND
GND	H8	Analog	Chip GND
GND	H9	Analog	Chip GND
GND	H12	Analog	Chip GND
GND	H13	Analog	Chip GND
GND	J4	Analog	Chip GND
GND	J5	Analog	Chip GND
GND	J6	Analog	Chip GND
GND	J7	Analog	Chip GND
GND	J8	Analog	Chip GND
GND	J9	Analog	Chip GND
GND	J10	Analog	Chip GND
GND	J13	Analog	Chip GND
GND	K1	Analog	Chip GND
GND	K3	Analog	Chip GND
GND	K4	Analog	Chip GND
GND	K5	Analog	Chip GND
GND	K6	Analog	Chip GND
GND	K8	Analog	Chip GND
GND	K10	Analog	Chip GND

Pin	No.	Type	Description
GND	K11	Analog	Chip GND
GND	K16	Analog	Chip GND
GND	L3	Analog	Chip GND
GND	L4	Analog	Chip GND
GND	L16	Analog	Chip GND
GND	M2	Analog	Chip GND
GND	M3	Analog	Chip GND
GND	M4	Analog	Chip GND
GND	M5	Analog	Chip GND
GND	M6	Analog	Chip GND
GND	M12	Analog	Chip GND
GND	N1	Analog	Chip GND
GND	N2	Analog	Chip GND
GND	N3	Analog	Chip GND
GND	N4	Analog	Chip GND
GND	N5	Analog	Chip GND
GND	N7	Analog	Chip GND
GND	N10	Analog	Chip GND
GND	N12	Analog	Chip GND
GND	N14	Analog	Chip GND
GND	N16	Analog	Chip GND
GND	P2	Analog	Chip GND
GND	P3	Analog	Chip GND
GND	P4	Analog	Chip GND
GND	P5	Analog	Chip GND
GND	P7	Analog	Chip GND
GND	P9	Analog	Chip GND
GND	P10	Analog	Chip GND
GND	P14	Analog	Chip GND
GND	R1	Analog	Chip GND
GND	R2	Analog	Chip GND
GND	R3	Analog	Chip GND
GND	R4	Analog	Chip GND
GND	R6	Analog	Chip GND
GND	R8	Analog	Chip GND
GND	R16	Analog	Chip GND

4.2 GPIO Pin-Mux

GPIO	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
GPIO_P0_0	I2S0_SEN_SCK	I2S0_MCU_SCK#	I2C_MCU_M0_SCL#	CODEC_PDM_CLK0#	ANTENNA_SWITCH#	DISPLAY_REFRESH_TE#	

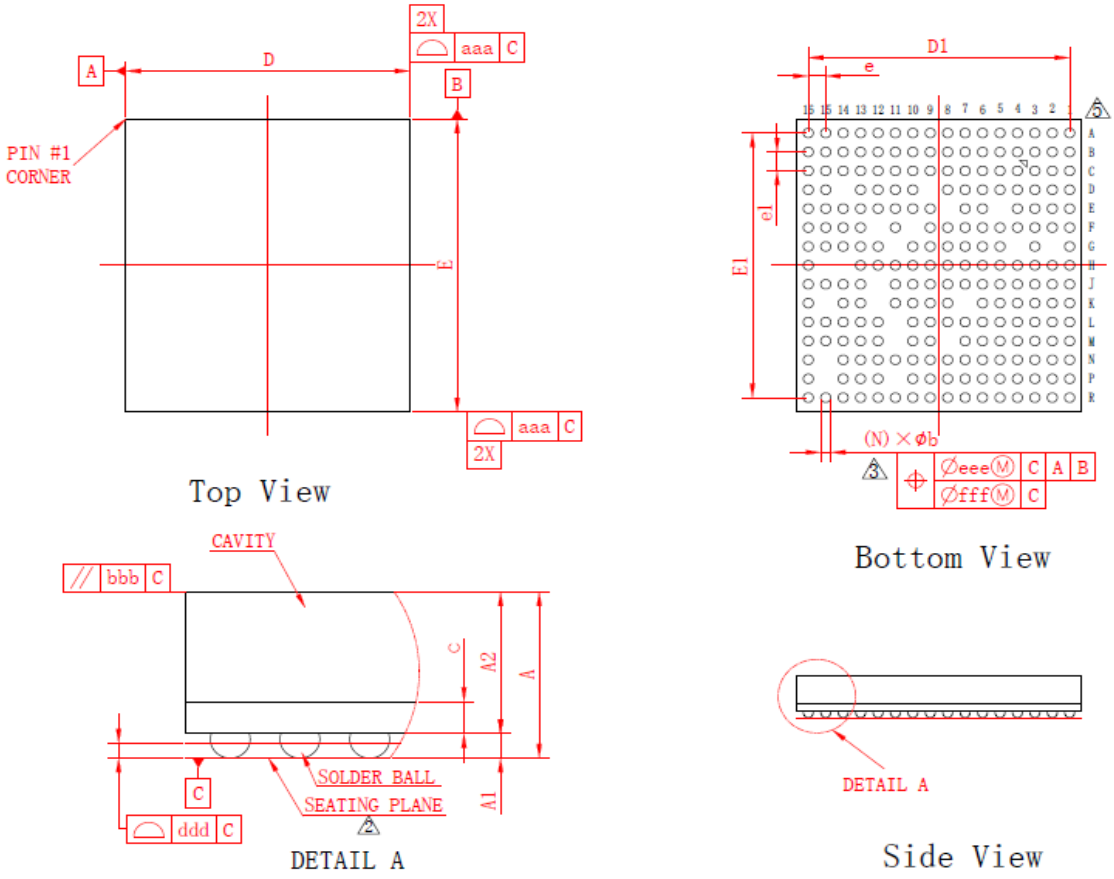
GPIO_P0_1	I2S0_SEN_WS	I2S0_MCU_WS#	I2C_MCU_M0_SDA#	CODEC_PDM_DATA0#	ANTENNA_SWITCH#	lcdpwm#	
GPIO_P0_2	I2S0_SEN_SDI0	I2S0_MCU_SDI0#	I2C_MCU_M1_SCL#	CODEC_PDM_DATA1#			
GPIO_P0_3	I2S0_SEN_SDO	I2S0_MCU_SDO#	I2C_MCU_M1_SDA#	CODEC_PDM_DATA2#			
GPIO_P0_4	I2C_SEN_M0_SCL	I2C_MCU_M0_SCL#	SPDIF_RX	I2S_MCLK#			
GPIO_P0_5	I2C_SEN_M0_SDA	I2C_MCU_M0_SDA#	SPDIF_TX	—			
GPIO_P0_6	I2C_SEN_M1_SCL	I2S1_MCU_SCK#	CLK_REQ_OUT		SWRX_BT#		
GPIO_P0_7	I2C_SEN_M1_SDA	I2S1_MCU_WS#	CLK_REQ_IN		SWTX_BT#		
GPIO_P1_0		I2C_MCU_M1_SCL#			ANTENNA_SWITCH#	SWRX_BT#	
GPIO_P1_1		I2C_MCU_M1_SDA#			ANTENNA_SWITCH#	SWTX_BT#	
GPIO_P1_2		I2S1_MCU_SDI#	I2S_MCLK#	QSPI_NAND_CLK#	CODEC_PDM_CLK0#	SDEMMC_CLK#	
GPIO_P1_3		I2S1_MCU_SDO#	CLKOUT#	QSPI_NAND_CS#	CODEC_PDM_DATA0#	SDEMMC_CMD#	
GPIO_P1_4	SPI0_SEN_CLK#	SPI0_MCU_CLK#		QSPI_NAND_D0#	CODEC_PDM_CLK1#	SDEMMC_DATA0#	SPI0_SLV_CLK#
GPIO_P1_5	SPI0_SEN_CS0#	SPI0_MCU_CS0#		QSPI_NAND_D1#	CODEC_PDM_DATA1#	SDEMMC_DATA1#	SPI0_SLV_CS0#
GPIO_P1_6	SPI0_SEN_DI_0#	SPI0_MCU_DI0#	SWRX_BT#	QSPI_NAND_D2#	CODEC_PDM_CLK2#	SDEMMC_DATA2#	SPI0_SLV_DIO#
GPIO_P1_7	SPI0_SEN_D_IO#	SPI0_MCU_DIO#	SWTX_BT#	QSPI_NAND_D3#	CODEC_PDM_DATA2#	SDEMMC_DATA3#	SPI0_SLV_DO#
GPIO_P2_0	I2C_SEN_M2_SCL#				ANTENNA_SWITCH#		smp_bt_pin0#
GPIO_P2_1	I2C_SEN_M2_SDA#				smp_bt_pin1#		
GPIO_P2_2			SWCK#		smp_bt_pin0	smp_bt_pin1#	
GPIO_P2_3			SWDIO#		smp_bt_vld	smp_bt_pin1#	
GPIO_P2_4	SPI1_SEN_CLK	SPI0_MCU_CLK#	PCM_CLK#	CODEC_PDM_CLK2#	SPI0_SLV_CLK#		
GPIO_P2_5	SPI1_SEN_CS0	SPI0_MCU_CS0#	PCM_FSYNC#	CODEC_PDM_DATA2#	SPI0_SLV_CS0#		
GPIO_P2_6	SPI1_SEN_DI_0	SPI0_MCU_DI0#	PCM_DIN#	CODEC_PDM_CLK1#	SPI0_SLV_DIO#		
GPIO_P2_7	SPI1_SEN_D_IO	SPI0_MCU_DIO#	PCM_DOUT#	CODEC_PDM_DATA1#	SPI0_SLV_DO#		

GPIO_P3_0	SPI0_SEN_CLK#	BT_ACTIVE#	CODEC_PDM_CLK2#	JTRST		PWM0#	
GPIO_P3_1	SPI0_SEN_CS0#	BT_PRIO#	CODEC_PDM_DATA2#	JTCK/SWCK#		PWM1#	
GPIO_P3_2	SPI0_SEN_DI_0#	BT_FREQ#		JTMS/SWDIO#	nbt_ble	PWM2#	
GPIO_P3_3	SPI0_SEN_D_IO#	WF_ACTIVE#	I2S_MCLK#	JTDI		PWM3#	
GPIO_P3_4	I2C_SEN_M2_SCL	I2C_MCU_M0_SDA#	—	JTDO		PWM4#	lcdpwm#
GPIO_P3_5	I2C_SEN_M2_SDA	I2C_MCU_M0_SCL#	—	—	—	PWM5#	DISPLAY_REFRESH_TE#
GPIO_P3_6	I2C_SEN_M3_SCL	SPI0_MCU_CS1#		CODEC_PDM_CLK1#	SWRX_BT#	PWM6#	SDEMMC_CLK#
GPIO_P3_7	I2C_SEN_M3_SDA	SPI0_MCU_DI1#	BT_WIFI_SW#	CODEC_PDM_DATA1#	SWTX_BT#	PWM7#	SDEMMC_CMD#
GPIO_P4_0	I2S0_MCU_SCK#		SDEMMC_DATA0#		WF_ACTIVE#		QSPI_NAND_CLK#
GPIO_P4_1	I2S0_MCU_WS#		SDEMMC_DATA1#		BT_ACTIVE#		QSPI_NAND_CS#
GPIO_P4_2	I2S0_MCU_SDI0#		SDEMMC_DATA2#		BT_PRIO#		QSPI_NAND_D0#
GPIO_P4_3	I2S0_MCU_SDO#		SDEMMC_DATA3#		BT_FREQ#		QSPI_NAND_D1#
GPIO_P4_4	I2C_MCU_M2_SCL#	I2S1_MCU_SCK#	SDEMMC_DATA4	PCM_CLK#	—		QSPI_NAND_D2#
GPIO_P4_5	I2C_MCU_M2_SDA#	I2S1_MCU_WS#	SDEMMC_DATA5	PCM_FSYNC#	—		QSPI_NAND_D3#
GPIO_P4_6	I2C_MCU_M3_SCL#	I2S1_MCU_SDI#	SDEMMC_DATA6	PCM_DIN#	—		
GPIO_P4_7	I2C_MCU_M3_SDA#	I2S1_MCU_SDO#	SDEMMC_DATA7	PCM_DOUT#	—		
GPIO_P5_0	—	QSPI_LCDC_CLK	WF_ACTIVE#				
GPIO_P5_1	—	QSPI_LCDC_CS	BT_ACTIVE#				
GPIO_P5_2	—	QSPI_LCDC_D0	BT_PRIO#				
GPIO_P5_3	—	QSPI_LCDC_D1	BT_FREQ#				
GPIO_P5_4	—	QSPI_LCDC_D2	BT_WIFI_SW#		—		
GPIO_P5_5	—	QSPI_LCDC_D3	—		—		
GPIO_P5_6		I2C_MCU_M2_SCL#	BT_WIFI_SW#	CODEC_PDM_CLK0#			
GPIO_P5_7		I2C_MCU_M2_SDA#	—	CODEC_PDM_DATA0#			
GPIO_P6_0		—	SDIO_CLK	PWM0#	SWRX_BT#		

GPIO_P6_1		—	SDIO_CMD	PWM1#	SWTX_BT#		
GPIO_P6_2			BT_WIFI_SW#	PWM2#	—	SPI0_MCU_CS1#	lcdpwm#
GPIO_P6_3			—	PWM3#		SPI0_MCU_DI1#	DISPLAY_REFRESH_TE#
GPIO_P6_4	I2S0_MCU_SCK#		BT_WIFI_SW#	PWM4#		SPI0_MCU_CLK#	
GPIO_P6_5	I2S0_MCU_WS#			PWM5#		SPI0_MCU_CS0#	
GPIO_P6_6	I2S0_MCU_SDI0#		CODEC_PDM_CLK0#	PWM6#	I2C_MCU_M3_SCL#	SPI0_MCU_DI0#	
GPIO_P6_7	I2S0_MCU_SDO#		CODEC_PDM_DATA0#	PWM7#	I2C_MCU_M3_SDA#	SPI0_MCU_DIO#	
GPIO_P7_0			SDIO_DATA0	PWM0#			
GPIO_P7_1			SDIO_DATA1	PWM1#			
GPIO_P7_2			SDIO_DATA2	PWM2#			
GPIO_P7_3	—		SDIO_DATA3	PWM3#			
GPIO_P7_4	—		SDIO_DATA4	PWM4#			
GPIO_P7_5	—		SDIO_DATA5	PWM5#			
GPIO_P7_6			SDIO_DATA6	PWM6#			
GPIO_P7_7			SDIO_DATA7	PWM7#			
GPIO_P8_0		—		PWM0#			lcdpwm#
GPIO_P8_1		—		PWM1#			DISPLAY_REFRESH_TE#
GPIO_P8_2		—		PWM2#			
GPIO_P8_3		—		PWM3#			
GPIO_P8_4		—		PWM4#			
GPIO_P8_5		—		PWM5#			
GPIO_P8_6		—		PWM6#			
GPIO_P8_7		—		PWM7#			
GPIO_P9_0				PWM0#			
GPIO_P9_1				PWM1#			
GPIO_P9_2				PWM2#			
GPIO_P9_3				PWM3#			
GPIO_P9_4				PWM4#			
GPIO_P9_5				PWM5#			
GPIO_P9_6				PWM6#			
GPIO_P9_7				PWM7#			

5 Package Dimensions

5.1 BGA Dimensions



symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.780	0.880	0.980	0.031	0.035	0.039
A1	0.080	0.130	0.180	0.003	0.005	0.007
A2	0.700	0.750	0.800	0.028	0.030	0.031
c	0.140	0.170	0.200	0.006	0.007	0.008
D	5.600	5.700	5.800	0.220	0.224	0.228
E	6.100	6.200	6.300	0.240	0.244	0.248
D1	---	5.250	---	---	0.207	---
E1	---	5.600	---	---	0.220	---
e	---	0.350	---	---	0.014	---
e1	---	0.400	---	---	0.016	---
b	0.150	0.200	0.250	0.006	0.008	0.010
aaa		0.100			0.004	
bbb		0.100			0.004	
ddd		0.080			0.003	
eee		0.150			0.006	
fff		0.050			0.002	
Ball Diam		0.200			0.008	
N		219			219	
MD/ME		16/15			16/15	

TECHNOLOGY SPECIFICATION[技术要求]

1. BALL PAD OPENING: 0.180mm; [球形防焊开口：0.180mm；]

△2 PRIMARY DATUM C AND SEATING PLANE ARE THE SOLDER BALLS;
[主要基准C和底面是锡球；]

△3 DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C; [尺寸b是测量最大锡球直径，平行于主要基准C；]

4. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd; [特殊特性C类：bbb, ddd；]

△5 THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY;
[PIN 1 标识仅供参考；]

6. BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;
[禁止使用一级环境管理物质；]

Figure 5-1 Package Dimensions

6 SMT Caution

6.1 Land Pad and Stencil Design

- Land Pad Guidelines:

  There are two types of PCB pads for BGA mounting: SMD (solder mask defined) or NSMD (non-solder-mask-defined). NSMD is recommended to fine-pitch BGA due to better overall land pattern registration accuracy and wider space for routing between adjacent pads. SMD pads are defined by the solder mask opening on the board pad. The opening of the solder mask is smaller than the underlying copper area for soldering to the associated bump. A NSMD pad has a solder mask opening larger than the copper pad. There are many factors influencing whether the PCB designer uses SMD or NSMD pads. Either type can successfully be used with BGA packages.

- Stencil Guidelines:

  Solder paste stencil design is critical for good solder joint formation, especially as the ball pitch decreases. The thickness of the stencil and the apertures determine the amount of solder paste deposited onto the PCB land pattern. Due to the fine pitch and small terminal geometry used on BGA, particular attention must be paid to the paste printing process. In process inspection for paste height, percent pad coverage, and registration accuracy to solderable land patterns is highly recommended.

6.2 Solder Reflow Profile

Temperature profile is the most important control in reflow soldering and it must be fine tuned to establish a robust process. The actual profile depends on several factors, including complexity or products, oven type, solder type, temperature difference across the PCB, oven and thermocouple tolerances, etc. Actual reflow temperature settings need to be determined by the end-user, based on thermal loading effects and on solder paste vendor recommendations.

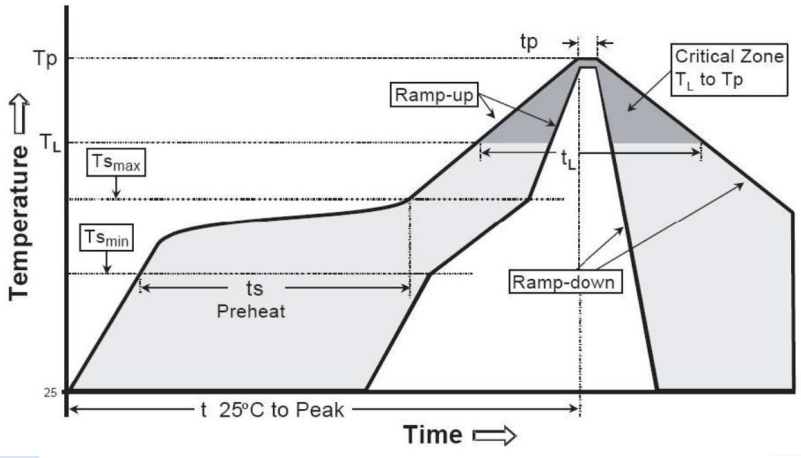


Figure 6-6-1 Solder Reflow Profile

Table 6-1 Package Peak Reflow Temperature - Sn/Pb

Package Thickness	Volume mm^3< 350	Volume mm^3≥ 350
< 2.5 mm	240 + 0°C / -5°C	225 + 0°C / -5°C
≥2.5 mm	225 + 0°C / -5°C	225 + 0°C / -5°C

Table 6-2 Package Peak Reflow Temperature - Pb-Free [a]

Package Thickness	Volume mm^3< 350	Volume mm^3 350 -2000	Volume mm^3> 2000
< 1.6 mm	260 + 0°C[a]	260 + 0°C	260 + 0°C
1.6mm to 2.5 mm	260 + 0°C	250 + 0°C	245 + 0°C
≥2.5 mm	250 + 0°C	245 + 0°C	245 + 0°C

(a) Tolerance: The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature(this means Peak reflow temperature +0 ℃.For example 260 ℃+ 0 ℃) at the rated MSL level.

Table 6-3 Solder Reflow Profile Feature

Profile Feature		Specification
Average Ramp-Up Rate (t_{smax} to t_p)		3°C/second max.
Pre_heat	Temperature Min (T_{smin})	150°C
	Temperature Max (T_{smax})	200°C
	Time (t_s)	60-120 seconds
Time Maintained above	Temperature (T_L)	217°C
	Time (t_L)	60-150 seconds
Peak/Classification Temperature (T_p)		260°C
Time within 5°C of Actual Peak Temperature (t_p)		20-40 seconds
Ramp-Down Rate		6°C/second max.
Time 25°C to Peak Temperature		8 minutes max.

6.3 RoHS Compliance

The products meet the requirements of Directive 2011/65/EU of Europe Parliament and of the Council on the Restriction of Hazardous Substance (RoHS). The products are free from halogenated or antimony trioxide-based flame retardants and other hazardous chemicals.

6.4 ESD Sensitivity

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result. ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site. BES products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, Protection of Electrical and Electronic Parts, Assemblies, and Equipment.
BES2700H-6X/8X ESD ratings will be available in Product Reliability Report of BES2700H-6X/8X.

6.5 Storage Alert

- The shelf life of BES2700H-6X/8X in a vacuum sealed bag with a temperature of less than 40°C and relative humidity (RH) of 90% is 24 months.
- The out-of-bag duration is the time for which a device can be on the factory floor before being installed onto a PCB. It depends on the MSL rating. For more information, see 8.4 Moisture Sensitivity Level.

7 Ordering Information

Part Number	Type	Package Size	Packing	MoQ(ea) [a]
BES2700H-6X/8X	BGA-219B	5.7x6.2x0.88 mm 0.35 mm pitch	Tape & Reel	3K

(a) MoQ: Minimum order quantity

7.1 Valid Part Numbers

Please contact the BES regional sales for the selection of the latest products.

Part Number	Flash
BES2700H-6X	4 MB
BES2700H-8X	8 MB

8 Tape and Reel Information

8.1 Tape Orientation

The following figure shows the general orientation of a BES2700H-6X/8X package in the carrier tape.

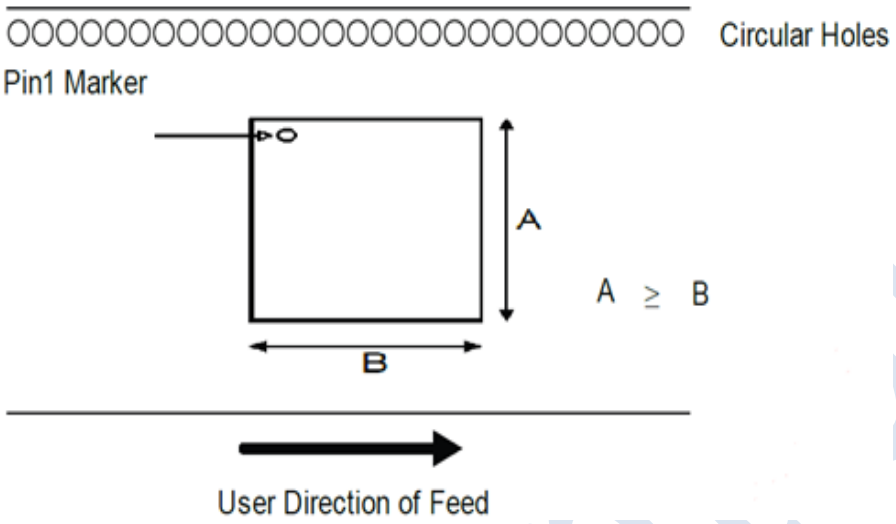


Figure 8-1 Tape Orientation

8.2 Reel Dimensions

The following figure shows the reel dimension of BES2700H-6X/8X.

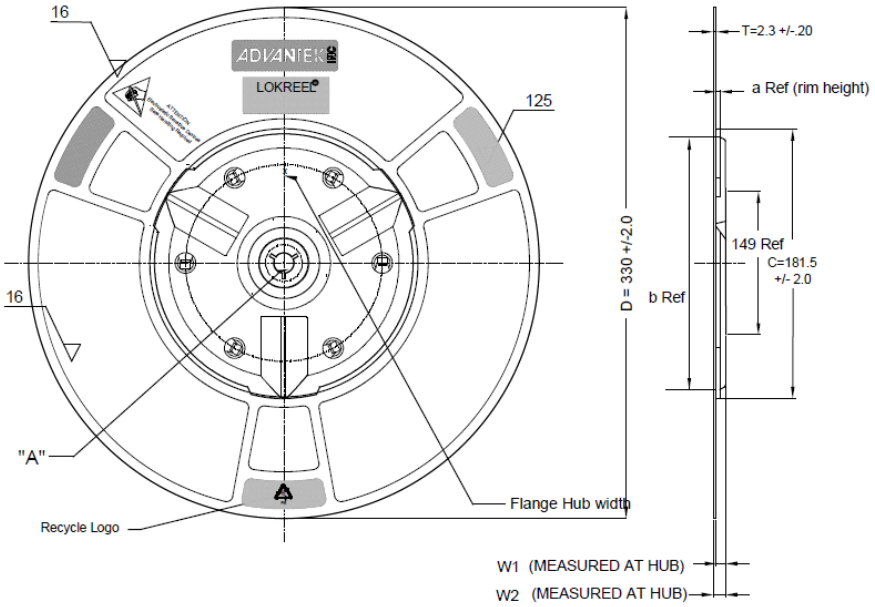


Figure 8-2 Reel Dimensions [(a)(b)]

(a) All dimensions in millimeters

(b) Reel color: Black, Each Plate products in 3000.

8.3 Tape Dimensions

The following figure shows the tape dimensions of BES2700H-6X/8X.

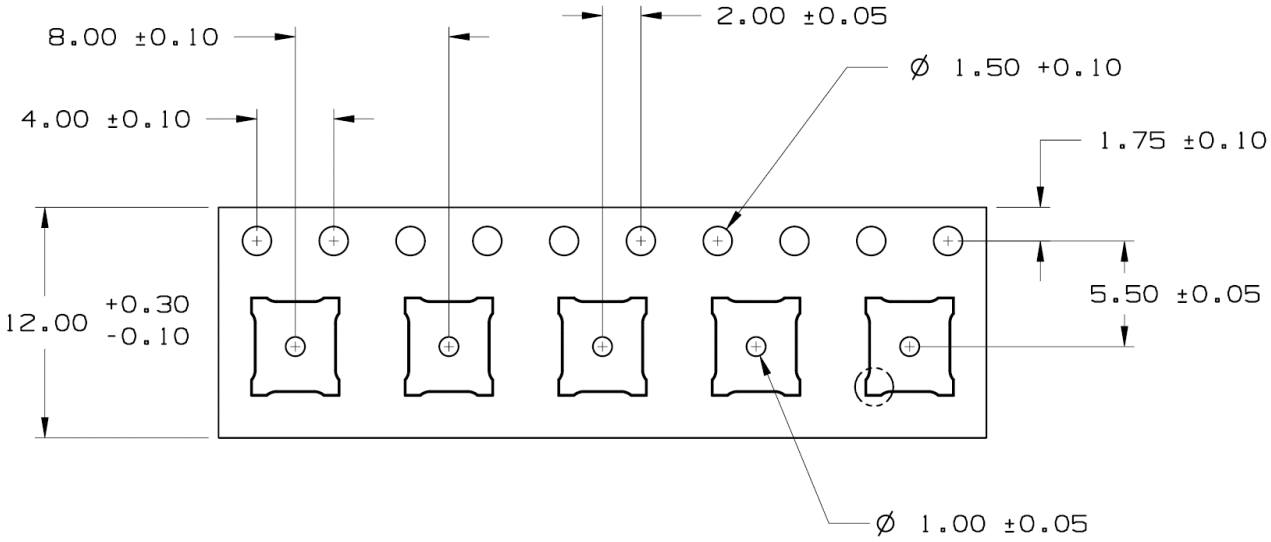


Figure 8-3 Tape Dimensions [a]

(a) All dimensions in millimeters

8.4 Moisture Sensitivity Level

BES2700H-6X/8X is qualified to the moisture sensitivity level MSL3 in accordance with JEDEC J-STD-020.