BT893X

Audio Player Microcontroller

Versions: 0.0.1

2023.12.28

Declaration

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Revision History

Date	Version	Comments	Revised by
2023-12-28	0.0.1	First draft	Leo

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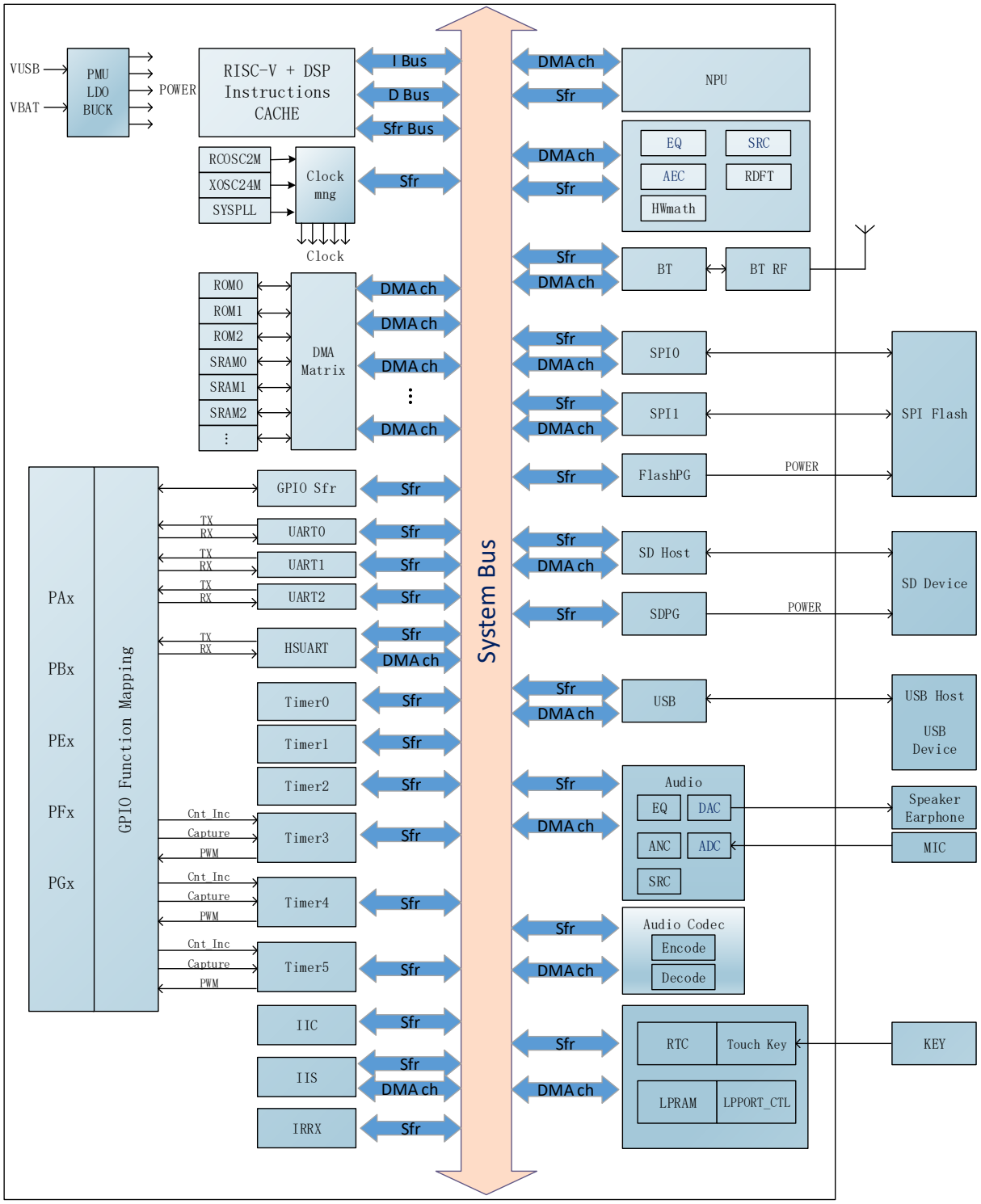
1 Product Overview

1.1 SoC Architecture



1.2 Product Features

CPU and Flexible IO

- High performance 32bit RISC-V processor Core with DSP instruction
- RISC-V typical speed: 140MHz
- Program memory: internal NOR flash
- Internal 320KB RAM for data and program
- Flexible GPIO pins with Programmable pull-up and pull-down resistors
- Support GPIO wakeup or interrupt

Bluetooth Radio

- Compliant with Bluetooth V5.4 + BR + EDR + BLE specification （QDID：207169）;
- Maximum TX output power +10.5dBm;
- RX Sensitivity with -94.5dBm @2M EDR;
- Support TWS communication with balance-efficiency Power consumption;
- Support TWS Master-slave switch;

Audio Interface

- High performance stereo DAC with 104dB SNR, support differential mode and VCMBUF mode;
- Five channels high performance ADC with 102dB SNR;
- Five channels MIC amplifier input;
- Support flexible audio EQ adjust;
- Support Sample rate 8, 11.025, 12, 16, 22.05, 32, 44.1, 48, 88.2,96, 176.4 and 192KHz;
- Two channels stereo Analog MUX;

Peripheral and Interfaces

- Support feedforward ANC, feedback ANC, hybrid ANC;
- Support Environmental Noise Cancellation (ENC);
- Support Neural Network Processing Unit (NPU);
- Support MPEG-1/2/3; AAC, SBC high quality decode;
- Support Low power Touch Key;
- Support Low power enter ear detect;
- 32-bit normal timer x 3; multi-function 32-bit timer x 3;
- WatchDog;
- Full-duplex normal UART x 3; high speed UART x 1；
- Master/Slave SPI x2;

- Master/Slave IIS x1;
- Master/Slave IIC x1;
- IR controller;
- SD Card Host controller x 1;
- Full speed USB 2.0 HOST/DEVICE controller x1;
- 10-bit SARADC x 16;
- Integrate IRTC;
- Build in PMU, such as charger/buck/LDO;

Temperature

- Operating temperature: -40℃ to +85℃;
- Storage temperature: -65℃ to +150℃.

2 Interrupts

Support vectorized interrupts, exceptions on illegal instructions and exceptions on load and store instructions to invalid addresses.

Exception vectors

Interrupt number	Address	Description
0	0x00	Reset
1	0x04	
2	0x08	Hardware breakpoint
3	0x0c	
4	0x10	Low priority interrupt
5	0x14	Watch point interrupt
6	0x18	Reserve
7	0x1c	Reserve
8	0x20~0x9c	High priority interrupt(see the following table)

High priority interrupt vectors

Interrupt number	Address	Description
0	0x20	Icache miss interrupt Dcache Miss interrupt
1	0x24	BT interrupt BLE interrupt BTDM interrupt
2	0x28	Software interrupt
3	0x2c	Timer0 interrupt
4	0x30	Timer1 interrupt
5	0x34	Timer2 interrupt
6	0x38	IR receiver interrupt
7	0x3c	USB control interrupt
8	0x40	Sd interrupt
9	0x44	
10	0x48	
11	0x4c	
12	0x50	
13	0x54	
14	0x58	UART0 interrupt UART1 interrupt UART2 interrupt
15	0x5c	HSUART interrupt

Interrupt number	Address	Description
		DVP interrupt
16	0x60	Timer3 interrupt
17	0x64	Timer4 interrupt
18	0x68	Timer5 interrupt
19	0x6c	
20	0x70	SPI1 interrupt
21	0x74	
22	0x78	
23	0x7c	Frequency detect interrupt Touch key interrupt
24	0x80	
25	0x84	
26	0x88	Port interrupt
27	0x8c	IIS interrupt
28	0x90	SARADC interrupt
29	0x94	RTC second or alarm interrupt LVD interrupt WDT interrupt
30	0x98	IIC interrupt BSP interrupt
31	0x9c	Tick0 interrupt Tick1 interrupt

2.1 Interrupts Special Registers

Register 2-1 PICCON: Peripheral interrupt control Register

Bit	Name	Mode	Default	Description
31:20	-	-	-	Unused
19	DBPCEN	WR	0	Debug pc store enable 0: disable 1: enable
18	AUTOGT	WR	0	Auto clock gating enable 0: disable 1: enable

Bit	Name	Mode	Default	Description
17	MULDIV2	WR	0	Multiple two clock enable bit 0: 1 clock finish 1: 2 clock finish
16	GIEM	WR	1	Global interrupt enable mask bit 0: disable interrupt 1: enable interrupt
15	BP7EN	WR	0	Breakpoint 7 interrupt enable bit 0: disable 1: enable
14	BP6EN	WR	0	Breakpoint 6 interrupt enable bit 0: disable 1: enable
13	BP5EN	WR	0	Breakpoint 5 interrupt enable bit 0: disable 1: enable
12	BP4EN	WR	0	Breakpoint 4 interrupt enable bit 0: disable 1: enable
11	BP3EN	WR	0	Breakpoint 3 interrupt enable bit 0: disable 1: enable
10	BP2EN	WR	0	Breakpoint 2 interrupt enable bit 0: disable 1: enable
9	BP1EN	WR	0	Breakpoint 1 interrupt enable bit 0: disable 1: enable
8	BP0EN	WR	0	Breakpoint 0 interrupt enable bit 0: disable

Bit	Name	Mode	Default	Description
				1: enable
7	-	-	-	Unused
6:5	HPSDEN	WR	0x0	High priority shadow register select bit 00: high priority 01: high priority 2 10/11: high priority 3
4	HP3INTEN	WR	0	High priority 3 interrupt enable bit 0: disable 1: enable
3	HP2INTEN	WR	0	High priority 2 interrupt enable bit 0: disable 1: enable
2	HPINTEN	WR	0	High priority interrupt enable bit 0: disable 1: enable
1	LPINTEN	WR	0	Low priority interrupt enable bit 0: disable 1: enable
0	GIE	WR	0	Global interrupt enable bit 0: disable interrupt 0: disable interrupt

Register 2-2 PICCONSET: Peripheral interrupt control set Register

Bit	Name	Mode	Default	Description
31:20	-	-	-	Unused
19	DBPCEN	W	0	Write 1 enable DBPCEN
18	AUTOGT	W	0	Write 1 enable AUTOGT
17	MULDIV2	W	0	Write 1 enable Multiple two clock
16	GIEM	W	0	Write 1 enable Global interrupt enable mask

Bit	Name	Mode	Default	Description
15	BP7EN	W	0	Write 1 enable breakpoint 7 interrupt
14	BP6EN	W	0	Write 1 enable breakpoint 6 interrupt
13	BP5EN	W	0	Write 1 enable breakpoint 5 interrupt
12	BP4EN	W	0	Write 1 enable breakpoint 4 interrupt
11	BP3EN	W	0	Write 1 enable breakpoint 3 interrupt
10	BP2EN	W	0	Write 1 enable breakpoint 2 interrupt
9	BP1EN	W	0	Write 1 enable breakpoint 1 interrupt
8	BP0EN	W	0	Write 1 enable breakpoint 0 interrupt
7	-	-	-	Unused
6	HPSDEN1	W	0	Write 1 enable shadow register select 1
5	HPSDEN0	W	0	Write 1 enable shadow register select 0
4	HP3INTEN	W	0	Write 1 enable High priority 3 interrupt
3	HP2INTEN	W	0	Write 1 enable High priority 2 interrupt
2	HPINTEN	W	0	Write 1 enable High priority interrupt
1	LPINTEN	W	0	Write 1 enable Low priority interrupt
0	GIE	W	0	Write 1 enable Global interrupt

Register 2-3 PICCONCLR: Peripheral interrupt control clear Register

Bit	Name	Mode	Default	Description
31:20	-	-	-	Unused
19	DBPCENDIS	W	0	Write 1 disable DBPCEN
18	AUTOGTDIS	W	0	Write 1 disable AUTOGT
17	MULDIV2DIS	W	0	Write 1 disable Multiple two clock
16	GIEMDIS	W	0	Write 1 disable Global interrupt enable mask

Bit	Name	Mode	Default	Description
15	BP7DIS	W	0	Write 1 disable breakpoint 7 interrupt
14	BP6DIS	W	0	Write 1 disable breakpoint 6 interrupt
13	BP5DIS	W	0	Write 1 disable breakpoint 5 interrupt
12	BP4DIS	W	0	Write 1 disable breakpoint 4 interrupt
11	BP3DIS	W	0	Write 1 disable breakpoint 3 interrupt
10	BP2DIS	W	0	Write 1 disable breakpoint 2 interrupt
9	BP1DIS	W	0	Write 1 disable breakpoint 1 interrupt
8	BP0DIS	W	0	Write 1 disable breakpoint 0 interrupt
7	-	-	-	Unused
6	HPSDDIS1	W	0	Write 1 disable shadow register select 1
5	HPSDDIS0	W	0	Write 1 disable shadow register select 0
4	HP3INTDIS	W	0	Write 1 disable High priority 3 interrupt
3	HP2INTDIS	W	0	Write 1 disable High priority 2 interrupt
2	HPINTDIS	W	0	Write 1 disable High priority interrupt
1	LPINTDIS	W	0	Write 1 disable Low priority interrupt
0	GIEDIS	W	0	Write 1 disable Global interrupt

Register 2-4 PICEN: Peripheral interrupt enable Register

Bit	Name	Mode	Default	Description
31:0	IntEN	WR	0x0	Interrupt 31 to 0 enable bit 0: disable 1: enable

Register 2-5 PICENSET: Peripheral interrupt enable set Register

Bit	Name	Mode	Default	Description
31:0	IntEN	W	0x0	Write 1 enable Interrupt 31 to 0

Register 2-6 PICENCLR: Peripheral interrupt enable clear Register

Bit	Name	Mode	Default	Description

Bit	Name	Mode	Default	Description
31:0	IntDIS	W	0x0	Write 1 disable Interrupt 31 to 0

Register 2-7 PICPR: Peripheral high priority interrupt selection Register

Bit	Name	Mode	Default	Description
31:0	IntPR	WR	0x0	Interrupt 31 to 0 priority selection bit 0: low priority interrupt 1: high priority interrupt

Register 2-8 PICPR1: Peripheral high priority interrupt selection Register1

Bit	Name	Mode	Default	Description
31:0	IntPR1	WR	0x0	Interrupt 31 to 0 priority selection 1 bit; {PICPR1, PICPR} 00: low priority interrupt 01: high priority interrupt 10: high priority 2 interrupt 11: high priority 3 interrupt

Register 2-9 PICADR: Peripheral interrupt address Register

Bit	Name	Mode	Default	Description
31:8	BADR	WR	0x800	Interrupt entry address
7:0	-	-	0x0	-

Register 2-10 PICPND: Peripheral interrupt pending Register

Bit	Name	Mode	Default	Description
31:3	IntPND[31:3]	R	0x0	Interrupt 31 to 3 pending bit 0: no interrupt pending 1: interrupt pending
2	SWIPND	WR	0	Software interrupt pending. Write 1 will clear software interrupt pending
1:0	IntPND[1:0]	R	0x0	Interrupt 1 to 0 pending bit 0: no interrupt pending 1: interrupt pending

3 GPIO Management

3.1 Features

1. Control GPIO input/output direction by using direction register;
2. Internal pull-up/pull-down resistor by using pull-up/pull-down resistor control register;
3. Select suitable output driving current capability;

3.2 GPIO general control register

Register 3-1 GPIOA: Port A data Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOA	WR	0x00	PAx data. Valid when PAx is used as GPIO 0: PAx is input low state when read and output low at PAx when write; 1:PAx is input high state when read and output high at PAx when write

Register 3-2 GPIOASET: Port A Set output data Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOASET	WO	X	Set PAx output data. Write 1 set output data. Write 0 affect nothing.

Register 3-3 GPIOACLR: Port A clear output data Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOACLR	WO	X	Clear PAx output data. Write 1 clear output data. Write 0 affect nothing.

Register 3-4 GPIOADIR: Port A direction Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOADIR	WR	0xFF	PAx direction control 0: Output 1: Input

Register 3-5 GPIOAPU: Port A pull-up register Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOAPU	WR	0x0	PAx 10KΩ pull-up resister control. Valid when PAx is used as input 0: disable 1: enable

Register 3-6 GPIOAPD: Port A pull-down resister Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOAPD	WR	0x0	PAx 10KΩ pull-down resister control. Valid when PAx is used as input 0: disable 1: enable

Register 3-7 GPIOAPU200K: Port A pull-up resister Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOAPU	WR	0x0	PAx 200KΩ pull-up resister control. Valid when PAx is used as input 0: disable 1: enable

Register 3-8 GPIOAPD200K: Port A pull-down resister Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOAPD	WR	0x0	PAx 200KΩ pull-down resister control. Valid when PAx is used as input 0: disable 1: enable

Register 3-9 GPIOAPU300: Port A pull-up resister Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOAPU	WR	0x0	PAx 300Ω pull-up resister control. Valid when PAx is used as input 0: disable 1: enable

Register 3-10 GPIOAPD300: Port A pull-down resister Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOAPD	WR	0x0	PAx 300Ω pull-down resister control. Valid when PAx is used as input 0: disable 1: enable

Register 3-11 GPIOADE: Port A digital function enable register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOADE	WR	0xFF	PAx digital function enable 0: Port used as analog IO 1: Port used as digital IO

Register 3-12 GPIOAFEN: Port A function mapping enable register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOAFEN	WR	0xFF	PAx function mapping enable 0: Port used as GPIO 1: Port used as function IO

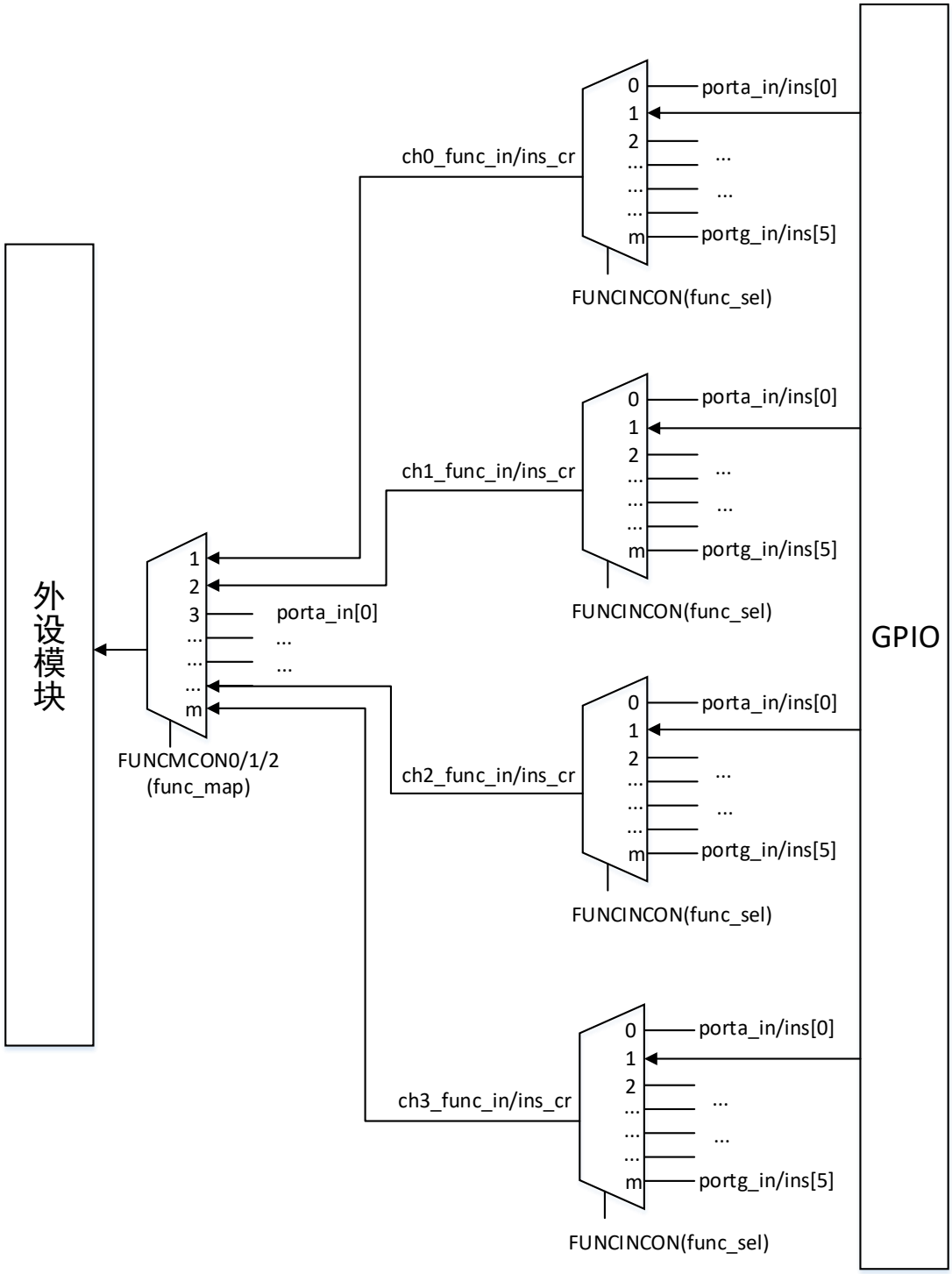
Register 3-13 GPIOADRV: Port A output driving select Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOADRV	WR	0x0	PAx output driving select 0: 8mA 1: 32mA

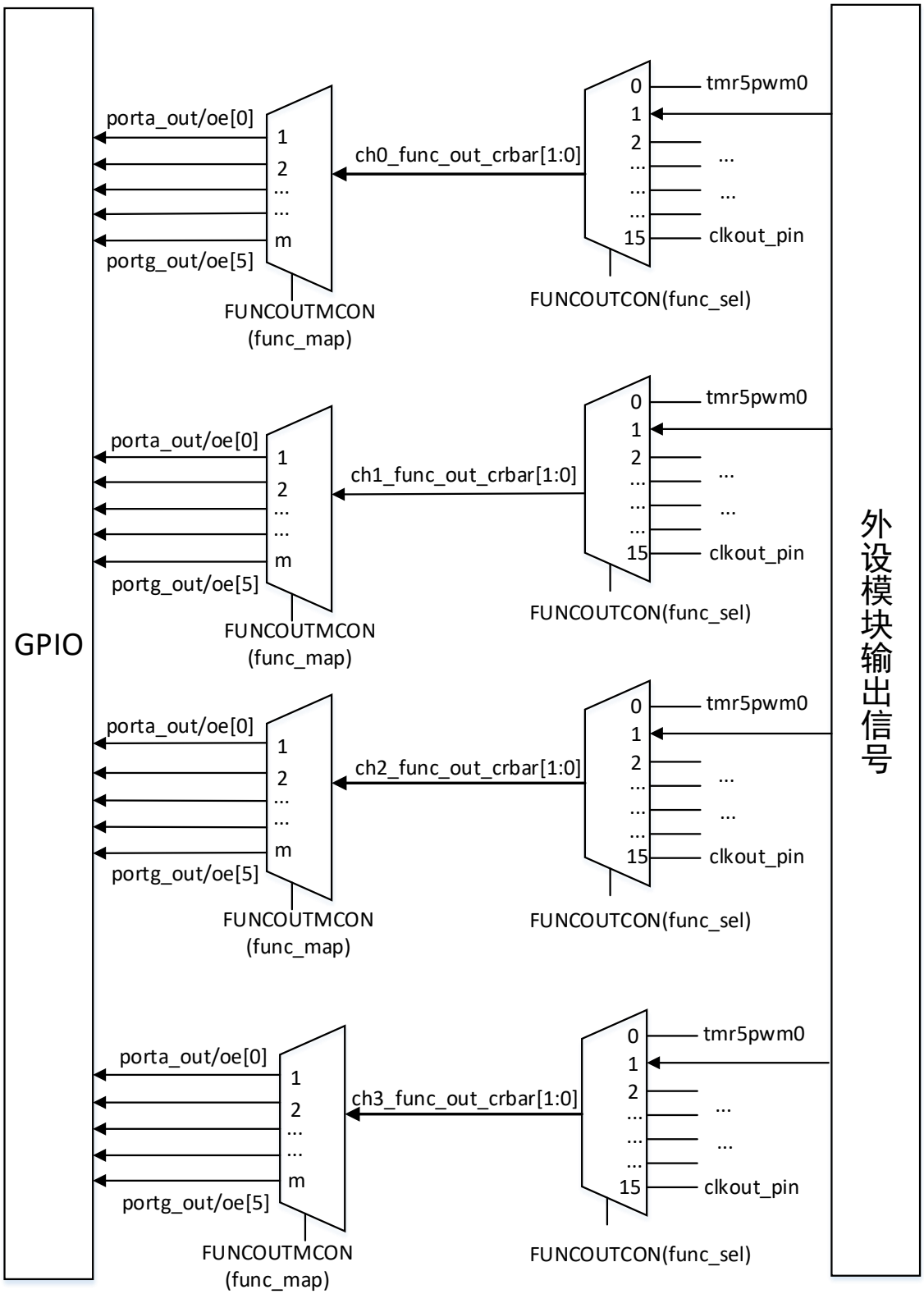
3.3 GPIO function mapping

3.3.1 crossbar function

1. Four channels function input mux



2. Four channels function output mux



Function input select table

FUNCINCON	
0	PA4 input
1	PA5 input
2	PA6 input
3	PA7 input
4	PB0 input
5	PB1 input
6	PB2 input
7	PB3 input
8	PB4 input
9	PB5 input
10	PE0 input
11	PE4 input
12	PE5 input
13	PE6 input
14	PE7 input
15	PF0 input
16	PF1 input
17	PG0 input
18	PG1 input
19	PG2 input
20	PG3 input
21	PG4 input
22	PG5 input

Function output select table

FUNCOUTCON	
0	TMR5PWM0
1	TMR5PWM1
2	TMR5PWM2
3	TMR5PWM3
4	UART0_TX
5	HSUT0_TX
6	URAT1_TX
7	IIC_SCL
8	IIC_SDA
9	CLKOUT

10	SPI1_DO
11	SPI1_D1
12	SPI1_CLK
13	URAT2_TX
14	Reserve
15	Reserve

Channel output mapping table

FUNCOUTMCON	
1	Map to PA4
2	Map to PA5
3	Map to PA6
4	Map to PA7
5	Map to PB0
6	Map to PB1
7	Map to PB2
8	Map to PB3
9	Map to PB4
10	Map to PB5
11	Map to PE0
12	Map to PE4
13	Map to PE5
14	Map to PE6
15	Map to PE7
16	Map to PF0
17	Map to PF1
18	Reserve
19	Reserve
20	Reserve
21	Reserve
22	Reserve
23	Reserve
24	Reserve
25	Reserve
26	Reserve
27	Reserve
28	Reserve
29	Reserve
30	Reserve
31	Reserve

Register 3-14 FUNCINCON: Port function input control Register

Bit	Name	Mode	Default	Description
31:30	-	-	-	Reserved
29:24	CH3INSEL	WR	0x0	Channel 3 function input select. Please lookup “Function input select table” Write 0x00 invalid, Write 0xff clear
23:22	-	-	-	Reserved
21:16	CH2INSEL	WR	0x0	Channel 2 function input select. Please lookup “Function input select table” Write 0x00 invalid, Write 0xff clear
15:14	-	-	-	Reserved
13:8	CH1INSEL	WR	0x0	Channel 1 function input select. Please lookup “Function input select table” Write 0x00 invalid, Write 0xff clear
7:6	-	-	-	reserved
5:0	CH0INSEL	WR	0x0	Channel 0 function input select. Please lookup “Function input select table” Write 0x00 invalid, Write 0xff clear

Register 3-15 FUNCOUTCON: Port function output control Register

Bit	Name	Mode	Default	Description
31:28	-	-	-	Reserved
27:24	CH3OUTSEL	WR	0x0	Channel 3 function output select. Please lookup “Function output select table” Write 0x00 invalid, Write 0xff clear
23:20	-	-	-	Reserved
19:16	CH2OUTSEL	WR	0x0	Channel 2 function output select. Please lookup “Function output select table” Write 0x00 invalid, Write 0xff clear
15:12	-	-	-	Reserved
11:8	CH1OUTSEL	WR	0x0	Channel 1 function output select. Please lookup “Function output select table” Write 0x00 invalid, Write 0xff clear
7:4	-	-	-	reserved
3:0	CH0OUTSEL	WR	0x0	Channel 0 function output select. Please lookup “Function output select table” Write 0x00 invalid, Write 0xff clear

Register 3-16 FUNCOUTMCON: Port function output control Register

Bit	Name	Mode	Default	Description
31:29	-	-	-	Reserved
28:24	CH3OUTMAP	WR	0x0	Channel 3 output mapping to which PAD. Please lookup “Channel output mapping table” Write 0x00 invalid, Write 0xff clear
23:21	-	-	-	Reserved
20:16	CH2OUTMAP	WR	0x0	Channel 2 output mapping to which PAD. Please lookup “Channel output mapping table” Write 0x00 invalid, Write 0xff clear
15:13	-	-	-	Reserved
12:8	CH1OUTMAP	WR	0x0	Channel 1 output mapping to which PAD. Please lookup “Channel output mapping table” Write 0x00 invalid, Write 0xff clear
7:5	-	-	-	reserved
4:0	CH0OUTMAP	WR	0x0	Channel 0 output mapping to which PAD. Please lookup “Channel output mapping table” Write 0x00 invalid, Write 0xff clear

Register 3-17 FUNCMCON0: Port function mapping control Register 0

Bit	Name	Mode	Default	Description
31:28	UT1RXMAP	WR	0x0	UART1 RX mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 0100: map to G4 0101: map to G5 0110: map to TX pin by UT1TXMAP select 1111: Clear these bits Others is reserved
27:24	UT1TXMAP	WR	0x0	UART1 TX mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 1111: Clear these bits Others is reserved
23:20	HSUTRXMAP	WR	0x0	High speed UART RX mapping 0000: no affect 0001: map to G1

Bit	Name	Mode	Default	Description
				0010: map to G2 0011: map to G3 0100: map to G4 0101: map to G5 0110: map to G6 0111: map to G7 1000: map to G8 1001: map to G9 1010: map to G10 1011: map to G11 1100: map to G12 1101: map to G13 1111: Clear these bits Others is reserved
19:16	HSUTTXMAP	WR	0x0	High speed UART TX mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 0100: map to G4 0101: map to G5 0110: map to G6 0111: map to G7 1000: map to G8 1001: map to G9 1010: map to G10 1111: Clear these bits Others is reserved
15:12	UT0RXMAP	WR	0x0	UART0 RX mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 0100: map to G4 0101: map to G5 0110: map to G6 0111: map to G7 1000: map to G8 0111: map to TX pin by UT0TXMAP select 1111: Clear these bits Others is reserved
11:8	UT0TXMAP	WR	0x0	UART0 TX mapping

Bit	Name	Mode	Default	Description
				0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 0100: map to G4 0101: map to G5 0110: map to G6 1111: Clear these bits Others is reserved
7:4	SPI0MAP	WR	0x0	SPI0 mapping 0000: no affect 0001: map to G1 0010: map to G2 1111: Clear these bits Others is reserved
3:0	SD0MAP	WR	0x0	SD0 mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 0100: map to G4 0101: map to G5 0110: map to G6 1111: Clear these bits Others is reserved

Register 3-18 FUNCMCON1: Port function mapping control Register 1

Bit	Name	Mode	Default	Description
31:28	T5PWM5MAP	WR	0x0	TMR5 PWM5 mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 1111: Clear these bits Others is reserved
27:24	T5PWM4MAP	WR	0x0	TMR5 PWM4 mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 1111: Clear these bits

Bit	Name	Mode	Default	Description
				Others is reserved
23:20	T5PWM3MAP	WR	0x0	TMR5 PWM3 mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 1111: Clear these bits Others is reserved
19:16	T5PWM2MAP	WR	0x0	TMR5 PWM2 mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 1111: Clear these bits Others is reserved
15:12	T5PWM1MAP	WR	0x0	TMR5 PWM1 mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 1111: Clear these bits Others is reserved
11:8	T5PWM0MAP	WR	0x0	TMR5 PWM0 mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 1111: Clear these bits Others is reserved
7:4	SPI1MAP	WR	0x0	SPI1 mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 0100: map to G4 0101: map to G5 1111: Clear these bits Others is reserved
3:0	CLKOUTMAP	WR	0x0	Clock output mapping 0000: no affect 0001: map to G1

Bit	Name	Mode	Default	Description
				0010: map to G2 0011: map to G3 0100: map to G4 0101: map to G5 0110: map to G6 0111: map to G7 1111: Clear these bits Others is reserved

Register 3-19 FUNCMCON2: Port function mapping control Register 2

Bit	Name	Mode	Default	Description
31:28	-	-	-	Unused
27:24	IICMAP	WR	0x0	IIC mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 0100: map to G4 0101: map to G5 0110: map to G6 0111: map to G7 1000: map to G8 1001: map to G9 1111: Clear these bits Others is reserved
23:20	IRMAP	WR	0x0	IR mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 0100: map to G4 0101: map to G5 0110: map to G6 0111: map to G7 1000: map to G8 1001: map to G9 1010: map to G10 1011: map to G11 1111: Clear these bits Others is reserved
19:16	TMR5MAP	WR	0x0	Timer5 PWM mapping

Bit	Name	Mode	Default	Description
				0000: no affect 0001: map to G1 1111: Clear these bits Others is reserved
15:12	UT2RXMAP	WR	0x0	UART2 RX mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 0100: map to TX pin by UT2TXMAP select 1111: Clear these bits Others is reserved
11:8	-	-	-	Unused
7:4	TMR3CPTMAP	WR	0x0	Timer3 capture Pin mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 0100: map to G4 0101: map to G5 0110: map to G6 0111: map to G7 1000: map to G8 1001: map to G9 1111: Clear these bits Others is reserved
3:0	IISMAP	WR	0x0	IIS mapping 0000: no affect 0001: map to G1 0010: map to G2 1111: Clear these bits Others is reserved

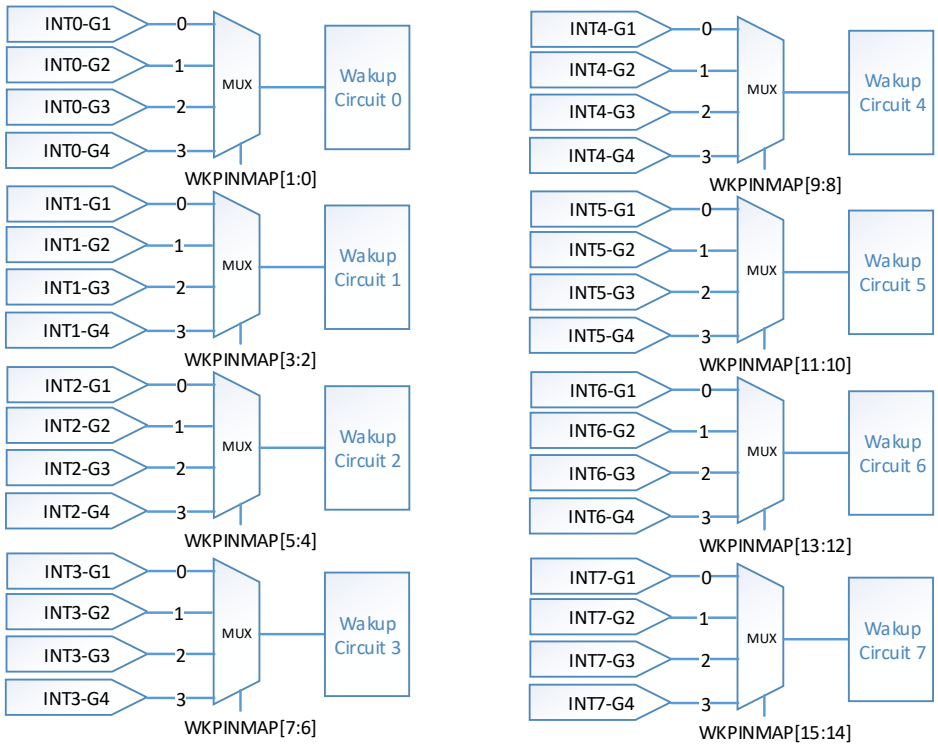
3.4 External Port interrupt wake up

Support eight wakeup source input, as the following table. Wakeup circuit 6 and wakeup circuit 7 is special for 32 port interrupts wake up.

Port interrupt source is:

Port_intsrc = {8'b0, VUSB_PIN, PG[5:0], PF[1:0], PE[7:4], PE[0],PB[5:0], PA[7:4]};

Port_intsrc			
0	PA4	16	PF1
1	PA5	17	PG0
2	PA6	18	PG1
3	PA7	19	PG2
4	PB0	20	PG3
5	PB1	21	PG4
6	PB2	22	PG5
7	PB3	23	VUSB_PIN
8	PB4	24	
9	PB5	25	
10	PE0	26	
11	PE4	27	
12	PE5	28	
13	PE6	29	
14	PE7	30	
15	PF0	31	



Register 3-20 WKPINMAP: Wake up pin mapping Register

Bit	Name	Mode	Default	Description
31:16	-	-	-	Unused
15:14	WK7MAP	WR	0x0	Wake up circuit 7 input mapping 00: unused 01: unused 10: unused 11: INT7-G4, PALL_RISE; should configure rise edge wakeup if use all pin rise edge wakeup
13:12	WK6MAP	WR	0x0	Wake up circuit 6 input mapping 00: INT6-G1, PE0 01: unused 10: unused 11: INT6-G4, PALL_FALL; should configure fall edge wakeup if use all pin fall edge wakeup
11:10	WK5MAP	WR	0x0	Wake up circuit 5 input mapping 00: INT5-G1, WKO(PB5) 01: INT5-G2, PB5 10: INT5-G3, PG5 11: unused
9:8	WK4MAP	WR	0x0	Wake up circuit 4 input mapping 00: INT4-G1, PB4 01: INT4-G2, PF1 10: INT4-G3, PG3 11: INT4-G4, PG4
7:6	WK3MAP	WR	0x0	Wake up circuit 3 input mapping 00: INT3-G1, PB3 01: INT3-G2, PE7 10: INT3-G3, PF0 11: INT3-G4, PG2
5:4	WK2MAP	WR	0x0	Wake up circuit 2 input mapping 00: INT2-G1, PB2 01: INT2-G2, PE5 10: INT2-G3, PE6 11: INT2-G4, PG1
3:2	WK1MAP	WR	0x0	Wake up circuit 1 input mapping 00: INT1-G1, PB1 01: INT1-G2, PE0 10: INT1-G3, PE4 11: INT1-G4, PG0
1:0	WK0MAP	WR	0x0	Wake up circuit 0 input mapping 00: INT0-G1, PA7

Bit	Name	Mode	Default	Description
				01: INT0-G2, PA6 10: INT0-G3, PA5 11: INT0-G4, PA4

Register 3-21 WKUPCON: Wake up control Register

Bit	Name	Mode	Default	Description
31:16	-	-	-	Unused
15:8	-	-	-	Unused
7:0	WKEN	WR	0x0	Wake up input 7~0 enable 0: disable 1: enable

Register 3-22 WKUPEDG: Wake up edge select Register

Bit	Name	Mode	Default	Description
31:24	-	-	-	Unused
23:16	WKPND	R	0x0	Wake up input 7~0 pending 0: no pending 1: wake up pending
15:8	-	-	-	Unused
7:0	WKEDG	WR	0x0	Wake up input 7~0 wakeup edge select 0: rising edge 1: falling edge

Register 3-23 WKUPIE: Wake up interrupt enable Register

Bit	Name	Mode	Default	Description
31	WKSLPEN	WR	0	Wake up sleep mode enable 0: disable 1: enable
30:20	-	-	-	Unused
19:18	PRISE_FIL	WR	0x0	PORT_INT_RISE filter select 0: disable filter

Bit	Name	Mode	Default	Description
				1: 2+2 counter 2: 2+8 counter 3: 2+32 counter
17:16	PFALL_FIL	WR	0x0	PORT_INT_FALL filter select 0: disable filter 1: 2+2 counter 2: 2+8 counter 3: 2+32 counter
15:8	-	-	-	Unused
7:0	WKIE	WR	0x0	Wake up input 7~0 interrupt enable 0: disable 1: enable

Register 3-24 WKUPCPND: Wake up clear pending Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
23:16	WKCPND	W	0x0	Wake up input 7~0 clear pending 0: no affect 1: clear wake up pending
15:0	-	-	-	Unused

Register 3-25 PORTINTEN: Port interrupt enable Register

Bit	Name	Mode	Default	Description
31:0	PORTINTEN	WR	0x0	Port interrupt 0~31 enable bit 0: disable 1: enable

Register 3-26 PORTINTEDG: Port interrupt edge select Register

Bit	Name	Mode	Default	Description
31:0	PORTINTEDG	WR	0x0	Port interrupt 0~31 edge select bit 0: rise edge

Bit	Name	Mode	Default	Description
				1: fall edge

Register 3-27 PORTINTRISESRC: Port rise edge wakeup source Register

Bit	Name	Mode	Default	Description
31:0	WKRSRC	R	0x0	Port interrupt 0~31 rise edge wake up source; Reference to PIN all wakeup source

Register 3-28 PORTINTFALLSRC: Port fall edge wakeup source Register

Bit	Name	Mode	Default	Description
31:0	WKFSRC	R	0x0	Port interrupt 0~31 fall edge wake up source; Reference to PIN all wakeup source

4 Timer

4.1 Features

1. Tick0/1, support 16bit Timer-mode, Counter-mode;
2. Timer0/1/2, support 32bit Timer-mode, Counter-mode;
3. Timer3/4, support 32bit Timer-mode, Counter-mode, Capture-mode;
4. Timer5, support 32bit Timer-mode, Counter-mode, Capture-mode and PWM mode;

4.2 Tick0/1, Timer0/1/2/3/4/5 Special Function Registers

Register 4-1 TICK0CON/TICK1CON/TMR0CON/TMR1CON/TMR2CON/TMR3CON/TMR4CON/TMR5CON: Tick0/1/Timer0/1/2/3/4 Control Register

Bit	Name	Mode	Default	Description
31:28	-	-	-	Unused
27	PWM5INV	WR	0	Timer pwm5 output invert enable bit 0: disable 1: enable
26	PWM5EN	WR	0	Timer pwm5 enable bit 0: disable 1: enable
25	PWM4INV	WR	0	Timer pwm4 output invert enable bit 0: disable 1: enable
24	PWM4EN	WR	0	Timer pwm4 enable bit 0: disable 1: enable
23	PWM3INV	WR	0	Timer pwm3 output invert enable bit 0: disable 1: enable
22	PWM3EN	WR	0	Timer pwm3 enable bit 0: disable 1: enable
21	PWM2INV	WR	0	Timer pwm2 output invert enable bit 0: disable 1: enable

Bit	Name	Mode	Default	Description
20	PWM2EN	WR	0	Timer pwm2 enable bit 0: disable 1: enable
19	PWM1INV	WR	0	Timer pwm1 output invert enable bit 0: disable 1: enable
18	PWM1EN	WR	0	Timer pwm1 enable bit 0: disable 1: enable
17	PWM0INV	WR	0	Timer pwm0 output invert enable bit 0: disable 1: enable
16	PWM0EN	WR	0	Timer pwm0 enable bit 0: disable 1: enable
15:14	MODE_SEL	WR	0x0	Timer mode selection 00: Timer or PWM mode 01: Capture mode at rising edge 10: Capture mode at falling edge 11: Capture mode at rising or falling edge
13	TICKEN	WR	0	Tick mode enable 0: timer counter will be clear when counter equal to PR 1: timer counter won't be clear when counter equal to PR, continues increase
12:11	-	-	-	Unused
10	CPTPND	R	0	Timer capture pending 0: no pending 1: capture pending
9	TMRPND	R	0	Timer overflow or capture pending 0: no pending 1: overflow or capture pending
8	CPT_IE	WR	0	Timer cpt interrupt enable 0: disable 1: enable
7	TIE	WR	0	Timer interrupt enable 0: disable 1: enable
6:4	PDIVSEL	WR	0x0	Pre-divider selection 000: prepare clock divide 1

Bit	Name	Mode	Default	Description
				001: prepare clock divide 2 010: prepare clock divide 4 011: prepare clock divide 8 100: prepare clock divide 16 101: prepare clock divide 32 110: prepare clock divide 64 111: unused
3:1	PCLKSEL	WR	0x0	Pre-divider clock source selection 000: system clock 001: sys_clkppp（PDIVSEL can't be set to 0 or 1） 010: xosc26m_clk 011: tmr_inc_pin 100: rc2m 101: rtc_rc2m 110: tmr_inc_cr 111: clkout_pinp
0	TMREN	WR	0	Timer enable bit 0: disable 1: enable

NOTE: The PWM relate register is effect only for Timer5

Register 4-2 TICK0CPND/TICK1CPND/TMR0CPND/TMR1CPND/TMR2CPND/TMR3CPND/TMR4CPND: Tick0/1/Timer0/1/2/3/4 clear pending Register

Bit	Name	Mode	Default	Description
31:13	-	-	-	Unused
12	PDCNTCLR	W	0	Timer pre-divider counter clear bit 0: inactive 1: clear pre-divider counter
11	-	-	-	Unused
10	CPTPCLR	W	0	Timer cpt pending clear bit 0: inactive 1: clear pending
9	TPCLR	W	0	Timer overflow pending clear bit 0: inactive 1: clear pending
8:0	-	-	-	Unused

Register 4-3 TICK0CNT/TICK1CNT: Tick0/1 counter Register

Bit	Name	Mode	Default	Description
31:16	-	-	-	Unused
15:0	TMRCNT	WR	0x0	Timer counter. TMRCNT will increase when timer is enabled. It overflows when TMRCNT = TMRPR, TMRCNT will be clear to 0x0 when overflow, and the interrupt flag will be set '1'. When in capture mode, TMRCNT will run from 0 to 65535, can't be clear when TMRCNT = TMRPR

Register 4-4 TICK0PR/TICK1PR: Tick0/1 period Register

Bit	Name	Mode	Default	Description
31:16	-	-	-	Unused
15:0	TMRPR	WR	0xffff	Timer period = TMRPR + 1

Register 4-5 TMR0CNT/TMR1CNT/TMR2CNT/TMR3CNT/TMR4CNT/TMR5CNT: Timer0/1/2/3/4/5 counter Register

Bit	Name	Mode	Default	Description
31:0	TMRCNT	WR	0x0	Timer counter. TMRCNT will increase when timer is enabled. It overflows when TMRCNT = TMRPR, TMRCNT will be clear to 0x0 when overflow, and the interrupt flag will be set '1'. When in capture mode, TMRCNT will run from 0 to 65535, can't be clear when TMRCNT = TMRPR

Register 4-6 TMR0PR/TMR1PR/TMR2PR/TMR3PR/TMR4PR/TMR5PR: Timer0/1/2/3/4/5 period Register

Bit	Name	Mode	Default	Description
31:0	TMRPR	WR	0xffffffff	Timer period = TMRPR + 1

Register 4-7 TMR3CPT/TMR4CPT/TMR5CPT: Timer3/4/5 capture Register

Bit	Name	Mode	Default	Description
31:0	TMRCPT	R	0x0	Timer capture register

Register 4-8 TMR5DUTY0/1/2/3/4/5: Timer5 pwm0/1/2/3/4/5 duty Register

Bit	Name	Mode	Default	Description
31:16	-	-	-	Unused
15:0	TMRDUTY	W	0x0	Timer pwm duty PWM high level length is TMRDUTY+1

Bit	Name	Mode	Default	Description
				PWM low level length is TMRPR-TMRDUTY

5 RTC

5.1 Features

1. Support 32bit Independent power supply real time counter;
2. Support alarm interrupt and second interrupt

5.2 Special Function Registers

Register 5-1 RTCCON: RTC Control Register

Bit	Name	Mode	Default	Description
31:23	-	-	-	Unused
22	INBOX	R	0	INBOX state 0: out of box 1: in box
21	VUSBOFF	R	0	VUSB off state 0: online 1: off state
20	VUSBONLINE	R	0	VUSB online state 0: not online 1: online
19	WKO_CIN	R	0	WKO pin state 0: WKO pin state is 0 1: WKO pin state is 1
18	RTCWKSLPPND	R	0	RTC wakeup sleep pending 0: no pending 1: pending
17	ALMPND	R	0	RTC alarm pending 0: no pending 1: alarm pending
16	RTC_ON	R	0	RTC on signal 0:off 1:on
15:13	-	-	-	Unused
12	INBOXIE	WR	0	INBOX interrupt enable 0: disable

Bit	Name	Mode	Default	Description
				1: enable
11	VUSBONIE	WR	0	VUSB online interrupt enable 0: disable 1: enable
10	INBOX_WKSLPEN	WR	0	INBOX online wakeup sleep enable 0: disable 1: enable
9	VUSBON_WKSLPEN	WR	0	VUSB online wakeup sleep enable 0: disable 1: enable
8	ALM_WKSLPEN	WR	0	RTC alarm wakeup sleep enable 0: disable 1: enable
7	RTC1S_WKSLPEN	WR	0	RTC1S wakeup sleep enable 0: disable 1: enable
6	VUSBRSTEN	WR	0	VUSB insert reset system enable 0: disable 1: enable
5	WKUPRSTEN	WR	0	RTC wake up power down mode reset system enable 0: disable 1: enable
4	ALMIE	WR	0	RTC alarm interrupt enable 0: disable 1: enable
3	RTC1SIE	WR	0	RTC 1S interrupt enable 0: disable 1: enable
2:1	BAUDSEL	WR	0x0	Increase clock selection 00: System Clock divide 1 01: System Clock divide 2 10: System Clock divide 6 11: System Clock divide 14
0	VRTCVSEL	WR	0	VRTC11 voltage select 0: control by rtccon4 bit24~bit22 1: control by rtccon4 bit27~bit25

Register 5-2 RTCCPND: RTC clear pending Register

Bit	Name	Mode	Default	Description
31	VBCNTCLR	W	0	Write 1 will clear VUSB reset delay counter and pending
30	VBCNTKST	W	0	Write 1 will kick start VUSB reset delay counter
29:28	VBCNTDIS	W	0x0	Write 0x3 clear VUSB reset delay counter and pending, at the same time, disable VUSB reset delay counter
27:19	-	-	-	Unused
18	CWKSLPPND	W	0	Write 1 will clear RTC wakeup sleep pending
17	CALMPND	W	0	Write 1 will clear RTC alarm pending
16:0	-	-	-	Unused

Register 5-3 VBRSTCON: VUSB reset control Register

Bit	Name	Mode	Default	Description
31	VBONLPND	R	0	VUSB online rise pending, VBCNTCLR will clear this pending
30	VBRSTMODE	WR	0	VUSB counter reset mode 0: VUSB insert rise edge kick start 1: Software kick start
29:20	VBRSTPR	WR	0x0	VUSB reset delay time is: n*1024 * Frc32k
19:0	VBRSTCNT	R	0x0	VUSB reset delay counter

5.3 Independent Power RTC Registers

Register 5-4 RTCCNT: RTC counter Register

Bit	Name	Mode	Default	Description
31:0	RTCCNT	WR	0x0	32bit RTC counter

Register 5-5 RTCALM: RTC alarm Register

Bit	Name	Mode	Default	Description
31:0	RTCALM	WR	0xffffffff	32bit RTC alarm

Register 5-6 RTCRAMADR: RTC ram address Register

Bit	Name	Mode	Default	Description

Bit	Name	Mode	Default	Description
31:0	RTCRAMADR	W	x	RTCRAM read or write start address

Register 5-7 RTCRAMDAT: RTC ram data Register

Bit	Name	Mode	Default	Description
31:0	RTCRAMDAT	WR	x	RTCRAM read or write data When read or write this register, ram address will be auto increase

Register 5-8 RTCCON0: RTC control Register 0

Bit	Name	Mode	Default	Description
31:26	-	-	-	-
25	EN_CAP2PLL	WR	0x0	Reference to pinlist
24:22	RSTIMESEL	WR	0x0	System reset time select 000: 64 * rc 32k 100: 32 * rc 32k 010: 8 * rc 32k 001: 2 * rc 32k Bit0 > bit1 > bit2
21	BGUV_RSTEN	WR	0	BGUV reset TKSWRSTN enable 0: disable 1: enable
20	RCOUT_SEL	WR	0	RTC output RC select bit 0: SNF_RC_RTC 1: RC2M_RTC
19	RING_SEL	WR	0x1	Reference to pinlist
18	SNF_RC_EN	WR	0x0	Reference to pinlist
17:16	SNF_RC_BIAS	WR	0x0	Reference to pinlist
15	Rev	-	-	Reserved
14	Rev	-	-	Reserved
13:12	CLK2MTKSSEL	WR	0x0	CLK2M to touch key clock select bit 00: 0 01: RC2M_RTC 10: SNF_RC_RTC 11: xosc_clkdiv12
11:10	CLK2MBTSSEL	WR	0x0	CLK2M to BT low power clock select bit 00: 0 01: RC2M_RTC

Bit	Name	Mode	Default	Description
				10: SNF_RC_RTC 11: xosc_clkdiv12
9:8	CLK2MRTCSSEL	WR	1	CLK2M in RTC power domain source select bit 00: 0 01: RC2M_RTC 10: SNF_RC_RTC 11: xosc_clkdiv12
7	PWRUP1ST	WR	1	RTC first power up flag 0: not first power up 1: first power up
6	EXT32KSEL	WR	0x0	External 32k clock sel 0: select clk2m_rtc_div64 1: select external 32k
5	TKSW_RSTN	WR	0	Touch key software reset bit 0: Touch key reset 1: Touch key reset disable
4	TKITF_EN	WR	1	Touch key between core interface enable bit 0: disable 1: enable
3	SNIFF_EN	WR	0	Sniff mode disable VDDCORE_EN enable 0: disable 1: enable
2	CLKOUT_EN	WR	0	RTC output RC clock to core enable 0: disable 1: enable
1	Rev	-	-	Reserved
0	RCOSC_EN	WR	0	RCOSC enable bit 0: disable 1: enable

Register 5-9 RTCCON1: RTC control Register 1

Bit	Name	Mode	Default	Description
11	VRTC11_HWCEN	WR	0	VRTC11 voltage can be change to normal config when wake up shut down mode 0: disable 1: enable
10	WKSRC_LAT_EN	WR	0x0	Wakeup pmu source latch enable bit 0: wakeup pmu source latch 1: wakeup pmu source

Bit	Name	Mode	Default	Description
9	EN_VDDTK	WR	0x1	Reference to pinlist
8	RST_SRC_SEL	WR	0x0	WKO reset source select 0: select WKO 1: select touch key 10s
7	VRTC_EN	WR	0x0	Reference to pinlist
6:0	-	-	-	-

Register 5-10 RTCCON2: RTC control Register 2

Bit	Name	Mode	Default	Description
31:17	RTCTMRCNT	R	0x0	RTC timer 1s counter, bit16~bit2
16:0	RTCTMRPR	WR	0x7fff	RTC timer 1s period

Register 5-11 RTCCON3: RTC control Register 3

Bit	Name	Mode	Default	Description
31:24	-	-	-	Unused
23	PDNMODE	WR	0	PDN mode enable 0: disable 1: enable
22	LVCORE_EN	WR	0	Low power VDDCORE enable 0: disable 1: enable
21:20	Rev	-	-	Reserved
19	PDCORE3	WR	0	Reference to pinlist
18	POR_BLKEN	WR	0	VDDCORE POR block enable; when this bit is 1, VDDCORE POR will be invalid 0: disable 1: enable
17	WK4_EN	WR	0	PORT wakeup PMU enable bit 0: disable 1: enable
16	WDT_WKEN	WR	0	RTC WDT wakeup enable bit 0: disable 1: enable
15	BGUV_WKEN	WR	0	BGUV wakeup enable bit 0: disable 1: enable

Bit	Name	Mode	Default	Description
14	TK_WKEN	WR	0	Touch key long press wakeup enable bit 0: disable 1: enable
13	BTWK_EN	WR	0	BT wake up enable bit 0: disable 1: enable
12	INBOX_WKEN	WR	0	INBOX wake up enable bit 0: disable 1: enable
11	VSUB_WKEN	WR	0	VUSB wake up enable bit 0: disable 1: enable
10	WKP_WKEN	WR	0	WK pin wake up enable bit 0: disable 1: enable
9	RTC1S_WKEN	WR	0	RTC one second wakeup enable bit 0: disable 1: enable
8	ALM_WKEN	WR	0	RTC alarm wakeup enable bit 0: disable 1: enable
7	EN_VIO_AON	WR	0	VDDIO always on enable bit Reference to pinlist
6	PDCOREEN	WR	1	Core power down enable bit 0: disable 1: enable
5	C2VLCEN	WR	1	VDDCORE bypass to VLCORE enable bit 0: disable 1: enable Reference to pinlist
4	PDCORE2	WR	0	Core power down 2 enable bit; only affect analog model except GPIO 0: disable 1: enable
3	R2VCLEN	WR	0	VRTC11 bypass to VLCORE power gate enable bit 0: disable 1: enable Reference to pinlist
2	VCOREEN	WR	1	VDDCORE enable bit 0: disable

Bit	Name	Mode	Default	Description
				1: enable
1	VIOEN	WR	1	VDDIO enable bit 0: disable 1: enable
0	VBTEN	WR	0	VDDBT enable bit 0: disable 1: enable

Register 5-12 RTCCON4: RTC control Register 4

Bit	Name	Mode	Default	Description
31:28	BGWRTRIM	WR	0x8	Reference to pinlist
27:25	VRTC_SEL1	WR	0x6	VRTC_VSEL=1, vrtc 11 voltage select bit Reference to pinlist
24:22	VRTC_SEL0	WR	0x6	VRTC_VSEL, vrtc 11 voltage select bit Reference to pinlist
21:20	VCORE_TC	WR	0x1	Reference to pinlist
19	EN_RTCBG_UVM	WR	0x1	Reference to pinlist
18:17	VIO_TC	WR	0x3	Reference to pinlist
16	VIOPD_EN	WR	1	Reference to pinlist
15	VIO_AON_SEL	WR	0x0	VDDIO always on select bit 0: disable 1: enable
14:12	VLCORE_SEL1	WR	0x3	Reference to pinlist
11:9	VLCORE_SEL0	WR	0x3	Reference to pinlist
8	USB4P5_SEL	WR	0	USB4P5 enable, When this bit is 1, usb4p5 output will affect VUSBOFF
7	VDDBTCAPSEL	WR	1	VDDBT cap select bit 0: VDDBT without cap 1: VDDBT with cap
6	VCORESVBT	WR	0	Reference to pinlist
5	VCORESVIO	WR	1	Reference to pinlist
4	EN_BUCKC	WR	0	Reference to pinlist
3	VCORE_LGM	WR	1	Reference to pinlist
2	VDDBT_TC	WR	0	Reference to pinlist
1:0	-	-	-	-

Register 5-13 RTCCON5: RTC control Register 5

Bit	Name	Mode	Default	Description
31:19	-	-	-	-
18:17	POWERFLAG	WR	0x0	Power flag
16	SRAMSD1_EN	WR	0x0	SRAM Low power shut down enable 0:disable 1:enable
15	SRAMSD_EN	WR	0x0	SRAM power shut down enable 0:disable 1:enable
14	SRAM_DS_EN	WR	0x0	SRAM deep sleep enable 0:disable 1:enable
13	SRAMLS_EN	WR	0x0	SRAM light sleep enable 0:disable 1:enable
12	IOLPIFEN	WR	1	Low power GPIO interface enable bit 0: select lowpower port config 1: select system port config
11	LPIFEN	WR	1	Low power interface enable bit(except GPIO) 0: disable 1: enable
10	LPRST	WR	0	Low power model reset bit 0: reset 1: release reset
9:8	PMU_RSV_P	WR	0	Reference to pinlist
7	REV	WR	0	Reserved
6	REV	WR	0	Reserved
5:4	VIOSEL	WR	0x0	VIO LDO mode select 00: normal mode 01: ultra-low power mode 10: Diode mode 11: low power mode
3:2	VCORESEL	WR	0x0	VCORE LDO mode select 00: normal mode 01: ultra-low power mode 10: Diode mode 11: low power mode
1	REV	WR	0	Reserved

Bit	Name	Mode	Default	Description
0	VBTLDOM	WR	1	VDDBT LDO mode select bit 0: buck mode 1: LDO mode

Register 5-14 RTCCON6: RTC control Register 6

Bit	Name	Mode	Default	Description
7	REV	WR	0	Reserved
6	REV	WR	0	Reserved
5:4	VIOSEL_SNF	WR	0x0	VIO LDO mode select(sniff_pdn_mode) 00: normal mode 01: ultra-low power mode 10: Diode mode 11: low power mode
3:2	VCORESEL_SNF	WR	0x0	VCORE LDO mode select(sniff_pdn_mode) 00: normal mode 01: ultra-low power mode 10: Diode mode 11: low power mode
1	REV	WR	0	Reserved
0	VBTLDOM_SNF	WR	1	VDDBT LDO mode select bit(sniff_pdn_mode) 0: buck mode 1: LDO mode

Register 5-15 RTCCON7: RTC control Register 7

Bit	Name	Mode	Default	Description
31:23	-	-	-	-
22	CHPWRUPDIS	WR	0	Charge current when insert VUSB disable bit 0: enable 1: disable
21	CH_CV2HG	WR	0x0	Reference to pinlist
20	CH_CVHG	WR	0x0	Reference to pinlist
19:18	CH_CV2SEL	WR	0x3	Reference to pinlist
17	EN_CH_CV2	WR	0	Reference to pinlist
16:15	VUSBOFFSEL	WR	0x0	VUSB OFF select for output to analog control 00: analog input as VUSB OFF 01: filter output from analog input 10: output 0

Bit	Name	Mode	Default	Description
				11: output 1
14:11	CHIEND	WR	0x2	Reference to pinlist
10	STARTUPSEL	WR	0	Select charge start up current 0 :30mA 1 :50mA
9:7	TRICKLESEL	WR	0x3	Select charge trickle current 000 :5mA 001 :10mA 010 :15mA 011 :20mA 100: 25mA 101: 30mA 110: 35mA 111: 40mA
6	PWRUPISEL	WR	0	Select charge current when insert VUSB; 0 :20mA 1 :30mA
5:0	SWICH	WR	0x3	Select charge current when software control Reference to pinlist

Register 5-16 RTCCON8: RTC control Register 8

Bit	Name	Mode	Default	Description
31	VBGPWRT	WR	0	Reference to pinlist
30	VBGCHT	WR	0	Reference to pinlist
29	EN_BGUVT	WR	0	Reference to pinlist
28:24	BG_TRIM	WR	0xf	Reference to pinlist
23	CH_VIOPLOAD	WR	0	Reference to pinlist
22:20	CH_VIOSEL	WR	0x2	Reference to pinlist
19	LEAK_USB	WR	0	Reference to pinlist
18:16	CH_LEAKAGE	WR	0	Reference to pinlist
15	VUSBDIV_EN	WR	0	vusb voltage divide enable bit 0: disable 1: enable
14:10	BGCH_TRIM	WR	0xf	Charger BG trim bit Reference to pinlist
9:8	VBAT_SEL	WR	0	Reference to pinlist
7	-	-	-	-

Bit	Name	Mode	Default	Description
6	CHARGE_EN	WR	1	Charger enable bit 0: disable 1: enable Reference to pinlist
5	EN_USB4P5	WR	0	VUSB enable bit 0: disable 1: enable
4	INBX_SEL	WR	0	Reference to pinlist
3:2	VRECHS	WR	0x1	Reference to pinlist
1	CHSTOPS	WR	0	Charger stop enable bit 0: enable charger function 1: disable charger function
0	VIOCHG_EN	WR	0	VUSB to VDDIO LDO enable bit 0: disable 1: enable

Register 5-17 RTCCON9: RTC control Register 9

Bit	Name	Mode	Default	Description
14	WDTWKP	WR	0	When write: WDT wake up pending clear 0: no affect 1: clear pending When read: WDT wake up software shutdown pending 0: no pending 1: pending
13	-	-	-	-
12	WK4WKP	WR	0	When write: Port wake up pending clear 0: no affect 1: clear pending When read: Port wake up software shutdown pending 0: no pending 1: pending
11	BGUVWKP	WR	0	When write: BGUV wake up pending clear 0: no affect 1: clear pending

Bit	Name	Mode	Default	Description
				When read: BGUV wake up software shutdown pending 0: no pending 1: pending
10	-	-	-	-
9	WK3WKP	WR	0	When write: WK pin3 wake up pending clear 0: no affect 1: clear pending When read: WK pin3 wake up software shutdown pending 0: no pending 1: pending
8	WK2WKP	WR	0	When write: WK pin2 wake up pending clear 0: no affect 1: clear pending When read: WK pin2 wake up software shutdown pending 0: no pending 1: pending
7	WK1WKP	WR	0	When write: WK pin1 wake up pending clear 0: no affect 1: clear pending When read: WK pin1 wake up software shutdown pending 0: no pending 1: pending
6	TKWKP	WR	0	When write: TK wake up pending clear 0: no affect 1: clear pending When read: TK wake up software shutdown pending 0: no pending 1: pending
5	BTWKP	WR	0	When write: BT wake up pending clear 0: no affect 1: clear pending

Bit	Name	Mode	Default	Description
				When read: BT wake up software shutdown pending 0: no pending 1: pending
4	INBOXWKP	WR	0	When write: INBOX wake up pending clear 0: no affect 1: clear pending When read: INBOX wake up software shutdown pending 0: no pending 1: pending
3	VUSBWKP	WR	0	When write: VUSB wake up pending clear 0: no affect 1: clear pending When read: VUSB wake up software shutdown pending 0: no pending 1: pending
2	WKPWKP	WR	0	When write: WK pin wake up pending clear 0: no affect 1: clear pending When read: WK pin wake up software shutdown pending 0: no pending 1: pending
1	RTC1SWKP	WR	0	When write: RTC 1 second pending clear 0: no affect 1: clear 1s pending When read: RTC 1 second wake up software shutdown pending 0: no second pending 1: second pending
0	ALMWKP	WR	0	When write: RTC alarm pending clear 0: no affect 1: clear alarm pending When read:

Bit	Name	Mode	Default	Description
				Alarm wake up software shutdown pending 0: no alarm pending 1: alarm pending

Register 5-18 RTCCON10: RTC control Register 10

Bit	Name	Mode	Default	Description
31	CVUSBI4SHWEN	W	0	Clear VUSB insert 4S hardware enable bit 0: no affect 1: Clear VUSB insert 4S hardware enable bit
30:16	-	-	-	-
15	RVUSBPND	WR	0	When write Clear VUSB insert reset counter and pending 0: no affect 1: clear VUSB insert reset counter & reset pending When read: VUSB 4S reset pending 0: no pending 1: pending
14	RWDTPND	WR	0	When write Clear RTC WDT 0: no affect 1: clear RTC WDT & clear RTC WDT reset pending When read: RTC WDT reset pending 0: no pending 1: pending
13	MCLR_PND	WR	0	When write MCLR pending clear 0: no affect 1: clear MCLR pending When read: MCLR pending 0: MCLR pending 1: MCLR pending
12	WK4_WKPMU	R	0	Port wake up pending 0: no pending 1: pending
11	BGUVPND	WR	0	When write BGUV pending clear 0: no affect

Bit	Name	Mode	Default	Description
				1: clear BGUV pending When read: BGUV pending 0: no BGUV pending 1: BGUV pending
10	WKP10SPND	WR	0	When write WK pin 10s pending clear 0: no affect 1: clear 10s pending When read: WK pin 10s pending 0: no 10s pending 1: 10s pending
9	WK3_WKPMU	WR	0	WK3 pending 0: no WK3 pending 1: WK3 pending
8	WK2_WKPMU	R	0	WK2 wake up pending 0: no pending 1: pending
7	WK1_WKPMU	R	0	WK1 wake up pending 0: no pending 1: pending
6	TK_WKPMU	R	0	TK wake up pending 0: no pending 1: pending
5	BT_WKPMU	R	0	BT wake up pending 0: no pending 1: pending
4	INBOX_WKPMU	R	0	INBOX wake up pending 0: no pending 1: pending
3	VUSBPND	WR	0	VUSB wake up pending 0: no pending 1: pending
2	WKP	R	0	WK pin wake up pending 0: no pending 1: pending
1	RTC1SPND	WR	0	When write: RTC 1 second pending clear 0: no affect

Bit	Name	Mode	Default	Description
				1: clear 1s pending When read: RTC 1 second pending 0: no second pending 1: second pending
0	ALMPND	WR	0	When write: RTC alarm pending clear 0: no affect 1: clear alarm pending When read: Alarm pending 0: no alarm pending 1: alarm pending

Register 5-19 RTCCON11: RTC control Register 11

Bit	Name	Mode	Default	Description
10	RTCWKSLPEN	WR	0	RTC timer wakeup sleep enable 0: disable 1: enable
9:8	RTCWKSLPS	WR	0x0	RTC timer wakeup sleep time select 00: 110ms 01: 220ms 10: 440ms 11: 880ms
7	VIOCHG_SWEN	WR	0	VUSB to VDDIO LDO select control bit 0: VUSB to VDDIO LDO enable by pmu_normal & VIOCHG_EN 1: VUSB to VDDIO LDO enable by VIOCHG_SWEN & VIOCHG_EN
6	VUSBWKSEL	WR	0	VUSB wakeup select 0: VUSB insert filter wakeup 1: VUSB pull out filter wakeup
5	VUSBFILSEL	WR	0	VUSB off filter select 0: 840us 1: 12ms
4	VUSBI4SHWENS	WR	0	VUSB insert 4s hardware enable select 0: disable VUSBI4SHWEN to control vusb insert 4s enable 1: enable VUSBI4SHWEN to control vusb insert 4s enable
3	VUSBFASEL	WR	0	VUSB filter insert, after fiter pull out enable bit 0: disable 1: enable

Bit	Name	Mode	Default	Description
2	WKPFEN	WR	1	WK pin filter enable bit 0:disable 1:enable
1:0	WKPFSEL	WR	0x0	WK pin filter select bit 00: 256* Frc 01: 1024* Frc 10: 4096* Frc 11: 16384* Frc

Register 5-20 RTCCON12: RTC control Register 12

Bit	Name	Mode	Default	Description
31:30	VUSBI4SHWEN	R	0	VUSB insert 4S hardware enable bit; when VUSB pull out, this bit will be set; Write RTCCON10 bit31 to 1 will clear this bit 00: disable Others is enable
29:20	-	-	-	-
19	RWDTSEL _WR	W	0	RTC WDT reset time select bit write enable 0: bit16~bit18 can't be write to RWDTSEL 1: bit16~bit18 can be write to RWDTSEL
18:16	RWDTSEL	WR	0x4	RTC WDT time select bit 000: 32 * Frc 001: 8192 * Frc 010: 16384 * Frc 011: 32768 * Frc 100: 65536 * Frc 101: 131072 * Frc 110: 262144 * Frc 111: 524288 * Frc
15	GPIO10SSEL _WR	W	0	GPIO reset time select bit write enable 0: bit12~bit14 can't be write to GPIO10SSEL 1: bit12~bit14 can be write to GPIO10SSEL
14:12	GPIO10SSEL	WR	0x1	The period 10s reset select: 262144 + n*65536) * Frc
11	WKO10SSEL _WR	W	0	WKO reset time select bit write enable 0: bit8~bit10 can't be write to WKO10SSEL 1: bit8~bit10 can be write to WKO10SSEL
10:8	WKO10SSEL	WR	0x1	The period 10s reset select: 262144 + n*65536) * Frc
7:6	RWDTEN	WR	0x0	RTC WDT enable 0x3: disable Others: enable

Bit	Name	Mode	Default	Description
5:4	GPIO10SEN	WR	0x0	GPIO 10s reset enable 0x3: disable Others: enable
3:2	VUSBI4SEN	WR	0x0	VUSB insert 4S reset enable 0x3: disable Others: enable
1:0	WKP10SEN	WR	0x0	WK pin 10s reset enable 0x3: disable Others: enable

Register 5-21 RTCCON13: RTC control Register 13

Bit	Name	Mode	Default	Description
23:20	IO_CIN	R	0x0	WK pin3~0 input state 0: WK pin input state is low 1: WK pin input state is high
19:16	WKPLVLS	WR	0	WK pin3~0 wakeup level select bit 0: low level wakeup 1: high level wakeup
15:12	WKPEN	WR	0x0	WK pin3~0 wakeup enable 0: disable 1: enable
11:8	WKPPD	WR	0x0	WK pin3~0 pulldown 10K enable 0: disable 1: enable
7:4	WKPPU	WR	0x0	WK pin3~0 pull up 10K enable 0: disable 1: enable
3:0	WKPIE	WR	0x0	WK pin3~0 input enable 0: disable 1: enable

6 Watchdog Timer

6.1 WDT Special Function Registers

Register 6-1 WDTCON: WDT Control Register

Bit	Name	Mode	Default	Description
31	WDTPND	R	0	WDT time out pending 0: no pending 1: pending
30:28	-	-	-	Unused
27:24	TMRSEL_WR	W	0	WDT time select bit write enable When write 0xa, bit20~bit22 can be write to TMRSEL, other value will no affect
23	-	-	-	Unused
22:20	TMRSEL	R	0x4	WDT time select bit 000: 1ms 001: 256ms 010: 512ms 011: 1024ms 100: 2048ms 101: 4096ms 110: 8192ms 111: 16384ms
19:16	WDTCSEL_WR	W	0	WDT clock select When write 0xa, WDTCSEL =0, when write 0x5, WDTCSEL =1. other value will no affect
16	WDTCSEL	R	0	WDT clock select bit 0:RC32K 1:X32K from 26M divider
15:12	WDTIE_WR	W	0	WDT interrupt disable When write 0xa, WDTIE will disable, when write 0x5, WDTIE will enable. other value will no affect
12	WDTIE	R	0	WDT interrupt enable bit 0: Disable 1: Enable
11:8	WDTRSTEN_WR	W	0	WDT reset disable When write 0xa, WDTRSTEN will disable, other value will no affect
8	WDTRSTEN	WR	1	WDT reset enable bit 0: Disable

Bit	Name	Mode	Default	Description
				1: Enable
7:4	WDTEN_WR	W	0	WDT disable When write 0xa, WDTEN will disable, other value will no affect
4	WDTEN	WR	1	WDT enable bit 0: Disable 1: Enable
3:0	WDTCLR	W	0	WDT clear bit When write 0xa, WDT counter and WDTPND will be clear

6.2 User Guide

1. configure WDT reset or interrupt
2. Select WDT time out
3. Clear WDT

7 UART0/1/2

7.1 Features

1. UART is a serial port capable of asynchronous transmission.
2. The UART can function in full duplex mode.

7.2 UART0/1/2 Special Function Registers

Register 7-1 UART0CON/UART1CON/UART2CON: UART0/1/2 Control Register

Bit	Name	Mode	Default	Description
31	TSKEN_EN	WR	0	Test mode key enable 0: disable 1: enable
30:28	-	-	-	Unused
27:24	KEYIE	WR	0	UART key match interrupt enable Write 0xa will enable, write 0x5 will disable.
23:20	KEYEN	WR	0x0	UART Key enable Write 0xa will enable uart key mode, write 0x5 will disable key mode.
19:16	RSTEN	WR	0	UART reset Key enable Write 0xa will enable uart reset key mode, write 0x5 will disable reset key mode. Note: uart2 default value is 1
15	RX_4BUF_ERROR	R	0	RX 4buf error 0: RX 4buf not error 1: RX 4buf error
14	-	-	-	-
13:11	RX_BCNT	R	0	RX byte cnt, CRXPND will decrease 1 when RX_BCNT isn't zero 0: no receive data 1: receive 1 byte data 2: receive 2 byte data 3: receive 3 byte data 4: receive 4 byte data 5,6,7: invalid
10	KEYMAT	R	0	Key match pending 0: key unmatch 1: key match

Bit	Name	Mode	Default	Description
9	RXPND	R	0	RX pending 0: RX one byte not finish 1: RX one byte finish
8	TXPND	R	1	TX pending 0: TX one byte not finish 1: TX one byte finish
7	RXEN	WR	0	RX enable 0: RX disable 1: RX enable Note: uart2 defalut value is 1
6	ONELINE	WR	0	One-line mode 0: TX/RX separate 1: TX/RX one line
5	FIXBAUD	WR	0	Fix baud enable 0: auto detect baud 1: fix baud
4	SB2EN	WR	0	Two Stop Bit enable 0: 1-bit Stop Bit 1: 2 bit Stop Bit
3	TXIE	WR	0	Transmit Interrupt Enable 0 = Transmit interrupt disable 1 = Transmit interrupt enable
2	RXIE	WR	0	Receive Interrupt Enable 0: Receiver interrupt disable 1: Receiver interrupt enable
1	BIT9EN	WR	0	BIT9 Enable Bit 0: Eight-bit mode 1: Nine-bit mode
0	UTEN	WR	0	UART Enable Bit 0: Disable UART module 1: Enable UART module

Register 7-2 UART0CPND/UART1CPND/UART2CPND: UART0/1/2 clear pending Register

Bit	Name	Mode	Default	Description
31:19	-	-	-	Unused
18	CBDCFM	W	0	Clear baud confirm, should re-detect baud
17:16	-	-	-	Unused
15	RX4BUF_ERROR_CLR	W	0	RX 4buf error clear

Bit	Name	Mode	Default	Description
				0: N/A 1: Clear RX 4buf error
14:11	-	-	-	Unused
10	CKEYMAT	W	0	Key match pending clear 0: N/A 1: Clear key match pending
9	CRXPND	W	0	RX pending clear 0: N/A 1: Clear RX Pending
8	CTXPND	W	0	TX pending clear 0: N/A 1: Clear TX Pending. Writing data to UTBUF will clear TXPND
7:0	-	-	-	Unused

Register 7-3 UART0BAUD/UART1BAUD/UART2BAUD: UART0/1/2 Baud Rate Register

Bit	Name	Mode	Default	Description
31:16	DARTBAUD	R	0x0	UART detect baud by hardware
15:0	BAUD	WR	x	UART Baud Rate Baud Rate =Fudet clock / (BAUD + 1)

Register 7-4 UART0DATA/UART1DATA/UART2DATA: UART0/1/2 Data Register

Bit	Name	Mode	Default	Description
31:9	-	-	-	Unused
8	BIT8	WR	x	UART Data bit 8
7:0	UARTDAT	WR	x	UART Data Write this register will load the data to transmitter buffer. Read this register will read the data from the receiver buffer..

7.3 User Guide

1. Set IO in the correct direction.
2. Configure UART0BAUD to choose sample rate
3. Enable UART0 by setting
4. Set TXIEor RXIE ‘to 1’ if needed
5. write data to UART0DATA
6. Wait for PND to change to ‘1’, or wait for interrupt

7. Read received data from UART0DATA if needed

8 HSUART0

8.1 Features

1、 Support full duplex mode
2、 Support async clock between UART interface part and control part
3、 Support interrupt
4、 Support 8/9 bit data mod，but not data parity checking.
5、 Support 16 bit baud rate setting.

HSUART TX：
1、 Support single byte TX
2、 Support DMA TX，minimum 1 Byte， maximum 1024 Byte
3、 Support DMA length configure by Byte
4、 Support DMA address configure by Byte
5、 Support 1/2 stop bit
6、 Support TXIE control
7、 Support TX pending

HSUART RX：
1、 Support single byte RX
2、 Support DMA RX，minimum 1 Byte， maximum 1024 Byte
3、 Support loop buffer DMA mode
4、 Support DMA length configure by Byte
5、 Support DMA address configure by Byte
6、 Always 1 stop bit，and not check stop bit
7、 Only 8bit data mode at RX DMA
8、 Support RXIE control
9、 Support RX pending

8.2 HSUART 0 Special Function Registers

Register 8-1 HSUT0CON: High speed UART Control Register

Bit	Name	Mode	Default	Description
31:19	-	-	-	Unused
18	ONELINE	WR	0	One-line mode 0: TX/RX separate 1: TX/RX one line
17	RXHFPND_IE	WR	0	RX DMA half_full pending interrupt enable 0: disable 1: enable

Bit	Name	Mode	Default	Description
16	RXOVEPND	R	0	RX overflow error pending 0: RX DMA buffer not overflow error 1: RX DMA buffer overflow error
15	TMROV	R	0	RX TIMER Overflow flag 0: RX timer not overflow 1:RX timer overflow
14	RXFAIL	R	0	RX Fail flag 0: RX DMA no error 1: RX DMA error
13	TXPND	R	1	TX pending 0: TX one byte/DMA n byte not finish 1: TX one byte/DMA n byte finish
12	RXPND	R	0	RX pending 0: RX one byte/DMA n byte not finish 1: RX one byte/DMA n byte finish
11	RXHF_PND	R	0	RX DMA half_full pending
10	HSUTTMREN	WR	0	HSUART DMA RX TIMER CNT enable 0: disable 1: enable
9	SPBITSEL	WR	0	TX Stop Bit select 0: 1 bit Stop Bit 1: 2 bit Stop Bit
8	TXBITSEL	WR	0	TX Data bit select 0:8-bit mode 1:9-bit mode
7	TXTRSMODE	WR	0	TX Transmit mode select 0: buffer mode 1:DMA mode
6	RXLPBUFEN	WR	0	RX DMA loop buffer mode enable bit 0: disable 1:enable
5	RXBITSEL	WR	0	RX Data bit select 0:8-bit mode 1:9-bit mode
4	RXTRSMODE	WR	0	RX Transmit mode select 0: buffer mode 1:DMA mode
3	TXIE	WR	0	Transmit Interrupt Enable 0 = Transmit interrupt disable

Bit	Name	Mode	Default	Description
				1 = Transmit interrupt enable
2	RXIE	WR	0	Receive Interrupt Enable 0: Receiver interrupt disable 1: Receiver interrupt enable
1	UTXEN	WR	0	UART TX Enable Bit 0: Disable TX UART module 1: Enable TX UART module
0	URXEN	WR	0	UART RX Enable Bit 0: Disable UART RX module 1: Enable UART RX module

Register 8-2 HSUT0CPND: HSUART clear pending Register

Bit	Name	Mode	Default	Description
31:18	-	-	-	-
17	CRXLBBUF	W	0	RX loopback buffer clear 0: N/A 1: Clear RX loopback buffer
16	CRXOVEPND	W	0	RX overflow error pending clear 0: N/A 1: Clear RX overflow error Pending.
15	CTMROV	W	0	RX timer overflow flag clear 0: N/A 1: Clear flag
14	CRXFAIL	W	0	RX Fail clear 0: N/A 1: Clear RX fail flag
13	CTXPND	W	0	TX pending clear 0: N/A 1: Clear TX Pending
12	CRXPND	W	0	RX pending clear 0: N/A 1: Clear RX Pending. Writing data to UTBUF will clear TXPND
11	CRXHFPND	W	0	RX DMA half pending clear 0: N/A 1: Clear RX overflow Pending.
10	CCTSPND	W	0	CTS status changing pending clear 0: N/A 1: Clear CTS status changing pending

Bit	Name	Mode	Default	Description
9:2	-	-	-	Unused
1	CUTTX	W	0	HS TX interface clear 0: N/A 1: clear to idle status at hsuartclk domain
0	CUTRX	W	0	HS RX interface clear 0: N/A 1: clear to idle status at hsuartclk domain

Register 8-3 HSUT0BAUD: HSUART Baud Rate Register

Bit	Name	Mode	Default	Description
31:16	HSUTRXBAUD	WR	0	HSUART RX Baud Rate Baud Rate =source clock / (HSUTRXBAUD + 1)
15:0	HSUTTXBAUD	WR	0	HSUART TX Baud Rate Baud Rate =source clock / (HSUTTXBAUD + 1)

Register 8-4 HSUT0DATA: HSUART Data Register

Bit	Name	Mode	Default	Description
31:9	-	-	-	Unused
8	HSUTBIT8	W	x	UART Data bit 8
7:0	HSUTDAT	W	x	UART Data Write this register will load the data to transmitter buffer.

Register 8-5 HSUT0TXCNT: HSUART TX counter Register

Bit	Name	Mode	Default	Description
31:16	-	-	-	Unused
15:0	TXCNT	WR	0	HSUART TX DMA byte counter

Register 8-6 HSUT0TXADR: HSUART TX DMA start address Register

Bit	Name	Mode	Default	Description
31:19	-	-	-	-
19:0	HSUTTXADR	WR	0	HSUART TX DMA start address

Register 8-7 HSUT0RXCNT: HSUART RX counter Register

Bit	Name	Mode	Default	Description

Bit	Name	Mode	Default	Description
31:16			-	Unused
15:0	RXCNT	WR	0	HSUART RX DMA size

Register 8-8 HSUT0RXADR: HSUART RX DMA start address Register

Bit	Name	Mode	Default	Description
31:19	-	-	-	-
19:0	HSUTRXADR	WR	0	HSUART RX DMA start address

Register 8-9 HSUT0FIFOCNT: HSUART RX FIFO counter Register

Bit	Name	Mode	Default	Description
31:16	-	-	-	Unused
15:0	RXFIFOCNT	R	0	HSUART RX data counter left

Register 8-10 HSUT0RXFIFO: HSUART RX Data FIFO Register

Bit	Name	Mode	Default	Description
31:10	-	-	-	Unused
9	RXFIFO_DONE	R	0	RXFIFO read from SRAM done 0: read not finish 1; read done Auto clear by kick RXFIFO_RD bit
8	RXFIFO_RD	W	0	RX read pulse 0: N/A 1: read fifo kick start
7:0	RXFIFO	R	x	UART RX Data Read this register will read the data from the receiver SRAM buffer

Register 8-11: HSUT0TMR HSUART RX TIMER Register

Bit	Name	Mode	Default	Description
31:16	-	-	-	Unused
15:0	HSUTTMR	WR	0	HSUART DMA RX TIMER CNT

Register 8-12 HSUT0FCCON: HSUART Flow Control Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused

Bit	Name	Mode	Default	Description
7	RTS_SW	WR	1	Write 0 to pull low RTS(valid),only active in manual mode
6	RTSS	R	0	RTS status
5	CTSS	R	0	CTS status
4	CTSPND	R	0	CTS status changing pending
3	RTS_MODE	WR	0	RTS control mode 0:hardware automatic control mode 1:manual mode enable
2	CTSIE	WR	0	CTS Interrupt Enable 0: CTS interrupt disable 1: CTS interrupt enable
1	URTS_EN	WR	0	RTS flow control enable 0: disable 1: enable
0	UCTS_EN	WR	0	CTS flow control enable 0: disable 1: enable

8.3 User Guide

8.3.1 SYNC configure

1. Configure RX 8/9 bit data mode by **RXBITSEL,HSUTTMREN**,**HSUT0TMR**.
2. Configure TX **TXBITSEL**,**SPBITSEL**
3. Configure **HSUT0BAUD**
4. Configure RXEN,TXEN

8.3.2 TX 1 byte with buffer

1. Configure GPIO in the correct direction.
2. Configure **HSUT0CON** CLKSRC bit for high speed interface working source clock
3. Configure **HSUT0CON** buffer mode ,8/9bit mode, 1/2 stop bit mode
4. Configure**HSUT0BAUD** baud- rate
5. Enable **UTXEN** by setting
6. Configure **TXIE**to1' if needed
7. write data to **HSUT0DATA** to kick start TX
8. Wait for **TXPND** to change to '1', or wait for interrupt
9. Clear Pending

8.3.3 TX n byte with DMA

1. Configure GPIO in the correct direction.
2. Configure **HSUT0CON** CLKSRC bit for high speed interface working source clock

3. Configure **HSUT0CON** DMA mode ,8bit mode, 1/2 stop bit mode
4. Configure**HSUT0BAUD** baud- rate
5. Configure TX DMA start address **HSUT0TXADR**
6. Enable **UTXEN** by setting
7. Configure **TXIE**to1' if needed
8. write data count to **HSUT0TXCNT**to kick start TX
9. Wait for **TXPND** to change to '1', or wait for interrupt
10. Clear Pending

8.3.4 RX 1 byte with buffer

1. Configure GPIO in the correct direction.
2. Configure **HSUT0CON** CLKSRC bit for high speed interface working source clock
3. Configure **HSUT0CON** buffer mode ,8/9bit mode
4. Configure**HSUT0BAUD** baud- rate
5. Enable **URXEN** by setting
6. Configure **RXIE**to1' if needed
7. Wait for **RXPND** to change to '1', or wait for interrupt
8. read data from **HSUT0FIFO**
9. Clear Pending for next rx data

note: if read rx data not in time, data will be covered by next rx done

8.3.5 RX n byte with DMA & loopbuffer disable

1. Configure GPIO in the correct direction.
2. Configure **HSUT0CON** CLKSRC bit for high speed interface working source clock
3. Configure **HSUT0CON** DMA mode ,8bit mode, not loopbuffer mode
4. Configure**HSUT0BAUD** baud- rate
5. Configure RX DMA start address **HSUT0RXDADR**
6. Enable **URXEN** by setting
7. Configure **RXIE**to1' if needed
8. write data count to **HSUT0RXCNT**to kick start RX
9. Wait for **RXPND** to change to '1', or wait for interrupt
10. read RX data from SRAM or **HSUT0RXFIFO**
11. Clear Pending, and will clear **HSUT0FIFOCNT** at the same time

8.3.6 RX n byte with DMA & loopbuffer enable

1. Configure GPIO in the correct direction.
2. Configure **HSUT0CON** CLKSRC bit for high speed interface working source clock
3. Configure **HSUT0CON** DMA mode ,8bit mode, loopbuffer mode
4. Configure**HSUT0BAUD** baud- rate
5. Configure RX DMA address **HSUT0RXADR**
6. ~~write data RX countand FIFO overflow count to **HSUT0RXCNT**~~
7. Enable **URXEN** by setting
8. write data count to **HSUT0RXCNT**to kick start RX
9. Configure **RXIE**to1' if needed
10. Wait for **RXPND** to change to '1', or wait for interrupt, or time to check **HSUT0FIFOCNT**

11. read RX data from SRAM or **HSUT0RXFIFO**
12. Clear Pending, and will not clear **HSUT0FIFOCNT** at the same time
13. write data count to **HSUT0RXCNT**，wait for next RXDONE

Reading from SRAM:

1, get start address from HSUT0FIFOADR or program save variable

2, get data count from HSUT0FIFOCNT or program save variable

3,read N byte data from SRAM

4,if not DMA loopbuffer mode, clear RXPND will clear HSUT0FIFOCNT

5,if DMA loopbuffer mode, write N to SUBRXCNT（HSUT0CPND[16:0]）to dec HSUT0FIFOCNT.

Reading from HSUT0 FIFO

1,get data count from HSUT0FIFOCNT

2,set RXFIFO[8] to 1, and will auto clear RXFIFO[9]

3,wait RXFIFO[9] change to 1

4,get data from RXFIFO[7:0]

5,loop n times from step 2 to 4.

8.3.7 DMA RX TIMER MODE:

DMA RX HSUT0TMR support for all DMA RX mode.

HSUT0TMR Counter enable：

1，set function enable bit

2，write data count to HSUT0RXCNT will pre-enable

3，wait for HSUT0FIFOCNT ! = 0 and counter will be enable

HSUT0TMR Counter increase:

1, TMRCNT increase 1 when RX BUS IDLE for 1 bit baud-rate time

HSUT0TMR clear：

1, TMRCNT clear by RX BUS falling edge

2, TMRCNT clear by DMA RX kick start

3, TMRCNT clear by clear HSTMROV_PND

if HSTMROV_PND setting, HSUT0TMR disable until next DMA RX kick start

8.3.8 Application Note:

1, For loopbuffer mode:

There is keeping save data to SRAM when reading HSUT0RXFIFO. If reading speed slower then RX data rate,

RXFIFO will increase till overflow.

If overflow happened, RXOVPND flag will be set. RX data will only save in internal buffer but not DMA to SRAM. After reading FIFO end, clear RXOVPND will clear HSUT0FIFOCNT at the same time.

2, For DMA fail flag

If RX DMA to SRAM is blocked by other DMA channel for a long time, DMA error will happened. Next Rx data will cover the current data.

3，FLAG set and clear

TXPND：

set：buffer： TX 1 byte finish
DMA： TX n byte finish
clear：buffer： Write HSUT0DATA
DMA： Write HSUT0TXCNT
all mode：write 1 to HSUT0CPND[13]

RXPND:
set：buffer： RX 1 byte done
DMA： RX and WRITE n byte to SRAM finish；
HSUT0TMRCNT enable and TMROV set
RXOV_set
clear：write USHT0CPND[12] or write HSUT0RXCNT

RXOVPND：
set：At DMA loopbuffer mode, RXFIFOCNT reach maximum（MAXFIFOCNT）and try to write data to SRAM.
clear：
disable URXEN
disable DMA mode
disable LOOPBUFFER mode
write 1 to HSUT0CPND[11]

RXFAIL：
set：DMA is writing data to SRAM, but next data had input to update DMA data
clear：
disable URXEN
disable DMA mode
write 1 to HSUT0CPND[14]

TMR_OV：
set：TMRCNT check UTRX BUS IDLE time larger then setting
clear：

disable URXEN

disable DMA mode

disabletmrcnt_en

write 1 to HSUT0CPND[15]

RXDMAEN & write to HSUT0RXCNT

4,FOR HSUT0DADR writing

Writing to HSUT0DASR , will also update these internal address :

FIFO read start address: fiford_adr

RXDMA start address: dmarx_wadr

5,FOR RXOVPND process

It is working at DMA loopbuffer mode.

After RXOVPND was set. It's recommend program process as flow：

1，If data overflow happen，RXPND and RXOVPND setting at the same time

2，Enter RXPND process first，get HSUT0FIFOCNT，and read data from RXFIFO

3，Enter RXOVPND，get HSUT0FIFOCNT，and read data from RXFIFO。

HSUT0FIFOCNT ！= 0 If RXPND setting by received RXCNT byte data

HSUT0FIFOCNT = 0 If RXPND setting by RXOVPND

4，Clear RXOVPND

It will be also clear RXFIFOCNT and initial RXFIFO_ADR to current RXWR_ADR by HSUT0CPND[11].

6,FOR RTS/CTS hardware flow control

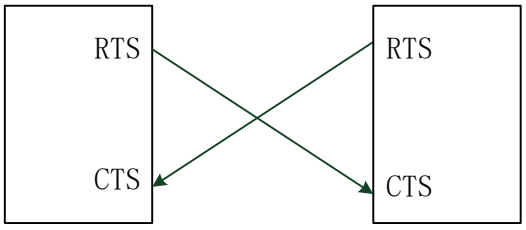
CTS: if CTS_EN = 1 , the sender will check whether CTS is low before sending data each time;

In tx_buffer mode ,when CTS is high and write hsutdata,data will not be sent;but after some time cts's falling edge will trigger the sending of data;after that,if you don't want to send data again,please don't clear tx_done.

In tx_dma mode , during sending data,CTS is pulled high;after CTS is pulled low , the remaing data will be automatically sent .

RTS: if RTS_EN =1 , in rx_buffer mode : RTS is high by default,you can pulldown RTS by sw in manual mode , after receiving 1 byte RTS is pulled high automatically.

In rx_dma mode : after receiving the start bit of the last 1byte of data , RTS will be pulled high. in loop mode ,rts will be pulled low when fifo_rd or clear rxloopbuffer ;in ~loop mode,after reading all the data ,if you write new hsutrxcnt, rts will be pulled low.



9 SPI1

9.1 Features

SPI1 can support different mode

1. general 3 wire mode, 1-bit clock in/out, 1-bit data output, 1-bit data input
2. 2 wire mode, 1-bit clock in/out, 1-bit data output or input;
3. 2 data bus mode, 1-bit clock in/out, 2-bit data output or input;
4. 4 data bus mode, 1-bit clock in/out, 4-bit data output or input;

9.2 SPI1 Special Function Registers

Register 9-1 SPI0CON: SPI Control Register

Bit	Name	Mode	Default	Description
31:17	-	-	-	Unused
16	SPIPND	R	0	SPI pending 0: not finish SPI rx/tx 1: finish SPI rx/tx
15:14	-	-	-	Unused
13	HOLDENSW	WR	0	SPI software hold enable 0: disable 1: enable
12	HOLDENTX	WR	0	SPI hold enable when bt tx 0: disable 1: enable
11	HOLDENRX	WR	0	SPI hold enable when bt rx 0: disable 1: enable
10	SPIOSS	WR	0	SPI sample data is at the same clock edge with output data 0: SPI sample data is at the difference clock edge with output data 1: SPI sample data is at the same clock edge with output data
9	SPIMBEN	WR	0	SPI multiple bit bus enable bit 0: disable 1: enable
8	SPILF_EN	WR	0	SPI LFSR enable bit 0: disable

Bit	Name	Mode	Default	Description
				1: enable
7	SPIIE	WR	0	SPI interrupt enable 0: disable 1: enable
6	SMPS	WR	0	SPI output edge select bit, when SPIOSS = 0, sample data and output data is at different clock edge; when SPIOSS = 1, sample data and output data is at the same clock edge 0: output data at the falling edge; 1: output data at the rising edge;
5	CLKIDS	WR	0	SPI clock state when idle 0: clock stay at 0 1: clock stay at 1
4	RXSEL	WR	0	When in DMA mode or 2-wire mode, configure SPI Receive or Transmit select bit 0: transmit 1: receive
3:2	BUSMODE	WR	0x0	Data bus width select bit 00:3-wire mode; 1bit data in, 1bit data out 01:2-wire mode; 1bit data in/out 10: 2bit bidirectional data bus 11: 4bit bidirectional data bus
1	SPISM	WR	0	Slave mode select bit 0: master mode 1:slave mode
0	SPIEN	WR	0	SPI Enable Bit 0: Disable 1: Enable

Register 9-2 SPI0BAUD: SPI Baud Rate Register

Bit	Name	Mode	Default	Description
31:16	-	-	-	Unused
15:0	SPI0BAUD	W	0	SPI Baud Rate Baud Rate =Fsys clock / (SPI_BAUD+1)

Register 9-3 SPI0CPND: SPI clear pending Register

Bit	Name	Mode	Default	Description
31:17	-	-	-	Unused
16	SPICPND	W	0	Write 1 will clear SPI pending
15:0	-	-	-	Unused

Register 9-4 SPI0BUF: SPI0 receive/send Data Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	SPI0BUF	WR	x	SPI Data Write this register will load the data to transmitter buffer. Read this register will read the data from the receiver buffer..

Register 9-5 SPI0DMACNT: SPI0 DMA counter Register

Bit	Name	Mode	Default	Description
31:11	-	-	-	Unused
10:0	SPI0DMACNT	W	x	SPI DMA byte counter Write this register will kick start spi send/receive data Total number of bytes received / send is SPI0DMACNT

Register 9-6 SPI0DMAADR: SPI0 DMA address Register

Bit	Name	Mode	Default	Description
31:21	-	-	-	Unused
20:0	SPI0DMAADR	W	x	SPI DMA byte address

9.3 User Guide

SPI Normal 1bit-Mode Operation Flow:

1. Set 3-wire mode or 2-wire mode and select the pin map
2. Select RXSEL for Transmit or receive
3. Configure clock frequency
4. Select one of the four timing mode
5. Enable SPI module by setting SPIEN ‘1’
6. Set SPIIE ‘1’ if needed
7. Write data to SPIBUF to kick-start the process
8. Wait for SPIPND to change to ‘1’, or wait for interrupt
9. Read received data from SPIBUF if needed
10. Go to Step 8 to start another process if needed or turn off SPI0by clearing SPIIE and SPIEN

SPI Normal Multi-Bit-Mode Operation Flow:

1. Set data bus width (bus4 or bus 2) and select the pin map

2. Select RXSEL for Transmit or receive
3. Configure clock frequency
4. Select one of the four timing mode
5. Enable SPI module by setting SPIEN ‘1’
6. Set SPIIE ‘1’ if needed
7. Write data to SPIBUF to kick-start the process
8. If data bus width is 2 bit, write SPIBUF twice kick-start the transmission
9. If data bus widths are 4 bit, write SPIBUF four times kick-start the transmission
10. However, when receive data, only need write once to kick-start receive process
11. Wait for SPIPND to change to ‘1’, or wait for interrupt
12. Read received data from SPIBUF if needed
13. Go to Step 8 to start another process if needed or turn off SPI by clearing SPIIE and SPIEN

SPI1 DMA Mode Operation Flow:

1. Set IO in the correct direction and data width mode.
2. Select RXSEL for DMA direction
3. Configure clock frequency
4. Select one of the four timing modes
5. Enable SPI module by setting SPIEN to ‘1’
6. Set SPIIE ‘1’ if needed
7. configure SPI0DMAADR；
8. Write data to SPI0_DMACNT to kick-start a DMA process
9. Wait for SPIPND to change to ‘1’, or wait for interrupt
10. Go to Step 8 to start another DMA process if needed or turn off SPI0 by clearing SPI0EN

10 IIS

10.1 Features

1. Support sample rate 44.1/48 KHz
2. Support out data source from SRC
3. Support out data source from memory DMA
4. Support in data DMA to memory
5. Support IIS master 16/32 bit data mode
6. Support IIS slave mode
7. Support IIS normal mode and left-justified mode
8. Support PCM master mode
9. Support DMA interrupt
10. Support DMA address re-load

10.2 IIS Special Function Registers

Register 10-1 IISCON0: IIS Control Register

Bit	Name	Mode	Default	Description
31	SRC_SEL	WR	0-	SRC_SEL 0:SRC0 1:SRC1
30	WSINV	WR	0	WS_INV 0:NORMAL 1:INV →left_justified mode
29:24	SLVAECNT	R	0	Slave mode bit detect
23	SRC_DATA_IDONE	R	0	0:DATA DON'T COME 1:SRC DATA PULSE COME
22	SRC_MAUL_EN	WR	0	PULSE_POS CHOSE 0:PULSE 1:SRC_MAUL_KS
21	SRC_MAUL_KS	W	0	MAUL KICK START
20:18	Rev.	WR	-	Unused

Bit	Name	Mode	Default	Description
17	DMAIDONE	WR	0	Read: 0: DMA in not done flag 1: DMA in done flag Write: 0: No active 1: Clear DMA in done flag Note: If do AND/ORoperate this register, TMP = IISCON0 & 0XFFFCFFFF first;
16	DMAODONE	WR	0	Read: 0: DMA out not done flag 1: DMA out done flag Write: 0: No active 1: Clear DMA out done flag Note: If do AND/ORoperate this register, TMP = IISCON0 & 0XFFFCFFFF first;
15	DMAIERR	R	0	DMA Ibuffer over write error flag
14	DMAOERR	R	0	DMA Obuffer over write error flag
13	WIREMODE	WR	0	1/2 wire mode control 0: 2 wire mode (iisdi and iisdo) 1: 1 wire mode (iisdi or iisdo)
12	ONEWIRECTL	WR	0	1 wire mode dir control 0: output 1: input
11	PCMMODE	WR	0	PCM master mode enable 0: disable 1: enable
10	DMAOMDEN	WR	0	DMA output request mask delay enable(for system very fast than IIS interface) 0: disable 1: enable
9	IISMCLKOE	WR	0	IIS MCLK clock output enable
8	DMAIINTEN	WR	0	DMA input interrupt enable 0: disable 1: enable
7	DMAOINTEN	WR	0	DMA output interrupt enable 0: disable 1: enable
6	DIEN	WR	0	DMA input enable 0: disable

Bit	Name	Mode	Default	Description
				1: enable
5	DOEN	WR	0	DMA output enable 0: disable 1: enable
4	DODATSEL	WR	0	data output source select 0: data output from SRC 1: data output from memory DMA
3	DATDLYMODE	WR	0	master data mode 0: left-justified mode (data delay 0 clock after WS change) 1: IIS normal mode (data delay 1 clock after WS change)
2	BITMODE	WR	0	IIS bit mode at master function 0:16 bit 1:32 bit
1	IISMODE	WR	0	IIS mode sel 0: master mode 1: slave mode
0	IIS_EN	WR	0	IIS Enable Bit 0: Disable 1: Enable

Register 10-2 IISBAUD: IIS baudrate Register

Bit	Name	Mode	Default	Description
31:15	-	-	-	Unused
11:7	bclkdiv	WR	0	Bclkdivcnt from IIS interface clock
6:0	mclkdiv	WR	0	Mclkdivcnt from IIS interface clock

Master mode baud rate configure

MCLK = F_interface/ (mclkdiv+1)

BCLK = MCLK / (sclkdiv+1)

LRCLK = MCLK / (n+1); n = 16*2 for 16bit mode, n=32*2 for 32 bit mode

Register 10-3 IISDMACNT: IIS DMA Counter Register

Bit	Name	Mode	Default	Description
31:11	-	-	0	Unused
10:0	IISDMACNT	WR	0	DMA word counter

Register 10-4 IISDMAOADR0:IIS DMA Output Address 0 Register

Bit	Name	Mode	Default	Description
31:24	-	-	-	Unused
23:0	IISDMAOADR0	RW	0	Dma output address 0

Register 10-5 IISDMAOADR1:IIS DMA Output Address 1 Register

Bit	Name	Mode	Default	Description
31:24	-	-	-	Unused
23:0	IISDMAOADR1	RW	0	Dma output address 1

Register 10-6 IISDMAIADR0:IIS DMA Input Address 0 Register

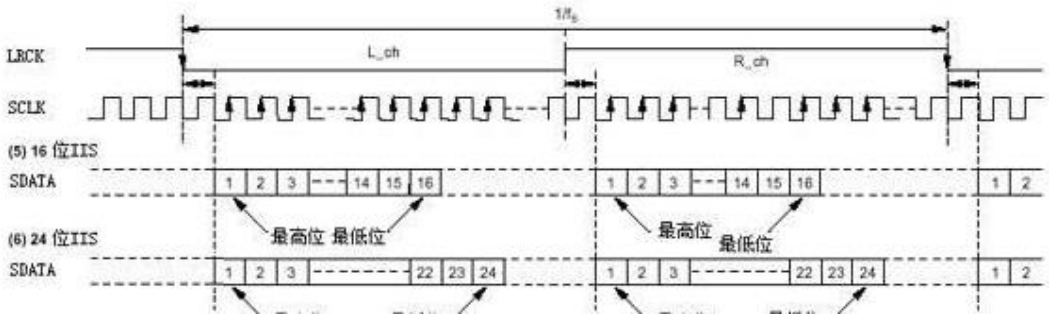
Bit	Name	Mode	Default	Description
31:24	-	-	-	Unused
23:0	IISDMAIADR0	RW	0	Dma input address 0

Register 10-7 IISDMAIADR1:IIS DMA Input Address 1 Register

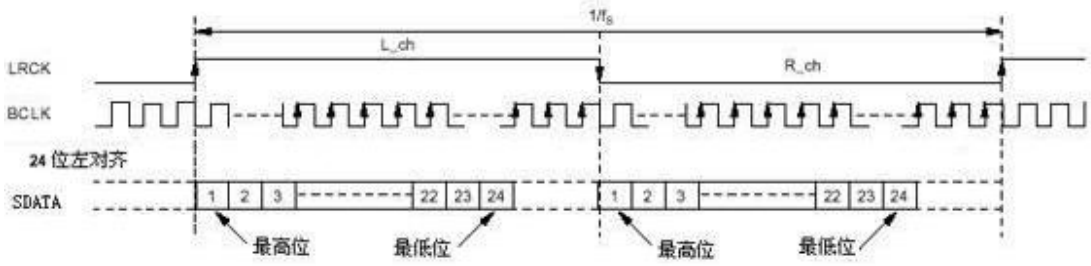
Bit	Name	Mode	Default	Description
31:24	-	-	-	Unused
23:0	IISDMAIADR1	RW	0	Dma input address 1

10.3 User Guide

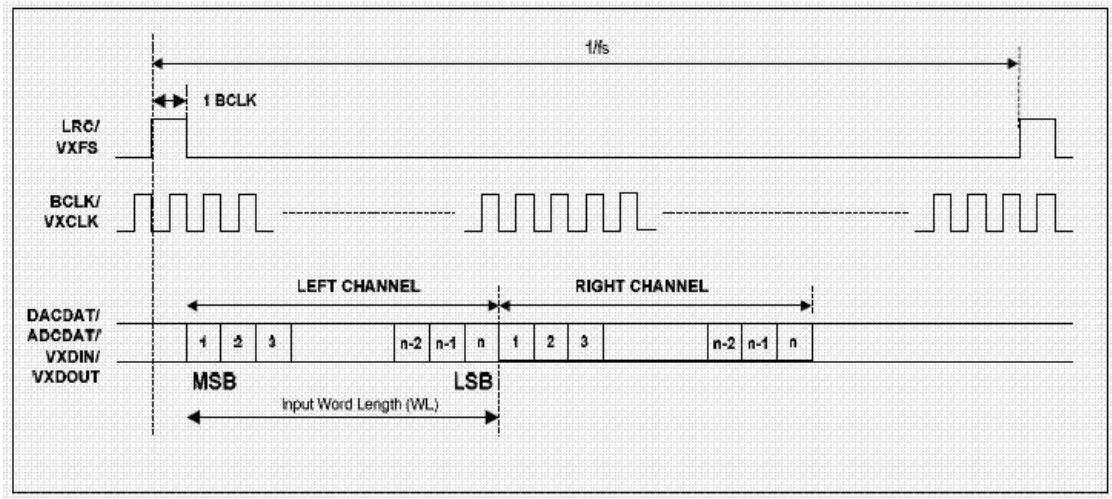
IIS normal mode:



IIS left-justified mode



PCM master mode:



IIS master mode Operation Flow:

1. Configure IO mapping
2. Configure IIS clock select DAC clock, XOSC52M or system pll clock div
3. Configure IIS IISBAUD for MCLK,BCLK clock div
4. Configure data output source from SRC or memory DMA
5. Configure DMACNT, DMAIADR0,DMAIADR1,DMAOADR0,DMAOADR1 if need
6. Configure IISCON0
7. Wait for DMA done flag or interrupt if need
8. Clear DMA DONE flag and update DMAIADR1 or DMAOADR1
9. Loop step 7

IIS slave mode Operation Flow:

1. Configure IO mapping
2. Configure IIS clock select DAC clock, XOSC52M or system pll clock div
3. Configure data output source from memory DMA
4. Configure DMACNT, DMAIADR0,DMAIADR1,DMAOADR0,DMAOADR1 if need

5. Configure IISCON0
6. Wait for DMA done flag or interrupt if need
7. Clear DMA DONE flag and update DMAIADR1 or DMAOADR1
8. Read IISCON0 to get slave data value bitcnt if need
9. Loop step 7

IIS PCM master mode Operation Flow:

1. Configure IO mapping
2. Configure IIS clock select DAC clock, XOSC52M or system pll clock div
3. Configure data output source from memory DMA
4. Configure DMACNT, DMAIADR0,DMAIADR1,DMAOADR0,DMAOADR1 if need
5. Configure IISCON0 for master mode, output IIS normal mode, 16 bit data mode
6. Wait for DMA done flag or interrupt if need
7. Clear DMA DONE flag and update DMAIADR1 or DMAOADR1
8. Loop step 7

DMA address reloads Operation guide:

1. Prepare data in buffer
2. Before kick start, configure buffer 0 to DMAADR 0, configure buffer1 to DMAADR 1
3. Kick start
4. Wait DMA pending and DMAADR1 will be auto load to DMAADR0
5. Configure next data buffer address to DMAADR1 when data ready
6. Loop to step4

11 IIC

11.1 Features

1. Support IIC one master;
2. Support asynchronous clock source from RC2M or XOSC26M;
3. Support out data maximum 4 Byte;
4. Support in data maximum 4 Byte;
5. Support IIC done interrupt

11.2 IIC Special Function Registers

Register 11-1 IICON0: IIC Control Register

Bit	Name	Mode	Default	Description
31	DONE	R	0	IIC DONE flag
30	ACKSTATUS	R	0	RX IIC slave ACK status 0: RX ACK 1: RX NAK
29	CLR_DONE	W	0	DONE flag clear 0: 1: clear
28	KS	W	0	Kick start 0: 1: Kick start
27	CLR_ALL	W	0	Clear All status 0: 1: clear
26	ERR_PND	R	0	IIC SCL force low timeout flag
26:15	Rev.	WR	-	Unused
14	RX_NACK_EN	WR	0	Send NACK to the master device in slave mode 1: Enable 0: Disable
13	SMP_SEL	WR	0	Data sample edge selection in slave mode 1: Rising 0: Falling
12	MDOE	WR	0	IIC controller work mode select

Bit	Name	Mode	Default	Description
				1: Slave 0: Master
11	WR	-	Unused	Rev.
10	WSCL_OPT	WR	0	IIC wait SCL release from slave option 0: disable 1: enable
9:4	POSDIV	WR	0	IIC SCL pose div counter 0: div 1 1: div2 … N: div N+1
3:2	HOLDCNT	WR	0	SDA hold cnt when SCL failing 0: 1 cycle 1: 2 cycle …
1	INTEN	WR	0	IIC interrupt 0: disable 1: enable
0	IIC_EN	WR	0	IIC Enable Bit 0: Disable 1: Enable

Register 11-2 IICON1: IIC Control Register

Bit	Name	Mode	Default	Description
31:13	-	-	-	Unused
12	TXNAK_EN	WR	0	IIC TX NAK when read last data enable
11	STOP_EN	WR	0	IIC TX STOP enable
10	WDAT_EN	WR	0	IIC TX DATA enable
9	RDAT_EN	WR	0	IIC RX data enable
8	CTL1_EN	WR	0	IIC TX ctl 1 enable
7	START1_EN	WR	0	IIC TX start 1 enable
6	ADR1_EN	WR	0	IIC TX adr 1 enable
5	ADR0_EN	WR	0	IIC TX adr 0 enable
4	CTL0_EN	WR	0	IIC TX ctl 0 enable

Bit	Name	Mode	Default	Description
3	START0_EN	WR	0	IIC TX start 0 enable
2:0	DATA_CNT	WR	0	RX/TX data counter 0: 0 byte 1: 1 byte … N: N byte

Master mode baud rate configure
IICCLK = source clk / (preclkdiv+1)
SCL = IICCLK / (posdiv+1)

Register 11-3 IICCMDA: IIC CMD/ADR Register

Bit	Name	Mode	Default	Description
31:24	CTL1	WR	0	Control 1 data
23:16	ADR1	WR	0	Address 1 data
15:8	ADR0	WR	0	Address 0 data
7:0	CTL0	WR	0	Control 0 data

Register 11-4 IICDATA: IIC DATA Register

Bit	Name	Mode	Default	Description
31:24	DATA3	WR	0	Data 3
23:16	DATA2	WR	0	Data 2
15:8	DATA1	WR	0	Data 1
7:0	DATA0	WR	0	Data 0

Register 11-5 IICDMAADR: IIC DMA ADDRESS Register

Bit	Name	Mode	Default	Description
31:2	DMAADR	WR	0	Dma base address
1:0	-	-	-	unused

Register 11-6 IICDMACNT: IIC DMA ADDRESS Register

Bit	Name	Mode	Default	Description
31:16	DMACNT	WR	0	Dma byte length
15:3	-	-	-	unused
2	DMA_DONE	R	0	Dma Done Status

Bit	Name	Mode	Default	Description
1	DMA_RD_EN	WR	0	DMA Read From Memory Enable Bit 0: Disable 1: Enable
0	DMA_EN	WR	0	DMA Enable Bit 0: Disable 1: Enable

Register 11-7 IICSSTS: IIC Slave Status Register (Valid only in slave mode)

Bit	Name	Mode	Default	Description
31:21	Rev.	-	-	Reserved
20	STOP_CLR	W	0	Write 1 to clear the STOP flag.
19	RESTART_CLR	W	0	Write 1 to clear the RESTART flag.
18	START_CLR	W	0	Write 1 to clear the START flag.
17	TXVLD_SET	W	0	Write 1 to set TXVLD flag
16	RXVLD_SET	W	0	Write 1 to set RXVLD flag
15:11	Rev.	-	-	Reserved
10:8	DATA_CNT_R	R	0X0	read-only RX/TX data counter 0: byte 1: 1byte … N: N byte
7	Rev	-	-	Reserved
6	STX	R	0	Controller in slave transfer mode.
5	SRX	R	0	Controller in slave receiver mode.
4	STOP	R	0	Master send a STOP sign.
3	RESTART	R	0	Master send a RESTART sign and matched address
2	START	R	0	Master start a START sign and matched address
1	TXVLD	R	0	4-byte data register full flag In slave transfer mode, software set this bit to start work.
0	RXVLD	R	1	4-byte data register empty flag In slave receiver mode, software set this bit to start work.

11.3 User Guide

IIS master mode Operation Flow:

1. Configure IO mapping, SDA set pullup enable
2. Configure IIC clock select from RC 2M or XOSC 26M, set pre_div clock
3. Configure IIC IICCON0
4. Configure IICCMDA for control byte and address byte
5. Configure IICDATA for WRITE data
6. Configure IICCON1
7. Kick start
8. Wait done flag or interrupt if need
9. Clear DMA DONE flag and update IICCMDA or IICDATA
10. Loop step 7

12 IR receiver

12.1 IR RX Special Function Registers

Register 12-1 IRRXCON: IR RX Control Register

Bit	Name	Mode	Default	Description
31:18	-	-	-	Unused
17	KEYRELS	R	0	IR key release pending 0: not release 1: key release pending
16	RXPND	R	0	IR RX data finish pending 0: not finish 1: finish
15:5	-	-	-	Unused
4	IRWKEN	WR	0	IR RX wake up sleep mode enable 0: disable 1: enable
3	IR32KSEL	WR	0	IR RX 32K configure select 0: 1M clock select 1: 32K clock select
2	IRRXSEL	WR	0	IR RX data select 0: 32bit data 1: 16bit data
1	IRIE	WR	0	IR RX interrupt enable 0: disable 1: enable
0	IREN	WR	0	IR RX enable 0: disable 1: enable

Register 12-2 IRRXCPND: IRRX clear pending Register

Bit	Name	Mode	Default	Description
31:18	-	-	-	Unused
17	CRELSPND	W	0	Clear key release pending 0: no affect 1: clear pending
16	CRXPND	W	0	Clear RX finish pending 0: no affect

Bit	Name	Mode	Default	Description
				1: clear pending
15:0	-	-	-	Unused

Register 12-3 IRRXDAT: IRRX data Register

Bit	Name	Mode	Default	Description
31:0	RXDAT	R	0	IR RX data

Register 12-4 IRRXPR0: IR RX period configure Register0

Bit	Name	Mode	Default	Description
31	-	-	-	Unused
30:16	RPTPR	W	0x2bf1	IR repeat time period = (RPTPR + 1) * (1M or 32K)
15	-	-	-	Unused
14:0	DATPR	W	0x34bb	IR data time period = (DATPR + 1) * (1M or 32K)

Register 12-5 IRRXPR1: IR RX period configure Register1

Bit	Name	Mode	Default	Description
31	-	-	-	Unused
30:16	ONERR	W	0x8c9	IR data 1 time period = (ONEPR + 1) * (1M or 32K)
15	-	-	-	Unused
14:0	ZERORR	W	0x45f	IR data 0 time period = (ZEROPR + 1) * (1M or 32K)

Register 12-6 IRRXERR0: IR RX error configure Register0

Bit	Name	Mode	Default	Description
31:28	-	-	-	Unused
27:16	RPTERR	W	0x0	IR repeat time error = (RPTERR + 1) * (1M or 32K)
15:12	-	-	-	Unused
11:0	DATERR	W	0x0	IR data time error = (DATERR + 1) * (1M or 32K)

Register 12-7 IRRXERR1: IR RX error configure Register1

Bit	Name	Mode	Default	Description
31:20	TOPR	W	0x0	IR time out length = (TOPR + 1) * 64 * (1M or 32K)
19:10	ONEERR	W	0x0	IR data 1 time error = (ONEERR + 1) * (1M or 32K)
9:0	ZEROERR	W	0x0	IR data 0 time error = (ZEROERR + 1) * (1M or 32K)

12.2 User Guide

1. Set IR RX bit select
2. Enable IR RX
3. Wait for pending or interrupt
4. Read IRRXDAT or detect RPTPND

13 Touch Key

13.1 Special Function Registers

Register 13-1 TKIE: Touch Key interrupt Control Register

Bit	Name	Mode	Default	Description
31	TKTPCHPND	R	0	Touch key temperature channel pending 0: no pending 1: touch key temperature channel pending When this pending is set, temperature channel tk_cnt is larger or less than rbase_cnt
30	TKVPND	R	0	Touch key variance pending 0: no touch key variance pending 1: touch key variance pending
29	PTOPND	R	0	Touch key press timeout exception pending 0: no press timeout exception pending 1:press timeout exception pending
28	TELPND	R	0	Touch ear larger exception pending 0: no touch ear larger exception pending 1: touch ear larger exception pending
27	TESPND	R	0	Touch ear smaller exception pending 0: no touch ear smaller exception pending 1: touch ear smaller exception pending
26	TEBCNTPND	R	0	Touch ear bcnt valid pending 0: no touch ear bcnt valid pending 1: touch ear bcnt valid pending
25	TESTA	R	0	Touch ear state pending 0: no touch ear press pending 1: touch ear press state pending
24	TKTOPND	R	0	Touch key variance timeout exception pending 0: no touch key variance timeout exception pending

Bit	Name	Mode	Default	Description
				1: touch key variance timeout exception pending
23	TKRPND	R	0	Touch key in range exception pending 0: no touch key in range exception pending 1: touch key in range exception pending
22	TKLPND	R	0	Touch key larger exception pending 0: no touch key larger exception pending 1: touch key larger exception pending
21	TKSPND	R	0	Touch key smaller exception pending 0: no touch key smaller exception pending 1: touch key smaller exception pending
20	TKBCNTPND	R	0	Touch key bcnt valid pending 0: no touch key bcnt valid pending 1: touch key bcnt valid pending
19	TKSTA	R	0	Touch key state pending 0: no touch key press pending 1: touch key press state pending
18	TKERRPND	R	0	Touch key error pending 0: no touch key error pending 1: touch key error pending When this pending is set, should check configure; if tkcdpr time is longer than tkdlypr, this pending will be set
17	TKOVPND	R	0	Touch key counter overflow pending 0: no touch key overflow pending 1: touch key overflow pending When this pending is set, should decrease tkcdpr
16	TKPND	R	0	Touch key timer pending 0: no touch key timer pending 1: touch key timer pending
15	TKTPCHPNDIE	WR	0	Touch key temperature channel pending interrupt enable 0: disable

Bit	Name	Mode	Default	Description
				1: enable
14	TKVPNDIE	WR	0	Touch key variance interrupt enable 0: disable 1: enable
13	PTOPNDIE	WR	0	Touch key press timeout exception pending interrupt enable 0: disable 1: enable
12	TELPNDIE	WR	0	Touch ear larger exception pending interrupt enable 0: disable 1: enable
11	TESPNDIE	WR	0	Touch ear smaller exception pending interrupt enable 0: disable 1: enable
10	TEBCNTPNDIE	WR	0	Touch ear bcnt valid pending interrupt enable 0: disable 1: enable
9	TESTAIE	WR	0	Touch ear state pending interrupt enable 0: disable 1: enable
8	TKTOPNDIE	WR	0	Touch key variance timeout exception pending interrupt enable 0: disable 1: enable
7	TKRPNDIE	WR	0	Touch key in range exception pending interrupt enable 0: disable 1: enable
6	TKLPNDIE	WR	0	Touch key larger exception pending interrupt enable 0: disable 1: enable
5	TKSPNDIE	WR	0	Touch key smaller exception pending interrupt enable

Bit	Name	Mode	Default	Description
				0: disable 1: enable
4	TKBCNTPNDIE	WR	0	Touch key bcnt valid pending interrupt enable 0: disable 1: enable
3	TKSTAIE	WR	0	Touch key state pending interrupt enable 0: disable 1: enable
2	TKERRPNDIE	WR	0	Touch key error pending interrupt enable 0: disable 1: enable
1	TKOVPNDIE	WR	0	Touch key counter overflow pending interrupt enable 0: disable 1: enable
0	TKPNDIE	WR	0	Touch key pending interrupt enable 0: disable 1: enable

Register 13-2 TKCPND: Touch key clear pending Register

Bit	Name	Mode	Default	Description
31	CTKTPCHPND	W	0	Write 1 will clear TKTPCHPND pending
30	CTKVPND	W	0	Write 1 will clear touch key variance pending
29:28	-	-	-	Unused
27	CTEEPND	W	0	Write 1 will clear touch ear exception pending, include TESPND, TELPND, TERPND
26	CTEBPND	W	0	Write 1 will clear touch ear bcnt valid pending
25	CTESTA	W	0	Write 1 will clear touch ear state pending
24:22	-	-	-	Unused

Bit	Name	Mode	Default	Description
21	CTKEPND	W	0	Write 1 will clear touch key exception pending, include TKSPND, TKLPND, TKRPND, TKTOPND
20	CTKBPND	W	0	Write 1 will clear touch key bcnt valid pending
19	CTKSTA	W	0	Write 1 will clear touch key state pending
18:17	-	-	-	-
16	CTKPND	W	0	Write 1 will clear touch key pending
15:0	-	-	-	Unused

Register 13-3 TKCON: Touch key control Register

Bit	Name	Mode	Default	Description
31	TERUPDBEN	WR	0	Touch ear range pending update base_cnt enable 0: disable 1: enable
30	TELUPDBEN	WR	0	Touch ear large pending update base_cnt enable 0: disable 1: enable
29	TESUPDBEN	WR	0	Touch ear small pending update base_cnt enable 0: disable 1: enable
28	TEBCNTVAL	WR	0	Touch ear base_cnt valid bit 0:invalid 1: valid
27	TKBCNTVAL	WR	0	Touch key base_cnt valid bit 0:invalid 1: valid
26	TKTOUPDBEN	WR	0	Touch key variance timeout pending update base_cnt enable 0: disable 1: enable

Bit	Name	Mode	Default	Description
25	TKRUPDBEN	WR	0	Touch key range pending update base_cnt enable 0: disable 1: enable
24	TKLUPDBEN	WR	0	Touch key large pending update base_cnt enable 0: disable 1: enable
23	TKSUPDBEN	WR	0	Touch key small pending update base_cnt enable 0: disable 1: enable
22	TESTAWKEN	WR	0	Touch ear state wakeup enable 0: disable 1: enable
21	TKSTAWKEN	WR	0	Touch key state wakeup enable 0: disable 1: enable
20	TKPNDWKEN	WR	0	Touch key pending wakeup enable 0: disable 1: enable
19	TKPTOUPDBEN	WR	0	Touch key press timeout pending update base_cnt enable 0: disable 1: enable
18	-	-	-	-
17	TEBCNTVALSEL	WR	0	Touch ear bcnt valid hardware clear enable 0: disable 1: enable
16	TKBCNTVALSEL	WR	0	Touch key bcnt valid hardware clear enable 0: disable 1: enable
15	TKRST_DIS	WR	0	Touch key analog reset disable bit

Bit	Name	Mode	Default	Description
				0: Touch key analog hardware reset 1: Touch key disable reset
14	TKAEN_ATSEL	WR	0	Touch key analog hardware auto enable select bit 0: touch key analog should enable all the time 1: hardware auto enables when touch key is used
13	TKAEN_SW	WR	0	Touch key analog enable when TKAEN_ATSEL = 0 0: disable 1: enable
12	DIV2SEL	WR	0	TK clock source divide 2 select 0: no divide 2 1: divide 2
11	TKCEN	WR	0	Touch key clock enable 0: disable 1: enable
10	TKVEN	WR	0	Touch key variance enable 0: disable 1: enable
9	TKTPCHCHKEN	WR	0	Touch key temperature channel check enable 0: disable 1: enable
8	TEEN	WR	0	Touch ear enable 0: disable 1: enable
7:5	TKSEL	WR	0x0	Touch key pin select 000: select TK0 001: select TK1 010: select TK2 011: select TK3 100: select TK4
4:2	TESEL	WR	0x0	Touch ear pin select

Bit	Name	Mode	Default	Description
				000: select TK0 001: select TK1 010: select TK2 011: select TK3 100: select TK4
1	BCNTSEL	WR	0	Touch key or touch ear new base_cnt select bit 0: select base_cnt + 1/2 * delta as new base_cnt 1: select TCNT as new base_cnt
0	TKEN	WR	0	Touch key enable 0: disable 1: enable

Register 13-4 TKCON1: Touch key control Register 1

Bit	Name	Mode	Default	Description
31:24	TK_PWUP	WR	0x00	Touch key analog setup time
23:22	-	-	-	-
21:16	TKCHPND	WR	0x00	TK channel 5 to 0 pending
15:14	-	-	-	-
13:8	TKCHPND_EN	WR	0x00	TK channel 5 to 0 pending enable bit; when enable, then channel pending will set 0:disable 1:enable
7:6	-	-	-	-
5:0	TKCH	WR	0x00	TK channel 5 to 0 enable bit select 0:disable 1:enable

Register 13-5 TKCON2: Touch key control Register 2

Bit	Name	Mode	Default	Description
31:28	TO_BCNT_THD	WR	0x0	Time out base counter threshold

Bit	Name	Mode	Default	Description
27:16	RELS_VARI_THD	WR	0x0	Release variance threshold
15:4	PRESS_VARI_THD	WR	0x0	Press variance threshold
3	RELS_FIL_SEL	WR	0	Release variance after filter 0: before filter 1: after filter
2	PRESS_FIL_SEL	WR	0	Press variance after filter 0: before filter 1: after filter
1	RELS_VARI_EN	WR	0	Release variance enable bit 0: disable 1: enable
0	PRESS_VARI_EN	WR	0	Press variance enable bit 0: disable 1: enable

Register 13-6 TKACON0: Touch key analog control Register 0

Bit	Name	Mode	Default	Description
31:30	-	-	-	unused
29:25	TK5_ITRIM	WR	0x4	Touch key channel5 ITRIM select
24:20	TK4_ITRIM	WR	0x4	Touch key channel4 ITRIM select
19:15	TK3_ITRIM	WR	0x4	Touch key channel3 ITRIM select
14:10	TK2_ITRIM	WR	0x4	Touch key channel2 ITRIM select
9:5	TK1_ITRIM	WR	0x4	Touch key channel1 ITRIM select
4:0	TK0_ITRIM	WR	0x4	Touch key channel0 ITRIM select

Register 13-7 TKACON1: Touch key analog control Register 1

Bit	Name	Mode	Default	Description
31:15	-	-	-	-

Bit	Name	Mode	Default	Description
14:10	TK5_CTRIM	WR	0x0	Touch key channel0 CTRIM select
9:8	TK4_CTRIM	WR	0x0	Touch key channel0 CTRIM select
7:6	TK3_CTRIM	WR	0x0	Touch key channel0 CTRIM select
5:4	TK2_CTRIM	WR	0x0	Touch key channel0 CTRIM select
3:2	TK1_CTRIM	WR	0x0	Touch key channel0 CTRIM select
1:0	TK0_CTRIM	WR	0x0	Touch key channel0 CTRIM select

Register 13-8 TK0CNT/TK1CNT/TK2CNT/TK3CNT/TK4CNT/TK5CNT: Touch key channel0/1/2/3/4/5 counter Register

Bit	Name	Mode	Default	Description
31:16	-	-	-	unused
15:0	TKxCNT	R	0x0	Touch key channel 0/1/2/3/4/5 counter

Register 13-9 TKCDPR0: Touch key charge and discharge period Register 0

Bit	Name	Mode	Default	Description
31	-	-	-	unused
30:16	TK1CDPR	W	0x0	Touch key channel 1 charge and discharge period (TKCDPR+1)
15	-	-	-	unused
14:0	TK0CDPR	W	0x0	Touch key channel 0 charge and discharge period (TKCDPR+1)

Register 13-10 TKCDPR1: Touch key charge and discharge period Register 1

Bit	Name	Mode	Default	Description
31	-	-	-	unused
30:16	TK3CDPR	W	0x0	Touch key channel 3 charge and discharge period (TKCDPR+1)
15	-	-	-	unused

Bit	Name	Mode	Default	Description
14:0	TK2CDPR	W	0x0	Touch key channel 2 charge and discharge period (TKCDPR+1)

Register 13-11 TKCDPR2: Touch key charge and discharge period Register 2

Bit	Name	Mode	Default	Description
31	-	-	-	unused
30:16	TK5CDPR	W	0x0	Touch key channel 5 charge and discharge period (TKCDPR+1)
15	-	-	-	unused
14:0	TK4CDPR	W	0x0	Touch key channel 4 charge and discharge period (TKCDPR+1)

Register 13-12 TKDLYPR: Touch key channel time period Register

Bit	Name	Mode	Default	Description
31:30	DLYLPR	WR	0x0	All channel long time period, high two bit, for shut down
29:25	TK5DLYPR	W	0x1f	Touch key channel 5 time period, TK5DLYPR
24:20	TK4DLYPR	W	0x1f	Touch key channel 4 time period, TK4DLYPR
19:15	TK3DLYPR	W	0x1f	Touch key channel 3 time period, TK3DLYPR
14:10	TK2DLYPR	W	0x1f	Touch key channel 2 time period, TK2DLYPR
9:5	TK1DLYPR	W	0x1f	Touch key channel 1 time period, TK1DLYPR
4:0	TK0DLYPR	W	0x1f	Touch key channel 0 time period, TK0DLYPR

Register 13-13 TKTMR: Touch key times Register

Bit	Name	Mode	Default	Description
31:20	TO_EXCEPT	W	0x0	Touch key variance time out length
19:16	FIL_VAL	W	0x0	Touch key base_cnt valid filter length, EAR_FIL_VAL+1
15:8	FIL_EXCEPT	W	0x0	Touch key state exception filter length, FIL_EXCEPT+1

Bit	Name	Mode	Default	Description
7:4	FIL_HIGH	W	0x0	Touch key state high state filter length, FIL_HIGH+1
3:0	FIL_LOW	W	0x0	Touch key state low state filter length, FIL_LOW+1

Register 13-14 TKBCNT: Touch key base counter Register

Bit	Name	Mode	Default	Description
31:16	TKBCNT_AVG	R	0x0	Touch key base counter average value
15:0	TKBCNT	WR	0x0	Touch key base counter

Register 13-15 TKPTHD: Touch key press threshold Register

Bit	Name	Mode	Default	Description
31:28	PTO_EXCEPT	W	0x0	Touch key press time out length. Bit11~bit8
27:14	TKRTHD	W	0x0	Touch key release threshold
13:0	TKPTHD	W	0x0	Touch key press threshold

Register 13-16 TKETHD: Touch key exception threshold Register

Bit	Name	Mode	Default	Description
31:28	-	-	-	unused
27:14	TKLTHD	W	0x0	Touch key larger threshold
13:0	TKSTHD	W	0x0	Touch key smaller threshold

Register 13-17 TETMR: Touch ear times Register

Bit	Name	Mode	Default	Description
31:20	-	-	-	unused
19:16	EAR_FIL_VAL	W	0x0	Touch ear base_cnt valid filter length, EAR_FIL_VAL+1
15:8	EAR_FIL_EXCEPT	W	0x0	Touch ear state exception filter length, EAR_FIL_EXCEPT+1
7:4	EAR_FIL_HIGH	W	0x0	Touch ear state high state filter length, EAR_FIL_HIGH+1
3:0	EAR_FIL_LOW	W	0x0	Touch ear state low state filter length, EAR_FIL_LOW+1

Register 13-18 TEBCNT: Touch ear base counter Register

Bit	Name	Mode	Default	Description
31:16	TEBCNT_AVG	R	0x0	Touch ear base counter or delta when exception happen; When TEBCNT_AVG is delta value, BIT23 is signed bit, delta should be enlarge when read
15:0	TEBCNT	WR	0x0	Touch ear base counter

Register 13-19 TEPTHD: Touch ear press threshold Register

Bit	Name	Mode	Default	Description
31:28	-	-	-	-
27:14	TERTHD	W	0x0	Touch ear release threshold
13:0	TEPTHD	W	0x0	Touch ear press threshold

Register 13-20 TEETHD: Touch ear exception threshold Register

Bit	Name	Mode	Default	Description
31:28	-	-	-	unused
27:14	TELTHD	W	0x0	Touch ear larger threshold
13:0	TESTHD	W	0x0	Touch ear smaller threshold

Register 13-21 TKVARI: Touch key variance Register

Bit	Name	Mode	Default	Description
31:16	TKVARI	R	0x0	Touch key variance
15:0	TKVTHD	WR	0x0	Touch key variance threshold

Register 13-22 TKVARITHD: Touch key variance threshold Register

Bit	Name	Mode	Default	Description
31:24	TKVFIL	WR	0x0	Touch key variance filter count
23:18	TKBADD	WR	0x0	Touch key base counter adder value
17:12	TKAETHD	WR	0x0	Touch key average equal threshold
11:0	TKARTHD	WR	0x0	Touch key average range threshold

Register 13-22 TKVARIRP: Touch key press variance Register

Bit	Name	Mode	Default	Description
31:16	-	-	-	-
15:0	TKVARIRP	R	0x0	Touch key press variance

Register 13-23 TKRBCNT: Touch key rbase counter Register

Bit	Name	Mode	Default	Description
31:16	-	-	-	-
23:8	RBASECNT	WR	0x0	Touch key channel 5 temperature change rbase counter
7:0	RBASETHD	WR	0x0	Touch key channel 5 temperature change rbase counter threshold

14 SDADC

14.1 Features

1. 5ch mode: support 5 channels 24bits ADC,FSOUT<=48K
2. 7ch mode: support 5 channels 24bits ADC + 2 channels ANC_OUT downsample data path, FSOUT<=32K
3. DMA support stereo/mono,24bits/16bits mode

14.2 SDADC Special Function Registers

Register 14-1 SDADCCON: SDADC Control Register

Bit	Name	Mode	Default	Description
31:13	-	-	-	Reserve
12	ANC1_DS_EN	W/R	0	ANC1 data down sample adc enable 0: disable 1: enable
11	ANC0_DS_EN	W/R	0	ANC0 data down sample adc enable 0: disable 1: enable
10	ADC4_ADC_DS_EN	W/R	0	ADC4 channel adc path enable 0: disable 1: enable
9	ADC3_ANC_DS_EN	W/R	0	ADC3 channel anc path enable 0: disable 1: enable
8	ADC3_ADC_DS_EN	W/R	0	ADC3 channel adc path enable 0: disable 1: enable
7	ADC2_ANC_DS_EN	W/R	0	ADC2 channel anc path enable 0: disable 1: enable
6	ADC2_ADC_DS_EN	W/R	0	ADC2 channel adc path enable 0: disable 1: enable
5	ADC1_ANC_DS_EN	W/R	0	ADC1 channel anc path enable 0: disable 1: enable
4	ADC1_ADC_DS_EN	W/R	0	ADC1 channel adc path enable 0: disable 1: enable
3	ADC0_ANC_DS_EN	W/R	0	ADC0 channel anc path enable 0: disable 1: enable
2	ADC0_ADC_DS_EN	W/R	0	ADC0 channel adc path enable 0: disable 1: enable

Bit	Name	Mode	Default	Description
1	ADC_7CH_EN	W/R	0	support 7 channels enable 0: 5 ch, each ch's fsout max 48K 1: 7 ch, each ch's fsout max 32K
0	ADC_TOTAL_EN	W/R	0	SDADC enable 0: disable 1: enable

Register 14-2 SDADC0CON/SDADC1CON/SDADC2CON/SDADC3CON/SDADC4CON

Bit	Name	Mode	Default	Description
31:22	-	-	-	Reserve
21	ADC_N6DB_EN	W/R	0	ADC bits-stream -6dB enable 0: disable 1: enable
20:17	ADC_BITS_SEL	W/R	0	ADC bits-stream select 0: itself ch bits-stream 1: MIC0 bits-stream 2: MIC1 bits-stream 3: MIC2 bits-stream 4: MIC3 bits-stream 5: MIC4 bits-stream 6: DACL speaker signal 7: DACR speaker siganl
16	ADC_SP_SEL	W/R	0	ADC sample clk edge select 0: posedge 1: negedge
15:11	-	-	-	Reserve
10:9	ANC_CIC_ORDER	W/R	0	ANC cic order select 0: 3 order 1: 4 order 2: 2 order
8	ANC_FSOUT_SEL	W/R	0	ANC output samplerate select 0: 192K 1: 384K
7:6	-	-	-	Reserve
5:4	ADC_CIC_ORDER	W/R	0	ADC cic order select 0: 3 order 1: 4 order 2: 2 order
3:0	ADC_FSOUT_SEL	W/R	0	ADC output samplerate select 0: 48K 1: 32K

Bit	Name	Mode	Default	Description
				2: 24K 3: 16K 4: 12K 5: 8K 6: 96K(only support 3 channels) 7: 192K(nonsupport digital GAIN) 8: 384K(nonsupport digital GAIN)

Register 14-3 SDADC0RMDCCON/SDADC1RMDCCON/SDADC2RMDCCON/SDADC3RMDCCON /SDADC4RMDCCON

Bit	Name	Mode	Default	Description
31:8	SW_DC	W	0	software dc offset
31:8	GETDC_OUT	R	0	hardware getdc value
7	GETDC_FLAG	R	0	getdc flag 0: getdc not done 1: getdc done
6	GETDC_EN	W/R	0	get dc offset enable 0: disbale 1: enable
5	SW_DC_EN	W/R	0	software dc offset enable 0: disbale 1: enable
4:2	RMDC_SEL	W/R	0	remove dc offset highpass filter config,Fc at ~0dB,settling time rmdc_bits= 0: 18，Fc = 5.269Hz，Time = 213ms 1: 13，Fc = 168.6Hz，Time = 6.7ms 2: 15，Fc = 42.15Hz，Time = 26.7ms 3: 16，Fc = 21.07Hz，Time = 53.3ms 4: 17，Fc = 10.53Hz，Time = 106.7ms 5: 19，Fc = 2.634Hz，Time = 426.7ms 6: 20，Fc = 1.317Hz，Time = 853.3ms 7: 21，Fc = 0.658Hz，Time = 1706ms
1	RMDC_ORDER	W/R	0	rmdc filter order select 0: 1 order RC filter 1: 2 order RC filter
0	RMDC_EN	W/R	0	adc remove dc offset enable 0: disbale 1: enable

Register 14-4 SDADC0GAIN/SDADC1GAIN/SDADC2GAIN/SDADC3GAIN/SDADC4GAIN

Bit	Name	Mode	Default	Description

Bit	Name	Mode	Default	Description
31:16	ANC_GAIN	W/R	0x400	ANC path digital GAIN gain = 20log10(ANC_GAIN/2^10)
15:0	ADC_GAIN	W/R	0x400	ADC path digital GAIN gain = 20log10(ADC_GAIN/2^10)

Register 14-5 ANCDSCON

Bit	Name	Mode	Default	Description
31:26	-	-	-	Reserve
25:22	ANC0_DS_SEL	W/R	0	ANC0 down sample datain select 0: ADC0_ANC_DOUT 1: ADC1_ANC_DOUT 2: ADC2_ANC_DOUT 3: ADC3_ANC_DOUT 4: DACL_MUSIC 5: DACR_MUSIC 6: ANC0_FF_DOUT 7: ANC0_FB_DOUT 8: ANC1_FF_DOUT 9: ANC1_FB_DOUT 10: DACL speaker signal 11: DACR speaker siganl
21:20	ANC1_CIC_ORDER	W/R	0	ANC1 down sample cic order select 0: 3 order 1: 4 order 2: 2 order
19:17	ANC1_FSOUT_SEL	W/R	0	ANC1 down sample path output samplerate select 0: 32K 1: 32K 2: 24K 3: 16K 4: 12K 5: 8K
16	ANC1_IN_384K_EN	W/R	0	ANC1 down sample path input samplerate select 0: 192K 1: 384K
15:10	-	-	-	Reserve
9:6	ANC0_DS_SEL	W/R	0	ANC0 down sample datain select 0: ADC0_ANC_DOUT 1: ADC1_ANC_DOUT 2: ADC2_ANC_DOUT

Bit	Name	Mode	Default	Description
				3: ADC3_ANC_DOUT 4: DACL_MUSIC 5: DACR_MUSIC 6: ANC0_FF_DOUT 7: ANC0_FB_DOUT 8: ANC1_FF_DOUT 9: ANC1_FB_DOUT 10: DACL speaker signal 11: DACR speaker siganl
5:4	ANC0_CIC_ORDER	W/R	0	ANC0 down sample cic order select 0: 3 order 1: 4 order 2: 2 order
3:1	ANC0_FSOUT_SEL	W/R	0	ANC0 down sample path output samplerate select 0/1: 32K 2: 24K 3: 16K 4: 12K 5: 8K
0	ANC0_IN_384K_EN	W/R	0	ANC0 down sample path input samplerate select 0: 192K 1: 384K

Register 14-6 ANCDSGAIN

Bit	Name	Mode	Default	Description
31:16	ANC1_GAIN	W/R	0x400	ANC0 down sample path digital GAIN gain = 20log10(ANC1_GAIN/2^10)
15:0	ANC0_GAIN	W/R	0x400	ANC1 down sample path digital GAIN gain = 20log10(ANC0_GAIN/2^10)

Register 14-7 VADCON0: SDADC VAD Control Register0

Bit	Name	Mode	Default	Description
31:7	-	-	-	Reserve
6	VADTICKDETECT	W/R	0	VAD tick detect enable 0:enable 1:disable
5:4	VADFLENSEL	W/R	0	VAD Frame Size select 00:128 sample length 01:256 sample length 10:512 sample length

Bit	Name	Mode	Default	Description
				11:1024 sample length
3:1	VADSEL	W/R	0	VAD select channel 0: ADC0 1: ADC1 2:ADC2 3:ADC3 4:ADC4
0	VADEN	W/R	0	VAD enable bit 0: disable 1 : enable

Register 14-8 VADCON1: SDADC VAD Control Register1

Bit	Name	Mode	Default	Description
31:30	-	-	-	Reserve
29:16	VadFramePosCntT	W/R	0	Threshold of Vad Pos Frame Counter
15:14	-			
13:0	VadFramePosCntT	W/R	0	Threshold of Vad Neg Frame Counter

Register 14-9 VADCON2: SDADC VAD Control Register2

Bit	Name	Mode	Default	Description
31:15	VadPosMask	W/R	0	Flg Smooth Mask for Pos Flg: 0xff means:15 consecutive pos flg is pos frame
15:0	VadNegMask	W/R	0	Flg Smooth Mask for Pos Flg ,0xff means:15 consecutive neg flg is neg frame

Register 14-10 VADDMACON: VAD DMA Control Register

Bit	Name	Mode	Default	Description
31:16	VADFSMPOFFSET	R	0	Left channel DMA buffer Samples offset at VAD Flag generate
15:0	DMASMPOFFSET	R	0	Left channel DMA buffer Samples offset

14.3 SDADC DMA Special Function Registers

Register 14-11 SDADCDMAFLAG: SDADC DMA Flag register

Bit	Name	Mode	Default	Description
31:25	-	-	-	Reserve
24	VAD_FLAG	R	0	0: not done 1: done
23	ANC2_DMA_SAMPLE _DONE	R	0	0: not done 1: done
22	ANC2_DMA_HALF_DONE	R	0	0: not done 1: done
21	ANC2_DMA_ALL_DONE	R	0	0: not done 1: done
20	ANC1_DMA_SAMPLE _DONE	R	0	0: not done 1: done
19	ANC1_DMA_HALF_DONE	R	0	0: not done 1: done

Bit	Name	Mode	Default	Description
18	ANC1_DMA_ALL_DONE	R	0	0: not done 1: done
17	ANC0_DMA_SAMPLE _DONE	R	0	0: not done 1: done
16	ANC0_DMA_HALF_DONE	R	0	0: not done 1: done
15	ANC0_DMA_ALL_DONE	R	0	0: not done 1: done
14	ADC4_DMA_SAMPLE _DONE	R	0	0: not done 1: done
13	ADC4_DMA_HALF_DONE	R	0	0: not done 1: done
12	ADC4_DMA_ALL_DONE	R	0	0: not done 1: done
11	ADC3_DMA_SAMPLE _DONE	R	0	0: not done 1: done
10	ADC3_DMA_HALF_DONE	R	0	0: not done 1: done
9	ADC3_DMA_ALL_DONE	R	0	0: not done 1: done
8	ADC2_DMA_SAMPLE _DONE	R	0	0: not done 1: done
7	ADC2_DMA_HALF_DONE	R	0	0: not done 1: done
6	ADC2_DMA_ALL_DONE	R	0	0: not done 1: done
5	ADC1_DMA_SAMPLE _DONE	R	0	0: not done 1: done
4	ADC1_DMA_HALF_DONE	R	0	0: not done 1: done
3	ADC1_DMA_ALL_DONE	R	0	0: not done 1: done
2	ADC0_DMA_SAMPLE _DONE	R	0	0: not done 1: done
1	ADC0_DMA_HALF_DONE	R	0	0: not done 1: done
0	ADC0_DMA_ALL_DONE	R	0	0: not done 1: done

Register 14-12 SDADCDMACLR: SDADC DMA Flag clear register

Bit	Name	Mode	Default	Description
31:25	-	-	-	Reserve
24	VAD_FLAG	W	0	write 1 clear
23	ANC2_DMA_SAMPLE _DONE	W	0	write 1 clear
22	ANC2_DMA_HALF_DONE	W	0	write 1 clear
21	ANC2_DMA_ALL_DONE	W	0	write 1 clear
20	ANC1_DMA_SAMPLE _DONE	W	0	write 1 clear
19	ANC1_DMA_HALF_DONE	W	0	write 1 clear
18	ANC1_DMA_ALL_DONE	W	0	write 1 clear
17	ANC0_DMA_SAMPLE _DONE	W	0	write 1 clear
16	ANC0_DMA_HALF_DONE	W	0	write 1 clear
15	ANC0_DMA_ALL_DONE	W	0	write 1 clear
14	ADC4_DMA_SAMPLE _DONE	W	0	write 1 clear
13	ADC4_DMA_HALF_DONE	W	0	write 1 clear
12	ADC4_DMA_ALL_DONE	W	0	write 1 clear
11	ADC3_DMA_SAMPLE _DONE	W	0	write 1 clear
10	ADC3_DMA_HALF_DONE	W	0	write 1 clear

Bit	Name	Mode	Default	Description
9	ADC3_DMA_ALL_DONE	W	0	write 1 clear
8	ADC2_DMA_SAMPLE _DONE	W	0	write 1 clear
7	ADC2_DMA_HALF_DONE	W	0	write 1 clear
6	ADC2_DMA_ALL_DONE	W	0	write 1 clear
5	ADC1_DMA_SAMPLE _DONE	W	0	write 1 clear
4	ADC1_DMA_HALF_DONE	W	0	write 1 clear
3	ADC1_DMA_ALL_DONE	W	0	write 1 clear
2	ADC0_DMA_SAMPLE _DONE	W	0	write 1 clear
1	ADC0_DMA_HALF_DONE	W	0	write 1 clear
0	ADC0_DMA_ALL_DONE	W	0	write 1 clear

Register 14-13 SDADC0DMACON/SDADC1DMACON/SDADC2DMACON/SDADC3DMACON/ SDADC4DMACON/ANC0DMACON/ANC1DMACON/ANC2DMACON

Bit	Name	Mode	Default	Description
31:10	-	-	-	Reserve
9	VAD_IE	W/R	0	Vad interrupt enable(SDADC0DMACON) 0: disable 1: enable
8	DMA_SAMPLE _IE	W/R	0	DMA one sample pending interrupt enable 0: disable 1: enable
7	DMA_HALF _IE	W/R	0	DMA half done pending interrupt enable 0: disable 1: enable
6	DMA_ALL _IE	W/R	0	DMA all done pending interrupt enable 0: disable 1: enable
5:3	DMA_WDAT1_SEL	W/R	0	DMA data1 select，ANC2 DMA data is DACL_MUSIC，DACR_MUSIC 0: ADC0_DOUT 1:ADC1_DOUT 2:ADC2_DOUT 3:ADC3_DOUT 4:ADC4_DOUT 5:ANC0_DS_DOUT 6:ANC1_DS_DOUT
2	DMA_DATA_MODE	W/R	0	DMA data mode 0:24bits 1:16bits
1	DMA_STEREO	W/R	0	DMA stereo/mono 0:mono 1:stereo
0	DMA_EN	W/R	0	DMA enable 0: disable 1: enable

Register 14-14 SDADC0DMAADDR/SDADC1DMAADDR/SDADC2DMAADDR/SDADC3DMAADDR/ SDADC4DMAADDR/ANC0DMADDR/ANC1DMAADDR/ANC2DMADDR

Bit	Name	Mode	Default	Description
31:0	DMA_ADDR	W/R	0	DMA begin address

Register 14-15 SDADC0DMASIZE/ SDADC1DMASIZE/ SDADC2DMASIZE/ SDADC3DMASIZE/ SDADC4DMASIZE/ANC0DMASIZE/ANC1DMASIZE/ANC2DMASIZE

Bit	Name	Mode	Default	Description
31:16	ADC_DATA[23:8]	R	0	adc data [23:8]
15:0	DMA_SIZE	W/R	0	DMA size samples number : DMA_SIZE + 1

15 SDDAC

15.1 Features

1. DAC support stereo/mono mode,stereo mode works at 48MHz and mono works at 24MHz
2. AUBUF write data support stereo/mono,24bits/16bits mode
3. DAC support 96K samplerate

15.2 Audio Buffer Special Function Registers

Register 15-1 AUBUF0DATA: Audio Buffer0 Data register

Bit	Name	Mode	Default	Description
31:0	AUBUF0DATA	W	-	If aubuf0_mode=1,DAC is 16bits mode [31:16] is right channel audio buffer data [15:0] is left channel audio buffer data If aubuf0_mode=0, DAC is 24bits mode [23:0] is left channel audio buffer data

Register 15-2 AUBUF0DATAR24: Audio Buffer0 stereo24 right Data register

Bit	Name	Mode	Default	Description
31:0	AUBUF0DATAR24	W	-	If aubuf0_mode=1, DAC is 16bits mode Unused If aubuf0_mode=0, DAC is 24bits mode [23:0] is right channel audio buffer data

Register 15-3 AUBUF0CON: Audio Buffer0 configuration register

Bit	Name	Mode	Default	Description
31:24	-	-	-	Reserve
23	AUBUF0_SMPCHG_DONE	R	0	aubuf0 sample rate change flag 0: sample rate change done 1: sample rate changing
22	AUBUF0_DATA_READY	R	0	aubuf0 data ready/ music play 0:not ready,stop play 1: ready,play music
21	AUBUF0_LR_FLAG_CLR	W	0	aubuf0 LR Flag clear 0: invalid 1: clear
20	AUBUF0_FIFOBACK_SEL	W/R	0	aubuf0 FIFO back up SFR read select 0: AUBUF0BACKUP lock at AUBUFFIFOCNT read

Bit	Name	Mode	Default	Description
				1: AUBUF0BACKUP without lock
19	AUBUF0_STARTSIZE_X2	W/R	0	aubuf0 start play sample size x2 enable 0: disable 1:enable If enable ,audio start play sample size = AUBUF0_START_SEL*2
18	HIGHSR_CNT _EN	W/R	0	dac high sample rate count enable 0: disable 1: enable
17	AUBUF0_PEAK_CLR	W	0	peak register lear 0: invalid 1: clear
16	AUBUF0_PEAK_DETECT	W/R	0	aubuf0 peak detect enable 0: disable 1: enable
15:11	-	-	-	Reserve
10:9	AUBUF0_START_SEL	W/R	0	aubuf0 start play sample size select 00: AU0_START_SIZE 01: AU0_START_SIZE/2 10: AU0_START_SIZE /4 11: AU0_START_SIZE /8
8	AUBUF0_FULL	R		0: not full,can write data to aubuf0 1: full
7:6	AUBUF0_START_SIZE	W/R	1	aubuf0 start play sample size 00: 64 01: 128 10: 256 11: 512
5	AUBUF0_PEND	R	0	aubuf0 pend 0: AUBUF0FIFOCNT>AUBUF0_THRESHOLD 1: AUBUF0FIFOCNT<=AUBUF0_THRESHOLD
4	AUBUF0_INTEN	W/R	0	aubuf0 interrupt enable 0: disable 1: enable
3:2	-	-	-	Reserve
1	AUBUF0_PEND_CLR	W	0	aubuf0 pend clear 0: invalid 1: clear
0	AUBUF0_RST	W	0	0: invalid 1: reset

Register 15-4 AU0PEAKMAXLEFT:

Bit	Name	Mode	Default	Description
31:0	AU0_L_PEAKMAX	R	0	aubuf0 left channel peak max

Register 15-5 AU0PEAKMINLEFT:

Bit	Name	Mode	Default	Description
31:0	AU0_L_PEAKMIN	R	0	aubuf0 left channel peak min

Register 15-6 AU0PEAKMAXRIGHT:

Bit	Name	Mode	Default	Description
31:0	AU0_R_PEAKMAX	R	0	aubuf0 right channel peak max

Register 15-7 AU0PEAKMINRIGHT:

Bit	Name	Mode	Default	Description
31:0	AU0_R_PEAKMIN	R	0	aubuf0 right channel peak min

Register 15-8 AUBUF0STARTADDR: Audio Buffer0 Start Adder

Bit	Name	Mode	Default	Description
31:0	AUBUF0_STARTADDR	R	0	aubuf0 dma start addr

Register 15-9 AUBUF0SIZE: Audio Buffer Size

Bit	Name	Mode	Default	Description
31:16	AUBUF0_THRESHOLD	W/R	0	aubuf0 threshold AUBUF0_FIFOCNT<= AUBUF0_THRESHOLD and AUBUF0_INT_EN==1 will generate audio buffer interrupt
15:0	AUBUF0_SIZE	W/R	0	Aubuf0 dma size

Register 15-10 AUBUF0FIFOCNT: Audio Buffer0 Size

Bit	Name	Mode	Default	Description
31:18	AUBUF0_FIFOCNT	R	0	aubuf0 fifo counter
17:0	AUBUF0_HIGHSRCNT	R	0	aubuf0 high samplerate counter (6.144 MHz or 5.6448 MHz)

Register 15-11 AUBUF0BACKUP:

Bit	Name	Mode	Default	Description
31:0	AUBUF0_BACKUP	R	0	aubuf0 FIFO CNT BACK UP Time to display = AUBUF0BACKUP*Tin + AUBUF0FIFOCNT&0x3ffff*Tout Tin : is the input sample cycle Tout : is the out sample cycle

Register 15-12 AUBUF0PTR: Audio Buffer0 read write Ptr

Bit	Name	Mode	Default	Description
31:16	AUBUF0_RDPTR	R	0	aubuf0 read ptr
15:0	AUBUF0_WRPTR	R	0	aubuf0 write ptr

Register 15-13 AUBUF1DATA: Audio Buffer1 Data register

Bit	Name	Mode	Default	Description
31:0	AUBUF1DATA	W	-	If aubuf1_mode=1,SRC1 is 16bits mode [31:16] is right channel audio buffer data [15:0] is left channel audio buffer data If aubuf1_mode=0, SRC1 is 24bits mode [23:0] is left channel audio buffer data

Register 15-14 AUBUF1DATAR24: Audio Buffer1 stereo24 right Data register

Bit	Name	Mode	Default	Description
31:0	AUBUF1DATAR24	W	-	If aubuf1_mode=1, SRC1 is 16bits mode Unused If aubuf1_mode=0, SRC1 is 24bits mode [23:0] is right channel audio buffer data

Register 15-15 AUBUF1CON: Audio Buffer1 configuration register

Bit	Name	Mode	Default	Description
31:24	-	-	-	Reserve
22	AUBUF1_DATA_READY	R	0	aubuf0 data ready/ music play 0:not ready,stop play 1: ready,play music
21	AUBUF1_LR_FLAG_CLR	W	0	aubuf0 LR Flag clear 0: invalid 1: clear
19	AUBUF1_STARTSIZE_X2	W/R	0	Aubuf1 start play sample size x2 enable 0: disable 1:enable If enable ,audio start play sample size = AUBUF0_START_SEL*2
17	AUBUF1_PEAK_CLR	W	0	peak register lear 0: invalid 1: clear
15:11	-	-	-	Reserve
10:9	AUBUF1_START_SEL	W/R	0	Aubuf1 start play sample size select 00: AU1_START_SIZE 01: AU1_START_SIZE/2 10: AU1_START_SIZE /4 11: AU1_START_SIZE /8
8	AUBUF1_FULL	R		0: not full,can write data to aubuf0 1: full
7:6	AUBUF1_START_SIZE	W/R	1	Aubuf1 start play sample size 00: 64 01: 128 10: 256 11: 512

Bit	Name	Mode	Default	Description
5	AUBUF1_PEND	R	0	Aubuf1 pend 0: AUBUF1FIFOCNT>AUBUF1_THRESHOLD 1: AUBUF1FIFOCNT<=AUBUF1_THRESHOLD
4	AUBUF1_INTEN	W/R	0	Aubuf1 interrupt enable 0: disable 1: enable
3:2	-	-	-	Reserve
1	AUBUF1_PEND_CLR	W	0	aubuf1pend clear 0: invalid 1: clear
0	AUBUF1_RST	W	0	0: invalid 1: reset

Register 15-16 AUBUF1STARTADDR: Audio Buffer0 Start Adder

Bit	Name	Mode	Default	Description
31:0	AUBUF1_STARTADDR	R	0	Aubuf1 dma start addr

Register 15-17 AUBUF1SIZE: Audio Buffer Size

Bit	Name	Mode	Default	Description
31:16	AUBUF1_THRESHOLD	W/R	0	aubuf0 threshold AUBUF1_FIFOCNT<= AUBUF1_THRESHOLD and AUBUF1_INT_EN==1 will generate audio buffer interrupt
15:0	AUBUF1_SIZE	W/R	0	Aubuf1 dma size

Register 15-18 AUBUF1FIFOCNT: Audio Buffer1 Size

Bit	Name	Mode	Default	Description
31:18	AUBUF1_FIFOCNT	R	0	Aubuf1 fifo counter
17:0	AUBUF1_HIGHSRCNT	R	0	Aubuf1 high samplerate counter (6.144 MHz or 5.6448 MHz)

Register 15-19 AUBUF1PTR: Audio Buffer1 read write Ptr

Bit	Name	Mode	Default	Description
31:16	AUBUF1RDPTR	R	0	Audio Buffer1 read ptr
15:0	AUBUF1WRPTR	R	0	Audio buffer1 write ptr

Register 15-20 AUBUF0DMACON: GPDMA to audio buffer0 control register

Bit	Name	Mode	Default	Description
31:16	DMASIZE	W/R	0	Au buffer DMA Sizes Word size : input stereo 24bits = (2*samples -1)*4 input stereo 16bits or mono 24bit = (samples-1)*4 Input mono 16bits= (samples-1)*2
15:10				
9				
8	DMADONE	R	0	DMA0 done flag

Bit	Name	Mode	Default	Description
				0: not done 1:done
7	Mute Fadeout	W/R	0	Au buffer DMA data Mute Fadeout enable 0: release mute(fade in) 1: enable mute (fade out)
6	Mute Fade Size	W/R	0	Mute fade size select 0: 512 samples 1:256 samples
5	DMAIE1	W/R	0	GPDMA0 interrupt enable 0: disable 1:enable
4:3	DMAMODE	W/R	0	DMA Data input mode : stereo/mono,24bits/16bits 00: mono 24bits mode 01: mono 16bits mode 10: stereo 24bits mode 11: stereo 16bits mode
2:1				
0	DMAEN	W/R	0	DMA enable 0: disable 1:enable

Register 15-21 AUBUF0DMAADR: audio buffer0 DMA Start Adder

Bit	Name	Mode	Default	Description
31:0	DMAADRST0		0	DMA Start Adder0

Register 15-22 AUBUF0DMAKICK: audio buffer0 KICK control register

Bit	Name	Mode	Default	Description
25:16	FadeCount	R	0x200	
15：9				
8	DMA0DONECLR	W	0	Write 1 clear DMA0 Done Flag
7:3				
2	FadeClr			Fade Count clear
1	FadeSet	W	0	Fade Count Set
0	DMA0KICK	W	0	Write 1 kick start GPDMA0

Register 15-23 AUBUF1DMACON: GPDMA to audio buffer1 control register

Bit	Name	Mode	Default	Description
31:16	DMASIZE	W/R	0	Au buffer DMA Sizes Word size : input stereo 24bits = (2*samples -1)*4 input stereo 16bits or mono 24bit = (samples-1)*4 Input mono 16bits= (samples-1)*2
15:9				
8	DMADONE	R	0	DMA0 done flag 0: not done 1:done
7	Mute Fadeout	W/R	0	Au buffer DMA data Mute Fadeout enable 0: release mute(fade in) 1: enable mute (fade out)
6	Mute Fade Size	W/R	0	Mute fade size select

Bit	Name	Mode	Default	Description
				0: 512 samples 1:256 samples
5	DMAIE1	W/R	0	GPDMA0 interrupt enable 0: disable 1:enable
4:3	DMAMODE	W/R	0	DMA Data input mode : stereo/mono,24bits/16bits 00: mono 24bits mode 01: mono 16bits mode 10: stereo 24bits mode 11: stereo 16bits mode
2:1				
0	DMAEN	W/R	0	DMA enable 0: disable 1:enable

Register 15-24 AUBUF1DMAADR: audio buffer1 DMA Start Adder

Bit	Name	Mode	Default	Description
31:0	DMAADRST0		0	DMA Start Adder0

Register 15-25 AUBUF1DMAKICK: audio buffer1 KICK control register

Bit	Name	Mode	Default	Description
25:16	FadeCount	R	0x200	
15:9	-	-	-	-
8	DMA0DONECLR	W	0	Write 1 clear DMA0 Done Flag
7:3	-	-	-	-
2	FadeClr			Fade Count clear
1	FadeSet	W	0	Fade Count Set
0	DMA0KICK	W	0	Write 1 kick start GPDMA0

Register 15-26 AU0DMAICON: Audio0 DMA input control register

Bit	Name	Mode	Default	Description
10	DMAHALFDONECLR	W	0	write 1 clear half done
9	DMAALLDONECLR	W	0	write 1 clear all done
8	DMAHALFDONE	W/R	0	Dma half done 0: not done 1:done
7	DMAALLDONE	W/R	0	Dma all done 0: not done 1:done
6	MONO2STEREO	W/R	0	dmain mono to stereo enable 0:disable 1: enable
5	EQDMAINEN	W/R	0	eq dmain enable,96k/48k 24bits data 0:disable 1: enable
4	ANCDMAINEN	W/R	0	anc dmain enable,384k/192k 24bits data 0:disable 1: enable
3	DACDMAINEN	W/R	0	dac dmain enable,only support 192k 24bits data

Bit	Name	Mode	Default	Description
				0:disable 1: enable
2	HALFINTEN	W/R	0	Dma half full interrupt enable 0: disable 1: enable
1	ALLINTEN	W/R	0	Dma all full interrupt enable 0:disable 1: enable
0	DMAEN	W/R	0	Dma enable 0:disable 1: enable

Register 15-27 AU0DMAIADR: Audio0 DMA Input Start Addr

Bit	Name	Mode	Default	Description
31:0	Au0DmaInStartAddr	W/R	0	Audio0 Anc Dma input Start Addr

Register 15-28 AU0DMAISIZE: Audio0 DMA Input Size

Bit	Name	Mode	Default	Description
31:16				
15:0	Au0DmaInSize	W/R	0	Audio0 Anc Dma input Size.the configure need to -1
				Note: for example,128 samples dac stereo: AU0DMAISIZE =128*2-1 dac mono: AU0DMAOSIZE=128-1

Register 15-29 AU0DMAOCON: Audio0 DMA out control register

Bit	Name	Mode	Default	Description
9	DMAHALFDONECLR	W	0	write 1 clear half done
8	DMAALLDONECLR	W	0	write 1 clear all done
7	DMAHALFDONE	W/R	0	DmaOut half done 0: not done 1:done
6	DMAALLDONE	W/R	0	DmaOut all done 0: not done 1:done
5:4				
3	DMAMODE	W/R	0	DmaOutMode 0: 24bits 1:16bits
2	HALFINTEN	W/R	0	DmaOut half full interrupt enable 0: disable 1: enable
1	ALLINTEN	W/R	0	DmaOut all full interrupt enable 0:disable 1: enable
0	DMAOUTEN	W/R	0	DmaOut enable 0:disable 1: enable Should enable DMAOUTEN first,then enable DACDIGCON0[26]

Register 15-30 AU0DMAOADR: Audio0 DMA out Start Adder

Bit	Name	Mode	Default	Description

Bit	Name	Mode	Default	Description
31:0	Au0DmaOutStartAddr		0	Audio0 Dma out Start Adder

Register 15-31 AU0DMAOSIZE: Audio0 DMA Out Size

Bit	Name	Mode	Default	Description
15:0	Au0DmaOutSize		0	Audio 0 Dma Out Size DMA Samples Number : DMASiZE + 1
				Note: for example,128 samples dac stereo & AU0DMAOCON[3]=0, AU0DMAOSIZE=128*2-1 dac mono & AU0DMAOCON[3]=0, AU0DMAOSIZE=128-1 dac stereo & AU0DMAOCON[3]=1, AU0DMAOSIZE=128-1(data={R16,L16} dac momo & AU0DMAOCON[3]=1, AU0DMAOSIZE=128-1(data={0,L16}

15.3 SDDAC Special Function Registers

Register 15-32 DACDIGCON0: DAC Digital Control Register

Bit	Name	Mode	Default	Description
31:29	BFCOEFWRSEL	W/R	0	DAC EQ coef wr sel [31] 0 : left 1: right [30:29] 0:EQ16 1:EQ3 2:DRC
28	AUBUF1MODE	W/R	0	SRC1 AUBUF1DATA MODE 0:24bits 1:16bits
27	EXTOUTONLY	W/R	0	DAC extern out only enable 0: disable 1: enable
26	DacDmaOutEn	W/R	0	DAC SRC0 data Dma Out enable 0：disable 1: enable Should configure AU0DMAOCON[0] first,then enable DacDmaOutEn
25:24	DMAO_DATA_SEL	W/R	0	dmaout data sel 0: data before mix 1: data after mix(not dac volume) 2: data after dac volume 3: data after EQ0
23	EXTOUTEN	W/R	0	DAC extern out enable 0: disable 1: enable
22	Src1 Sample rate Syn	W/R	0	Src1 Sample Rate Synchronization Enable 0: disable 1:enable
21:18	Src1 in sample	W/R	0	If DACDIGCON3[24]=0, If DACDIGCON3[24]=1, 0 : 48K 0:96K 1: 44.1K 1:88.2K 2: 38K 2:76K 3: 32K 3:64K 4: 24K 4:48K

Bit	Name	Mode	Default	Description
				5: 22.05K 5:44.1K 6: 16K 6:32K 7: 12K 7:24K 8: 11.025K 8:22.05K 9: 8K 9:16K 10: 6K 10:12K 11: 4K 11:8K
17	DACPHYCLKOUTEN	W/R	0	DAC phy clk out enable 0: disable 1: enable
16	Src1En	W/R	0	Src Enable 0: disable 1: enable
15	DACCLKSEL	W/R	0	Analog DACCLK sel 0: falling edge 1:rising edge
14	AUBUFMODE	W/R	0	AUBUFDATA MODE 0:24bits 1:16bits
13	STEREO	W/R	0	DAC STEREO/MONO 0: mono 1: stereo
12	PhyBitEn	W/R	0	DAC SDM Bits PHY Input enable 0: disable 1: enable
11	PhyDwaEn	W/R	0	DAC DWA Level PHY input enable 0: disable 1: enable
10	DitherEn	W/R	0	Sdm Dither Enable 0: disable 1:enable
9	RmDcEn	W/R	0	Remove Dc offset Enable 0: disable 1: enable
8	Au1MixEn	W/R	0	Audio1 Mix Enable 0: disable 1: enable
7	Au0MixEn	W/R	0	Audio0 Mix Enable 0: disable 1: enable
6	Src0 Sample rate Syn	W/R	0	Src0 Sample Rate Synchronization Enable 0: disable 1:enable
5:2	Src0 in sample	W/R	0	If DACDIGCON3[24]=0, If DACDIGCON3[24]=1, 0 : 48K 0:96K 1: 44.1K 1:88.2K 2: 38K 2:76K 3: 32K 3:64K 4: 24K 4:48K 5: 22.05K 5:44.1K 6: 16K 6:32K 7: 12K 7:24K 8: 11.025K 8:22.05K 9: 8K 9:16K

Bit	Name	Mode	Default	Description
				10: 6K 10:12K 11: 4K 11:8K
1	Src0 out sample rate	W/R	0	If DACDIGCON3[24]=0, If DACDIGCON3[24]=1, 0: 44.1K 0: 88.2K 1: 48 K 1:96K
0	DAC enable	W/R	0	0: disable 1: enable

Register 15-33 DACDIGCON1: DAC Digital Control Register

Bit	Name	Mode	Default	Description
31	IIS_PULSE_SEL	W/R	0	IIS pulse select 0: fix_iis_pulse 1: ext_out_pulse
30	MISUC_SUB_DC_EN	W/R	0	ANC music data sub trim dc enable 0: disable 1: enable
29	DACL_ANC_TEST	W/R	0	dacl output data select 0: dacl data 1: ancr data
28	DACR_ANC_TEST	W/R	0	dacr output data select 0: dacr data 1: ancr data
27	DACR_ADD_ANC_EN	W/R	0	dacr add anc data enable 0: disable 1: enable
26	DACL_ADD_ANC_EN	W/R	0	dacl add anc data enable 0: disable 1: enable
25:24	ANCR_ADD _SEL	W/R	0	ancl add data select 0: anc0_ldata 1: anc0_rdata 2: anc1_ldata 3: anc1_rdata
23	ANCR_ADD_EN	W/R	0	ancr data add ancr_add_sel data enable 0: disable 1: enable
22:21	ANCL_ADD _SEL	W/R	0	ancl add data select 0: anc0_ldata 1: anc0_rdata 2: anc1_ldata 3: anc1_rdata
20	ANCL_ADD_EN	W/R	0	ancl data add ancl_add_sel data enable

Bit	Name	Mode	Default	Description
				0: disable 1: enable
19:18	ANCR_DATA_SEL	W/R	0	ancr data select 0: anc0_rdata 1: anc0_ldata 2: anc1_ldata 3: anc1_rdata
17:16	ANCL_DATA_SEL	W/R	0	ancl data select 0: anc0_ldata 1: anc0_rdata 2: anc1_ldata 3: anc1_rdata
15:14	ANC_US_CIC_ORDER	W/R	0	ANC upsample cic order 0: 1order 1: 2order 2: 3order
13	DAC_ANC_SPR	W/R	0	DAC anc samplerate 0:192K 1:384K
12	DAC_ANC_EN	W/R	0	DAC anc path enable 0: disable 1: enable
11	LCDWA_HEN	W/R	0	set LCDWA all bit high level 0: disable 1: enable
10	LCDWA_LEN	W/R	0	set LCDWA all bit low level 0: disable 1: enable
9	RCDWA_HEN	W/R	0	set RCDWA all bit high level 0: disable 1: enable
8	RCDWA_LEN	W/R	0	set RCDWA all bit low level 0: disable 1: enable
7	RA2S_EN	W/R	0	ADCR analog output to DACR SDM input path enable 0: disable 1: enable
6	LA2S_EN	W/R	0	ADCL analog output to DACL SDM input path enable 0: disable 1: enable
5	RA2A_EN	W/R	0	ADCR analog output to DACR SDM output path enable 0: disable

Bit	Name	Mode	Default	Description
				1: enable
4	LA2A_EN	W/R	0	ADCL analog output to DACL SDM output path enable 0: disable 1: enable
3	UNOPT_EN	WR	0x0	sdm not optimize Zero-Pole enable 0: sdm optimize Zero-Pole 1: sdm don't optimize Zero-Pole
2	SDM_COEF_SEL	W/R	0	SDM coef select
1	SDM_SCALE_SEL	W/R	0	SDM input scale select 0: 0.9531 1: 0.9375
0	SDM_LSH_SEL	W/R	0	SDM input leftrash select 0: 6bits 1: 5bits

Register 15-34 DACDIGCON2: DAC Digital Control Register

Bit	Name	Mode	Default	Description
23:0	DC_EXPECT	W/R	0	DC offset expect for sdm1(dac power on)

Register 15-35 DACDIGCON3: DAC Digital Control Register

Bit	Name	Mode	Default	Description
30	RSDM_DIN_INV_EN	W/R	0	RSDM din signal inv enable 0: disable 1: enable
29	LSDM_DIN_INV_EN	W/R	0	LSDM din signal inv enable 0: disable 1: enable
28:27	IIS_OUT_SEL	W/R	0	iis out dac data select 0: data before mix 1: data after mix(not dac volume) 2: data after dac volume
26	SRC1_BYPASS_EN	W/R	0	Src1 data bypass SRC1 filter enable 0: disable 1: enable
25	SRC0_BYPASS_EN	W/R	0	Src0 data bypass SRC0 filter enable 0: disable 1: enable
24	DAC_96K_EN	W/R	0	DAC output 96K/88.2K enable 0: disable 1: enable
19	SDM1_DIN_SEL	W/R	0	Sdm1 input data sel

Bit	Name	Mode	Default	Description
				0: DC_EXPECT 1: DACL data
18	SDM1_UNOPT_EN	W/R	0	Sdm1 unopt enable 0: disable 1: enable
17	SDM1_DITHER_EN	W/R	0	Sdm1 dither enable 0: disable 1: enable
16	SDM1_EN	W/R	0	Sdm1 enable 0: disable 1: enable
15:8	DC_SAMPLES_STEP	W/R	0	DC fade one step time = DC_SAMPLES_STEP / 6.144M
7:4	DC_FADE_STEP	W/R	0	DC fade step = 2^ DC_FADE_STEP
3	DC_DONE	R	0	DC offset fade/set done 0: not done 1: done
2	DC_FADE_DIR	W/R	0	DC offset fade dir 0: increment 1: decrease
1	DC_DIRECT_SET	W	0	DC offset direct set Write 1, dc offset direct set to DC_EXPECT
0	DC_KICK	W	0	DC fade kick start Write 1 kick start,dc offset fadein to DC_EXPECT

Register 15-36 DACVOLCON: DAC Volume register

Bit	Name	Mode	Default	Description
23:0	Dac Volume	W/R	0x007fff	= DacVolume / 2^15,support >0db abjust
27:24	Volume Step	W/R	0	= 2^VolumeStep
28	VolumeDone	W/R	0	0: Volume not Match 1: Volume Match Confige DACVOLCON will clear VolumeDone flag
30	Direct Set	W	0	Write 1 direct set volume

Register 15-37 SRC0VOLCON: SRC0 Volume register

Bit	Name	Mode	Default	Description
23:0	SRC0 Volume	W/R	0x007fff	= Src0Volume / 2^15,support >0db abjust
27:24	Volume Step	W/R	0	= 2^VolumeStep
28	VolumeDone	W/R	0	0: Volume not Match 1: Volume Match Confige SRC0VOLCON will clear VolumeDone flag

Bit	Name	Mode	Default	Description
30	Direct Set	W	0	Write 1 direct set volume

Register 15-38 SRC1VOLCON: SRC1 Volume register

Bit	Name	Mode	Default	Description
23:0	SRC1 Volume	W/R	0x007fff	= Src1Volume / 2^15,support >0db abjust
27:24	Volume Step	W/R	0	= 2^VolumeStep
28	VolumeDone	W/R	0	0: Volume not Match 1: Volume Match Confige SRC1VOLCON will clear VolumeDone flag
30	Direct Set	W	0	Write 1 direct set volume

Register 15-39 AU0LMIXCOEF :Audio0 Left Channel Mix Coeff register

Bit	Name	Mode	Default	Description
15:0	AU0LMIXLC0	W/R	0	
31:16	AU0LMIXRC0	W/R	0	
				AU0LOUT = (AU0LIN* AU0LMIXLC0 + AU0RIN* AU0LMIXRC0)/2^15

Register 15-40 AU0RMIXCOEF :Audio0 Right Channel Mix Coeff register

Bit	Name	Mode	Default	Description
15:0	AU0RMIXLC1	W/R	0	
31:16	AU0RMIXRC1	W/R	0	
				AU0ROUT = (AU0LIN* AU0RMIXLC1 + AU0RIN* AU0RMIXRC1)/2^15

Register 15-41 AU1LMIXCOEF :Audio1 Left Channel Mix Coeff register

Bit	Name	Mode	Default	Description
15:0	AU1LMIXLC0	W/R	0	
31:16	AU1LMIXRC0	W/R	0	
				AU1LOUT = (AU1LIN* AU1LMIXLC0 + AU1RIN* AU1LMIXRC0)/2^15

Register 15-42 AU1RMIXCOEF :Audio1 Right Channel Mix Coeff register

Bit	Name	Mode	Default	Description
15:0	AU1RMIXLC1	W/R	0	
31:16	AU1RMIXRC1	W/R	0	
				AU1ROUT = (AU1LIN* AU1RMIXLC1 + AU1RIN* AU1RMIXRC1)/2^15

Register 15-43 DACRMDCCON: DAC Remove DC register

Bit	Name	Mode	Default	Description
0	RmDcKick	W/R	0	Remove Dc kick Write 1 kick start
1	DcDirectSet	W/R	0	Direct Set DC Write 1 Direct Set Dc
2	DcDirL	W/R	0	DC Direction left

Bit	Name	Mode	Default	Description
				0： decrease 1：increment
3	DcDirR	W/R	0	DC Direction right 0： decrease 1：increment
4	RmDcComp	W/R	0	Remove DC complete select 0：according to digital match 1：according to analog match
5	AngCmpInvEn	W/R	0	Analog Complete inv enable 0: disable 1: enable
9:6	DcStepSel	W/R		Remove Dc Step = 2^ DcStepSel
10	RmDcDone	W/R	0	Remove DC done 0：not done 1: done
11	AngCmpL	R	0	Analog compare Left out
12	AngCmpR	R	0	Analog compare right out
14	DcDirSel	W/R	0	DC fade dir select 0:auto dir 1: use DcDirL/ DcDirR

Register 15-44 DACLDCEXP: Remove DC expect register

Bit	Name	Mode	Default	Description
23:0	DcExpL	W/R	0	Left channel Dc expect

Register 15-45 DACRDCEXP: Remove DC expect register

Bit	Name	Mode	Default	Description
23:0	DcExpR	W/R	0	Right channel Dc expect

Register 15-46 PhaseComp: SRC Phase Compensation Register

Bit	Name	Mode	Default	Description
31:28				Unused
27:16	PhaseComp1	W/R	0	SRC1 Phase compensate;signed number speed = 1+ PhaseComp1/(FsIn/48K*1920)
15:12				Unused
11:0	PhaseComp0	W/R	0	SRC0 Phase compensate;signed number speed = 1+ PhaseComp0/(FsIn/48K*1920)

Register 15-47 KEYTONECON0: DAC key tone Register0

Bit	Name	Mode	Default	Description
31:16	KEYTONE_SIZES	W/R	0	DAC keytone play sizes (KEYTONE_MODE==0) KEYTONE_SIZES > FADE_STEP_SEL*256*2 Playtime = KEYTONE_SIZES/Fs
15:11				

Bit	Name	Mode	Default	Description
10	KEYTONE_DONE	R	0	DAC keytone done (KEYTONE_MODE==0) 0: not done 1: done
9	KEYTONE_FADEOUT_DONE	R	0	DAC keytone fadeout done 0: not done 1: done
8	KEYTONE_FADEIN_DONE	R	0	DAC keytone fadein done 0: not done 1: done
7	KEYTONE_KICK	W/R		DAC keytone kick start (KEYTONE_MODE==0) Write 1 kick start
6	KEYTONE_MODE	W/R		DAC keytone mode select 0: play size mode 1: fade type mode
5:4	KEYTONE_VOL_SEL	W/R	0	DAC keytone volume select 0: 0 dB 1: -6 dB 2: -12 dB 3: -24 dB
3:2	FADE_STEP_SEL	W/R	0	DAC keytone fade step select 0: 1 1: 2 2: 4 3: 8
1	FADE_TYPE	W/R	0	DAC keytone fade type (KEYTONE_MODE==1) 0: fadeout 1: fadein
0	KEYTONE_EN	W/R	0	DAC keytone enable 0: disable 1: enable

Register 15-48 KEYTONECON1: DAC key tone Register1

Bit	Name	Mode	Default	Description
31:0	ANGLE_STEP	W/R	0	DAC keytone angle step , Adjust keytone wave freq. = round(360.0/(Fs/Ftone)*2^29/45.0)

Register 15-49 DACBQ0CON: DAC BQ0 Control Register

Bit	Name	Mode	Default	Description
31:29	BiqCoefScaleR0	W/R	0	R channel EQ coef scale
28:26	BiqCoefScaleL0	W/R	0	L channel EQ coef scale
25	BiqCoefScaleEn	W/R	0	EQ coef fix30/31 enable 0: disable

Bit	Name	Mode	Default	Description
				1: enable
22	BiqYShSel	W/R	0	EQ max gain adjust select 0: 12dB 1: 24dB
16	CoefFix27/31	W/R	0	BQ0 Coef Fix Q27/Q31 enable (if BiqCoefScaleEn,Q31) 0: disable 1: enable
15	CoefFix26/30	W/R	0	BQ0 Coef Fix Q26/Q30 enable(if BiqCoefScaleEn,Q30) 0: disable 1: enable
14	CoefFix27/31	W/R	0	BQ0 Coef Fix Q27/Q31 enable (if BiqCoefScaleEn,Q31) 0: disable 1: enable
14:10	Band1	WR	0	BQ0 band1 parameter,the configure need sub 1 DAC output 48k/44.1k，max band1 = 19； DAC output 96k/88.2k & BQ1_EN & DRC_EN，max band1 = 7； DAC output 96k/88.2k & ~BQ1_EN & DRC_EN，max band1 = 9; DAC output 96k/88.2k & ~BQ1_EN & ~DRC_EN，max band1 = 11；
9:5	Band0	WR	0	DAC output 48k/44.1k，max band0 = 19； DAC output 96k/88.2k & BQ1_EN & DRC_EN，max band0 = 7； DAC output 96k/88.2k & ~BQ1_EN & DRC_EN，max band0 = 9; DAC output 96k/88.2k & ~BQ1_EN & ~DRC_EN，max band0 = 11；
5	Hybrid	WR	0	BQ0 hybrid enable bit 0: disable 1: enable
4	FadeOutEn	WR	0	BQ0 fade out enable bit 0: fade out idle 1: fade out operate
3	ChangeEn	WR	0	BQ0 change enable bit 0: change idle 1: change operate
2	FadeInEn	WR	0	BQ0 fade in enable bit 0: fade in idle 1: fade in operate
1	ClrKick	WO	0	BQ0 coef memory clear bit Write 1 valid
0	EN	WR	0	BQ0 enable bit 0: disable 1: enable

Register 15-50 DACBQ1CON: DAC BQ1 Control Register

Bit	Name	Mode	Default	Description
31:29	BiqCoefScaleR	W/R	0	R channel EQ coef scale
28:26	BiqCoefScaleL	W/R	0	L channel EQ coef scale

Bit	Name	Mode	Default	Description
25	BiqCoefScaleEn	W/R	0	EQ coef fix30/31 enable 0: disable 1: enable
22	BiqYShSel	W/R	0	EQ max gain adjust select 0: 12dB 1: 24dB
21	DrcRmsDw	WR	0	DRC RMS calculate input data width 0: Low 24bit valid 1: Saturate 24bit
20	DrcInSel	WR	0	BQ1/DRC input source select bit 0: After EQ0 1: Before EQ0
19:18	DrcCoefCnt	WR	0	DRC coef count parameter,the configure need sub 1
17	DrcDetType	WR	0	DRC detect type bit 0: Peak 1: RMS
16	DrcEN	WR	0	DRC enable bit 0: disable 1: enable
15	CoefFix26/30	W/R	0	BQ0 Coef Fix Q26/Q30 enable(if BiqCoefScaleEn,Q30) 0: disable 1: enable
14	CoefFix27/31	W/R	0	BQ0 Coef Fix Q27/Q31 enable (if BiqCoefScaleEn,Q31) 0: disable 1: enable
13:10	Band1	WR	0	BQ1 band1 parameter,the configure need sub 1
9:6	Band0	WR	0	BQ1 band0 parameter,the configure need sub 1
5	Hybrid	WR	0	BQ1 hybrid enable bit 0: disable 1: enable
4	FadeOutEn	WR	0	BQ1 fade out enable bit 0: fade out idle 1: fade out operate
3	ChangeEn	WR	0	BQ1 change enable bit 0: change idle 1: change operate
2	FadeInEn	WR	0	BQ1 fade in enable bit 0: fade in idle 1: fade in operate
1	ClrKick	WO	0	BQ1 coef memory clear bit Write 1 valid
0	EN	WR	0	BQ1 enable bit 0: disable

Bit	Name	Mode	Default	Description
				1: enable

Register 15-51 DACBQCPND: DAC BF clear pending register

Bit	Name	Mode	Default	Description
2	CoefWrFlag	RO	0	Coef write flag bit 0: once write done 1: write busy
1	CoefWrPend	RO	0	Coef write done pending bit Write 1 to clear this bit
0	MemClrPend	RO	0	Memory clear done pending bit Write 1 to clear this bit

Register 15-52 DACBQCOEF: Peripheral BQ coef register

Bit	Name	Mode	Default	Description
31:0	COEF	WO	0	Coef register

15.4 User Guide

1. Release clkgate and soft_rstn:
2. Reset audio Buffer
3. Configure audio buffer size
4. Configure stereo/mono，24bits/16bits mode
5. Enable dac

16 Characteristics

16.1 PMU Parameters

Table 16-1 PMU voltage input Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
VUSB	Charger Voltage input	4.6	5.0	5.5	V	
VBAT	Voltage input	3.0	3.7	4.5	V	

Table 16-2 3.3V LDO Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
VDDIO	3.3V LDO voltage output	2.4	3.3	3.6	V	Light Loading condition Step 0.1v
△VVDDIO	Output Mismatch 1-sigma	-	17	-	mV	VDDIO=3.3v
ILOAD	Maximum output current	-	-	150	mA	@VBAT=3.6v
ISC	Short Circuit Current Limit	-	-	750	mA	@VBAT=3.8v

Table 16-3 1.25V LDO Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
VDDBT/BT_AVDD	1.25V LDO voltage output	0.85	1.25	1.6	V	Light Loading condition Step 0.05v
△VVDDBT	Output Mismatch 1-sigma	-	9	-	mV	VDDBT=1.25v
ILOAD	Maximum output current	-	-	100	mA	@VBAT=3.0v
ISC	Short Circuit Current Limit	-	-	300	mA	@VBAT=3.8v

Table 16-4 1.1V LDO Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
VDDCORE	1.1V LDO voltage output	0.7	1.1	1.475	V	Light Loading condition Step 0.025v
△VVDDCORE	Output Mismatch 1-sigma	-	6	-	mV	VDDCORE=1.1v
ILOAD	Maximum output current	-	-	75	mA	@VBAT=3.6v
ISC	Short Circuit Current Limit	-	-	300	mA	@VBAT=3.8v

Table 16-5 1.25V BUCK Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
VDDBT	1.25V BUCK voltage output	0.85	1.25	1.6	V	Light Loading condition Step=0.05v
△VVDDBT	Output Mismatch 1-sigma	-	6	-	mV	VDDBT=1.25v
ILOAD	Maximum output current	-	-	360	mA	@VBAT=3.8v
ISC	Short Circuit Current Limit	-	-	360	mA	@VBAT=3.8v

Table 16-6 1.1V BUCK Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
VDDCORE	1.1V BUCK voltage output	0.7	1.1	1.475	V	Light Loading condition Step=0.025v
△VVDDCORE	Output Mismatch 1-sigma	-	6	-	mV	VDDCORE=1.1v
ILOAD	Maximum output current	-	-	360	mA	@VBAT=3.8v
ISC	Short Circuit Current Limit	-	-	360	mA	@VBAT=3.8v

16.2 IO Parameters

Table 16-6 I/O Parameters

GPIO—Electrical Characteristics							
Symbol	Description	Related GPIO	Min	Typical	Max	Units	Conditions
VIL	Low-level input voltage		-0.3		1.27	V	VDDIO=3.3V
VIH	High-level input voltage		2.03		3.6	V	VDDIO=3.3V
Driver Ability 1	Output Driver Ability 1			32		mA	VDDIO=3.3V
Driver Ability 0	Output Driver Ability 0			8		mA	VDDIO=3.3V
RPUP0	Internal pull-up resister 0		8	10	12	KΩ	
RPUP1	Internal pull-up resister 1		0.24	0.3	0.36	KΩ	
RPUP2	Internal pull-up resister 2		160	200	240	KΩ	
RPDN0	Internal pull-down resister 0		8	10	12	KΩ	
RPDN1	Internal pull-down resister 1		0.24	0.3	0.36	KΩ	
RPDN2	Internal pull-down resister 2		160	200	240	KΩ	

Table 16-7 Internal Resistor Characteristics

Port	General Output	High Drive	Internal Pull-Up Resistor（Ω）	Internal Pull-Down Resistor（Ω）	Comment
PA4-PA7 PB0-PB5 PE0, PE5-PE7 PF0-PF1 PG0-PG5	6mA	24mA	300/10K/200K	300/10K/200K	Internal pull-up/pull-down resistance accuracy +/-20%
PE4	6mA	24mA	10K	10K	

16.3 Audio DAC Parameters

Table 16-8 Audio DAC Normal Mode Parameters

Mode	Sym	Characteristics	Min	Typ	Max	Unit	Conditions
Differential Mode	SNR		-	104.1	-	dB	VCM cap=1uF VDDDAC cap=NC simulation with 32Ω loading Fin=1KHz
	THD+N		-	-93	-	dB	VCM cap=1uF VDDDAC cap=NC simulation with 32Ω loading Fin=1KHz
	Max Output Range		-	-2.4		dBV	32ohm Loading
VCMBUF Mode	SNR			98.2		dB	VCM cap=1uF VDDDAC cap=NC simulation with 32Ω loading Fin=1KHz
	THD+N			-77.6		dB	VCM cap=1uF VDDDAC cap=NC simulation with 32Ω loading Fin=1KHz
	Max Output Range			-8.6		dBV	32ohm Loading

Table 16-9 Audio DAC Expanded Mode Parameters

Mode	Sym	Characteristics	Min	Typ	Max	Unit	Conditions
Differential Mode	SNR		-	104	-	dB	VCM cap=1uF VDDDAC cap=NC simulation with 32Ω loading Fin=1KHz
	THD+N		-	-95	-	dB	VCM cap=1uF VDDDAC cap=NC simulation with 32Ω loading Fin=1KHz
	Output Range	Maximum output voltage	-	0		dBV	32ohm Loading@VCM=1.2V
VCMBUF Mode	SNR			102.7		dB	VCM cap=1uF VDDDAC cap=NC simulation with 32Ω loading Fin=1KHz

Mode	Sym	Characteristics	Min	Typ	Max	Unit	Conditions
	THD+N			-72.5		dB	VCM cap=1uF VDDDAC cap=NC simulation with 32Ω loading Fin=1KHz
	Output Range			-1.9		dBV	32ohm Loading@VCM=1.2V

16.4 Audio ADC Parameters

Table 16-10 Audio ADC Parameters

Mode	Sym	Characteristics	Min	Typ	Max	Unit	Conditions
ADC Mode	SNR		-	102	-	dB	VCM cap=NC VDDMIC cap=1uF tran noise simulation Input -2dBV @ Fin=1KHz
	THD+N		-	-97	-	dB	
	Input Range	Maximum input voltage	-	-2	-	dBVrms	
PGA + ADC DIFF Mode	PGA Gain		-6		42	dB	-6 / 0~42dB@step=3dB
	SNR			94		dB	VCM cap=NC VDDMIC cap=1uF diff input Input 0dBV @ Fin=1KHz PGA Gain=0dB
	THD+N			-86		dB	
	Input Range	Maximum input voltage	-	3	-	dBVrms	
PGA + ADC SINGLE Mode	PGA Gain		-6		42	dB	-6 / 0~42dB@step=3dB
	SNR			92		dB	VCM cap=NC VDDMIC cap=1uF single input Input 0dBV @ Fin=1KHz PGA Gain=0dB
	THD+N			-63		dB	
	Input Range	Maximum input voltage	-	1	-	dBVrms	

16.5 BT Parameters

Table 16-11 BT Parameters

Characteristics	Min	Typical	Max	Unit	Conditions
Transmit Power	-	9	10.5	dBm	
RMS DEVM	-	5.5	-	%	Maximum TX power 2-DH5 packet
Peak DEVM	-	15	20	%	
EDR Relative Transmit Power	-	-0.2	-	dB	
Sensitivity @ Basic Rate	-	-94.5	-	dBm	BER=0.1%, using DH5 packet
Sensitivity @ EDR	-	-94.5	-	dBm	BER=0.01%, using 2-DH5 packet

16.6 Current Parameters

Table 16-12 Current Parameters

Mode	Characteristics	Min	Typ	Max	Unit	Conditions
With DC DC Buck Mode	TX RF Current @Pout = 0dBm		TBC		mA	VBAT=3.3V
	RX RF Current @Sensitivity level		TBC		mA	
	Supply Current @Sleep with RAM retention		TBC		uA	
	Supply Current @Deep sleep		TBC		uA	
	Supply Current @Power Down		TBC		uA	
	Supply Current @Sniff		TBC		uA	500ms interval
	Supply Current @Discoverable		TBC		uA	500ms interval
W/O DC DC LDO Mode	TX RF Current @Pout = 0dBm		TBC		mA	VBAT=3.3V
	RX RF Current @Sensitivity level		TBC		mA	
	Supply Current @ Sleep with RAM retention		TBC		uA	
	Supply Current @Deep sleep		TBC		uA	
	Supply Current @Power Down		TBC		uA	
	Supply Current @Sniff		TBC		uA	500ms interval
	Supply Current @Discoverable		TBC		uA	500ms interval

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