COMPSYS701 Advanced Digital Design, 2025

Individual Project (20%)

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The Individual Project (IP) is related to the research of functionalities that are primary candidates for hardware acceleration of digital signal processing algorithms that will be used as Application Specific Processors (ASP) in Heterogeneous Multiprocessor System-on-Chip (HMPSoC). It has the following requirements on the individual students:

1. Exploring typical functions that are often used in fields such as digital signal processing, identification of those functions that would be of interest for hardware implementation and encapsulation of each function into an Application-Specific Processor (ASP) within the HMPSoC; this ASP will be referred to in the project as Data Processing ASP or DP-ASP.
2. Selection of a function for individual implementation, with the examples of functions specified below, which are related to the application of frequency measurement of the power system in real time [1] (as a case study), and implemented in digital hardware as a part of DP-ASP. Each student's final choice of a specific function to implement as a system component should be co-ordinated with the other members of the group/team. The individually developed component of each member of the team should work together with the functions (components) implemented by the other team members when implementing frequency measurement functionality [1]. The selected function can be executed/invoked by a call from ReCOP, a call from Nios II or configured for automatic chaining and execution on data (stream) coming from the ASPs connected to TDMA-MIN NoC in critical part of HMPSoC.
3. Design of the ASP that implements the selected functions within your DP-ASP; this must include specification of an interface of DP-ASP with the TDMA-MIN NoC, as well as of the protocol how the function can be used.

Application-Specific Processor

Examples of connections of each DP-ASP to the external world are Analogue-to-Digital Converters (ADC) with associated ADC-ASP, Digital-to-Analogue Converter (DAC) with associated DAC-ASP, and similar sources/destinations that can be connected to the ASP directly or encapsulated into specialised ASPs connected to the NoC. Also, specialised ASPs that emulate ADC and DAC enable creation of testbeds for selected functionalities without connecting to the physical world but mimicking operation of the physical world are candidates for these ASPs. For example, instead of connecting frequency measurement unit to a continuous power system signal (voltage), the same functionality can be achieved, for testing purposes, by making an ASP (ADC-ASP) that generates digital samples of the continuous signal using look up tables.

In our frequency measurement application we will deal with "periodic" signal, in this case power system signal. The examples of kernel signal processing operations on the input signal are:

(1) Direct passthrough - taking the input data samples and immediately outputting them to a specified destination over NoC.
(2) Linear Filter – as a moving average filter for input time series sequence which can store the resulting signal to a memory for a further processing. Moving window size is programmable and can be L= 4 or L=8. For the boundaries of array, a solution has to be defined.

$$Y(i) = \frac{\sum \mathrm{X(k)}}{\mathrm{L}}, k = i, i+1, \dots, i+L-1$$

where X represents the input samples.

(3) Correlation function of the time series sequence samples stored in a memory (autocorrelation)

(4) Peak detection - where the recorded time series of input samples (or part of it) stored in an internal memory is processed and outputs the current maximum and minimum values for the specified/sampling period, as well as information on the time between successive peaks

(5) Detection of frequency of the incoming time series based on information from the peak detector

As discussed in the project brief, ASPs will be configured using instructions coming from the ReCOP and/or GPP (Nios II), will operate autonomously to perform their configured task, and may be included into a pipeline of ASPs to achieve more complex signal processing application requirements.

As an example, one configuration might involve four DP-ASPs, where ADC output signal is emulated within ADC-ASP using a look up table, being passed through a linear (averaging) filter ASP, then the autocorrelation ASP to extract some features of the processed signal, and finally to a peak detection ASP, with the peak detection output forwarded via NoC to the Nios II processor, leading to the following configuration that will be established from ReCOP node:

1. The ADC-ASP should be configured to provide time series samples to the ASP performing linear filtering (averaging filter).
2. The AVG-ASP used for linear filtering (averaging) should be configured to linear filter mode, with the output set to the ASP used for input signal autocorrelation, which is slightly modified in frequency measurement into the so called reference point function.
3. The COR-ASP for autocorrelation should be configured to receive the signal from the averaging filter ASP-DSP and forward its output to the peak detection PD-ASP.
4. The PD-ASP used for peak detection (PD) should be configured to peak detect mode, with output set to be forwarded to Nios II for calculating and displaying the final result of processing. Further use of the results which appear as a sequence of values that belongs to a time series is application specific and can be done using software executing on Nios II.

Once this configuration is established, the ADC-DSP will be triggered to periodically output data which will autonomously be passed through the required pipeline of DP-ASPs and the Nios II as the final destination where communication is established through the NoC. Prior to a reconfiguration of the aforementioned pipeline, the ADC-DSP should be deactivated to avoid spurious data travelling through the data pipeline.

Each student, upon agreement with the team/group members, will design one or two of the four introduced ASPs including its core functionality, parameterization for configuration purposes of the design and interfacing to the NoC and higher level interfacing to enable the functional pipeline of the ASPs.

In order to design a DP-ASP, all command responses of the DP-ASP have to be precisely defined and format of all packets exchanged between nodes on NoC (ReCOP, NiOS II and ASPs) be specified. The RTL level model of the DP-ASP has to be defined and it has to include all data storage elements, interface to the NoC (NI), datapath of ASP and its control unit. Analysis of performance/area trade-off (time to perform the operation against the required resources to implement the DP-ASP) for the ASP should be performed and the options of parallelisation, to increase the throughput, of the required operations be discussed, which can be achieved by using more processing elements such as multipliers, adders etc within the datapath.

In the adopted approach to critical part of HMPSoC as specified in the design requirements documents, network interface (NI) for all types of nodes could be identical, and as such can be considered part of NoC fabric.

In some application scenarios, DP-ASPs have to provide internal memory for temporary storage of data (memory array; FIFO or similar). Access to this memory is controlled by dedicated controllers that enable, for example, continuous storage for part of a stream of data of certain length in real-time and making it available for processing within DP-ASPs.

In this individual project (IP) we will assume that the maximum number of nodes connected to the single TDMA-MIN is 8 and the datapath within the NoC fabric allows transfers of 32 bits from any node to any other node at once (in a single clock cycle).

The result of the research has to be presented in the following forms:

- Minimum 4-page single column report (10 pt. font, Times New Roman) that includes the functional description of the selected algorithm(s), diagram(s) of overall DP-ASP structure and its datapath, summary of capabilities, the instructions on how the DP-ASP is used by a third party, and references.
- The design of the DP-ASP; individual designs will be used by the design team to integrate into HMPSoC. The design has to be tested with realistic external requirements implemented within the testbed (in ModelSim) and synthesised into an IP block that can be instantiated in HMPSoC in any number of instances in DE1-SoC. Hardware resource usage and the speed (max clock frequency) of the designed component should be reported.

More details on the frequency measurement and the IP, further explanations and expectation from individual students will be given in lecture time and in direct consultations.

Reference:

1. Z Salcic, R Mikhael, 2000. A new method for instantaneous power system frequency measurement using reference points detection, Electric Power Systems Research, Volume 55, Issue 2, 1 August 2000, Pages 97-102, https://doi.org/10.1016/S0378-7796(99)00102-9, also available on Canvas.

This IP project brief establishes the scope for the IP. Minor further changes may be required and will be published in the weeks before the end of study break.

When making partitioning of the frequency measurement circuitry students can consult the lecturers and Tas and also make their own proposals.