Lab 1: Introduction to Verilog HDL

Objective

- ✓ Review fundamental logic components.
- ✓ Introduce Verilog HDL modeling and verification.

Prerequisite

- ✓ Fundamentals of logic gates.

Experiments

1 Design and verify a BCD-to-Excess-3 code converter (input: **abcd**, output: **wxyz**, **a** and **w** are the MSB).
   1.1 Write the Boolean function/logic equation.
   1.2 Draw the related logic diagram.
   1.3 Construct the Verilog RTL code for the converter and use a testbench to simulate the logic behavior for verification.

2 Design and verify an unsigned 2-bit x 2-bit binary multiplier (multiplicand **a** (a_1a_0), multiplier **b** (b_1b_0), and product **c** ($c_3c_2c_1c_0$)).
   2.1 Write the Boolean function/logic equation.
   2.2 Draw the related logic diagram.
   2.3 Construct the Verilog RTL code for the multiplier and use a testbench to simulate the logic behavior for verification.

3 Design a 3-bit binary adder/subtractor with input **a** ($a_2a_1a_0$), **b** ($b_2b_1b_0$), m as the operator control (0 for addition and 1 for subtraction); output **s** ($s_2s_1s_0$), **v** as overflow indicator.
   3.1 Write the Boolean function/logic equation.
   3.2 Draw the related logic diagram.
   3.3 Construct the Verilog RTL code for the function and use a testbench to simulate the logic behavior for verification.

4 (Bonus) For two 3-bit unsigned numbers **a** ($a_2a_1a_0$) and **b** ($b_2b_1b_0$), build a logic circuit to
5 output **o**($o_2o_1o_0$) as the smaller number and use a testbench for verification.

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