Lab 4: Counters and Shifters II

Objective

- ✓ Review sequential circuits.
- ✓ Review shift registers.

Prerequisite

- ✓ Fundamentals of logic gates.
- ✓ Clocking concepts
- ✓ Logic modeling in Verilog HDL.

Experiments

1 Construct a 4-bit synchronous binary up counter ($b_3b_2b_1b_0$) with the 1-Hz clock frequency from lab2 and use 4 LEDs for display.

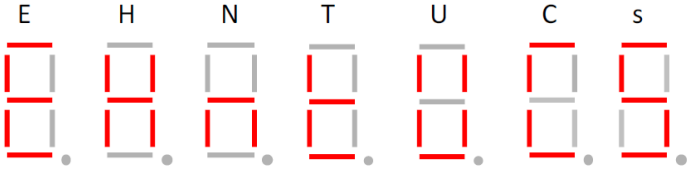
I/O	$f_{crystal}$	b_3	b_2	b_1	b_0
Site	W5	V19	U19	E19	U16

2 Combine the 4-bit synchronous binary up counter from exp1 with a binary-to-seven-segment-display decoder (from lab2-exp3) to display the binary counting in 7-segment display.

3 Construct a single digit BCD **up** counter with the divided clock as the clock frequency and display on the seven-segment display.
- 3.1 Construct a BCD up counter.
- 3.2 Construct a BCD-to-seven-segment display decoder (from lab2-exp2).
- 3.3 Combine the above two together.

4 Construct a single digit BCD **down** counter with the divided clock as the clock frequency and display on the seven-segment display.
- 4.1 Construct a BCD up counter.
- 4.2 Construct a BCD-to-seven-segment display decoder (from lab2-exp2).
- 4.3 Combine the above two together.

5 Use the idea from pre-lab2. We can do something on the seven-segment display. Assume we have the pattern of E, H, N, T, U, C, S for seven-segment display as shown below. Try to implement the scrolling pre-stored pattern NTHUEECS with the four seven-segment displays.



6 (Bonus) Construct a 30-second count down timer (stop at 00).

TA: _____

