Lab 5: Timer and Stopwatch I

Objective

- ✓ Review sequential circuits.
- ✓ Review finite state machine (FSM).

Prerequisite

- ✓ Fundamentals of logic gates.
- ✓ Logic modeling in Verilog HDL.

Pre-labs

1 Construct a 30-second down counter with pause function. When the counter goes to 0, all the LEDs will be lighted up. You can use one push button for reset and one other for pause/start function.
   1.1 Write the spec (inputs, outputs, and function table) of the design.
   1.2 Draw the related block/logic diagram.
   1.3 Use a FSM to implement the function of pause/start function. Use one LED to represent current state.
   1.4 Use Verilog to implement 1.3 and verify the design with simulation results.

Experiments

1 Construct a 30-second down counter with pause function. When the counter goes to 0, all the LEDs will be lighted up. You can use one push button for reset and one other for pause/start function.
   1.1 Implement a periodic 30-second down counter and demo with the FPGA board.
   1.2 Implement Prelab 1.3 and demo with the FPGA board.
   1.3 Combine 1.2 and 1.3 to finish the experiment.

2 The same function as Exp. 1. Instead of using two push buttons for reset/pause/start, try to use just one push button to finish the design. (Hint: You can press the push button longer to represent the reset)

3 (Bonus) Use two push buttons to control a multi-function stop timer (mode selection, reset, start, stop). The stop timer has two modes: 30-second/1-minute countdown. When being reset, the seven-segment display shows the digits 30/1:00. When the timer counts to 0, it will stop.
   3.1 List the specification of the detector.
   3.2 Design the FSM used in this design.
   3.3 Draw the block diagram/logic schematic.
   3.4 Implement the stop timer with FPGA demo board.

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