Lab 6: Timer and Stopwatch II

Objective

- ✓ Implement the timer and stopwatch functions.

Prerequisite

- ✓ Fundamentals of logic gates.
- ✓ Logic modeling in Verilog HDL.
- ✓ Simple logic development and FSM control

Experiments

1 Implement a stopwatch function (00:00-59:59) with the FPGA board.
  1.1 Use the four (Seven-Segment Displays, SSDs) as the display. The left two digits represent the minute and the right two digits represent the second.
  1.2 Use two push buttons to control the function. Use one button to control start/stop and the other to control the lap and reset. When the stopwatch counts, press the 'lap' button will freeze the SSDs but the stopwatch continues counting, and when press the 'lap' button again, the SSDs will start to show current time.

2 Implement a timer (can support as long as 23:59) with the following functions.
  2.1 Use one DIP switch as the 'setting' control. When the 'setting' is ON, you can use two buttons to set the minute and second.
  2.2 Use other two buttons to control the timer operation. One button for start/stop and the other button for pause/resume.
  2.3 When the time goes to 0, light up all the LEDs.

3 (Bonus) Integrate the above two functions together with only three buttons.

- Note: You can use one addition button for reset in this lab.

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