A Design for High Speed Leading-Zero Counter

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***Abstract*—Leading-zero counter (LZC) is a basic component in floating point operation. This paper aims at speeding up the operation of LZC. Based on new derived Boolean functions and complex logic gates, 8-bit LZC circuit is accomplished. Moreover, 16-bit LZC architecture is implemented in Xilinx field-programmable gate array (FPGA) and 32-bit LZC structure is realized on the platform of Application Specific Integrated Circuit (ASIC) in 65nm technology. Synthesis results are obtained on their special platforms. By comparison, our proposed design is faster than the reported designs.**

***Index Terms*—floating point unit, leading-zero counter, leading-zero detector and logic gate**

I. Introduction

Leading-zero counter (LZC) has wide application in many aspects. LZC is an essential element in floating-point arithmetic such as add and subtract [1] [2]. And it is also used to test circuit performance of leading-zero anticipation and detection [3] [4]. Moreover, counting leading-zero is a special instruction in some certain types of processor. So, the research of fast LZC design is necessary and there are some investigations about it. [3] implements the function through suggested multiplexer. [4] compares the circuit performances designed by logic gate and the suggested multiplexer. [5] gives the simplified equations and its architecture is the fastest at that time. And then improved circuits [6] and [7] are completed in new logic architectures separately. Both of them are faster than the contrast design [5].

In this paper, section I gives the research status about LZC. Section II introduces the function of LZC and section III presents the proposed architectures. Next, comparison and analysis about simulation results are presented in section IV. In section V, a conclusion is given.

II. Principle and general design of LZC

Leading-zero is the consecutive zeros from the most-significant bit (MSB) to the first non-zero digital in a binary number. Function of leading-zero counter is to calculate the amount of zeros.

For a circuit input denoted as $A_7A_6A_5A_4A_3A_2A_1A_0$, whose MSB is on the left end. Thus, the number of zero is calculated from the left. $VZ_2Z_1Z_0$ is the output of the 8-bit LZC circuit. Output bits are associate with input bits. When all input bits are zero, V is marked to one. For other situations of input, value of $Z_2Z_1Z_0$ can be used to indicate them.

In the case of $A_7 \cdots A_0$=00000000, number of leading-zero is eight signed as $(1000)_2$. Subscript 2 means that the number is represented in binary form. And in the other case $A_7 \cdots A_0$=00001000, the output bits can be written as $(0100)_2$. Therefore, the general relationships between input $A_7A_6A_5A_4A_3A_2A_1A_0$ and output $VZ_2Z_1Z_0$ are obtained in accordance with the above description. For the 8-bit LZC circuit, Boolean functions are expressed as the followings:

$$\overline{V} = A_7 + A_6 + A_5 + A_4 + A_3 + A_2 + A_1 + A_0 \quad (1)$$

$$\overline{Z_2} = A_7 + A_6 + A_5 + A_4 \quad (2)$$

$$\overline{Z_1} = A_7 + A_6 + \overline{A_5} \cdot \overline{A_4} \cdot (A_3 + A_2) \quad (3)$$

$$\overline{Z_0} = A_7 + \overline{A_6} \cdot A_5 + \overline{A_6} \cdot \overline{A_4} \cdot A_3 + \overline{A_6} \cdot \overline{A_4} \cdot \overline{A_2} \cdot A_1 \quad (4)$$

III. Proposed LZC structure design

As far as we know, reducing the number of logic gates on the longest path can speed up the operation. Latency of various logic gates are distinct. Exploring different circuit implementations and executing the circuit as soon as possible is out work. So 8-bit LZC circuit can be accomplished by complex logic gates instead of simple logic gates such as OR and AND.

Seen from equations (1)-(4), the longest path of 8-bit LZC circuit is the path from inputs to $\overline{Z_0}$. The last two items in formula (4) have a similar part $\overline{A_6} \cdot \overline{A_4}$ which can be merged into one. Furthermore, AND gate consists of NAND and NOT gates, and OR gate is composed of NOR and NOT gates. Thus, the remaining parts $A_3+\overline{A_2}\cdot A_1$ and $A_7+\overline{A_6}\cdot A_5$ of formula (4) can be implemented by the complex logic gate $A_3 + \overline{A_2} \cdot A_1$ which is integrated with these simple logic gates AND and OR. In addition, $\overline{A} + \overline{B} \cdot \overline{C}$ can be replaced by $\overline{A \cdot (B + C)}$. Therefore $\overline{Z_0}$ is expressed as equation (5).

$$\overline{Z_0} = \overline{\overline{A_7 + (\overline{A_6} \cdot A_5)} \cdot [(A_6 + A_4) + \overline{A_3 + (\overline{A_2} \cdot A_1)}]} \quad (5)$$

Using the above method to simplify $\overline{Z_1}$, formula (3) can be written as formula (6). For $\overline{Z_2}$, we realize it by NOR and NAND gates rather than OR gates. The improved structure of $\overline{Z_2}$ is presented as formula (7). In the same way, $\overline{V}$ can be implemented as $\overline{Z_2}$. Thus, equation $\overline{V}$, after simplify, is written as expression (8).

$$\overline{Z_1} = \overline{\overline{A_7 + A_6} \cdot [(A_5 + A_4) + \overline{A_3 + A_2}]} \quad (6)$$

$$\overline{Z_2} = \overline{\overline{A_7 + A_6} \cdot \overline{A_5 + A_4}} \quad (7)$$

$$\overline{V} = \overline{\overline{A_7 + A_6} \cdot \overline{A_5 + A_4}} + \overline{\overline{A_3 + A_2} \cdot \overline{A_1 + A_0}} \quad (8)$$

The proposed architecture of the 8-bit LZC circuit is constructed as Fig.1. In picture, a normal NOR gate and an adjacent small AND gate which contains a tiny circle are as a combination which represents the complex logic gate

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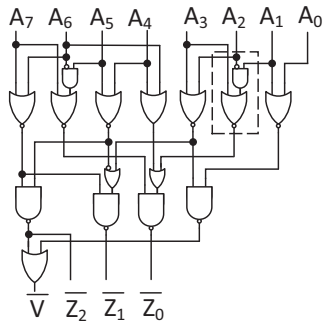

Fig. 1: The proposed structure of 8-bit LZC

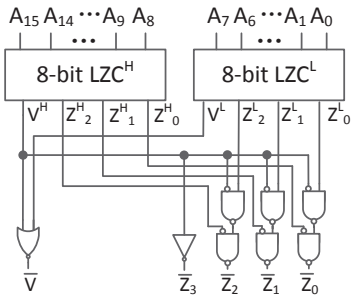

Fig. 2: The proposed structure of 16-bit LZC

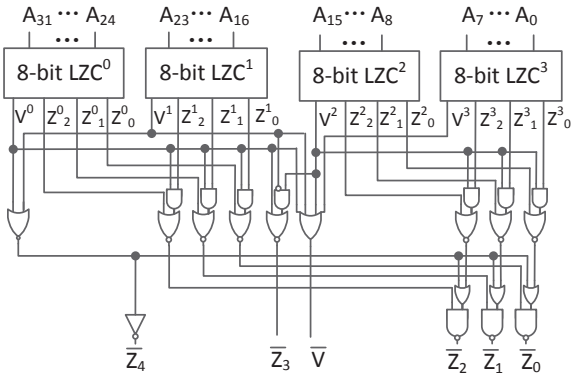

Fig. 3: The proposed structure of 32-bit LZC

TABLE I: Results and comparison about different designs

Design	Platform	Input	Delay
[5]	XC3S250E	16-bit	14.293ns
[6]	XC3S250E	16-bit	11.189ns
this work	XC3S250E	16-bit	9.018ns
[5]	65nm-TSMC	32-bit	0.512ns
[7]	65nm-TSMC	32-bit	0.408ns
this work	65nm-SMIC	32-bit	0.230ns

$\overline{A_3 + \overline{A_2} \cdot A_1}$. The tiny circle denotes logic NOT. Another complex logic gate $\overline{A \cdot (B + C)}$ is signified in an overall which is composed by a small OR gate and an adjacent normal NAND gate.

Moreover, we also construct 16-bit and 32-bit LZC circuits. The 16-bit LZC circuit is built by NAND gate as shown in Fig.2. Besides, the 32-bit LZC circuit is composed by two kinds of complex logic gates illustrated as Fig.3. To both of them, 8-bit LZC is used as the basic component unit.

IV. Result

Circuits are described with Verilog HDL. Using the proposed structure, we implement the 16-bit LZC circuit in Xilinx ISE on the family of Sparan3E and the FPGA device is XC3S250E on the package of FT256 with the speed -4. In addition, 32-bit LZC circuit is completed in design compiler based on SMIC 65nm technology.

Synthesis results are obtained on special platforms and listed in Table 1. Compared with the latency, we know that our designs of 16-bit and 32-bit LZC circuit are faster than the reported designs.

V. Conclusion

The LZC is the basic component in floating point processor. All of the floating point adder and subtractor are depend on the LZC. Therefore, research to accelerate the LZC is essential. In this paper, 8-bit LZC circuit structure is simplified using complex logic gate. Based on this, 16-bit and 32-bit LZC circuits are also simulated. Synthesis results show that our designs have better performance than the reported designs in delay. This improvement is useful in floating point processor.

Acknowledgment

This work is supported by the National Natural Science Foundation of China under Grant No.61674086.

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