Andrew Li

andyli@mit.edu • 402-979-2488 • https://andrewli.dev

EDUCATION

Massachusetts Institute of Technology (MIT) **2021 – 2025**

B.S. in Electrical Engineering and Computer Science (4.9/5.0)

- Digital System Design (FPGAs), Performance Engineering (C/x86), Distributed Systems, Operating Systems, Computer Architecture, Signal Processing, Nanoelectronics, Electromagnetism Applications

EXPERIENCE

Undergraduate Researcher, MIT CSAIL – Cambridge, MA **Feb 2024 – Present**

- Implementing training on an FPGA DNN accelerator with photonic matrix multiplication testbed
- Writing Verilog modules to perform quantized stochastic gradient descent simulated with Verilator
- Setup custom PetaLinux build, DDR4 and CMAC (100Gbps) IP cores on Xilinx Zynq UltraScale+ RFSoC

Software Engineer Intern, Expensify, Inc. – New York, NY **Jun 2023 – Dec 2023**

- Worked with SQLite team to speed up queries in login API command from over a second to <10ms
- Optimized new expensive hashing compliance requirements with 50% reduction in API timings
- Implemented mobile receipt upload and scan feature for a conference with 1-month turnaround
- Reviewed PRs and wrote design specifications for new features

Software Engineer Intern, Palo Alto Networks – Santa Clara, CA **May 2022 – Aug 2022**

- Created customer data access control system for Global Customer Support (GCS) team
- Integrated system with roles, permissions, scopes into existing SAML/Kubernetes infrastructure
- Wrote design specifications and onboarded new team member to hand off project

PROJECTS

Voxos

- Designed an FPGA-based vocoder instrument with hi-fi audio synthesis and external MIDI support
- Implemented custom audio signal processing pipeline without IP capable of hi-fi 24-bit at 48kHz
- Implemented USB2.0 host controller and audio I/O drivers (SPI, I2S, UART) from datasheets
- Learned audio processing techniques and MATLAB for filter design in under 1 month
- Wrote testbenches in SystemVerilog and Verilator to verify filter designs frequency response

Fenix

- Developed RTOS for STM32 Cortex-M7 chip to learn bare-metal systems and freestanding C
- Wrote ethernet driver, network stack with MAC, ARP, ICMP, IP, and basic TCP support without HAL

WHS Scheduler

- Created iOS/Android app with >10,000 downloads for Westside High School students to track their day
- Reverse-engineered legacy ASP.NET web app to scrape and process schedules
- Maintained app and worked with school administration for 5 years

SKILLS

Languages	C/C++, x86/ARM ASM, Python, JavaScript, TypeScript, PHP, SystemVerilog, MATLAB, SQL
Software	Docker, GCC/GDB, Altium, Vivado, AWS, Azure, React, React Native, ESP-IDF
Misc.	Writing documentation, reading datasheets/code, quick learner, teaching, jazz saxophone

AWARDS

MIT Emerson Jazz Fellow, MIT Philip Loew Award for Creative Accomplishment, National YoungArts Winner