

Agenda

1. i.MX6 HW Design Reference Board. (go through schematic of i.MX6 SDP)
2. i.MX6 Hardware Development Guide. (IMX6DQ6SDLHDG.pdf)
3. i.MX HW Checking List. (Excel file of i.MX6 HW Design Checking List)
4. i.MX6 Power design
5. DDR Calibration and Stress Test.
6. IOMux Tool
7. i.MX6 Hardware bring up



i.MX 6 HW Design Reference Board

Related Hardware materials

- SABRESDP_DESIGNFILES.zip/SABRE_AI_DESIGNFILES.zip: SDP/AI board schematic/layout.
- IMX6DQ6SDLHDG.pdf: i.MX6 hardware design guide, include schematic/layout checkpoints, iomux tools, Bring up, IBIS/BSDL, RMI interface.
- IMX6DQ/DLS_AI/CEC.pdf: i.MX6 Datasheet: include chipset electrical Characteristics like the voltage range, Max current and Power sequence.
- IMX6DQ/DLS_RM.pdf: i.MX6 Chipset reference manual.
- AN4509: i.MX6DQ Power Consumption Measurement.
- AN4576: i.MX6DLS Power Consumption Measurement.
- IMX6_IOMUX_TOOL: iomux configuration tools.
- Mfgtools-Rel-4.1.0_130816_MX6Q_UPDATER.tar.gz: MFG tools.
- L3.0.35_4.1.0_130816_images_MX6.tar.gz: linux demo image.
- HW Design Checking List for i.Mx6 Rev2.6.xlsx: i.MX6 hardware check list, download from : <https://community.freescale.com/docs/DOC-93819>
- DDR_Stress_Tester_v1.0.2.zip: DDR test tools, download from: <https://community.freescale.com/docs/DOC-96412>
- i.Mx6DQSDL DDR3 Script Aid: DDR configuration tools, Download from: <https://community.freescale.com/docs/DOC-94917>
- Freescale i.MX6 DRAM Port Application Guide-DDR3 <https://community.freescale.com/docs/DOC-101708>

i.MX6 Reference Solution Related Material

Freescalr • i.MX Applications Processors • i.MX 6 Series Processors • RDBMX6SABREPLAT

SABRE Platform for Smart Devices Based on the i.MX 6 Series

Overview Documentation **Software & Tools** Buy / Parametrics

Buy Export to Excel Expand All Sections

Jump Start Your Design

- Get Started With SABRE-SDP and Google Android OS
Unleash the power of the i.MX 6 Series using the new SABRE-SDP development...

Popular with Other Engineers

- i.MX 6SoloLite Evaluation Kit
- i.MX 6 Series Software and Development Tool Resources
- Design files, including hardware schematics, Gerbers, and OrCAD files.
- Design files, including hardware schematics, Gerbers, and OrCAD files.

Show ▾

Hardware Development Tools (4) Expand All	Sort by Modified Date
Printed Circuit Boards and Schematics-Schematics (1)	(2)
Programmers (Flash, etc.) (3)	(3)

Software Development Tools (7) Expand All	Sort by Modified Date
Debuggers and Runtime Analysis (1)	
IDE - Debug, Compile and Build Tools (2)	
Initialization/Boot/Device Driver Code Generation (1)	
Lab and Test Software (1)	
Snippets, Boot Code, Headers, Monitors, etc. (2)	

Run-time Software (18) Expand All	Sort by Modified Date
Operating System Software-Board Support Packages (12)	(4)
Middleware-Codecs and other Algorithms (6)	

1. Select “SABRE Platform for Smart Devices”
2. Hardware Material (Schematic, PCB, Gerber. etc);

SABRE Board for Smart Devices (SDB)

i.MX 6Quad 1Ghz Cortex-A9 Processor

- Can be configured as i.MX 6Dual
- Freescale MMPF0100 PMIC
- 1 GB DDR3 memory (non terminated)
- 3" x 7" 8-layer PCB

Part Numbers: MCIMX6Q-SDB (\$399)

Display (9.7"): MCIMX-LVDS1 (\$499)

Display (4.3"): MCIMX28LCD (\$199)

Display connectors

- 2x LVDS connectors
- Connector for 24 bit 4.3" 800x480 WVGA with 4-wire touch screen
- HDMI Connector

Audio

- Wolfson Audio Codec
- Microphone and headphone jacks

Expansion Connector

- Camera CSI port signals
- I2C, SSI, SPI signals



Tools Support

- Lauterbach, ARM (DS-5), Macraigor debug/IDE tool chain

Connectivity

- 2x Full-size SD/MMC card slot
- 22-pin SATA connector
- 10/100/1000 Ethernet port
- 1x high-speed USB OTG port
- mPCI-e connector

Debug

- JTAG connector
- Serial to USB connector

Additional Features

- 3-axis Freescale accel
- eCompass
- Power supply
- No battery charger

OS Support

- Linux and Android IceCream Sandwich from Freescale;
- Others: support by 3rd parties

SABRE Platform for Smart Devices (SDP)

i.MX 6Quad 1GHz Cortex-A9 Processor i.MX 6DualLite 1GHz Cortex-A9 Processor

- Freescale MMPF0100 PMIC
- 1 GB DDR3 memory (non terminated)
- 3" x 7" 8-layer PCB

Part Numbers:

MCIMX6Q-SDP (\$999)
MCIMX6DL-SDP (\$999)

Display (4.3"): WiFi:

MCIMX28LCD (\$199)
Silex WiFi module

Display connectors

- Native 1024x768 LVDS display (comes with kit)
- 2nd LVDS connector
- Connector for 24 bit 4.3" 800x480 WVGA with 4-wire touch screen
- HDMI Connector
- MIPI DSI connector

Audio

- Wolfson Audio Codec
- Microphone and headphone jacks
- Dual 1W Speakers

Expansion Connector

- Enables parallel LCD or HDMI output
- Camera CSI port signals
- I2C, SSI, SPI signals

Tools Support

- Lauterbach, ARM (DS-5), Macraigor debug/IDE tool chain

Connectivity

- 2x Full-size SD/MMC card slot
- 22-pin SATA connector
- 10/100/1000 Ethernet port
- 1x high-speed USB OTG port
- mPCI-e connector

Debug

- JTAG connector
- Serial to USB connector

Additional Features

- 3-axis Freescale accel
- GPS receiver
- Ambient Light Sensor
- eCompass
- Dual 5MP Cameras
- Power supply
- Battery Charger
- Battery connectors

OS Support

- Linux and Android IceCream Sandwich from Freescale;
- Others: support by 3rd parties



SABRE Platform for Automotive Infotainment (AI)

CPU Card Details

• Power and Memory

- Freescale MMPF0100 PMIC
- 2 GB DDR3 memory (i.MX 6Dual/Quad)
- 1GB DDR3 memory (i.MX 6Solo)
- 32MB Parallel NOR Flash
- NAND Socket

Display

- LVDS connector
 - compatible with MCIMX-LVDS1
- Parallel RGB display interface
- HDMI output connector

Debug

- JTAG connector
- Debug UART connector

Connectivity and Expansion

- SD Card Slot
- High Speed USB OTG
- Ethernet
- SATA
- MIPI CSI
- PCIe
- MLB150 INIC connector
- 281-pin MXM card edge connector for main board expansion

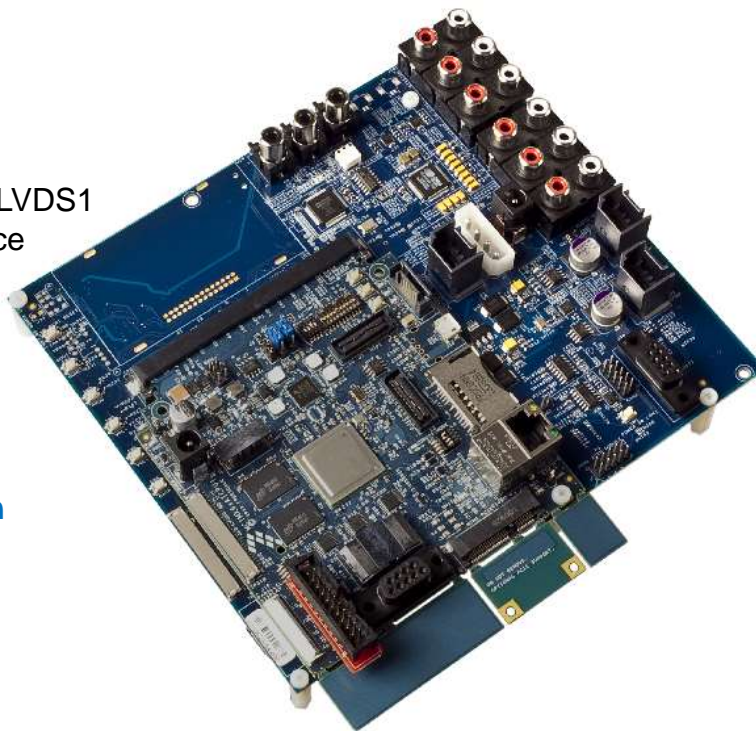
Part Numbers

Base Board: MCIMXABASEV1 (\$699)

CPU Cards: MCIMX6SAICPU1 (\$799)

MCIMX6QAICPU1 (\$799)

Display: MCIMX-LVDS1 (\$499)



Base Board Details

Can be reused from i.MX53 SABRE AI Connectivity and Expansion

- SD card slot (WiFi module or SD)
- Bluetooth or Bluetooth+WiFi header
- AM/FM tuner header
- Sirius XM Module header (de-pop'd)
- GPS (UART) module connector
- 2x CAN
- Dual High Speed USB Host connectors
- MLB 25/50 INIC connector
- SPI NOR flash

Display I/O

- LVDS connector
 - compatible with MCIMX-LVDS1
- Analog Video Input
- LVDS Input

Audio

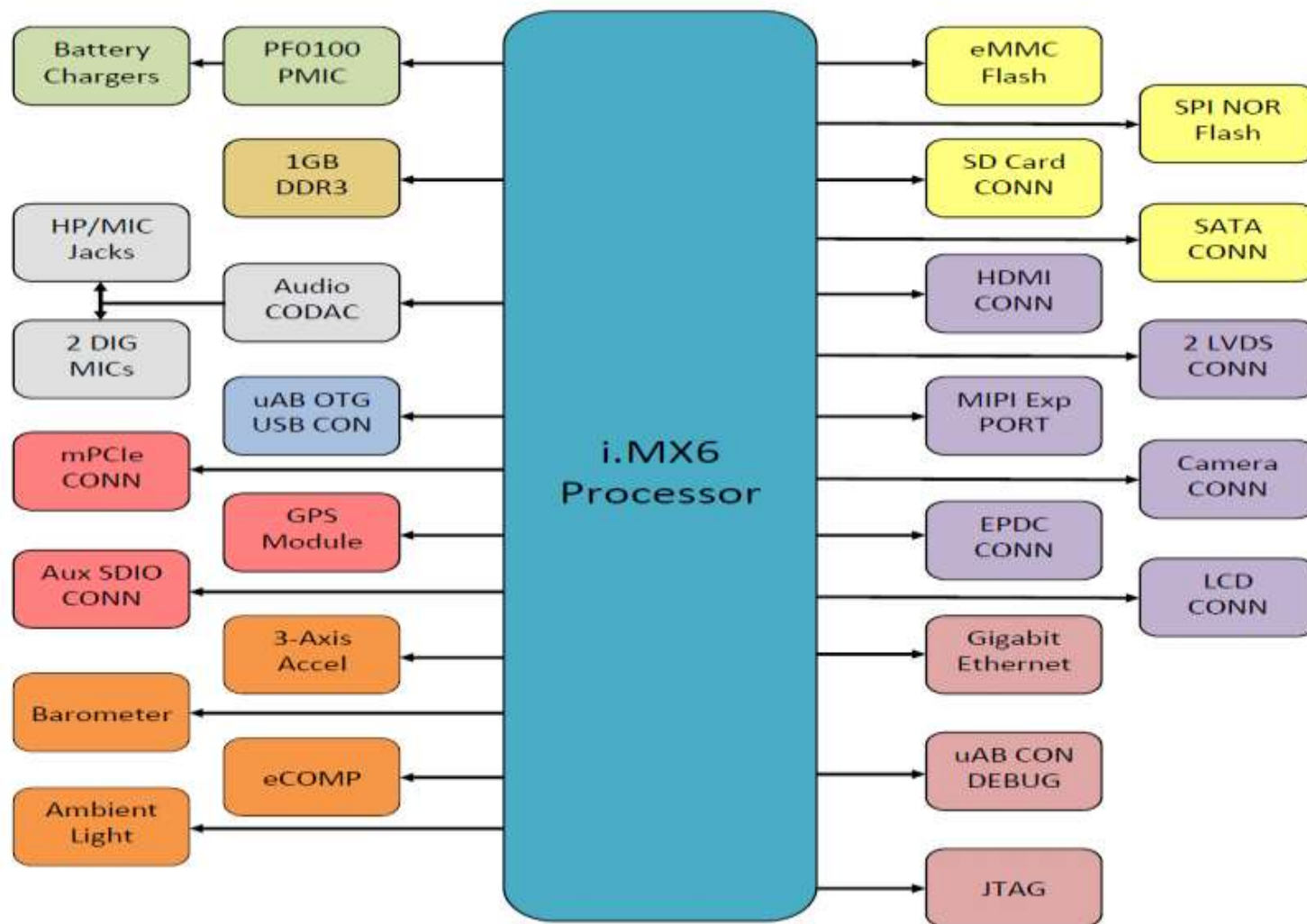
- Cirrus multichannel audio codec
 - Up to 8 outputs
 - Dual microphone inputs
 - Stereo Line Level Input
- SPDIF receiver

OS Support

- Linux
- Others: future support by 3rd parties

i.MX6 SMART DEVICE SYSTEM Block Diagram

Smart Device System Block Diagram



i.MX6 SMART DEVICE SYSTEM Schematic

- Here, open i.MX6 SabreSD Schematic, go through it.



i.MX 6 Hardware Development Guide

Suggestion:

- Pre-design:
Study the datasheet, power consumption, schematic to understand our chipset requirement.
- In-design:
Check the hardware design guide, iomux tools
- After-design:
Fill the HW design checking list, provide the iomux data to software.
- Hardware-bring up:
Check the power, power sequence, clock, reset, provide the boot configuration to software, run ddr test.
- Debug port: Suggest to have
 1. USB OTG Port: For image program, You can use it as USB host port, no problem. MFG just use USB device mode.
 2. Debug serial port, i.MX6 uboot can change to support every serial port as debug port.
 3. Sdcard slot: Suggest to keep at least one Sdcard slot, it will help to use the Sdcard boot, which can burn image directly from PC to Sdcard. No need to debug the MFG kernel.
 4. Jtag(optional).
 5. Suggest to use the GPIO Boot_cfg but not the fuse Boot_cfg. And boot mode pin can be pulled, because we can use the non-image boot to enter the download mode

i.MX6 Hardware Development Guide

- 1). Design Checklist
- 2). i.MX 6 Series Layout Recommendations
- 3). Requirements for Power Management
- 4). Avoiding Board Bring-up Problems

Here, open <<IMX6DQ6SDLHDG.pdf>>, go through it.



i.MX HW Checking List

i.MX HW Checking List

- Here, open << HW Design Checking List for i.Mx6 Rev2.6.xlsx>>, go through it.

Clear	1	Is voltage level matched on bus/signal/logic/buffer two side?
Clear	2	Suggest drawing pull-ups near pin area with power domain description in schematic.
Clear	3	Please take care clock source can meet requirement of peripheral devices. (frequency/driving capability/jitter/tolerance/fly-time etc.)
Clear	4	When Buffer/Level shifter/switch are used, SI impact on signal should be considered.
Clear	5	The control signals polarity for Direction Select/EN/RESET should be checked for all the devices.
Clear	6	IO configuration should be checked using IOMUX Tool which provided by Freescale.
Clear	7	The TEST and FAULT mode inputs of the individual chips should be tied to the proper level for normal operation.
Clear	8	Pin sequence/direction/genders of connector should be confirmed with Mechanical consideration.
Clear	9	Pull-ups and voltages should be verified for OC/OD signals.
Clear	10	Proper pull-up and pull-down resistor values provided to avoid excess sourcing or sinking current.
Clear	11	The polarities of the caps and diodes connected to -ve voltages should be verified.
Clear	12	Suggest all active low signals--include “_B” at end of the signal net name and all clock signals include “CLK” as part of net name.
Clear	13	Please confirm if all power source have sufficient power capacity and good enough ripple noise level for requirement of power input.
Clear	14	Power on/off sequencing should be verified when multiple power sources are used.
Clear	15	The current rating of Diodes/Inductors used in the power supply and other high current sections should be provided properly.
Clear	16	Please pay attention on EMI/EMC/ESD/Lightning consideration (decoupling caps/TVS diodes/chokes/filters/beads/fuses etc).
Clear	17	Please confirm if unused pins are configured properly following formal recommend.
Clear	18	Please confirm boot mode and configuration pins are set properly and can meet the actual boot requirement.
Clear	19	Please take care watch dog/cold/key reset system design, PMIC and boot device also should be reset at same time.

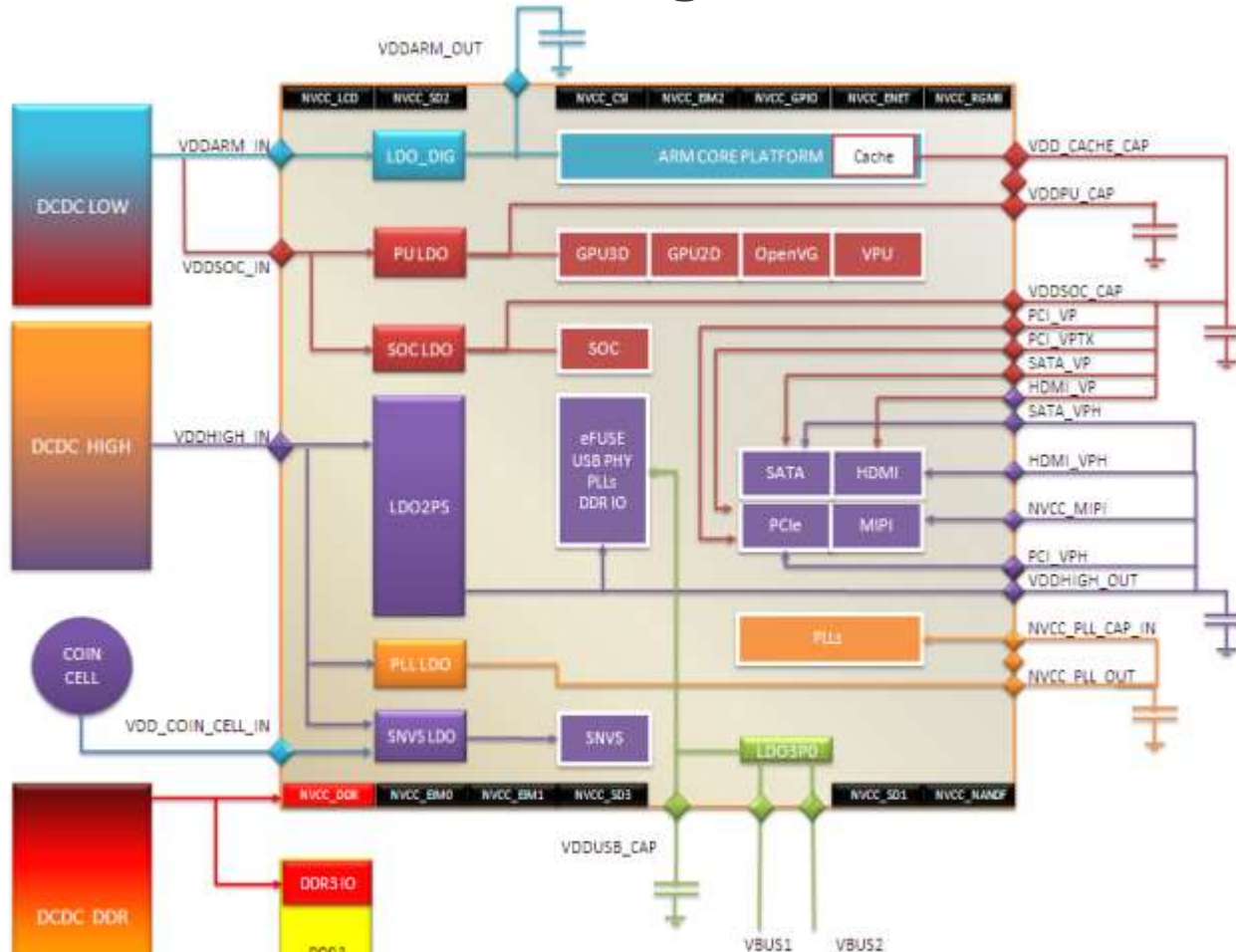


i.MX 6 Power Design

i.MX 6 Power Related doc

- IMX6DQCEC.pdf: i.MX 6Dual/6Quad Applications Processors for Consumer Products
- AN4509.pdf: i.MX 6Dual/6Quad Power Consumption Measurement
- IMX6SDLCEC.pdf: i.MX 6Solo/6DualLite Applications Processors for Consumer Products
- AN4576.pdf: i.MX 6DualLite Power Consumption Measurement
- SDP schematic(PF0100): SPF-27392.pdf
- Saberlite schematic(Discrete DCDC)(from boundarydevices)
- IMX6DQ6SDLHDG.pdf(optional): Design Checklist: Table 2-6. Power and decouple recommendations

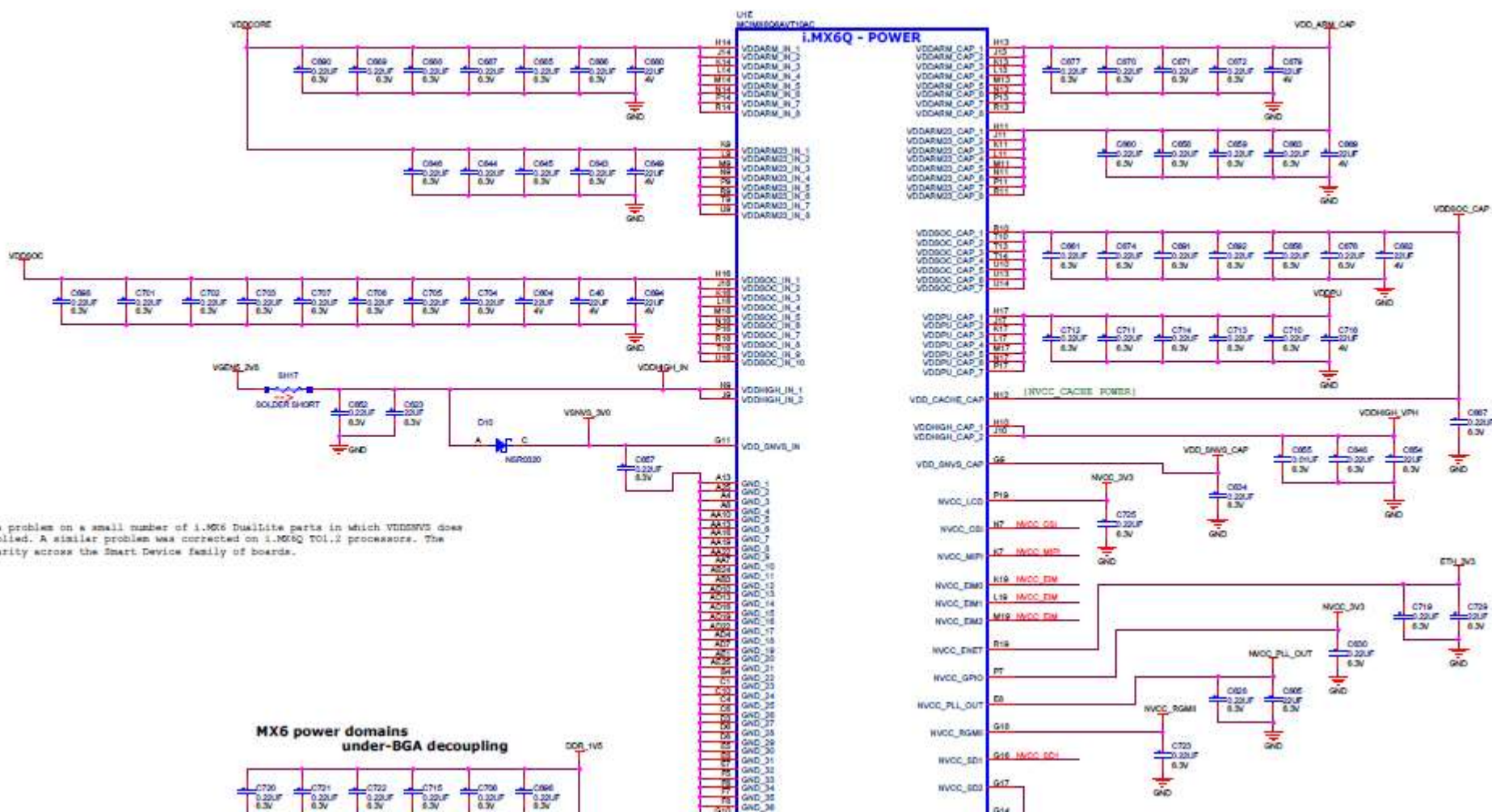
i.MX6 Dual/Quad: Integrated PMU



- **Just two external power rails**
 - Optional SRTC coin-cell rail
 - Optional USB PHY rail
- **Internal DVS and Power-Up Sequence and Reset. No need in 'smart' PMIC.**
- **All external supply rails could be shared with system components**
- **Two stage power conversion: external DCDC pre-regulation, integrated LDOs (incl. DVS)**
- **Total system level power delivery efficiency (including linear regulators) is similar to typical DCDC based PMU**
 - 90% or better in high power mode with internally bypassed FET
 - Better than 65% in low power modes

- **Lowest BoM – no multiple inductors, few external capacitors,**
- **System level: low cost PMIC or few discrete DCDC**
- **Maximal flexibility in power management system design**

Power Supply, and Common Hardware Design



i.MX 6 System - Power Design Considerations

- System Power Requirements(on each power rail)
 - Max Current requirement
 - Voltage range
- System Over-Voltage Protection
- Power On Sequencing
- System control functions
- Layout& decouple

i.MX 6 Power Rail Requirements

- To Function properly, the i.MX6 Processor requires nine different power rails (Some may be combined)
 - VDDARM
 - Power to ARM Cores
 - Allowed voltage: 0.9V – 1.5V
 - VDDSOC
 - VP Power to on chip System Peripherals (VDDSOC_CAP):
 - HDMI PHY, SATA PHY, PCIE PHY, & ARM Core Cache
 - Power to Image processing modules (VDDPU_CAP)
 - VPU, GPU2D, GPU3D, OpenVG
 - Allowed voltage: 0.9V – 1.5V

i.MX 6 Power Rail Requirements (con)

– VDDHIGH

- VPH Power to on chip System Peripherals (VDDHIGH_CAP)
 - MIPI, HDMI, SATA, PCIE, LVDS, USB, PLLs
- Power to misc Peripherals (NVCC_PLL_OUT)
 - USD, PLLs, 24 MHz Osc.
- Shared power of SNVS module
- Allowed voltage: 2.7V – 3.3V

– VSNVS

- 32 KHz Oscillator and SRTC functions
- Shared power of SNVS module
- Allowed voltage: 2.8V – 3.3V

i.MX 6 Power Rail Requirements (con)

- USB_H1/OTG_VBUS
 - Power to USB PHY
 - Allowed voltage: 4.4V – 5.25V
- NVCC_DRAM
 - Power supply for DRAM memory
 - Allowed voltage: 1.14V – 1.575V (Depends on type DRAM)
- Ethernet IO pins (NVCC_RGMII)
 - Allowed voltage: 1.14 – 1.9V
- General IO pins (NVCC_)
 - Typically 1.8V or 3.3V
 - Allowed voltage: 1.65V – 3.6V

i.MX 6 Power Rail Requirements - Summary

- In a typical application, six different voltages are required for the processor to function:

Function	Typical Voltage
VDDARM, VDDSOC	1.375V
VDDHIGH, VSNVS	3.0V
USB_VBUS	5.0V
NVCC_DRAM	1.5V
NVCC_3.3V	3.3V
NVCC_1.8V	1.8V

i.MX6 Power Requirements – VDDARM, VDDSOC

- Datasheet Max Requirements for VDDARM:
 - 3920 mA (Based on Power Virus Operation)
 - 2270 mA (Based on Drhystone Operation)
- Datasheet Max Requirements for VDDSOC:
 - 1890 mA
- Typical Maximum Current Requirements (AN4509):
 - Showing three separate video outputs
 - 1080p Video playback HDMI
 - 1080p Video playback IPU Parallel port (LCD)
 - 3D graphics through LVDS port
 - VDDARM: 1625 mA
 - VDDSOC: 1250 mA

i.MX6 Power Requirements – VDDHIGH, VSNVS

- Datasheet Max Requirements for VSNVS:
 - 300 μ A
 - Pull Up resistors on VSNVS will add to current requirements
- Datasheet Max Requirements for VDDHIGH:
 - 160 mA
- Typical Maximum Current Requirements (AN4509):
 - VDDHIGH: 85 mA

i.MX6 Power Requirements – DRAM, IO Pins

- Datasheet Max Requirements for DRAM:
 - 1900 mA
- Typical Maximum Current Requirements (AN4509):
 - DRAM: 1390 mA
- Datasheet requirements for IO Pins, use:
 - $I(A) = N \times C \times V \times (0.5 \times F)$
 - N – Number of IO pins supplied
 - C – Equivalent external capacitive load (Farads)
 - V – IO voltage (Volts)
 - $(0.5 \times F)$ – Data change rate, where F = Frequency (Hz)
 - Typical = 2 - 3 mA for a 3.3V pin

Summary Power Requirements

Power Rail	Voltage	Typical	Maximum
VDDARM	1.375 V	1625 mA	3920 mA
VDDSOC	1.375 V	1250 mA	1890 mA
VDDHIGH	2.8V	85 mA	160 mA
VSNVS	3.0 V	-	300 uA
DRAM	1.5 V	1390 mA	1900 mA
USB	5.0 V	500 mA	530 mA
I/O Pins	3.3 V	300 mA	500 mA*
I/O Pins	1.8 V	50 mA	275 mA*

* Maximum values are mutually exclusive

Typical Consumer Device Power Requirements

Function	Voltage	Typical	Maximum
SD Card	3.3 V		100 mA
WIFI/BT	3.3 V		1000 mA
3G/4G Modem	3.3 V	2000 mA	3000 mA
LVDS	3.3 / 5 V		300 / 370 mA
HDMI	5 V		50 mA
Ethernet	3.3 V	130 mA	
Audio	1.8 / 5 V	40 / 100 mA	80 / 530 mA
SATA	5 V	500 - 1000 mA	1500 mA
eMMC	3.3 V	100 mA	200 mA
CAN	5 V		70 mA
GPS	1.5 / 3.3 V		20 / 100 mA
Camera	1.5 / 1.8 V		150 / 20 mA

Grand Total Power Requirements

Voltage	Typical	Full Power
1.375 V	1875 mA	5800 mA
1.5 V	1500 mA	2300 mA
1.8 V	100 mA	350 mA
3.0 V	160 mA	200 mA
3.3 V	2000 mA	5000 mA
5.0 V	1500 mA	3300 mA

i.MX 6 System - Power Design Considerations

- Total System Power Requirements
 - Fully loaded system @ High power: 10A
 - Typical System requirements (5V source): 2.9A
 - Typical System requirements (3.7V source): 4.1A
- System Over-Voltage Protection
 - Select Power components with high voltage tolerance
 - Design Over-Voltage protection sub-system
 - User battery charging circuit with protection.
- Power On Sequencing
- System control functions
 - Stand-by, reduced power options

i.MX 6 System - Power On/Off Sequencing

- Power On Sequencing

1. $VDD_SNVS_IN \leq VDDHIGH_IN$
 $VDD_SNVS_IN < \text{any other power supply}$ (FSL suggest $VDDHIGH_IN$ power with VDD_SNVS_IN or in step 2)
2. $VDDARM_IN \leq (VDDSOC_IN - 1\text{ms})$;
 $Vvddarm_cap \leq (Vvddsoc_cap + 50\text{mV})$: If $VDDARM_IN$ and $VDDSOC_IN$ are connected to different external supply sources

- Power Off Sequencing

N/A

- Notes:

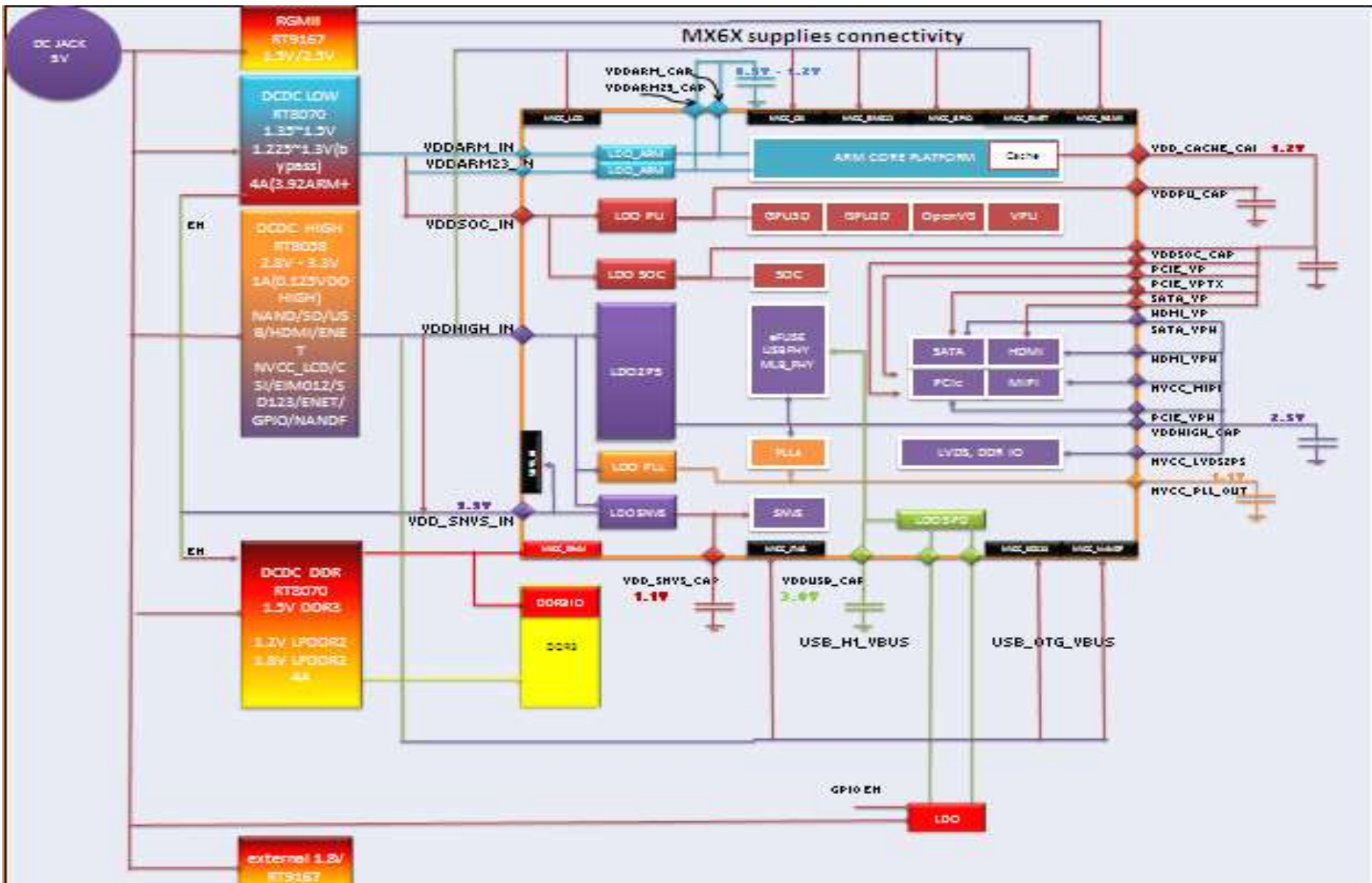
1. Need to ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies)
2. USB_OTG_VBUS and USB_H1_VBUS are not part of the power supply sequence and may be powered at any time

IMX6DQ6SDLHDG: Table 2-6. Power and decouple recommendations

- VGEN5 for VDDHIGH_IN and increase to 3V to align with datasheet
- Only one 22 μ F bulk capacitor should be connected to each of these on-chip LDO regulator outputs:
VDD_ARM/23/SOC/PU_CAP as near as possible with pins/vias. The distance should be less than 50mil between bulk cap and VDD_xx_CAP pins; ripple noise should be less than 5% Vp-p of supply voltage average value
- NVCC_LVDS2P5 must be powered-on even when not using the LVDS interface because The DDR pre-drivers share the NVCC_LVDS2P5 power rail with the LVDS interface

[illegible]

i.MX6 Dual/Quad: 5v Discrete Power





Develop Tools DDR Stress Test

DDR Stress Test Tool

- **What is DDR Stress Tester kit?**

It is downloadable test application architecture. A program running on PC (DDR_Stress_Tester.exe, which running on Command Prompt window) will download the test image to target board's IRAM with the help of UART/USB connection. The test image will do the DDR stress test and the result will be sent to PC through UART/USB and be printed on the Command Prompt window.

- **For mx6dq, mx6dls or mx6sl, UART is not supported.**
- **Support mx53, mx51, mx6dq, mx6dls and mx6sl.**

DDR Stress Test Tool *cont.*

```
C:\WINDOWS\system32\cmd.exe

D:\My Project\iMX6DQ\DDR Stress Test\DDR_Stress_Tester_U0.042\binary>dir
Volume in drive D is Work
Volume Serial Number is 44DB-F232

Directory of D:\My Project\iMX6DQ\DDR Stress Test\DDR_Stress_Tester_U0.042\binary

03/11/2013  02:34 PM    <DIR>          .
03/11/2013  02:34 PM    <DIR>          ..
03/11/2013  02:21 PM    <DIR>          scripts
12/25/2012  11:40 AM             504,832 DDR_Stress_Tester.exe
09/19/2011  01:07 PM             72,928 ddr-stress-test-mx51.bin
09/19/2011  01:08 PM             81,104 ddr-stress-test-mx53.bin
08/29/2012  04:10 PM             69,704 ddr-stress-test-mx6dl.bin
08/29/2012  04:05 PM             86,004 ddr-stress-test-mx6dq.bin
08/29/2012  03:55 PM             67,764 ddr-stress-test-mx6sl.bin
12/25/2012  10:47 AM             9,414 MX6Q_SabreSD_DDR3_register_programming_aid_v1.6.inc
               7 File(s)              891,750 bytes
               3 Dir(s)  13,718,409,216 bytes free

D:\My Project\iMX6DQ\DDR Stress Test\DDR_Stress_Tester_U0.042\binary>DDR_Stress_Tester -h
Usage: DDR_Stress_Tester [options]
Options:
  -h,                Show this help
  -v,                Display the version
  -t <string>        Select target(mx51,mx53, mx6x)
  -df <path>         Input ddr initialization script file(*.inc)
  -com <num>         select the PC's UART to be used(1,2,3...), for mx51/mx53 only
  -usb               select the PC's USB to be used

For mx6x, UART is not supported and USB is the default option.

Usage example:
  DDR_Stress_Tester -t mx53 -df mx53_ddr_script_filename -com 4
  DDR_Stress_Tester -t mx53 -df mx53_ddr_script_filename -usb
  DDR_Stress_Tester -t mx6x -df mx6x_ddr_script_filename

D:\My Project\iMX6DQ\DDR Stress Test\DDR_Stress_Tester_U0.042\binary>
```

Test Log [Link](#)



Develop Tools IOMux Tool

IOMUX Tool

• Application Window Overview

The screenshot displays the IOMUX Tool application window, titled "i.MX6DQ - Demo Board Rev. A". The window is divided into several panes:

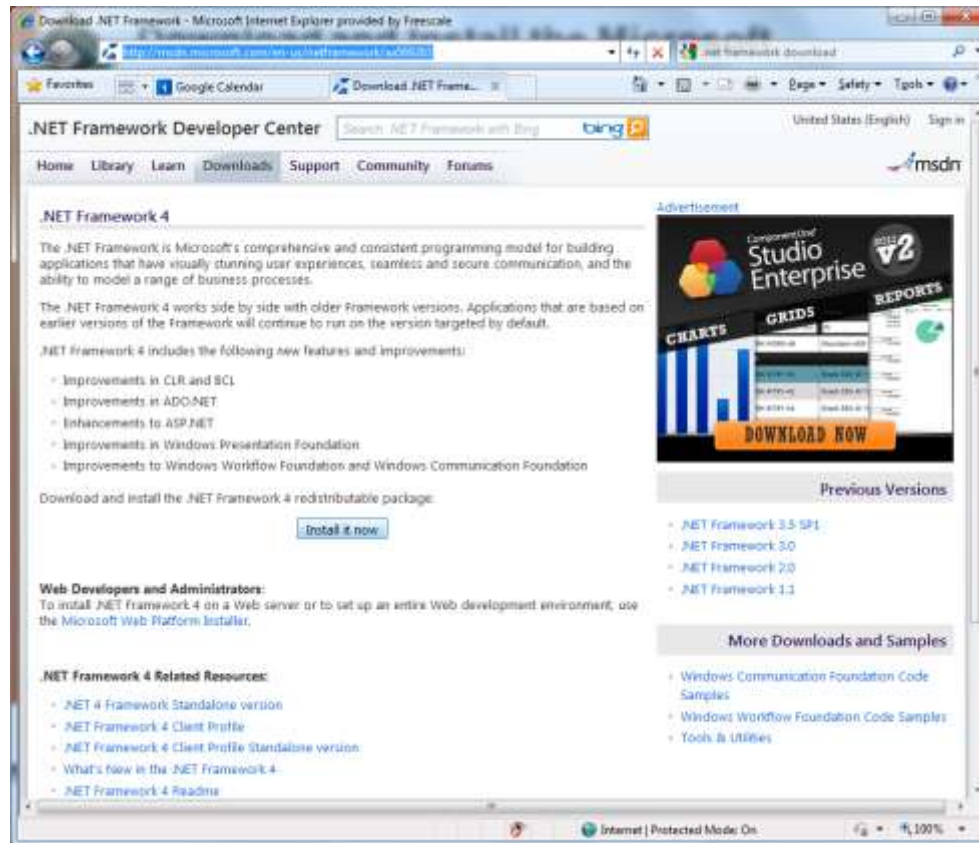
- Menus:** File, Device, Code, View, Help.
- Search Box:** Contains the text "TXD".
- Signal Selection Pane:** A tree view on the left showing the configuration of various signals. The "TXD_MUX" signal is selected, and its configuration is shown in the "Signal Selection Pane".
- Design Info Pane:** A table on the right showing the configuration of various signals. The table has columns: Peripheral/Signal, Ball, Pad Name (AltMode), Power Group, GPIO, and Signal Notes.
- Status Bar:** At the bottom, it shows "i.MX6DQ [20 of 197 muxed pins in use]" and "0 conflicts!".

The "Design Info Pane" table contains the following data:

Peripheral/Signal	Ball	Pad Name (AltMode)	Power Group	GPIO	Signal Notes
uart1 (8 of 8)					
CTS	G21	EIM_D19 (ALT4)	3.300V - WEIM_SEC	gpio3_GPIO[19]	
DCD	D25	EIM_D23 (ALT3)	3.300V - WEIM_SEC	gpio3_GPIO[23]	
DSR	G22	EIM_D25 (ALT7)	3.300V - WEIM_SEC	gpio3_GPIO[25]	
DTR	F22	EIM_D24 (ALT7)	3.300V - WEIM_SEC	gpio3_GPIO[24]	
RTS	F23	EIM_EB3 (ALT3)	3.300V - WEIM_SEC	gpio2_GPIO[31]	
RTS	G20	EIM_D20 (ALT4)	3.300V - WEIM_SEC	gpio3_GPIO[20]	
RXD_MUX	M3	CSIO_DAT11 (ALT3)	3.300V - IPU_CSI	gpio5_GPIO[29]	
TXD_MUX	M1	CSIO_DAT10 (ALT3)	3.300V - IPU_CSI	gpio5_GPIO[28]	
uart2 (4 of 4)					
CTS	G23	EIM_D28 (ALT4)	3.300V - WEIM_SEC	gpio3_GPIO[28]	
RTS	J19	EIM_D29 (ALT4)	3.300V - WEIM_SEC	gpio3_GPIO[29]	
RXD_MUX	E25	EIM_D27 (ALT4)	3.300V - WEIM_SEC	gpio3_GPIO[27]	
TXD_MUX	E24	EIM_D26 (ALT4)	3.300V - WEIM_SEC	gpio3_GPIO[25]	Connected to U12, auxiliary console
uart3 (4 of 4) Check power settings for NANDF, WEIM_SEC					
CTS	J20	EIM_D30 (ALT4)	3.300V - WEIM_SEC	gpio3_GPIO[30]	
RTS	H21	EIM_D31 (ALT4)	3.300V - WEIM_SEC	gpio3_GPIO[31]	
RXD_MUX	F16	SD4_CLK (ALT2)	1.800V - NANDF	gpio7_GPIO[10]	
TXD_MUX	B17	SD4_CMD (ALT2)	1.800V - NANDF	gpio7_GPIO[9]	
uart4 (4 of 4) Set power level for GPIO					
CTS	L3	CSIO_DAT17 (ALT3)	3.300V - IPU_CSI	gpio6_GPIO[3]	
RTS	L4	CSIO_DAT16 (ALT3)	3.300V - IPU_CSI	gpio6_GPIO[2]	
RXD_MUX	V6	KEY_ROW0 (ALT4)	0.000V - GPIO	gpio4_GPIO[7]	
TXD_MUX	W5	KEY_COL0 (ALT4)	0.000V - GPIO	gpio4_GPIO[6]	

Download and Install the Microsoft .NET Framework 4.0

- <http://msdn.microsoft.com/en-us/netframework/aa569263>



Select Modules and Signals for Board

- Check the UARTS: UART1, UART2 and UART3.
- Expand all signals under UART3.

The screenshot shows the IO Mux configuration tool for an i.MX6DQ board. The left pane displays a tree view of modules and signals. The right pane shows a table of selected signals and their configurations.

IO Mux - <untitled> *

File Device Code View Help

Search

Signals Ball Diagram Pads Registers Power General

i.MX6DQ - <board> <board revision> (IOMux Design File Version: r<version>)

[12 of 197 muxed pins in use] **8 conflicts!**

Peripheral/Signal	Ball	Pad Name (AltMode)	Power Group	GPIO	Signal Notes
uart1 (8 of 8) Set power level for IPU_CSI					
CTS	G21	EIM_D19 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[19]	
DCD	D25	EIM_D23 (ALT3)	0.000V - WEIM_SEC	gpio3_GPIO[23]	
DSR	G22	EIM_D25 (ALT7)	0.000V - WEIM_SEC	gpio3_GPIO[25]	
DTR	F22	EIM_D24 (ALT7)	0.000V - WEIM_SEC	gpio3_GPIO[24]	
RI	F23	EIM_EB3 (ALT3)	0.000V - WEIM_SEC	gpio2_GPIO[31]	
RTS	G20	EIM_D20 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[20]	
RXD_MUX	M3	CSI0_DAT11 (ALT3)	0.000V - IPU_CSI	gpio5_GPIO[29]	
TXD_MUX	M1	CSI0_DAT10 (ALT3)	0.000V - IPU_CSI	gpio5_GPIO[28]	
uart2 (4 of 4) Set power level for WEIM_SEC					
CTS	G23	EIM_D28 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[28]	
RTS	J19	EIM_D29 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[29]	
RXD_MUX	E25	EIM_D27 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[27]	
TXD_MUX	E24	EIM_D26 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[26]	
uart3 (4 of 4) Set power level for WEIM_SEC					
CTS	D25	EIM_D23 (ALT2)	0.000V - WEIM_SEC	gpio3_GPIO[23]	
RTS	F23	EIM_EB3 (ALT2)	0.000V - WEIM_SEC	gpio2_GPIO[31]	
RXD_MUX	G22	EIM_D25 (ALT2)	0.000V - WEIM_SEC	gpio3_GPIO[25]	
TXD_MUX	F22	EIM_D24 (ALT2)	0.000V - WEIM_SEC	gpio3_GPIO[24]	

i.MX6DQ [12 of 197 muxed pins in use] **8 conflicts!**

Accessing Muxed-Signal Info

The screenshot shows the IO Mux configuration tool for an i.MX6DQ. The left pane displays a tree of components, with UART3 (4 of 4) selected. The right pane shows the 'Signals' tab, which lists the muxed signals for the selected component. The table below is a representation of the data shown in the tool.

Peripheral/Signal	Ball	Pad Name (AltMode)	Power Group	GPIO	Signal Notes
uart1 (8 of 8) Set power level for IPU_CSI					
CTS	G21	EIM_D19 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[19]	
DCD	D25	EIM_D23 (ALT3)	0.000V - WEIM_SEC	gpio3_GPIO[23]	
DSR	G22	EIM_D25 (ALT7)	0.000V - WEIM_SEC	gpio3_GPIO[25]	
DTR	F22	EIM_D24 (ALT7)	0.000V - WEIM_SEC	gpio3_GPIO[24]	
RI	F23	EIM_EB3 (ALT3)	0.000V - WEIM_SEC	gpio2_GPIO[31]	
RTS	G20	EIM_D20 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[20]	
RXD_MUX	M3	CSIO_DAT11 (ALT3)	0.000V - IPU_CSI	gpio5_GPIO[29]	
TXD_MUX	M1	CSIO_DAT10 (ALT3)	0.000V - IPU_CSI	gpio5_GPIO[28]	
uart2 (4 of 4) Set power level for WEIM_SEC					
CTS	G23	EIM_D28 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[28]	
RTS	J19	EIM_D29 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[29]	
RXD_MUX	E25	EIM_D27 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[27]	
TXD_MUX	E24	EIM_D26 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[26]	
uart3 (4 of 4) Set power level for WEIM_SEC					
CTS	D25	EIM_D23 (ALT2)	0.000V - WEIM_SEC	gpio3_GPIO[23]	
RTS	F23	EIM_EB3 (ALT2)	0.000V - WEIM_SEC	gpio2_GPIO[31]	
RXD_MUX	G22	EIM_D25 (ALT2)	0.000V - WEIM_SEC	gpio3_GPIO[25]	
TXD_MUX	F22	EIM_D24 (ALT2)	0.000V - WEIM_SEC	gpio3_GPIO[24]	

The status bar at the bottom indicates 'i.MX6DQ [12 of 197 muxed pins in use]' and '8 conflicts!'.

Accessing Muxed-Signal Info

The screenshot shows the IO Mux configuration tool interface. On the left is a tree view of peripherals, including src, tcu, tpsmp, and several UART instances (uart1, uart2, uart3, uart4, uart5). The right pane displays the 'Signals' tab for the selected peripheral, showing a table of muxed signals.

IO Mux - <untitled> *

File Device Code View Help

Search

Signals Ball Diagram Pads Registers Power General

i.MX6DQ - <board> <board revision> (IOMux Design File Version: r<version>)

[12 of 197 muxed pins in use] **8 conflicts!**

Peripheral/Signal	Ball	Pad Name (AltMode)	Power Group	GPIO	Signal Notes
uart1 (8 of 8) Set power level for IPU_CSI					
CTS	G21	EIM_D19 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[19]	
DCD	D25	EIM_D23 (ALT3)	0.000V - WEIM_SEC	gpio3_GPIO[23]	
DSR	G22	EIM_D25 (ALT7)	0.000V - WEIM_SEC	gpio3_GPIO[25]	
DTR	F22	EIM_D24 (ALT7)	0.000V - WEIM_SEC	gpio3_GPIO[24]	
RI	F23	EIM_EB3 (ALT3)	0.000V - WEIM_SEC	gpio2_GPIO[31]	
RTS	G20	EIM_D20 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[20]	
RXD_MUX	M3	CSIO_DAT11 (ALT3)	0.000V - IPU_CSI	gpio5_GPIO[29]	
TXD_MUX	M1	CSIO_DAT10 (ALT3)	0.000V - IPU_CSI	gpio5_GPIO[28]	
uart2 (4 of 4) Set power level for WEIM_SEC					
CTS	G23	EIM_D28 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[28]	
RTS	J19	EIM_D29 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[29]	
RXD_MUX	E25	EIM_D27 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[27]	
TXD_MUX	E24	EIM_D26 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[26]	
uart3 (4 of 4) Set power level for WEIM_SEC					
CTS	D25	EIM_D23 (ALT2)	0.000V - WEIM_SEC	gpio3_GPIO[23]	
RTS	F23	EIM_EB3 (ALT2)	0.000V - WEIM_SEC	gpio2_GPIO[31]	
RXD_MUX	G22	EIM_D25 (ALT2)	0.000V - WEIM_SEC	gpio3_GPIO[25]	
TXD_MUX	F22	EIM_D24 (ALT2)	0.000V - WEIM_SEC	gpio3_GPIO[24]	

(weim_WEIM_D[24], ecspi4_SS2, ecspi1_SS2, ecspi2_SS2, gpio3_GPIO[24], audmux_AUD5_RXFS, uart1_DTR)

i.MX6DQ [12 of 197 muxed pins in use] **8 conflicts!**

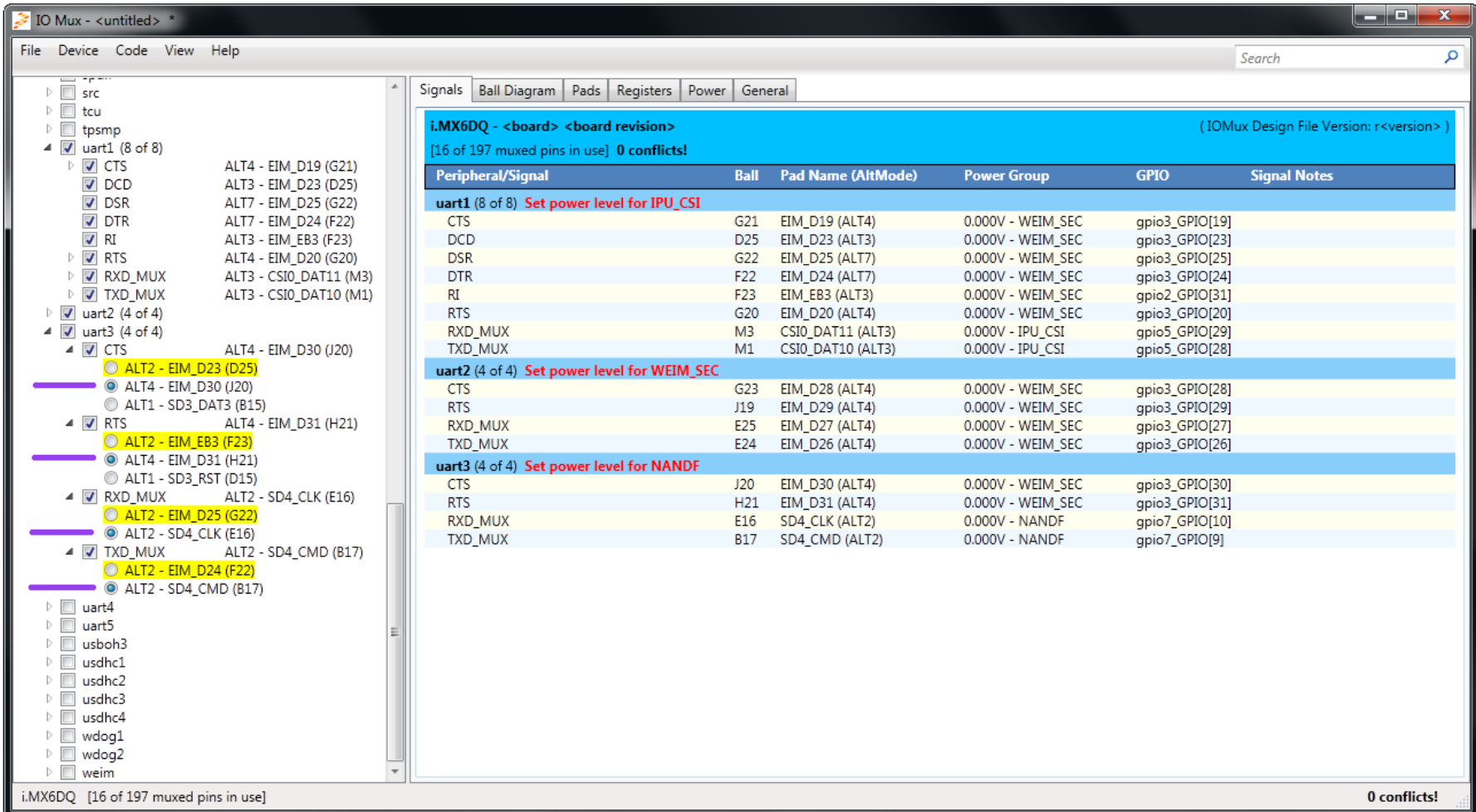
Resolve Conflicting Signals

Select ALT4 – EIM_D30(J20) for UART3/CTS.

Select ALT4 – EIM_D31(H21) for UART3/RTS.

Select ALT2 – SD4_CLK(E16) for UART3/RXD_MUX.

Select ALT2 – SD4_CMD(B17) for UART3/TXD_MUX.



IO Mux - <untitled> *

File Device Code View Help

Search

Signals Ball Diagram Pads Registers Power General

i.MX6DQ - <board> <board revision> (IOMux Design File Version: r<version>)

[16 of 197 muxed pins in use] **0 conflicts!**

Peripheral/Signal	Ball	Pad Name (AltMode)	Power Group	GPIO	Signal Notes
uart1 (8 of 8) Set power level for IPU_CSI					
CTS	G21	EIM_D19 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[19]	
DCD	D25	EIM_D23 (ALT3)	0.000V - WEIM_SEC	gpio3_GPIO[23]	
DSR	G22	EIM_D25 (ALT7)	0.000V - WEIM_SEC	gpio3_GPIO[25]	
DTR	F22	EIM_D24 (ALT7)	0.000V - WEIM_SEC	gpio3_GPIO[24]	
RI	F23	EIM_EB3 (ALT3)	0.000V - WEIM_SEC	gpio2_GPIO[31]	
RTS	G20	EIM_D20 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[20]	
RXD_MUX	M3	CSI0_DAT11 (ALT3)	0.000V - IPU_CSI	gpio5_GPIO[29]	
TXD_MUX	M1	CSI0_DAT10 (ALT3)	0.000V - IPU_CSI	gpio5_GPIO[28]	
uart2 (4 of 4) Set power level for WEIM_SEC					
CTS	G23	EIM_D28 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[28]	
RTS	J19	EIM_D29 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[29]	
RXD_MUX	E25	EIM_D27 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[27]	
TXD_MUX	E24	EIM_D26 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[26]	
uart3 (4 of 4) Set power level for NANDF					
CTS	J20	EIM_D30 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[30]	
RTS	H21	EIM_D31 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[31]	
RXD_MUX	E16	SD4_CLK (ALT2)	0.000V - NANDF	gpio7_GPIO[10]	
TXD_MUX	B17	SD4_CMD (ALT2)	0.000V - NANDF	gpio7_GPIO[9]	

i.MX6DQ [16 of 197 muxed pins in use] **0 conflicts!**

Adding Comments for Clarity

- Right-click the UART2/TXD_MUX row in the Signals tab to bring up the context menu.
- Clicking on the menu will bring up a text entry field where the user may enter text.

The screenshot shows the i.MX6DQ IO Mux configuration tool. The left pane displays a tree view of the device's pins and their associated signals. The right pane shows the 'Signals' tab, which lists the configured signals for the i.MX6DQ device. A context menu is open over the 'TXD_MUX' row of the 'uart2' group, allowing the user to add a comment.

Device: i.MX6DQ - <board> <board revision> (IOMux Design File Version: r<version>)

[16 of 197 muxed pins in use] 0 conflicts!

Peripheral/Signal	Ball	Pad Name (AltMode)	Power Group	GPIO	Signal Notes
uart1 (8 of 8) Set power level for IPU_CSI					
CTS	G21	EIM_D19 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[19]	
DCD	D25	EIM_D23 (ALT3)	0.000V - WEIM_SEC	gpio3_GPIO[23]	
DSR	G22	EIM_D25 (ALT7)	0.000V - WEIM_SEC	gpio3_GPIO[25]	
DTR	F22	EIM_D24 (ALT7)	0.000V - WEIM_SEC	gpio3_GPIO[24]	
RI	F23	EIM_EB3 (ALT3)	0.000V - WEIM_SEC	gpio2_GPIO[31]	
RTS	G20	EIM_D20 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[20]	
RXD_MUX	M3	CSIO_DAT11 (ALT3)	0.000V - IPU_CSI	gpio5_GPIO[29]	
TXD_MUX	M1	CSIO_DAT10 (ALT3)	0.000V - IPU_CSI	gpio5_GPIO[28]	
uart2 (4 of 4) Set power level for WEIM_SEC					
CTS	G23	EIM_D28 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[28]	
RTS	J19	EIM_D29 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[29]	
RXD_MUX	E25	EIM_D27 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[27]	
TXD_MUX	E24	EIM_D26 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[26]	
uart3 (4 of 4) Set power level for WEIM_SEC					
CTS	J20	EIM_D30 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[30]	
RTS	H21	EIM_D31 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[31]	
RXD_MUX	E16	SD4_CLK (ALT2)	0.000V - NANDF	gpio7_GPIO[10]	
TXD_MUX	B17	SD4_CMD (ALT2)	0.000V - NANDF	gpio7_GPIO[9]	

Context Menu: Edit comment for uart2_TXD_MUX signal/port...

Footer: i.MX6DQ [16 of 197 muxed pins in use] 0 conflicts!

Adding Comments for Clarity

The screenshot shows the IO Mux software interface for an i.MX6DQ board. The left pane displays a tree view of the device's components, including various UARTs and their associated pins. The right pane shows a table of peripheral configurations. A comment, "Connected to U12, auxiliary console", has been added to the entry for gpio3_GPIO[26], which is circled in purple.

Peripheral/Signal	Ball	Pad Name (AltMode)	Power Group	GPIO	Signal Notes
uart1 (8 of 8) Set power level for IPU_CSI					
CTS	G21	EIM_D19 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[19]	
DCD	D25	EIM_D23 (ALT3)	0.000V - WEIM_SEC	gpio3_GPIO[23]	
DSR	G22	EIM_D25 (ALT7)	0.000V - WEIM_SEC	gpio3_GPIO[25]	
DTR	F22	EIM_D24 (ALT7)	0.000V - WEIM_SEC	gpio3_GPIO[24]	
RI	F23	EIM_EB3 (ALT3)	0.000V - WEIM_SEC	gpio2_GPIO[31]	
RTS	G20	EIM_D20 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[20]	
RXD_MUX	M3	CSIO_DAT11 (ALT3)	0.000V - IPU_CSI	gpio5_GPIO[29]	
TXD_MUX	M1	CSIO_DAT10 (ALT3)	0.000V - IPU_CSI	gpio5_GPIO[28]	
uart2 (4 of 4) Set power level for WEIM_SEC					
CTS	G23	EIM_D28 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[28]	
RTS	J19	EIM_D29 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[29]	
RXD_MUX	E25	EIM_D27 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[27]	
TXD_MUX	E24	EIM_D26 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[26]	Connected to U12, auxiliary console
uart3 (4 of 4) Set power level for NANDF					
CTS	J20	EIM_D30 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[30]	
RTS	H21	EIM_D31 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[31]	
RXD_MUX	E16	SD4_CLK (ALT2)	0.000V - NANDF	gpio7_GPIO[10]	
TXD_MUX	B17	SD4_CMD (ALT2)	0.000V - NANDF	gpio7_GPIO[9]	

Ball Diagram View

The screenshot displays the IO Mux configuration tool for an i.MX6DQ processor. The interface includes a menu bar (File, Device, Code, View, Help), a search bar, and a tabbed view with 'Signals', 'Ball Diagram', 'Pads', 'Registers', 'Power', and 'General' selected. The 'Ball Diagram' tab shows a 26x26 grid of pins (A-AE, 1-25) color-coded by status: Ground (grey), Power (brown), Not Muxed (tan), Available (light yellow), In Use (green), and Conflicted (red). A legend at the bottom explains these colors. On the left, a tree view lists various peripheral signals and their alternative functions (ALTs). A tooltip for pin M3 (CSIO_DAT11) lists its associated signals: M3 - CSIO_DAT11, uart1_RXD_MUX (ALT3), ipu1_CSIO_D[11] (ALT0), audmux_AUD3_RXFS (ALT1), ecspi2_SS0 (ALT2), sdma_DEBUG_PC[5] (ALT4), gpio5_GPIO[29] (ALT5), mmdc_MMDC_DEBUG[34] (ALT6), and cheetah_TRACE[8] (ALT7). The status bar at the bottom indicates 'i.MX6DQ [16 of 197 muxed pins in use]' and '0 conflicts!'.

IO Mux - <untitled> *

File Device Code View Help

Search

Signals Ball Diagram Pads Registers Power General

spdif
src
tcu
tpsmpr
uart1 (8 of 8)
 CTS ALT4 - EIM_D19 (G21)
 DCD ALT3 - EIM_D23 (D25)
 DSR ALT7 - EIM_D25 (G22)
 DTR ALT7 - EIM_D24 (F22)
 RI ALT3 - EIM_EB3 (F23)
 RTS ALT4 - EIM_D20 (G20)
 RXD_MUX ALT3 - CSIO_DAT11 (M3)
 TXD_MUX ALT3 - CSIO_DAT10 (M1)
uart2 (4 of 4)
uart3 (4 of 4)
 CTS ALT4 - EIM_D30 (J20)
 ALT2 - EIM_D23 (D25)
 ALT4 - EIM_D30 (J20)
 ALT1 - SD3_DAT3 (B15)
 RTS ALT4 - EIM_D31 (H21)
 ALT2 - EIM_EB3 (F23)
 ALT4 - EIM_D31 (H21)
 ALT1 - SD3_RST (D15)
 RXD_MUX ALT2 - SD4_CLK (E16)
 ALT2 - EIM_D25 (G22)
 ALT2 - SD4_CLK (E16)
 TXD_MUX ALT2 - SD4_CMD (B17)
 ALT2 - EIM_D24 (F22)
 ALT2 - SD4_CMD (B17)
uart4
uart5
usboh3
usdhc1
usdhc2
usdhc3
usdhc4
wdog1
wdog2
weim

M3 - CSIO_DAT11
uart1_RXD_MUX (ALT3)
ipu1_CSIO_D[11] (ALT0)
audmux_AUD3_RXFS (ALT1)
ecspi2_SS0 (ALT2)
sdma_DEBUG_PC[5] (ALT4)
gpio5_GPIO[29] (ALT5)
mmdc_MMDC_DEBUG[34] (ALT6)
cheetah_TRACE[8] (ALT7)

Ground Power Not Muxed Available In Use Conflicted

i.MX6DQ [16 of 197 muxed pins in use] 0 conflicts!

Pads “Spreadsheet” View

IO Mux - <untitled> *

File Device Code View Help

Search

Signals Ball Diagram Pads Registers Power General

spdif
src
tcu
tpsm
uart1 (8 of 8)
 CTS ALT4 - EIM_D19 (G21)
 DCD ALT3 - EIM_D23 (D25)
 DSR ALT7 - EIM_D25 (G22)
 DTR ALT7 - EIM_D24 (F22)
 RI ALT3 - EIM_EB3 (F23)
 RTS ALT4 - EIM_D20 (G20)
 RXD_MUX ALT3 - CSIO_DAT11 (M3)
 TXD_MUX ALT3 - CSIO_DAT10 (M1)
uart2 (4 of 4)
uart3 (4 of 4)
 CTS ALT4 - EIM_D30 (J20)
 ALT2 - EIM_D23 (D25)
 ALT4 - EIM_D30 (J20)
 ALT1 - SD3_DAT3 (B15)
 RTS ALT4 - EIM_D31 (H21)
 ALT2 - EIM_EB3 (F23)
 ALT4 - EIM_D31 (H21)
 ALT1 - SD3_RST (D15)
 RXD_MUX ALT2 - SD4_CLK (E16)
 ALT2 - EIM_D25 (G22)
 ALT2 - SD4_CLK (E16)
 TXD_MUX ALT2 - SD4_CMD (B17)
 ALT2 - EIM_D24 (F22)
 ALT2 - SD4_CMD (B17)
uart4
uart5
usboh3
usdhc1
usdhc2
usdhc3
usdhc4
wdog1
wdog2
weim

BALL	PAD NAME	POWER GROUP	DEFAULT MODE	ALT0 MODE	ALT1 MODE	ALT2 MODE
D4	CSI_REXT	MIPI				
D5	CLK2_P	ANATOP				
D6	GND					
D7	CLK1_P	ANATOP				
D8	GND					
D9	RTC_XTALI	ANATOP				
E1	CSI_D2M	MIPI				
E10	USB_H1_DP	ANATOP				
E11	TAMPER	RESET				
E12	TEST_MODE	RESET				
E13	SD3_DAT6	SD3	ALT5	usdhc3_DAT6	uart1_RXD_MUX	pcie_ctrl_DIAG_STATUS_BUS_MUX[
E14	SD3_DAT0	SD3	ALT5	usdhc3_DAT0	uart1_CTS	can2_TXCAN
E15	NANDF_WP_B	NANDF	ALT5	rawnand_RESETN	ipu2_SISG[5]	pcie_ctrl_DIAG_STATUS_BUS_MUX[
E16	SD4_CLK	NANDF	ALT5	usdhc4_CLK	rawnand_WRN	uart3_RXD_MUX
E17	NANDF_D6	NANDF	ALT5	rawnand_D6	usdhc2_DAT6	gpu3d_GPU_DEBUG_OUT[6]
E18	SD4_DAT4	NANDF	ALT5	rawnand_D12	usdhc4_DAT4	uart2_RXD_MUX
E19	SD1_DAT2	SD1	ALT5	usdhc1_DAT2	ecspi5_SS1	gpt_CMPOUT2
E2	CSI_D2P	MIPI				
E20	SD2_DAT1	SD2	ALT5	usdhc2_DAT1	ecspi5_SS0	weim_WEIM_CS[2]
E21	RGMII_TD2	RGMII	ALT5	mipi_hsi_ctrl_RX_DATA	enet_RGMII_TD2	
E22	EIM_EB2	WEIM_SEC	ALT5	weim_WEIM_EB[2]	ecspi1_SS0	ccm_DI1_EXT_CLK
E23	EIM_D22	WEIM_SEC	ALT5	weim_WEIM_D[22]	ecspi4_MISO	ipu1_DIO_PIN1
E24	EIM_D26	WEIM_SEC	ALT5	weim_WEIM_D[26]	ipu1_DI1_PIN11	ipu1_CSI0_D[1]
E25	EIM_D27	WEIM_SEC	ALT5	weim_WEIM_D[27]	ipu1_DI1_PIN13	ipu1_CSI0_D[0]
E3	CSI_D0P	MIPI				
E4	CSI_D0M	MIPI				
E5	GND					
E6	GND					

i.MX6DQ [16 of 197 muxed pins in use]

0 conflicts!

Configuring IOMUXC Registers

- Select UART3/RXD_MUX in the left-hand pane.
- All of the IOMUXC Registers associated with the AD4_CLK(E16) pad are shown on the Registers Tab in the right-hand pane.

IO Mux - C:\ViewStorage\IOMux_Tool.v3\Apps.Net\IOMux\bin\Release\i.MX6DQ_DemoBoard_Rev.A\IoMuxDesign.r1.xml *

File Device Code View Help

Search

Signals Ball Diagram Pads Registers Power General

These are the configuration registers for currently selected pad: E16-SD4_CLK.

Pad: **E16** Pad Name: **SD4_CLK**

Mode: **ALT2** Instance: **uart3** Port: **RXD_MUX**

Note: Please use the tree control on the left to change the MUX_MODE of the IOMUXC_SW_MUX_CTL_PAD_SD4_CLK register.

Register Name	Address	Value
IOMUXC_SW_MUX_CTL_PAD_SD4_CLK	0x020E02F8	0x00000002
SION (4)	Software Input On Field	Default: SION_DISABLED
MUX_MODE (2-0)	MUX Mode Select Field	Default: ALT5
IOMUXC_UART3_IPP_UART_RXD_MUX_SELECT_INPUT	0x020E0930	0x00000003
DAISY (1-0)		Default: SEL_EIM_D24_ALT2
IOMUXC_SW_PAD_CTL_PAD_SD4_CLK	0x020E06E0	0x0001B0B0
HYS (16)	Hysteresis Enable Field	Default: HYS_ENABLED
PUS (15-14)	Pull Up / Down Config. Field	Default: PUS_100KOHM_PU
PUE (13)	Pull / Keep Select Field	Default: PUE_PULL
PKE (12)	Pull / Keep Enable Field	Default: PKE_ENABLED
ODE (11)	Open Drain Enable Field	Default: ODE_DISABLED
SPEED (7-6)	Speed Field	Default: SPD_100MHZ
DSE (5-3)	Drive Strength Field	Default: DSE_40OHM
SRE (0)	Slew Rate Field	Default: SRE_SLOW

i.MX6DQ [20 of 197 muxed pins in use] 0 conflicts!

Drag a Signal to another Module

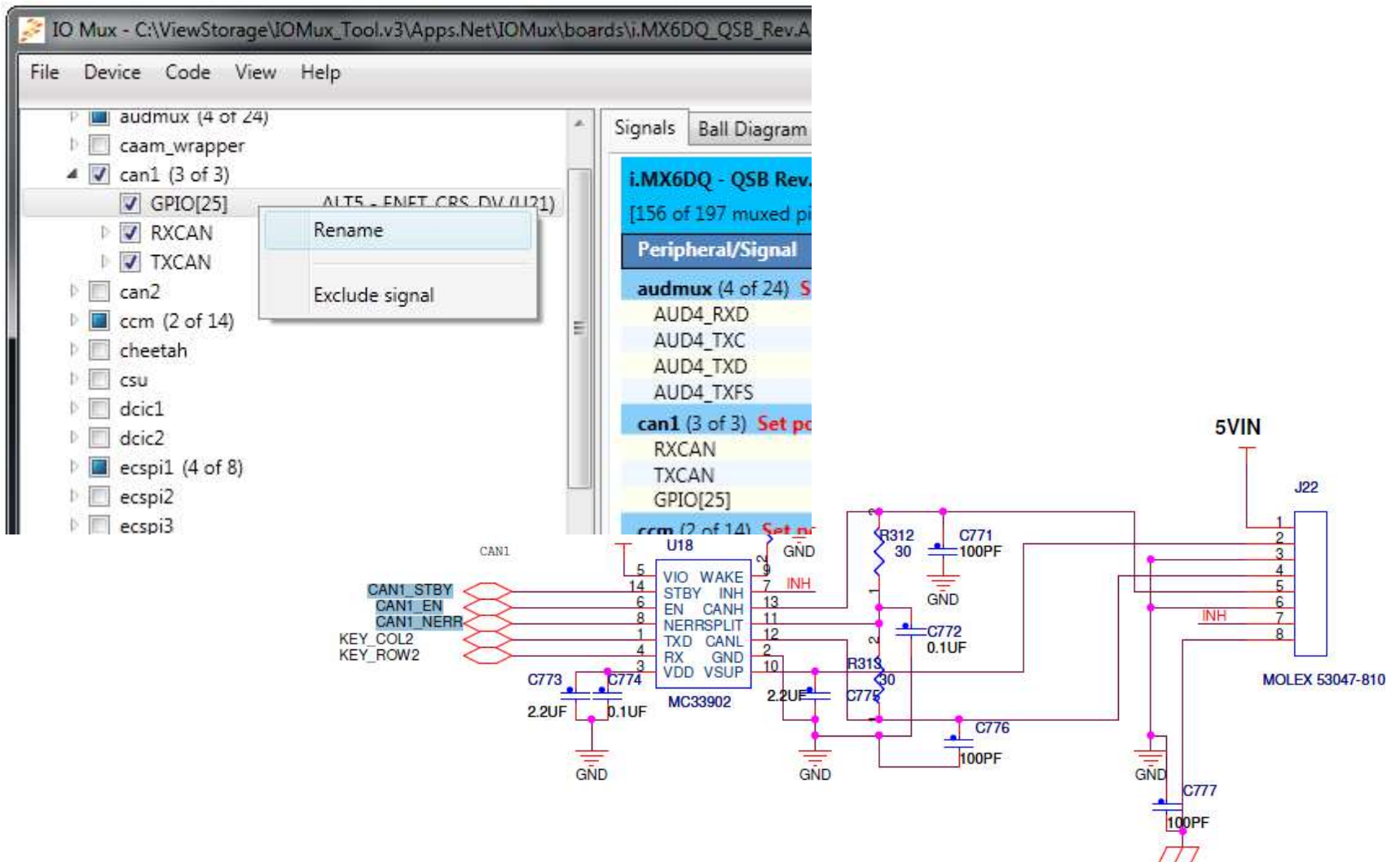
The screenshot shows the IO Mux software interface with the following components:

- Left Panel (Device Tree):** A tree view of the device modules. The **gpio1** module (10 of 32) is selected, and its pins are listed. A purple circle highlights **GPIO[25]** in the list.
- Right Panel (Signals):** A table of signals and their configurations. The **MX6DQ - QSB Rev. A** design is selected. The table shows various signals and their configurations, including power levels and GPIO assignments.

Signals Table:

Peripheral/Signal	Ball	Pad Name (AltMode)	Power Group	GPIO	Signal Notes
audmux (4 of 24) Set power level for SD2					
AUD4_RXD	A22	SD2_DAT0 (ALT3)	0.000V - SD2	gpio1_GPIO[15]	
AUD4_TXC	B22	SD2_DAT3 (ALT3)	0.000V - SD2	gpio1_GPIO[12]	
AUD4_TXD	A23	SD2_DAT2 (ALT3)	0.000V - SD2	gpio1_GPIO[13]	
AUD4_TXFS	E20	SD2_DAT1 (ALT3)	0.000V - SD2	gpio1_GPIO[14]	
can1 (2 of 2) Set power level for GPIO					
RXCAN	W4	KEY_ROW2 (ALT2)	0.000V - GPIO	gpio4_GPIO[11]	
TXCAN	W6	KEY_COL2 (ALT2)	0.000V - GPIO	gpio4_GPIO[10]	
ccm (2 of 14) Set power level for GPIO					
CLKO	T5	GPIO_0 (ALT0)	0.000V - GPIO	gpio1_GPIO[0]	SGTL5000 - sys_mclk
CLKO2	R7	GPIO_3 (ALT4)	0.000V - GPIO	gpio1_GPIO[3]	J5 - Camera mclk
ecspi1 (4 of 8) Set power level for GPIO					
MISO	U7	KEY_COL1 (ALT0)	0.000V - GPIO	gpio4_GPIO[8]	
MOSI	V6	KEY_ROW0 (ALT0)	0.000V - GPIO	gpio4_GPIO[7]	
SCLK	W5	KEY_COL0 (ALT0)	0.000V - GPIO	gpio4_GPIO[6]	
SS0	U6	KEY_ROW1 (ALT0)	0.000V - GPIO	gpio4_GPIO[9]	
enet (14 of 39) Set power level for ENET					
MDC	V20	ENET_MDC (ALT1)	0.000V - ENET	gpio1_GPIO[31]	
MDIO	V23	ENET_MDIO (ALT1)	0.000V - ENET	gpio1_GPIO[22]	
RGMIIR_RD0	C24	RGMIIR_RD0 (ALT1)	0.000V - RGMII	gpio6_GPIO[25]	
RGMIIR_RD1	B23	RGMIIR_RD1 (ALT1)	0.000V - RGMII	gpio6_GPIO[27]	
RGMIIR_RD2	B24	RGMIIR_RD2 (ALT1)	0.000V - RGMII	gpio6_GPIO[28]	
RGMIIR_RD3	D23	RGMIIR_RD3 (ALT1)	0.000V - RGMII	gpio6_GPIO[29]	
RGMIIR_RX_CTL	D22	RGMIIR_RX_CTL (ALT1)	0.000V - RGMII	gpio6_GPIO[24]	
RGMIIR_RXC	B25	RGMIIR_RXC (ALT1)	0.000V - RGMII	gpio6_GPIO[30]	
RGMIIR_TD0	C22	RGMIIR_TD0 (ALT1)	0.000V - RGMII	gpio6_GPIO[20]	
RGMIIR_TD1	F20	RGMIIR_TD1 (ALT1)	0.000V - RGMII	gpio6_GPIO[21]	
RGMIIR_TD2	E21	RGMIIR_TD2 (ALT1)	0.000V - RGMII	gpio6_GPIO[22]	
RGMIIR_TD3	A24	RGMIIR_TD3 (ALT1)	0.000V - RGMII	gpio6_GPIO[23]	
RGMIIR_TX_CTL	C23	RGMIIR_TX_CTL (ALT1)	0.000V - RGMII	gpio6_GPIO[26]	
RGMIIR_TXC	D21	RGMIIR_TXC (ALT1)	0.000V - RGMII	gpio6_GPIO[19]	
gpio1 (10 of 32) Set power level for ENET					
GPIO[16]	A21	SD1_DAT0 (ALT5)	0.000V - SD1		J5 - Camera GD

Rename Signal to Match Schematics



CAN1 Module with All Signals

- Comments auto-generated to denote original Module/Signal.

The screenshot shows the IO Mux software interface for the i.MX6DQ-QSB Rev. A. The left pane displays a tree view of modules, with 'can1' selected. The right pane shows a table of signals and their configurations. A purple circle highlights a comment for GPIO1[25] and GPIO1[26] and GPIO1[27].

Peripheral/Signal	Ball	Pad Name (AltMode)	Power Group	GPIO	Signal Notes
audmux (4 of 24) Set power level for SD2					
AUD4_RXD	A22	SD2_DAT0 (ALT3)	0.000V - SD2	gpio1_GPIO[15]	
AUD4_TXC	B22	SD2_DAT3 (ALT3)	0.000V - SD2	gpio1_GPIO[12]	
AUD4_TXD	A23	SD2_DAT2 (ALT3)	0.000V - SD2	gpio1_GPIO[13]	
AUD4_TXFS	E20	SD2_DAT1 (ALT3)	0.000V - SD2	gpio1_GPIO[14]	
can1 (5 of 5) Set power level for ENET					
RXCAN	W4	KEY_ROW2 (ALT2)	0.000V - GPIO	gpio4_GPIO[11]	
TXCAN	W6	KEY_COL2 (ALT2)	0.000V - GPIO	gpio4_GPIO[10]	
CAN1_STBY	U21	ENET_CRS_DV (ALT5)	0.000V - ENET		
CAN1_NERR	W22	ENET_RXD1 (ALT5)	0.000V - ENET		
CAN1_EN	W21	ENET_RXD0 (ALT5)	0.000V - ENET		
ccm (2 of 14) Set power level for GPIO					
CLKO	T5	GPIO_0 (ALT0)	0.000V - GPIO	gpio1_GPIO[0]	SGTL5000 - sys_mclk
CLKO2	R7	GPIO_3 (ALT4)	0.000V - GPIO	gpio1_GPIO[3]	J5 - Camera mclk
ecspi1 (4 of 8) Set power level for GPIO					
MISO	U7	KEY_COL1 (ALT0)	0.000V - GPIO	gpio4_GPIO[8]	
MOSI	V6	KEY_ROW0 (ALT0)	0.000V - GPIO	gpio4_GPIO[7]	
SCLK	W5	KEY_COL0 (ALT0)	0.000V - GPIO	gpio4_GPIO[6]	
SS0	U6	KEY_ROW1 (ALT0)	0.000V - GPIO	gpio4_GPIO[9]	
enet (14 of 39) Set power level for ENET					
MDC	V20	ENET_MDC (ALT1)	0.000V - ENET	gpio1_GPIO[31]	
MDIO	V23	ENET_MDIO (ALT1)	0.000V - ENET	gpio1_GPIO[22]	
RGMIIR_RD0	C24	RGMIIR_RD0 (ALT1)	0.000V - RGMII	gpio6_GPIO[25]	
RGMIIR_RD1	B23	RGMIIR_RD1 (ALT1)	0.000V - RGMII	gpio6_GPIO[27]	
RGMIIR_RD2	B24	RGMIIR_RD2 (ALT1)	0.000V - RGMII	gpio6_GPIO[28]	
RGMIIR_RD3	D23	RGMIIR_RD3 (ALT1)	0.000V - RGMII	gpio6_GPIO[29]	
RGMIIR_RX_CTL	D22	RGMIIR_RX_CTL (ALT1)	0.000V - RGMII	gpio6_GPIO[24]	
RGMIIR_RXC	B25	RGMIIR_RXC (ALT1)	0.000V - RGMII	gpio6_GPIO[30]	
RGMIIR_TD0	C22	RGMIIR_TD0 (ALT1)	0.000V - RGMII	gpio6_GPIO[20]	
RGMIIR_TD1	F20	RGMIIR_TD1 (ALT1)	0.000V - RGMII	gpio6_GPIO[21]	
RGMIIR_TD2	E21	RGMIIR_TD2 (ALT1)	0.000V - RGMII	gpio6_GPIO[22]	
RGMIIR_TD3	A24	RGMIIR_TD3 (ALT1)	0.000V - RGMII	gpio6_GPIO[23]	
RGMIIR_TX_CTL	C23	RGMIIR_TX_CTL (ALT1)	0.000V - RGMII	gpio6_GPIO[26]	

Comments auto-generated to denote original Module/Signal:

- WAS Instance:gpio1 Signal:GPIO[25]
- WAS Instance:gpio1 Signal:GPIO[26]
- WAS Instance:gpio1 Signal:GPIO[27]

Code Reflects Added Signals

- Basic Code Style as a Tooltip.

The screenshot shows the IO Mux configuration tool interface. On the left, a tree view lists various components and pins. The center pane displays a table of peripheral signals with columns for Peripheral/Signal, Ball, Pad Name (AltMode), Power Group, GPIO, and Signal Notes. The right pane shows a code editor with a tooltip for the signal GPIO[15].

Peripheral/Signal	Ball	Pad Name (AltMode)	Power Group	GPIO	Signal Notes
audmux (4 of 24) Set power level for SD2					
AUD4_RXD	A22	SD2_DAT0 (ALT3)	0.000V - SD2	gpio1_GPIO[15]	
AUD4_TXC	B22	SD2_DAT3 (ALT3)	0.000V - SD2	gpio1_GPIO[12]	
AUD4_TXD	A23	SD2_DAT2 (ALT3)	0.000V - SD2	gpio1_GPIO[13]	
AUD4_TXFS	E20	SD2_DAT1 (ALT3)	0.000V - SD2	gpio1_GPIO[14]	
can1 (5 of 5) Set power level for ENET					
can1 (5 of 5)					
can2					
ccm (2 of 14)					
cheetah					
csu					
dcic1					
dcic2					
ecspi1 (4 of 8)					
ecspi2					
ecspi3					
ecspi4					
ecspi5					
enet (14 of 39)					
epit1					
epit2					
esai1					
gpio1 (7 of 29)					
GPIO[0] ALT5 - GPIO_0 (T5)					
GPIO[1] ALT5 - GPIO_1 (T4)					
GPIO[10] ALT5 - SD2_CLK (C21)					
GPIO[11] ALT5 - SD2_CMD (F19)					
GPIO[12] ALT5 - SD2_DAT3 (B22)					
GPIO[13] ALT5 - SD2_DAT2 (A23)					
GPIO[14] ALT5 - SD2_DAT1 (E20)					
GPIO[15] ALT5 - SD2_DAT0 (A22)					
GPIO[16] ALT5 - SD1_DAT0 (A21)					
GPIO[17] ALT5 - SD1_DAT1 (C20)					
GPIO[18] ALT5 - SD1_CMD (B21)					
GPIO[19] ALT5 - SD1_DAT2 (F19)					

```
// Function to config iomux for instance can1.
void can1_iomux_config(void)
{
    // Config gpio1_RXCAN to pad KEY_ROW2(W4)
    write(0x00000002, IOMUXC_SW_MUX_CTL_PAD_KEY_ROW2); // SION_DISABLED, ALT2
    write(0x00000000, IOMUXC_CAN1_IPP_IND_CANRX_SELECT_INPUT); // SEL_KEY_ROW2_ALT2
    // HYS_ENABLED, PUS_100KOHM_PU, PUE_PULL, PKE_ENABLED, ODE_DISABLED, SPD_100MHZ, DSE_40OHM, SRE_SLOW
    write(0x0001B0B0, IOMUXC_SW_PAD_CTL_PAD_KEY_ROW2);

    // Config can1_TXCAN to pad KEY_COL2(W6)
    write(0x00000002, IOMUXC_SW_MUX_CTL_PAD_KEY_COL2); // SION_DISABLED, ALT2
    // HYS_ENABLED, PUS_100KOHM_PU, PUE_PULL, PKE_ENABLED, ODE_DISABLED, SPD_100MHZ, DSE_40OHM, SRE_SLOW
    write(0x0001B0B0, IOMUXC_SW_PAD_CTL_PAD_KEY_COL2);

    // Config can1_CAN1_STBY to pad ENET_CRS_DV(U21)
    // WAS Instance:gpio1 Signal:GPIO[25]
    write(0x00000005, IOMUXC_SW_MUX_CTL_PAD_ENET_CRS_DV); // SION_DISABLED, ALT5
    // HYS_ENABLED, PUS_100KOHM_PU, PUE_PULL, PKE_ENABLED, ODE_DISABLED, SPD_100MHZ, DSE_40OHM, SRE_SLOW
    write(0x0001B0B0, IOMUXC_SW_PAD_CTL_PAD_ENET_CRS_DV);

    // Config can1_CAN1_NERR to pad ENET_RXD1(W22)
    // WAS Instance:gpio1 Signal:GPIO[26]
    write(0x00000005, IOMUXC_SW_MUX_CTL_PAD_ENET_RXD1); // SION_DISABLED, ALT5
    // HYS_ENABLED, PUS_100KOHM_PU, PUE_PULL, PKE_ENABLED, ODE_DISABLED, SPD_100MHZ, DSE_40OHM, SRE_SLOW
    write(0x0001B0B0, IOMUXC_SW_PAD_CTL_PAD_ENET_RXD1);

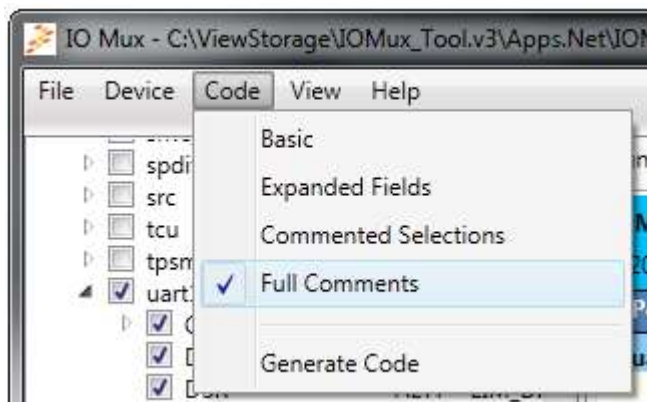
    // Config can1_CAN1_EN to pad ENET_RXD0(W21)
    // WAS Instance:gpio1 Signal:GPIO[27]
    write(0x00000005, IOMUXC_SW_MUX_CTL_PAD_ENET_RXD0); // SION_DISABLED, ALT5
    // HYS_ENABLED, PUS_100KOHM_PU, PUE_PULL, PKE_ENABLED, ODE_DISABLED, SPD_100MHZ, DSE_40OHM, SRE_SLOW
    write(0x0001B0B0, IOMUXC_SW_PAD_CTL_PAD_ENET_RXD0);
}
```

WAS Instance:gpio1 Signal:GPIO[25]
WAS Instance:gpio1 Signal:GPIO[26]
WAS Instance:gpio1 Signal:GPIO[27]
SGTL5000 - sys_mclk
J5 - Camera mclk
I5 - Camera GP

0 conflicts!

Generate Configuration Code

- Several Code-Styles available in the Code Menu.
- Examples are shown in the User's Guide.
- Click “Generate Code” to create the files for the current design.



Try it

uart2 (4 of 4)			
CTS			
RTS	J19	EIM_D29 (ALT4)	
RXD_MUX	E25	EIM_D27 (ALT4)	
TXD_MUX	E24	EIM_D26 (ALT4)	



i.MX 6 Hardware bring up

i.MX6 Hardware bring up: Doc&Tools.

- IMX6DQ6SDLHDG.pdf: Chapter 8 Avoiding Board Bring-up Problems.
- IMX6XRM.pdf:Chapter7 System Boot, Chapter 60:System Reset Controller(SRC)
- MFG tools, DDR test tools.
- USB line;有源可限流电源，万用表，示波器

i.MX6 Hardware bring up: Step 1 目视检查

- 检查主要器件是否有错贴的情况，比如说二极管，三极管，有没有安装位置反向或旋转的问题。
- 可以在PCBA时使用X光检查，有条件的使用BSDL检查来确认焊接与连线

i.MX6 Hardware bring up: Step 2 电源检查

- 使用万用表，先空板检查每个电源有没有对地短路的情况。
- 使用限流电源上电，检查i.MX6每路电源的电压是否符合我们datasheet要求，量测电压是要求在电源输出端和i.MX6电源输入端(越近越好，如在滤波电容上量测)都量测一下，以避免IR跌落。VDD_ARM/SOC_IN供给i.MX6内部逻辑电路，需要仔细检查，VDD_SNVS_IN, NVCC_JTAG, NVCC_DRAM也对正常启动很重要，NVCC_LVDS2V5也供给了DDR I/O Pads,也必须要正常供给。
- i.MX6在各路电源稳定后，才能释放reset(POR_B)。
- 如前电源上电时序要求，检查上电时序。

i.MX6 Hardware bring up: Step 3 时钟检查

- 一般在电源电压正确，无跌落，24Mhz和32K晶体会自动起振。
- 可使用示波器量测这两个时钟，如果24Mhz不工作，则系统不能启动，如果外部没有32K，或32K不工作，则i.MX6会自动使用内部晶振，但根据new errata IM6DQCE Rev.4, 07/2014 : ERR007926 ROM: 32 kHz internal oscillator timing inaccuracy may affect SD/MMC, NAND, and OneNAND boot, 由于内部rom code的GPT使用这个时钟，而GPT被用于外设访问中一些event和timeout控制，所以不稳定的时钟有可能导致rom codes读取外设失败，所以请参考errata fix solution:使用外部时钟，或如果使用32K晶体，要加reset时钟芯片等待32K稳定。

i.MX6 Hardware bring up: Step 4 准备bring up文档

一般硬件工程师需要准备三份文档描述板级设计

- 电源文档: 每一路电源的源，供给到？输出，输入电压，测量点,时序。如SDP schematic:

	Voltage	Power Up Sequence	Current Drawn (mA)	SYS 4V2 Current (mA)	NOTES
SW1A	1.375	1	2155	1001	
SW1B					
SW1C	1.375	2	1590	739	
SW2	3.3	5	653	728	
SW3A	1.5	3	1500	760	
SW3B					
SW4	3.15	6	200	213	
SWBST	5.0	13	300	507	
VGEN1	1.5	9	100	0	Supplied from SW4
VGEN2	1.5	10	250	0	Supplied from SW4
VGEN3	2.8	11	70	66	
VGEN4	1.8	12	310	189	
VGEN5	2.8	10	75	71	See Note on Page 20
VGEN6	3.3	8	160	178	
VSNVS	3.0	0	0.2	0	
VREFDDR	0.75	3	10	3	
Total System Current Requirements:				4454	

Voltage	Rail Name	Block	Generated By	Current Capability (mA)	NOTES
5.0	PMIC_5V	USB	PF0100 SWBST	600	
		LVDS1			
	AUX_5V	HDMI	MAX8815	1000	
		SATA			
3.3	GEN_3V3	LVDS0	PF0100 SW2	2000	NVCC_LCD NVCC_EIM0/1/2 NVCC_GPIO NVCC_SD2/3 NVCC_NANDF NAND_ITAG
		CAN			
		EMMC			
		SD3			
		NOR			
		SATA			
		LVDS			
		HDMI			
		MIPI			
		mPCIe			
3.15	AUX_3V15	SENSORS	PF0100 VGEN6	200	NVCC_ENET
		ETH			
		EXP HDR			
		TOUCH			
2.8	VDDHIGH_1N	IMX6	PF0100 VGEN5	100	
	VGEN2_2V5	CAMERA	PF0100 VGEN3	100	
2.5	GEN_2V5	SATA	IMX6 VDDHIGH_CAP	TBD	NVCC_MIPI
		HDMI			
		MIPI			
		mPCIe			
1.8	GEN_1V8	AUDIO	PF0100 VGEN4	350	NVCC_SD1 NVCC_CSI
		CAMERA			
1.5	VGEN2_1V5	ACC	PF0100 VGEN2	250	
	VGEN1_1V5	CAMERA	PF0100 VGEN1	100	
		GPS	PF0100 VGEN1	100	
		mPCIe	PF0100 VGEN1	100	
1.375	DDR_1V5	DDR	PF0100 SW3A/B	2500	
	VDDCORE	ARMCORE	PF0100 SW1A/B	2500	
0.75	VDDSOC	VDDSOC	PF0100 SW1C	1750	
	VREFDDR	DOR	PF0100 VREFDDR	10	

i.MX6 Hardware bring up: Step 4 准备bring up文档

- IOMUX文档：可以使用iomux工具导出，也可以手动准备，内容最好包括：

管脚名脚	管序号	网络名	IOMUX	用于
CSI0_DATA10	M1	UART1_TX	ALT3	UART1_TX

以方便软件工程师配置IOMUX，这个表应该至少包括所有数字管脚，软件工程师根据这个表来配置iomux文件：arch\arm\mach-mx6\Board-mx6q_sabersd.h

```
static iomux_v3_cfg_t mx6q_sabresd_pads[] = {  
...
```

```
/* UART1 for debug */
```

```
MX6Q_PAD_CSI0_DAT10__UART1_TXD, //CSI0_DAT10为管脚名，UART1_TX为功能名。
```

Notes:

- 1 i.MX6基本所有的可做为GPIO 的pin在reset状态下都是iomux设为gpio，gpio设为输入高阻，iopad设为100K上拉的。
- 2 i.MX6的datasheet中也列出了一些例外:For most of the signals, the state during reset is same as the state after reset, However, there are few signals for which the state during reset is different from the state after reset: EIM_A16~A25, EIM_DA0~DA15, EIM_EB1~EB3, EIM_LBA/RW/WAIT, GPIO_17/19, KEY_COL0, 请注意有一些pin是用于boot gpio的。

i.MX6 Hardware bring up: Step 4 准备bring up文档

- Boot_Cfg文档：说明Boot_cfg配置，以SDP的eMMC boot为例

Fuse	SBMR1	定义	GPIO管脚	默认值	设置值	默认值定义
BOOT_CFG1[7:6]	Bit7_6	启动设备接口	EIM_DA7_6	00	01	01: Boot from USDHC
BOOT_CFG1[5]	bit5	SD/MMC Sel	EIM_DA5	0	1	0: SD/eSD/SDXC; 1: MMC/eMMC
BOOT_CFG1[4]	bit4	Fast Boot Suppo	EIM_DA4	0	0	0:Normal Boot; 1: Fast Boot
BOOT_CFG1[3:2]	bit3_2	SD/MMC速度模式	EIM_DA3_2	00	00	MMC: 0x: High Speed Mode;1x:Normal Speed Mode SD: 0x: High/Normal; 10:SDR50; 11:SDR104
BOOT_CFG1[1]	bit1	SD Power Cycle eMMC Reset	EIM_DA1	0	0	MMC: 0:eMMC reset disabled. 1:eMMC reset enabled via SD_RST pad(on USDHC3/4) SD: 0: No power cycle 1:Power cycle enabled vis SD_RST pad(on USDHC3/4)
BOOT_CFG1[0]	bit0	SD Loopback Clock Source Sel(SDR50/104 only)	EIM_DA0	0	0	0: through SD pad 1: direct
BOOT_CFG2[7:5]	bit15_13	Bus Width/SD Calibration Step	EIM_DA15~13	000	010	SD: Bus Width: xx0:1bit; xx1:4bit. SD Calibration Step: 00x~11x:1~3 delay cells MMC 000~010: 1,4,8bit. 101~110: 4,8bit DDR(MMC4.4)

i.MX6 Hardware bring up: Step 4 准备bring up文档

Fuse	SBMR1	定义	GPIO管脚	默认值	设置值	默认值定义
BOOT_CFG2[4:3]	Bit12_11	启动设备接口	EIM_DA12_11	00	11	00~11: USDHC1~4
BOOT_CFG2[2]	Bit10	DLL Override(eMMC)	EIM_DA10	0	0	0: Boot ROM default; 1: Apply value per fuse MMC_DLL_DLY[6:0]
BOOT_CFG2[1]	Bit9	Boot ACK disable/Pull down During Power Cycle Enable	EIM_DA9	0	0	MMC: 0: Boot ACK Enabled; 1: Boot ACK Disabled. SD: 0: Use the default SD pad settings during power cycle. 1: Set Pull down on SD pads during power cycle
BOOT_CFG2[0]	bit8	Override Pad Settings	EIM_DA8	0	0	0: Use the default values. 1: Use PAD_SETTINGS values.

SDP的Boot Select为: 所以eMMC启动的SBMR1=0Xxxx5860

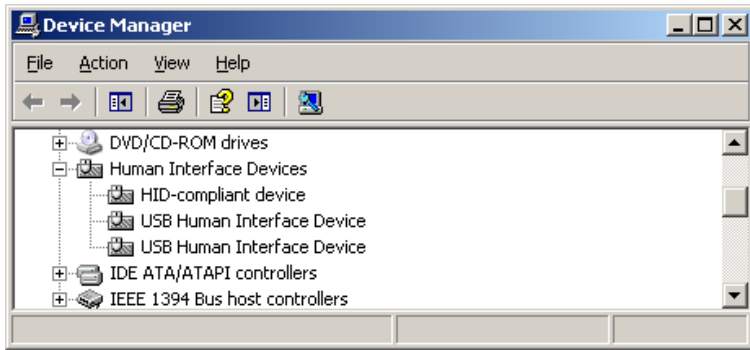
Boot Select Table

8	7	6	5	4	3	2	1
BT_CFG1_7	BT_CFG1_6	BT_CFG1_5	BT_CFG1_4	BT_CFG2_6	BT_CFG2_5	BT_CFG2_4	BT_CFG2_3
011X = MMC/eMMC Boot				X0 = 1-bit X1 = 4-bit 10 = 8-bit		01 = SD2 Boot 10 = SD3 Boot 11 = SD4 Boot	
010X = SD/eSD Boot				X0 = 1-bit X1 = 4-bit		01 = SD2 Boot 10 = SD3 Boot 11 = SD4 Boot	
0010 = SATA Boot				X	X	X	0

i.MX6 Hardware bring up: Step 5 确认启动配置

i.MX6在上电正确，时钟正确，POR正确后，会首先执行内部的ROM codes，这个ROM codes,首先会读取SBMR2寄存器的值，来判断启动模式，如果为下载模式，则进入下载模式。如果为正常启动模式则会根据读取SBMR1寄存器的值来初始化相应启动设备的控制器，并尝试去读取相应设备上的镜像，并认证。如果认证成功，则根据镜像开头的数据结构来初始化外部DDR，然后将镜像拷贝到外存，并跳转到外存执行bootloader。如果镜像认证失败，则又进入下载模式。

进入下载模式后，i.MX6会通过USB OTG口与host PC联系，并报告为一个HID设备。所以从PC上可以看到一个USB HID设备信息。如果有这个信息报出，证明i.MX6的最小系统工作了(电源，时钟，POR，内部ROM codes已经执行并进入了下载模式)。



如果我们已经设置为正常启动模式，并且配置boot_cfg相应的GPIO，则可以使用示波器量测启动设备上相应的时钟：

- Nand: CE pin for read enable clock
- SPI-NOR: Slave Select or Clock pin.
- MMC/SD: SD_CLK pin.

如果有时钟，则说明ROM codes已经开始读取相应启动设备，硬件Boot_cfg GPIO配置是正确的。如果没有，则说明Boot_cfg GPIO配置可能有问题，需要再次检查硬件。

i.MX6 Hardware bring up: Step 6 测试外部内存

i.MX6最小系统工作以后，下一步需要保证外部内存已经工作了，这样才可以确保bootloader软件可以工作。所以接下来需要测试外部DDR。

- 根据DDR datasheet,使用Mx6DQSDL DDR3 Script Aid工具来生成DDR初始化脚本。

- 连接硬件，运行 DDR_Stress_Tester.exe
- -t mx6x -df MX6QD_SabreSD_DDR3_528MHz_64bit.inc，根据提示来校准DDR及进行压力测试。如果压力测试通过，则说明外部DDR工作正常。

- DDR测试详细请参看文档MX6X_DDR3_调校_应用手册_V1.doc

- DDR初始化脚本可作为bootloader中的DDR初始化数据结构用,在文件:uboot\board\freescall\mx6q_sabersd\flash_header.s

- 使用\uboot-2009.08\include\configs\mx6q_sabresd_iram.h可以编译出基于内部iRam运行的uboot,对比运行在外部DDR的uboot可以判断是否为外部DDR问题。



i.MX6 Hardware bring up: 完成

以上步骤完成后，则可以初步说明i.MX6系统(i.MX6, 电源，外部DDR)工作正常。可以进行接下来的软件bring up工作。软件定制基本包括：

- 根据DDR初始化脚本来配置uboot的flash_header数据结构。
- 根据IOMUX文档来配置uboot和内核的iomux数组。
- 根据板级的外设情况来准备一个相对较小的内核，并编译出MFG和正常内核。
- 使用MFG烧写启动设备，调试MFG内核。
- 烧写成功后，启动，如果有uboot串口消息打出，则可以使用串口消息来继续调试。

i.MX6 Hardware bring up: 一些调试方法 1 :确认启动配置

刚才说到可以通过量测启动设备相应的管脚clock信号来判断Boot_cfg设置是否正确，而如果MFG及MFG镜像可以工作，也可以使用MFG直接读取SBMR1寄存器来获取：

1. 将MFG的uboot换成正常启动的uboot，即替换掉 \Mfgtools-Rel-4.1.0_130816_MX6Q_UPDATER\Profiles\MX6Q Linux Update\OS Firmware\ u-boot-mx6q-sabresd.bin(MFG的uboot和正常启动的uboot对比一个不同就是MFG的uboot取消了等待3S输入的功能，而正常的uboot可以)
2. 启动板子，进入下载模式(boot mode为下载，或是启动镜像认证失败都会进入)。
3. 进入下载模式后就可以运行MFG，将正常启动的uboot镜像下载到外部内存并运行起来。
4. 在串口上键入“空格”，停下uboot,然后使用uboot的”md”命令就可以读取sbmr1寄存器：“md 020d8004” (sbmr1寄存器地址)，在SDP, eMMC 启动时为0x00005860，与上文我们配置的一致。

所以总结下来如果系统因为启动模式不对而进入到下载模式，我们可以通过MFG来精确确认SBMR1寄存器值，从而了解是那些Boot_Cfg GPIO配置不对。



www.Freescale.com