Table 11. Terms and symbols used in *Table 12* (continued)

Column		Symbol	Definition
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 12. Pin assignment and description

Pin				Pin name (function upon reset)	Pin type	I/O structure(1)	Current group	Note	Alternate functions	Additional functions
SO8N	TSSOP20	LQFP32	LQFP48							
-	-	-	1	PC13	I/O	-	N	-	TIM1_BK	TAMP_IN1, RTC_TS, RTC_OUT1, WKUP2
-	-	-	2	PC14-OSC32_IN (PC14)	I/O	-	N	-	TIM1_BK2	OSC32_IN
1	2	2	-	PC14-OSC32_IN (PC14)	I/O	-	N	-	TIM1_BK2	OSC32_IN, OSC_IN
-	3	3	3	PC15-OSC32_OUT (PC15)	I/O	-	N	-	OSC32_EN, OSC_EN	OSC32_OUT
-	-	-	4	VBAT	S	-	-	-	-	VBAT
-	-	-	5	VREF+	S	-	-	-	-	-
2	4	4	6	VDD/VDDA	S	-	-	-	-	-
3	5	5	7	VSS/VSSA	S	-	-	-	-	-
-	-	-	8	PF0-OSC_IN (PF0)	I/O	-	S	-	TIM14_CH1	OSC_IN
-	-	-	9	PF1-OSC_OUT (PF1)	I/O	-	S	-	OSC_EN	OSC_OUT
4	6	6	10	NRST	I/O	-	S	-	-	NRST
4	7	7	11	PA0	I/O	-	S	-	SPI2_SCK, USART2_CTS,	ADC_IN0, TAMP_IN2,WKUP1
4	8	8	12	PA1	I/O	-	S	-	SPI1_SCK/I2S1_CK, USART2_RTS_DE_CK, I2C1_SMBA, EVENTOUT	ADC_IN1

Table 12. Pin assignment and description (continued)

Pin				Pin name (function upon reset)	Pin type	I/O structure[1]	Current group	Note	Alternate functions	Additional functions
SO8N	TSSOP20	LQFP32	LQFP48							
4	9	9	13	PA2	I/O	-	S	-	SPI1_MOSI/I2S1_SD, USART2_TX,	ADC_IN2, WKUP4,LSCO
-	10	10	14	PA3	I/O	-	S	-	SPI2_MISO, USART2_RX, EVENTOUT	ADC_IN3
-	-	-	15	PA4	I/O	-	S	-	SPI1_NSS/I2S1_WS, SPI2_MOSI, TIM14_CH1, EVENTOUT	ADC_IN4, RTC_OUT2
-	11	11	-	PA4	I/O	-	S	-	SPI1_NSS/I2S1_WS, SPI2_MOSI, TIM14_CH1, EVENTOUT	ADC_IN4, TAMP_IN1, RTC_TS, RTC_OUT1, WKUP2
-	12	12	16	PA5	I/O	-	S	-	SPI1_SCK/I2S1_CK, EVENTOUT	ADC_IN5
-	13	13	17	PA6	I/O	-	S	-	SPI1_MISO/I2S1_MCK, TIM3_CH1, TIM1_BK, TIM16_CH1	ADC_IN6
-	14	14	18	PA7	I/O	-	S	-	SPI1_MOSI/I2S1_SD, TIM3_CH2, TIM1_CH1N, TIM14_CH1, TIM17_CH1	ADC_IN7
5	15	15	19	PB0	I/O	-	S	-	SPI1_NSS/I2S1_WS, TIM3_CH3, TIM1_CH2N	ADC_IN8
5	15	16	20	PB1	I/O	-	S	-	TIM14_CH1, TIM3_CH4, TIM1_CH3N, EVENTOUT	ADC_IN9
-	15	17	21	PB2	I/O	-	S	-	SPI2_MISO, EVENTOUT	ADC_IN10
-	-	-	22	PB10	I/O	-	S	-	SPI2_SCK, I2C2_SCL	ADC_IN11
-	-	-	23	PB11	I/O	-	S	-	SPI2_MOSI, I2C2_SDA	ADC_IN15
-	-	-	24	PB12	I/O	-	S	-	SPI2_NSS, TIM1_BK, EVENTOUT	ADC_IN16
-	-	-	25	PB13	I/O	-	S	-	SPI2_SCK, TIM1_CH1N, I2C2_SCL, EVENTOUT	-
-	-	-	26	PB14	I/O	-	S	-	SPI2_MISO, TIM1_CH2N, I2C2_SDA, EVENTOUT	-
-	-	-	27	PB15	I/O	-	S	-	SPI2_MOSI, TIM1_CH3N, EVENTOUT	RTC_REFIN
5	15	18	28	PA8	I/O	-	S	-	MCO, SPI2_NSS, TIM1_CH1, EVENTOUT	-

Table 12. Pin assignment and description (continued)

Pin				Pin name (function upon reset)	Pin type	I/O structure[1]	Current group	Note	Alternate functions	Additional functions
SO8N	TSSOP20	LQFP32	LQFP48							
-	-	19	29	PA9	I/O	-	S	-	MCO, USART1_TX, TIM1_CH2, SPI2_MISO, I2C1_SCL, EVENTOUT	-
-	-	20	30	PC6	I/O	-	S	-	TIM3_CH1	-
-	-	-	31	PC7	I/O	-	S	-	TIM3_CH2	-
-	-	21	32	PA10	I/O	-	S	-	SPI2_MOSI, USART1_RX, TIM1_CH3, TIM17_BK, I2C1_SDA, EVENTOUT	-
-	-	-	33	PA11 [PA9]	I/O	-	N	-	SPI1_MISO/I2S1_MCK, USART1_CTS, TIM1_CH4, TIM1_BK2, I2C2_SCL	-
5	16	22	-	PA11 [PA9]	I/O	-	N	-	SPI1_MISO/I2S1_MCK, USART1_CTS, TIM1_CH4, TIM1_BK2, I2C2_SCL	ADC_IN15
-	-	-	34	PA12 [PA10]	I/O	-	N	-	SPI1_MOSI/I2S1_SD, USART1_RTS_DE_CK, TIM1_ETR, I2S_CKIN, I2C2_SDA	-
6	17	23	-	PA12 [PA10]	I/O	-	N	-	SPI1_MOSI/I2S1_SD, USART1_RTS_DE_CK, TIM1_ETR, I2S_CKIN, I2C2_SDA	ADC_IN16
7	18	24	35	PA13	I/O	-	N	-	SWDIO, IR_OUT, EVENTOUT	ADC_IN17
8	19	25	36	PA14-BOOT0	I/O	-	N	-	SWCLK, USART2_TX, EVENTOUT	ADC_IN18, BOOT0
8	19	26	37	PA15	I/O	-	N	-	SPI1_NSS/I2S1_WS, USART2_RX, EVENTOUT	-
-	-	-	38	PD0	I/O	-	N	-	EVENTOUT, SPI2_NSS, TIM16_CH1	-
-	-	-	39	PD1	I/O	-	N	-	EVENTOUT, SPI2_SCK, TIM17_CH1	-
-	-	-	40	PD2	I/O	-	N	-	TIM3_ETR, TIM1_CH1N	-
-	-	-	41	PD3	I/O	-	N	-	USART2_CTS, SPI2_MISO, TIM1_CH2N	-

Table 12. Pin assignment and description (continued)

Pin				Pin name (function upon reset)	Pin type	I/O structure[1]	Current group	Note	Alternate functions	Additional functions
SO8N	TSSOP20	LQFP32	LQFP48							
-	20	27	42	PB3	I/O	-	N	-	SPI1_SCK/I2S1_CK, TIM1_CH2, USART1_RTS_DE_CK, EVENTOUT	-
-	20	28	43	PB4	I/O	-	N	-	SPI1_MISO/I2S1_MCK, TIM3_CH1, USART1_CTS, TIM17_BK, EVENTOUT	-
8	20	29	44	PB5	I/O	-	N	-	SPI1_MOSI/I2S1_SD, TIM3_CH2, TIM16_BK, I2C1_SMBA	WKUP6
8	20	30	45	PB6	I/O	-	N	-	USART1_TX, TIM1_CH3, TIM16_CH1N, SPI2_MISO, I2C1_SCL, EVENTOUT	-
-	-	-	46	PB7	I/O	-	N	-	USART1_RX, SPI2_MOSI, TIM17_CH1N, I2C1_SDA, EVENTOUT	-
1	1	31	-	PB7	I/O	-	N	-	USART1_RX, SPI2_MOSI, TIM17_CH1N, I2C1_SDA, EVENTOUT	ADC_IN11
1	1	32	47	PB8	I/O	-	N	-	SPI2_SCK, TIM16_CH1, I2C1_SCL, EVENTOUT	-
1	2	1	48	PB9	I/O	-	N	-	IR_OUT, TIM17_CH1, SPI2_NSS, I2C1_SDA, EVENTOUT	-

1. Will be provided later

Table 13. Port A alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	SPI2_SCK	USART2_CTS	-	-	-	-	-	-
PA1	SPI1_SCK/ I2S1_CK	USART2_RTS _DE_CK	-	-	-	-	I2C1_SMBA	EVENTOUT
PA2	SPI1_MOSI/ I2S1_SD	USART2_TX	-	-	-	-	-	-
PA3	SPI2_MISO	USART2_RX	-	-	-	-	-	EVENTOUT
PA4	SPI1_NSS/ I2S1_WS	SPI2_MOSI	-	-	TIM14_CH1	-	-	EVENTOUT
PA5	SPI1_SCK/ I2S1_CK	-	-	-	-	-	-	EVENTOUT
PA6	SPI1_MISO/ I2S1_MCK	TIM3_CH1	TIM1_BKIN	-	-	TIM16_CH1	-	-
PA7	SPI1_MOSI/ I2S1_SD	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	-	-
PA8	MCO	SPI2_NSS	TIM1_CH1	-	-	-	-	EVENTOUT
PA9	MCO	USART1_TX	TIM1_CH2	-	SPI2_MISO	-	I2C1_SCL	EVENTOUT
PA10	SPI2_MOSI	USART1_RX	TIM1_CH3	-	-	TIM17_BKIN	I2C1_SDA	EVENTOUT
PA11	SPI1_MISO/ I2S1_MCK	USART1_CTS	TIM1_CH4	-	-	TIM1_BKIN2	I2C2_SCL	-
PA12	SPI1_MOSI/ I2S1_SD	USART1_RTS _DE_CK	TIM1_ETR	-	-	I2S_CKIN	I2C2_SDA	-
PA13	SWDIO	IR_OUT	-	-	-	-	-	EVENTOUT
PA14	SWCLK	USART2_TX	-	-	-	-	-	EVENTOUT
PA15	SPI1_NSS/ I2S1_WS	USART2_RX	-	-	-	-	-	EVENTOUT

Table 14. Port B alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	SPI1_NSS/ I2S1_WS	TIM3_CH3	TIM1_CH2N	-	-	-	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	-	-	-	-	EVENTOUT
PB2	-	SPI2_MISO	-	-	-	-	-	EVENTOUT
PB3	SPI1_SCK/ I2S1_CK	TIM1_CH2	-	-	USART1_RTS _DE_CK	-	-	EVENTOUT
PB4	SPI1_MISO/ I2S1_MCK	TIM3_CH1	-	-	USART1_CTS	TIM17_BKIN	-	EVENTOUT
PB5	SPI1_MOSI/ I2S1_SD	TIM3_CH2	TIM16_BKIN	-	-	-	I2C1_SMBA	-
PB6	USART1_TX	TIM1_CH3	TIM16_CH1N	-	SPI2_MISO	-	I2C1_SCL	EVENTOUT
PB7	USART1_RX	SPI2_MOSI	TIM17_CH1N	-	-	-	I2C1_SDA	EVENTOUT
PB8	-	SPI2_SCK	TIM16_CH1	-	-	-	I2C1_SCL	EVENTOUT
PB9	IR_OUT	-	TIM17_CH1	-	-	SPI2_NSS	I2C1_SDA	EVENTOUT
PB10	-	-	-	-	-	SPI2_SCK	I2C2_SCL	-
PB11	SPI2_MOSI	-	-	-	-	-	I2C2_SDA	-
PB12	SPI2_NSS	-	TIM1_BKIN	-	-	-	-	EVENTOUT
PB13	SPI2_SCK	-	TIM1_CH1N	-	-	-	I2C2_SCL	EVENTOUT
PB14	SPI2_MISO	-	TIM1_CH2N	-	-	-	I2C2_SDA	EVENTOUT
PB15	SPI2_MOSI	-	TIM1_CH3N	-	-	-	-	EVENTOUT

Table 15. Port C alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC6	-	TIM3_CH1	-	-	-	-	-	-
PC7	-	TIM3_CH2	-	-	-	-	-	-
PC13	-	-	TIM1_BKIN	-	-	-	-	-
PC14	-	-	TIM1_BKIN2	-	-	-	-	-
PC15	OSC32_EN	OSC_EN	-	-	-	-	-	-

Table 16. Port D alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	EVENTOUT	SPI2_NSS	TIM16_CH1	-	-	-	-	-
PD1	EVENTOUT	SPI2_SCK	TIM17_CH1	-	-	-	-	-
PD2	-	TIM3_ETR	TIM1_CH1N	-	-	-	-	-
PD3	USART2_CTS	SPI2_MISO	TIM1_CH2N	-	-	-	-	-

Table 17. Port F alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0	-	-	TIM14_CH1	-	-	-	-	-
PF1	OSC_EN	-	-	-	-	-	-	-