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Scalable energy–efficient magnetoelectric spin–orbit logic

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Since the early 1980s, most electronics have relied on the use of complementary metal–oxide–semiconductor (CMOS) transistors. However, the principles of CMOS operation, involving a switchable semiconductor conductance controlled by an insulating gate, have remained largely unchanged, even as transistors are miniaturized to sizes of 10 nanometres. We investigated what dimensionally scalable logic technology beyond CMOS could provide improvements in efficiency and performance for von Neumann architectures and enable growth in emerging computing such as artifical intelligence. Such a computing technology needs to allow progressive miniaturization, reduce switching energy, improve device interconnection and provide a complete logic and memory family. Here we propose a scalable spintronic logic device that operates via spin–orbit transduction (the coupling of an electron's angular momentum with its linear momentum) combined with magnetoelectric switching. The device uses advanced quantum materials, especially correlated oxides and topological states of matter, for collective switching and detection. We describe progress in magnetoelectric switching and spin–orbit detection of state, and show that in comparison with CMOS technology our device has superior switching energy (by a factor of 10 to 30), lower switching voltage (by a factor of 5) and enhanced logic density (by a factor of 5). In addition, its non-volatility enables ultralow standby power, which is critical to modern computing. The properties of our device indicate that the proposed technology could enable the development of multi-generational computing.

Transistor technology scaling[1–3] has been enabled by controlling the conductivity of a semiconductor using an electric field applied across a high-quality insulating gate dielectric. This fundamental principle has remained largely unchanged since the seminal observations of Moore and Dennard et al.[4,5]. Yet in the past decade, transistor scaling has been enabled by direct improvements to the carrier transport[1,6,7], combined with superior electrostatic control[1–3,8]. In contrast to pure dimensional scaling[5], new transistor technologies have necessitated the use of strain[6], three-dimensional electrostatic gate control[2,8], manipulation of the effective carrier mass and band structure, and the gradual introduction of new materials for interface and work function control[9]. Despite the successful scaling in the size of transistors, voltage and frequency scaling have slowed[10]. Further decrease of voltage has been hampered by the Boltzmann limit of current control (60 mV for every change in current by a factor of 10 at room temperature). In response, a considerable effort to invent, demonstrate and benchmark beyond-CMOS devices got underway[11–13]. This effort includes alternative computing devices based on electron spin, electron tunnelling, ferroelectrics, strain and phase change[12,13] (see Methods for beyond-CMOS logic device options). However, a technologically suitable computational logic device that has superior energy efficiency, high logic density (that is, computed functions per unit area), non-volatility (to counteract leakage power) and efficient interconnects has remained elusive. The importance of these considerations has become evident during extensive modelling, benchmarking and evaluation of more than 25 beyond-CMOS device proposals[12,13]. With these considerations in view, we propose and demonstrate the building blocks for a new logic device that enables (1) voltage scaling, (2) scalable interconnects, (3) energy scaling and (4) the potential for multi-generational dimensional scaling.

Beyond-CMOS devices for replacing or enhancing the electronic transistor

Collective state switching devices are potential candidates for replacing or enhancing transistors. A collective state switch operates by the reversal of the material's order parameter (such as ferromagnetism, ferroelectricity and ferrotorodicity)[13] from Θ to $-\Theta$. It addresses sub-10-nm miniaturization by using collective order parameter dynamics, overcoming the 'Boltzmann tyranny', which is inherent to conductivity modulation, and providing a non-volatile nature to the computer. It is well documented that the 'Boltzmann tyranny' and leakage are the central challenges in traditional CMOS devices[1,2]. Logic based on collective state switching devices is a leading option for computational advances beyond the modern CMOS era owing to its (1) potential for superior energy per operation, (2) higher computational logical density and efficiency (that is, fewer devices required per combinatorial logic function) owing to the use of majority gates[14], (3) non-volatile memory-in-logic and logic-in-memory capability[15] and (4) amenability to traditional and emerging architectures (for example, neuromorphic[16] and stochastic computing[17]).

Among these possible collective state order parameters, ferroelectricity and multiferroicity are the preferred collective states for computing[13] owing to (1) the presence of a controllable, localized and phenomenologically strong carrier, the spontaneous dipole; (2) the switching efficiency of a ferroelectric with respect to the stability of the switch is given by the energy barrier per unit volume, $\lambda = E_{sw}/\Delta E(\Theta)$, where $\Delta E(\Theta)$ is the energy barrier relative to the stable state and E_{sw} is the total energy dissipated in switching; lower values of λ enable computing switches to operate at lower energies for a given energy barrier.

A vital consideration for a new technology is the need for highly compact nanoscale interconnects. While ferroelectric switching and the

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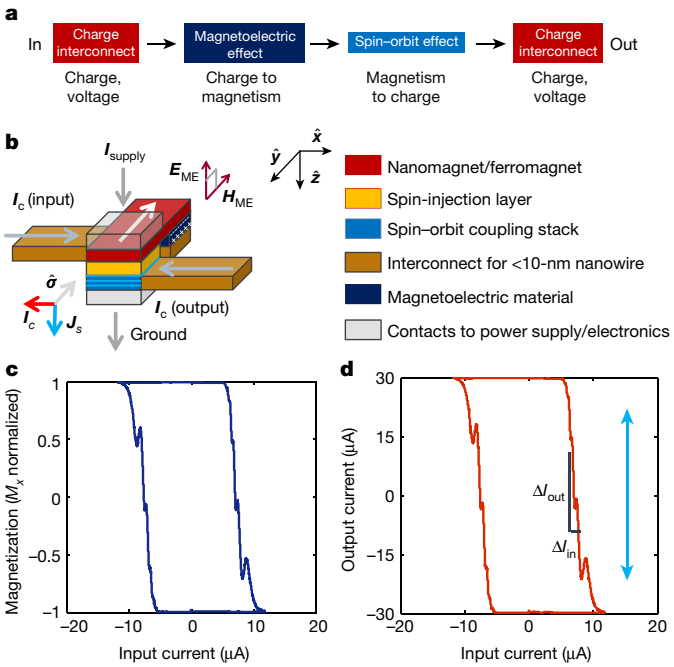

Fig. 1 | MESO logic transduction and device operation. a, Transduction of state variables for a cascadable charge-input and charge-output logic device. The magnetoelectric effect transduces the input information to magnetism, and the spin–orbit effect in a topological material transduces the magnetic state variable back to charge. **b**, MESO device formed with a magnetoelectric capacitor and a topological material. The device comprises a spin-injection layer for spin injection from the ferromagnet to the topological material, an interconnect made of a conductive material, and contacts to the power supply and ground. The logical state of the charge input (current in the $+\boldsymbol{x}$ direction) is inverted by the operation shown to charge output (current in the $-\boldsymbol{x}$ direction). Power for energy gain is injected from the power supply (arrows). Transduction mechanisms are calculated with magnetoelectric-vector SPICE models (see Methods and Supplementary Information). The white arrow represents the magnetization direction of the ferromagnet. Grey arrows represent electric currents at the input and output, power supply and ground. Injection of the power supply current allows for energy gain, large signal gain and the ability to drive larger output devices. **c**, Magnetoelectric transfer function, showing conversion of the charge input to ferromagnetic magnetization. **d**, Spin–orbit transfer function, showing conversion of a state to charge output. The response of the device is indicated for small signal gain (black line) and the full signal range (−15 μA to 15 μA; blue arrow). See Supplementary Fig. 1 for the two operating states of the MESO inverter device.

accompanying magnetoelectric switching of ferromagnets are perhaps the most energy-efficient charge-driven switching phenomena at the nanoscale and at room temperature, an efficient way to read out the state has been lacking. The discovery of strong spin–charge coupling in topological matter via a Rashba–Edelstein or topological two-dimensional electron gas[18–25] enables this proposal for a charge-driven, scalable logic computing device.

Spin–orbit logic device with magnetoelectric input signal nodes

We propose a logic computing device with magnetoelectric switching nodes and spin–orbit-effect readout operating at 100 mV, with an electrical interconnect. The magnetoelectric spin–orbit (MESO) device comprises two technologically scalable transduction mechanisms: ferroelectric/magnetoelectric switching[26–30] and topological conversion of spin to charge[19–24]. The device interfaces with electrical interconnects and is therefore charge-/voltage-driven and produces a charge/voltage output (Fig. 1a). The MESO device (Fig. 1b) comprises a magnetoelectric switching capacitor, a ferromagnet and a spin-to-charge conversion module (see 'Material requirements for 1–10-aJ-class MESO logic'). In Fig. 1b, when the input interconnect carries a positive current (current flowing in the $+\boldsymbol{x}$ direction), an electric field is set up in the magnetoelectric capacitor in the $-\boldsymbol{z}$ direction (into the plane). The resulting magnetoelectricity (represented as an effective field $\boldsymbol{H}_{ME}$), which may be comprised of an electrically controlled exchange bias or exchange anisotropy, switches the nanomagnet to the $-\boldsymbol{y}$ direction[27–30] (see Supplementary Information section A for details).

The readout (detection) of the state of the switch is enabled by the ongoing advances in spin-to-charge conversion using topological or high-spin–orbit-coupling (SOC) materials. A supply current is injected into the device, causing a flow of spin-polarized electrons from the ferromagnet into the SOC material. Owing to SOC spin-to-charge transduction (Fig. 1b), a charge current is generated at the output, in this case in the $-\boldsymbol{x}$ direction. Hence, the input charge state (positive voltage and current) is inverted by the MESO logic gate at the output.

We applied spin/magnetoelectric circuit theory[31,32] (see Supplementary Information section B) combined with stochastic magnetization dynamics solvers[32] (see Supplementary Information sections C and D) to obtain the transfer characteristics of the MESO logic device. We further used rigorous integrated-circuit solvers to validate and benchmark against spin-logic examples (Supplementary Information sections E and F). SPICE (simulation program with integrated circuit emphasis) circuit solvers were developed to incorporate the effects of: (1) magnetoelectric switching, (2) all the energy sources and dissipation elements (Supplementary Information sections G and H), (3) Landau–Khalatnikov dynamics of ferroelectric switching (Supplementary Information section I) and (4) peripheral charge circuitry (Supplementary Information section J). Details on simulations of energy scaling to <10 aJ (1 aJ = 10^{-18} J) using the power boundary method and component-level energy calculations are presented in Supplementary Information section K. The MESO inverter transfer functions, with magnetic and electric hysteresis, are shown in Fig. 1c, d. The input current I_{in} of the magnetization transfer function (Fig. 1c) relates the magnetoelectric stimulus with magnetization switching. It shows a small-signal gain ($d\hat{\boldsymbol{m}}/dI_{in}$, where $\hat{\boldsymbol{m}}$ is the magnetic moment unit vector for the nanomagnet's magnetization), which is advantageous for noise rejection. A large-signal gain of the output current, I_{out} (ratio I_{out}/I_{in}) is generated and controlled by the supply current (I_{supply}). A small-signal gain (dI_{out}/dI_{in}) of the device during switching can be seen in Fig. 1d. We show a scheme of the proposed short-/long-range interconnect in Fig. 2a, where the charge output of one MESO stage drives a charge current to switch the input of the next MESO stage[32,33]. Bidirectional logic switching of a cascaded six-stage MESO inverter chain is described in Supplementary Information section L.

Transduction mechanisms for the MESO device

We identified a scalable way to transduce the spin state of a nanomagnet to a charge state via spin–orbit effects[19–26,33–36], such as the interface Rashba–Edelstein effect (IREE) and spin-momentum locking in topological insulators. It has recently been shown that spin currents can be converted to charge currents that preserve the information encoded in spin polarization[34–37] (using resonant spin pumping in the quasi-static non-local spin-valve configuration[33]). Figure 2b shows how a current through a nanomagnet produces injection of spin-polarized electrons into a stack composed of materials with a high SOC coefficient (for example, Bi/Ag[22,37], topological insulators[21,24,34,35], oxides and two-dimensional materials[25,36]). In Fig. 2b, when $\hat{\boldsymbol{m}}$ is pointing in the $\hat{\boldsymbol{y}}$ direction and the flow of the injected spin current is $\boldsymbol{J}_s = J_s\hat{\boldsymbol{z}}$, with injected spin polarization along the $+y$ direction, charge current $\boldsymbol{I}_c$ is generated in the $\hat{x}$ direction. When the nanomagnet reverses to the $-\hat{\boldsymbol{y}}$ direction and the flow of injected spin current is still $\boldsymbol{J}_s = J_s\hat{\boldsymbol{z}}$, but with injected spin polarization along the $-y$ direction, a charge current $\boldsymbol{I}_c$ is generated in the $-\hat{x}$ direction. Hence, the magnetization direction of the nanomagnet is transduced into the direction of the electric current.

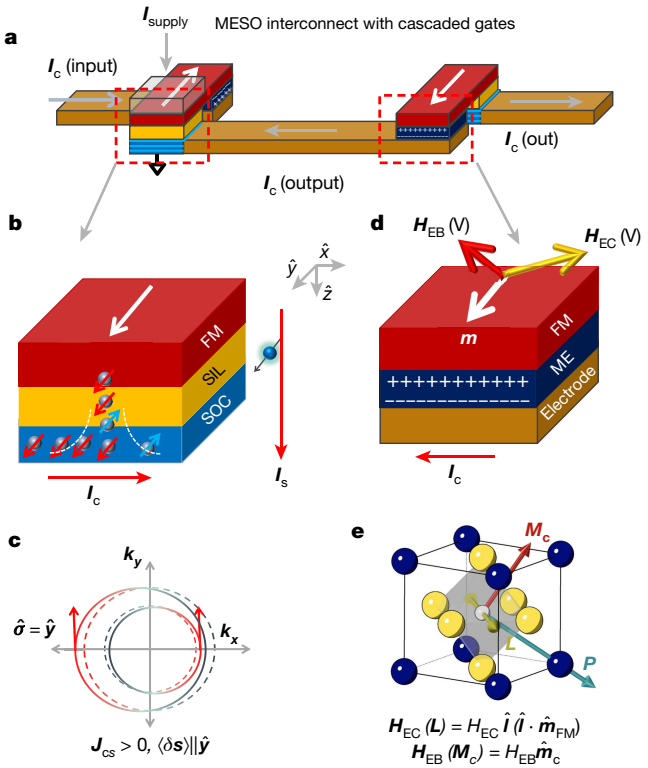

Fig. 2 | Operating mechanisms for MESO logic. a, A low-voltage-charge-based MESO interconnect with cascaded logic gates. Two inverters are chained together to form an interconnect. Arrows show the directions of the input and output currents of the device. Materials are as in Fig. 1. **b**, Operating mechanism for spin-to-charge conversion using a high-SOC material (SOC). A spin injection layer (SIL) is used where needed by the materials' interfaces. Spins injected from the ferromagnet (FM) in the $+\boldsymbol{z}$ direction with spin polarization along the $+\boldsymbol{y}$ (in-plane) direction cause a topologically generated charge current in the SOC layer. Small red and blue arrows indicate up and down spins, respectively, injected from the magnet. The large red arrows show the directions of the charge ($\boldsymbol{I}_c$) and injected spin ($\boldsymbol{I}_s$) currents. **c**, Schematic of the $\boldsymbol{k}$-space for spin-to-charge conversion at a two-dimensional electron gas with high SOC. Injecting a spin current polarized along the $+\boldsymbol{y}$ direction overpopulates the Fermi surface on one side of the topological material compared to the other side. This generates a net charge current in the $\boldsymbol{x}$ direction. The conversion has the right symmetry to convert the information of the ferromagnet to the charge current output. The dashed and solid lines depict the Fermi surface of the material before and after spin injection, respectively. Injected spin density $\langle \delta \boldsymbol{s} \rangle$ along the $+y$ direction leads to charge current $\boldsymbol{J}_{cs} > 0$. **d**, Operating mechanism for a magnetoelectric (ME) material. A ferromagnet is coupled via exchange/strain to the magnetoelectric material. $\boldsymbol{H}_{EB}$ and $\boldsymbol{H}_{EC}$ are the exchange bias and the exchange coupling from the magnetoelectric material to the ferromagnet, respectively, and $\boldsymbol{m}$ is the magnetization of the ferromagnet. **e**, A classic multiferroic–magnetoelectric material, $BiFeO_3$, is shown with the order parameters: polarization ($\boldsymbol{P}$), antiferromagnetism ($\boldsymbol{L}$) and weak canted magnetization ($\boldsymbol{M}_c$). The electric-field setup in a generic magnetoelectric/ferroelectric material produces exchange bias, coupling and anisotropy modulation for magnetostrictive effects. Yellow and blue spheres depict Bi and Fe atoms in a canonic room-temperature multiferroic $BiFeO_3$. $\hat{\boldsymbol{m}}_{FM}$, $\hat{\boldsymbol{m}}_c$ and $\hat{\boldsymbol{l}}$ represent the unit vectors of magnetization of the coupled layer, the magnetization of the canted spins and the antiferromagnetic axis, respectively. In general, the magneto-electric field generates an exchange coupling along the axial direction of $\hat{\boldsymbol{l}}$, the AFM axial direction and exchange bias, the direction of weak ferromagnetism $\hat{\boldsymbol{m}}_c$.

The spin–orbit mechanism responsible for spin-to-charge conversion at the interface is described by the Hamiltonian

$$H_R = \alpha_R (\boldsymbol{k} \times \hat{\boldsymbol{z}}) \cdot \hat{\boldsymbol{\sigma}} \quad (1)$$

where $\alpha_R = (k_{F+} - k_{F-})\hbar^2/2m$ is the Rashba coefficient ($\hbar$ is the Planck constant), $\boldsymbol{k}_{F+}$ and $\boldsymbol{k}_{F-}$ are the Fermi vectors of the two spin-split bands, $\hat{\boldsymbol{z}}$ is the unit vector normal to the interface, $\hat{\boldsymbol{\sigma}}$ is the vector of the Pauli spin matrices and $\boldsymbol{k}$ is the momentum of the electrons. In a simple model based on two Fermi contours in the Rashba electron gas (Fig. 2c), the density of spin polarization along the y axis, $\delta s_{y\pm}$ (Fig. 2b, c), and the charge current density along the x axis, $j_{cx\pm}$, can be related as[20,23]

$$\delta s_{y\pm} = \pm \frac{m}{2e\hbar k_{F\pm}} j_{cx\pm} \quad (2)$$

which yields the relation between spin density (per unit area) and charge current (per unit width) in a two-dimensional Rashba electron gas:

$$j_{cx} = \frac{e\alpha_R}{\hbar}\langle \delta s \rangle_y = \frac{\alpha_R \tau_s}{\hbar} j_{sy} = \lambda_{IREE} j_{sy} \quad (3)$$

where the relation between spin current and spin polarization is determined by the spin relaxation time τ_s as $j_s = e\delta s/\tau_s$, where e is the electron charge. For a pure helical ground state in topological systems, $\lambda_{IREE} = V_F\tau$, where V_F is the Fermi velocity and τ is the relaxation time for the spin distribution at an out-of-equilibrium interface. This results in the generation of a charge current in the interconnect that is proportional to the spin current (Fig. 2c). The transduction relates the linear charge current density j_{cx} (in units of ampere per metre) and the areal spin current density j_{sy} (spin current flowing along the z direction, comprised of spins oriented along the y direction; in units of ampere per square metre); see Supplementary Information section M and Supplementary Fig. 16.

Magnetoelectricity provides a highly energy-efficient mechanism for logic switching with intrinsic switching energy given by

$$E_{ME} = 2P_s V_c \quad (4)$$

where P_s is the switched polarization and V_c the critical voltage for switching. To the best of our knowledge, magnetoelectric/ferroelectric switching is the most energy-efficient mechanism at room temperature that scales to lateral dimensions of 10 nm and retains a stable collective order parameter. The switching mechanism for magnetoelectric switching of a ferromagnet is shown Fig. 2d, and a canonical room-temperature multiferroic magnetoelectric ($BiFeO_3$) is illustrated in Fig. 2e. In general, magnetoelectric switching can be accomplished by coupling the ferroelectricity/ferroelasticity to antiferromagnetism and/or a weak canted magnetic moment. The intrinsic switching energy for ferroelectric/magnetoelectric switching can approach 1 aJ per bit (about 30 times lower than the switching energy of advanced CMOS devices) by scaling the switched polarization to about 10 $\mu C\,cm^{-2}$ and switching voltages to 100 mV (Please see Supplementary Fig. 24 for low-voltage ferroelectric characterization of SRO/20 nm LBFO/SRO heterostructure). Both of these metrics are within the reach of experimental room-temperature materials (as shown in Table 1).

Miniaturization and scaling laws for MESO logic

We now derive and apply the scaling laws for magnetoelectric and spin–orbit transductions. For spin-to-charge conversion using inverse SOC (ISOC), the efficiency improves with reducing the width of the magnet, a highly desirable scaling feature. In the presence of topological coupling between spin and charge states in a Rashba system, we can write

$$\boldsymbol{I}_c = \frac{1}{w}\lambda'_{ISOC}(\hat{\boldsymbol{\sigma}} \times \boldsymbol{I}_s) \quad (5)$$

where w is the width of the magnet (the minimum feature size for the device), where λ'_{ISOC} is the effective SOC conversion length. The recent discovery of two-dimensional high-SOC systems indicates that the effective λ_{IREE} can be as high as 6 nm in Bi_2Se_3[34,35] and $LaAlO_3$/$SrTiO_3$[25,36,38]. To assess the suitability of spin–orbit logic for progressive

Table 1 | Device and material targets to enable 1–10-aJ-class MESO logic

	Device figure of merit	Nominal target	Material figures of merit	Nominal target (for 1–10 aJ per switch)
SOC materials	Spin-to-charge conversion, I_c/I_s	>50%	λ_{IREE}	>5 nm[25,35,36,38]
	Source resistance	>10 kΩ	Resistivity	>10 mΩ cm (refs [25,26,35,36,38])
Magnetoelectrics	Dimensions	$<10 \times 10 \times 10$ nm^3	Charge/area (for 1–10 aJ target)	0.5–5 μC cm^{-2} (ref. [42])
	Equivalent capacitance/area	<100 fF μm^{-2}	Coercive field	100–500 kV cm^{-1} (refs[27,30])
	Switching voltage	0.1 – 0.3 V	Magnetoelectric coefficient, α_{ME}	10 C^{-1} (refs [27,28])
	Write error rate	$<10^{-12}$	Reliability	$>10^{15}$
Interconnect	Resistance/ length	0.1–5 kΩ μm^{-1}	Resistivity	4–200 μΩ cm at 10 nm width[3]
	Capacitance/ length	10–100 aF μm^{-1}	Interlayer dielectric (dielectric constant)	1–10 (ref. [3])
	Peak currents	10–100 μA per magnet	Electromigration limit	>25 MA cm^{-1} at 10 nm width
Nanomagnet	Size	20 nm × 30 nm		
	Magnetic stability (barrier, Δ/kT)	40	Magnetization, M_s	<500 MA cm^{-1}
	Spin injection	>80%	Spin polarization	>80%

miniaturization (Moore's law), we show that the energy required to switch the device decreases with dimensional scaling of the device. This can be attributed to an improvement in the spin-to-charge conversion efficiency, η_{SOC}, with a reduction in the width W_{FM} of the nanomagnet ($\eta_{SOC} \propto 1/W_{FM}$) and a reduction in the switched charge of the magnetoelectric/ferroelectric node, Q, with areal scaling ($Q \propto W_{FM}^2$) . The energy required to switch a single MESO logic unit is given by

$$\begin{aligned} E_{MESO} &= E_{CME} + E_{IC} + E_{ISOC} + E_{RT} + E_{SG} \\ &= C_{me} V_{me}^2 \left(1 + \alpha \frac{W_{FM}}{\lambda'_{SOC}}\right) \end{aligned} \quad (6)$$

C_{me} is the equivalent capacitance, V_{me} is the switching voltage and α is the conversion factor. (see Supplementary Information sections G–K for detailed analytical and numerical energy calculations of the intrinsic magnetoelectric energy, E_{CME}, interconnect losses, E_{IC}, and losses in the spin-to-charge conversion layer, E_{ISOC}, in the driving electronics, E_{RT}, and in the supply–ground path, E_{SG}). Figure 3a shows the strong, cubic scaling of the MESO energy (E_{MESO}), where the energy is reduced by a factor of 8 for every reduction by a factor of 2 in feature size. The excellent scalability of MESO logic allows the switching energy of the MESO logic to approach 1 aJ per bit. Magnetoelectric switching also allows strong voltage scaling in energy per bit, where progressive voltage reduction enables lowering of the switching energy. Figure 3c shows a combination of scaling in energy/switching via voltage and effective IREE length towards the 0.1–10 aJ range.

Low-voltage (100 mV) charge interconnects for scaling below 10 nm

We now address one of the most demanding aspects of new computing technology: the interconnects that connect the devices at the nanoscale[39,40]. MESO logic can address the interconnect scaling problem, which has emerged as a major limitation when the width of the electrical wires reached <20 nm. Experimental data for highly scaled interconnects show that the resistivity of electrical wires increases according to the Mayadas–Shatzkes scaling law[41]

$$\rho = \rho_0 \left[1 + \frac{3\lambda_{ebulk}}{8t}\left(1 + \frac{p}{2}\right) + \frac{3\lambda_{ebulk}}{2D}\left(\frac{r}{1-r}\right)\right] \quad (7)$$

(where ρ_0 is the bulk resistivity, λ_{ebulk} is the electron mean free path, p is the specularity, r is the reflection parameter from grain boundaries, t is the thickness of the film and D the grain size) as the critical interconnect dimensions approach the electron mean free path. A second scaling issue with electrical interconnects is the high capacitance per unit length. Hence, it is of great interest to demonstrate a logic technology compatible with high-resistivity and high-capacitance interconnects.

MESO logic enables the development of a low-voltage charge interconnect that is amenable to highly scaled integrated circuits that comprise wires of 10–30 nm width. We show that MESO logic can tolerate the use of nanometallic interconnects with high resistivity (>1 mΩ cm; a 20–100-times less stringent requirement for the conductance of small-width interconnect material) and capacitance (>10 fF μm^{-1}; a 100-times less stringent requirement for the capacitance of the interconnects); see Supplementary Information section N. Figure 3b shows the dependence of switching time on the interconnect length at a metal resistivity of 100 μΩ cm and an effective 30 nm × 30 nm cross-sectional area of 900 nm^2. The switching speed of the MESO device scales linearly with interconnect length up to 1,000 nm at a line resistance of 100 Ω μm^{-1} and a capacitance of 100 aF μm^{-1} (see Supplementary Information section N). This would represent a substantial relaxation in the requirements placed on nanometallic interconnects compared to CMOS devices. This is in contrast to spin interconnects, where the signal, and thus the switching speed, degrade as $\exp(-x/L_{sf})$, where L_{sf} is the spin-flip length and x is the direction of transport. Hence, MESO logic alleviates the traditional problem of interconnects used for spin logic and allows continued scaling of metallic and semiconducting wires.

When compared with the leading beyond-CMOS and highly scaled advanced CMOS technologies, the MESO device provides sizeable gains in areal logic density, energy of operation and computational throughput. In Fig. 4a, we compare the energy delay and the logic density (area per function) of MESO logic with leading beyond-CMOS transistor technologies and highly scaled advanced CMOS devices. The majority logic gate, a universal gate that (together with NOT) can implement all Boolean logic functions, is used to build complex spin-logic functions, such as a 32-bit adder or a 32-bit arithmetic logic unit (ALU)[12], with the results shown in Fig. 4b (also see Supplementary Information section F). The proposed MESO logic device enables competitive energy delay performance compared to leading beyond-CMOS devices, while also allowing non-volatility. The MESO logic device enables considerable improvement compared to other spintronic devices owing to magnetoelectric switching. Gains in the delay are due to the use of electrical (rather than spin-based) interconnects and very compact majority-gate circuits (see Fig. 4c). The MESO device also enables energy reduction compared to CMOS logic operating at very low (0.3 V) supply voltages, owing to its ability to switch at even lower supply voltages (0.1 V). The speed of MESO logic units is comparable to that of low-power, low-leakage CMOS devices (0.3 V supply voltage). We note that at a low logic activity factor and intermittent usage, the non-volatility of the MESO device can offer further advantages compared to CMOS devices by eliminating standby power dissipation and enabling instant operation from standby. Figure 4c shows the advantage of the MESO device in terms of areal logic density compared to advanced CMOS technology.

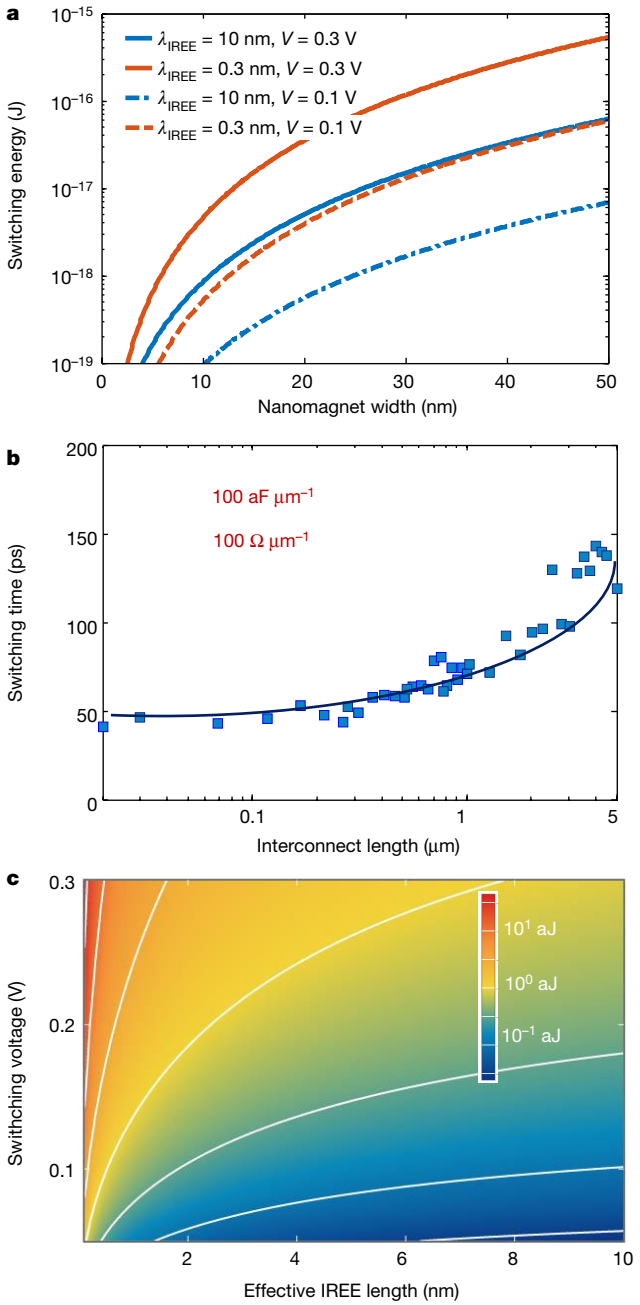

Fig. 3 | Energy and delay of the MESO device. Dimensional scaling of MESO logic shows improvement in switching energy as the devices get smaller. **a**, Cubic scaling with magnet width. **b**, Effect of the length of the interconnect (30 nm × 30 nm cross-section) on the (inverter) device performance, obtained from interconnect modelling of the MESO device. See Supplementary Information for the effects of the capacitance and length on device performance. We simulated the interconnect with 100 Ω μm^{-1} resistance and 100 aF μm^{-1} capacitance per unit length. **c**, Intrinsic switching energy of MESO (colour bar) with improvements in switching voltage and SOC strength (effective IREE length).

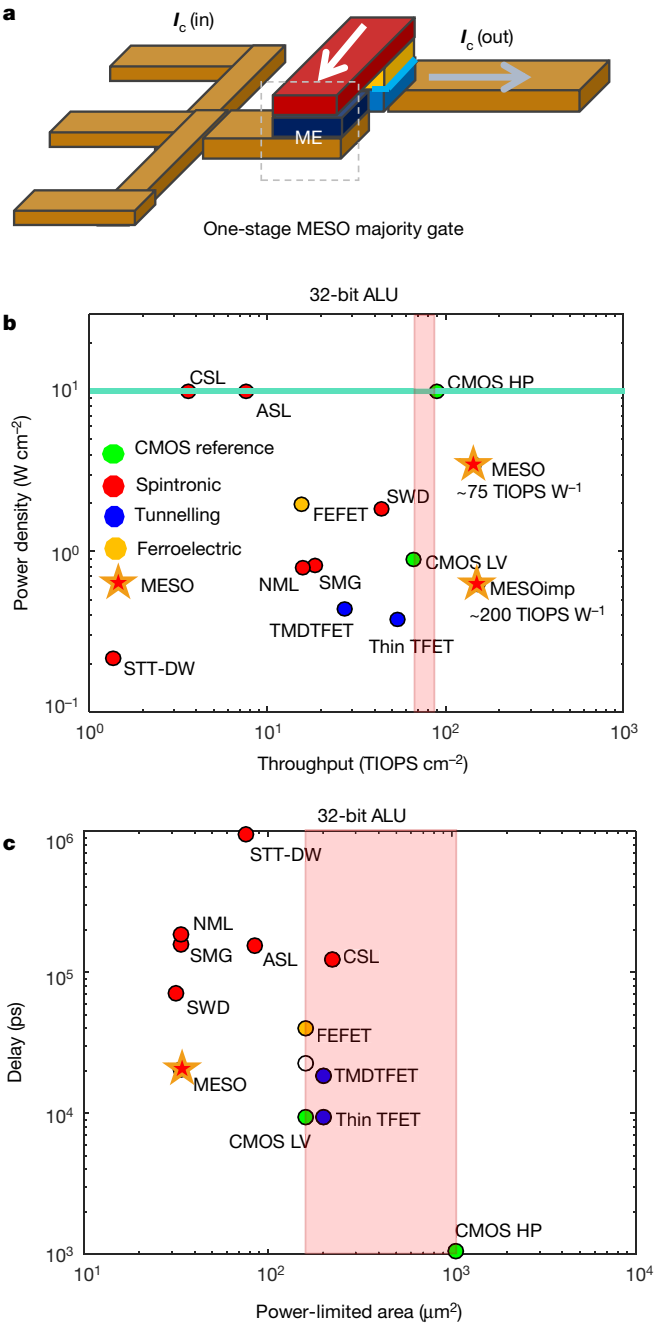

Fig. 4 | Performance and area of MESO device in comparison with advanced CMOS and leading beyond-CMOS devices. a, Scheme of a MESO majority logic gate used for benchmarking. **b**, Power per unit area versus throughput (that is, number of 32-bit ALU operations per unit time and unit area, in units of tera-integer operations per second; TIOPS) for CMOS and beyond-CMOS devices. The constraint of a power density not higher than 10 W cm^{-2} is implemented, when necessary, by inserting an empty area into the optimally laid out circuits. **c**, Delay of 32-bit ALU operation versus the power-limited area for CMOS and beyond-CMOS devices. Power-limited area comprehends the increase in area of the computational logic to meet the power density contraint of 10 W cm^{-2} in **b**. STT-DW, spin-transfer-torque domain-wall device; ASL, all-spin-logic device; CSL, charge spin logic; NML, nanomagnetic logic; SMG, spin majority gate; SWD, spin wave device; CMOS HP, high-performance CMOS at 0.73 V supply; CMOS LV, low-power CMOS operating at 0.3 V supply; FEFET, ferroelectric FET; Thin TFET, 2D-material vertical tunnel FET; TMDTFET, transition-metal dichalcogenide tunnel FET; see Methods.

Experimental progress on magneto–electrics and spin–orbit transduction

We now turn to the initial experimental manifestations of the two central concepts of the MESO device and conclude with a summary of innovations required to meet the MESO target of 100 mV and 1 aJ per bit. First we demonstrate a local-spin-injection device in which spin-polarized charge current I_s is injected from the ferromagnet (CoFe) into a spin–orbit material (Pt) (see Supplementary Information section P for the fabrication method and the device cross-section).

An open-circuit charge voltage V_{oc} that depends on the spin polarization of the injected spin current is measured across the Pt wire. The equivalent spin-to-charge-conversion resistance ($R_{SCC} = V_{oc}/I_s$) is plotted in

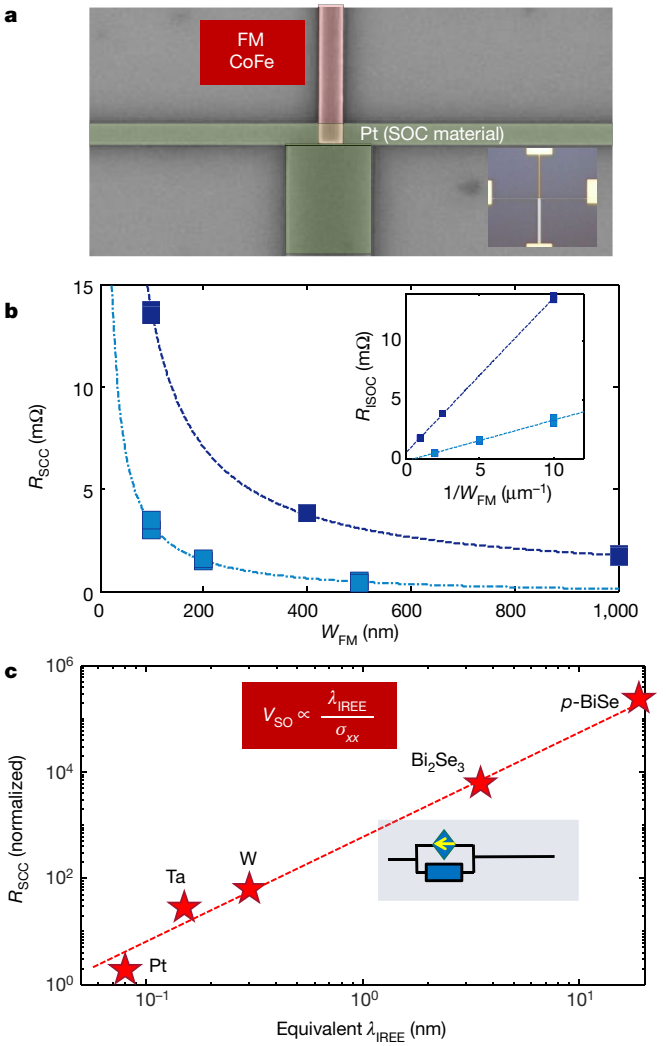

Fig. 5 | Spin–orbit readout for the MESO device. a, A proof-of-concept device for a spin–orbit readout mechanism in which a spin in a polarized charge current is passed into a spin–orbit material (Pt) from a CoFe ferromagnet. The inset shows a microscope image of the device. **b**, Charge readout of the spin state of the ferromagnet, measured using a non-local resistance (lateral voltage divided by vertical current). Shown are measured data from devices with various CoFe width and fixed Pt width of 100 nm (dark blue) and 400 nm (light blue). The inset shows linear fits to $1/W_{FM}$. **c**, Projected improvement in the spin–orbit readout through the use of topological insulators with low conductivity and high spin–orbit effects. V_{so} and σ_{xx} are the generated voltage and conductivity, respectively.

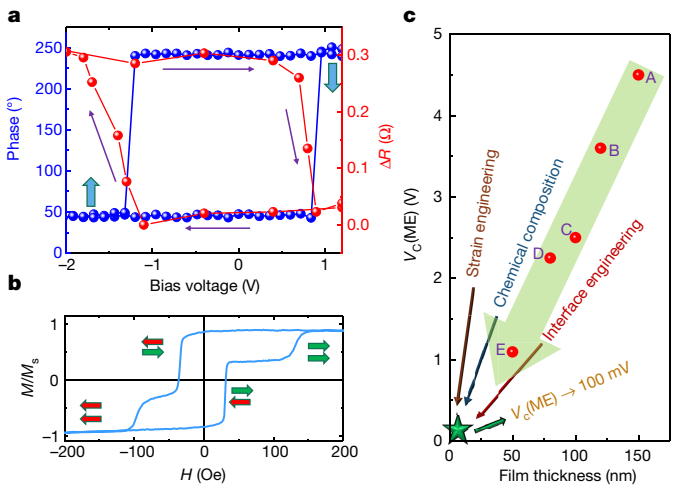

Fig. 6 | Progress of magnetoelectric transduction via MESO towards a voltage of 100 mV. a, Piezoelectric loop (blue) and applied-voltage-dependent resistance modulation (ΔR; red) of a Pt/CoFe/Cu/CoFe/LBFO/LSMO magnetoelectric spin-valve device depict 1 V magnetoelectric switching. The vertical axis shows the phase of the ferro-electric polarization response signal with respect to the input voltage. Purple arrows indicate the sweep direction in the measurement. **b**, Magnetization M_s of a giant magnetoresistive stack, normalized with the magnetization M of a thin film, as a function of magnetic field strength H. The bottom CoFe electrode of the giant magnetoresistive stack is exchange-coupled to $LaBiFeO_3$, showing exchange-induced anisotropy enhancement and exchange bias. **c**, Voltage scaling of magnetoelectric switching as a function of multiferroic film thickness. Data points A–D correspond to $BiFeO_3$ films of varying thickness with a $SrRuO_3$ bottom electrode. The switching voltage of the MESO device V_c(ME) is lowered down to 1.0 V using partial chemical substitution of Bi^{3+} (with La^{3+}), interface engineering (electrodes formed with $La_{0.7}Sr_{0.3}MnO_3$) and thickness scaling down to 40 nm. The ultimate goal of the MESO project is to be able to switch magnetoelectrically at 100 mV.

Fig. 5b. To study the dimensional scaling of the device, we measured R_{SCC} with two sets of test devices. Figure 5b shows measured data from devices with various CoFe widths W_{FM}. Test chip A (dark-blue line with Pt width 100 nm) comprises five different device geometries with dimensions $W_{FM} = 100$ nm, 100 nm, 400 nm, 1,000 nm and 1,000 nm and test chip B (light-blue line with Pt width is 400 nm) has five different device geometries with dimensions $W_{FM} = 100$ nm, 100 nm, 200 nm, 200 nm, 500 nm and 500 nm. We observe a dimensional scaling law, in accordance with the above expression for SOC spin-to-charge conversion; see inset for a linear fit to $1/W_{FM}$. The equivalent spin-to-charge conversion resistance scales favourably for high-resistivity topological materials as $R_{SCC} \propto \lambda_{IREE}/\rho$. For high-resistivity spin–orbit systems (see Table 1) we expect that R_{SCC} can be enhanced considerably. Combined with the areal scaling of the magnetoelectric capacitor, this provides a total device energy scaling of W_{FM}^3.

To illustrate the past year's remarkable progress in magnetoelectric transduction, we present in Fig. 6a–c representative magnetoelectric switching data of a CoFe/Cu/CoFe spin valve that is exchange-coupled to a 45-nm-thick $La_{0.1}Bi_{0.9}FeO_3$ (LBFO) layer using an applied voltage of only 1–2 V—although quasi-static ferroelectric switching has been achieved down to about 150 mV using LBFO as the magnetoelectric layer (see Supplementary Information section Q for details). Figure 6a shows the change in the resistance of the CoFe/Cu/CoFe spin valve as a function of voltage applied across the multiferroic LBFO thin film, along with the piezoelectric loop of the (CoFe/Cu/CoFe)/LBFO/LSMO capacitor structure. It is clear that both ferroelectric and concurrent magnetoelectric switching occur at about 1.0 V. This is enabled by the strong exchange coupling of the bottom CoFe layer of the CoFe/Cu/CoFe spin valve to the canted antiferromagnetic LBFO surface, which is evident from the magnetic hysteresis loop in Fig. 6b. Such an exchange-bias coupling can be reversed by an out-of-plane electric field. Figure 6c shows how rapidly this switching voltage has been decreasing over the past year, primarily through materials engineering of the switching behaviour of the $BiFeO_3$ layer, as well as through systematic thickness reductions. The ferroelectric saturation polarization and the switching voltage of $BiFeO_3$ can be tuned by the doping level of the rare-earth element, such as La or Sm[42]. The potential for further reductions in the switching voltage is illustrated through the quasi-static piezoelectric switching loop of a 20-nm-thick LBFO layer in contact with symmetric $SrRuO_3$ top and bottom electrodes, demonstrating a switching voltage of 130–150 mV (see details in Supplementary Information section Q). Further reductions in the switching voltage, which is the immediate focus of our research, should be possible through reduction of the LBFO film thickness and further careful tuning of the composition such that the polar distortion is delicately tuned to be as low as possible. Independent work by our group and others has shown that both the ferroelectric and antiferromagnetic orders are stable down to at least a few nanometres (see Supplementary Information). A proof of concept for an ultralow-switching-voltage ferroelectric ($La_xBi_{1-x}FeO_3$)

Table 2 | Material options for MESO logic

	Type 1	Type 2	Type 3
SOC materials for spin-to-charge conversion	High-SOC and topological oxides	Topological materials and superlattices	Two-dimensional transition-metal dichalcogenides
	Bi_2O_3[44], $SrIrO_3$[45], $SrTiO_3/LaAlO_3$[25,36,38]	$Bi_{1.5}Sb_{0.5}Te_{1.7}Se_{1.3}$[24], Bi_2Se_3[34,35], α-Sn[46], BiSb[47]	MoS_2[48], MX_2[49]
Magneto-electrics	Multiferroics	Magnetostrictive	Exchange bias
	$BiFeO_3$[27,30], $LaBiFeO_3$[42], $TbMnO_3$[50], $LuFeO_3/LuFe_2O_4$[51]	Fe_3Ga[52], $Tb_xDy_{1-x}Fe_2$[53], FeRh[28]	Cr_2O_3[29,54], Fe_2TeO_6[55]
Interconnect	Noble metals	Metal–semiconductor	Interlayer dielectric
	Cu, Ag, Co, Al, Ru	poly-Si, NiSi, CoSi, NiGe, TiSi	SiO_2, SiN, SiCOH, polymers
Nanomagnet	Nominal ferromagnets	Heusler alloys	
	Co, Fe, Ni, CoFe, NiFe	X_2YZ and XYZ alloys (for example, Co_2FeAl, Mn_3Ga)	

Three classes of materials (high-SOC oxides, topological materials and superlattices, and two-dimensional transition-metal dichalcogenides) are suitable for SOC-based spin-to-charge conversion. Magnetoelectrics belong to three classes: (1) multiferroics with magnetic (antiferromagnetic/ferromagnetic) and electric (ferroelectric) order parameters, (2) magnetostrictive, that is, one ferromagnetic-order-parameter material combined with a strain/piezoelectric material, and (3) exchange-bias materials, that is, one magnetic-order parameter with no ferroelectric/antiferroelectric order. Magnetostrictive materials are not directly suitable (because only 90° switching is feasible), but can be used to enhance magnetoelectric switching. Interconnect options comprise noble metals, metal–semiconductors (which exhibit excellent gap fill for interconnect processing and have short electron mean free paths) and interlayer dielectrics chosen for their low dielectric constant. Nanomagnets should be conductive to allow spin injection with the applied bias. Co-, Fe- and Ni-based ferromagnets or Heusler alloys are potential candidates, with low M_s and high spin polarization.

was obtained using symmetric conductive-oxide electrodes ($SrRuO_3$), from which the switching energy was estimated to be about1 aJ per bit for a contact area of 10 nm × 10 nm.

Material requirements for 1–10-aJ-class MESO logic

We describe the material scaling requirements for 1–10-aJ-class MESO logic scalable to critical dimensions of <10 nm or device density beyond 10^{10} cm^{-2}. In Table 1 we summarize the material scaling requirements for four classes of materials: a) SOC materials for spin-to-charge conversion, (2) magnetoelectrics for charge-to-spin conversion, (3) interconnects scalable to nanoscale widths and (4) nanomagnets. We considered the experimental values shown for the inverse Rashba–Edelstein parameters. A large-signal magnetoelectric coefficient of $10c^{-1}$ (c, speed of light) from magnetoelectric switching and low coercive voltages were obtained via rhombohedral distortion tuning and chemical substitution of multiferroics[42] with thickness scalability to 5–20 nm. The output resistance of the ISOC spin current source is a critical parameter that affects the driving ability of the MESO logic device (high source resistance is preferred for a current source; see Supplementary Information section H and Supplementary Fig. 9.) The requirement of low interconnect resistivity is considerably relaxed owing to the low-voltage, low-current operation of charge-mediated magnetoelectric logic. This is reflected in the resistivity target of 4–200 μΩ cm, which is comparable to the resistivity of scaled metal wires. Electromigration of the metal interconnect imposes a challenging limit on the switching speed by limiting the peak current in wires. MESO logic relaxes the electromigration requirements to 25 MA cm^{-2}, appreciably below the Belch limit for electromigration of interconnect metal candidates[43].

A focused effort using quantum materials can enable logic technology operating at 100 mV and 1 aJ per bit. The details of four fundamental material classes are presented in Table 2. SOC materials can be comprised of (1) high-SOC oxides (for example, W(O) and Bi_2O_3[44]) and oxides with strong topological effects ($SrIrO_3$[45] and $SrTiO_3/LaAlO_3$[25,36,38]), (2) topological materials ($Bi_{1.5}Sb_{0.5}Te_{1.7}Se_{1.3}$[24], Sn-$Bi_2Te_2Se$, Bi_2Se_3[34,35], α-Sn[46], BiSb[47]) and their superlattices and (3) transition-metal dichalcogenides with large spin–orbit effects (MoS_2[48], MX_2[49]). The magnetoelectric materials can be comprised of (1) multiferroics with coupling of the antiferromagnetic and ferroelectric orders (type -1 multiferroics $BiFeO_3$[27,30] and $LaBiFeO_3$[42]; type-2 multiferroics, such as $TbMnO_3$[50]; and improper multiferroics, such as $LuFeO_3/LuFe_2O_4$[51]), (2) magnetostrictive materials (Fe_3Ga[52], $Tb_xDy_{1-x}Fe_2$[53], FeRh[18]) and (3) electrically tuned exchange-mediated magnetoelectrics (Cr_2O_3[29,54] or Fe_2TeO_6[55]). The interconnect options scalable to dimensions smaller than the 10 nm critical width can be based on transition metals (Cu, Ag, Co, Al, Ru) or their semiconductor alloys (poly-Si, NiSi, CoSi, NiGe, TiSi), combined with low-interconnect-capacitance materials (SiO_2, SiN, SiCOH, polymers). The nanomagnetic materials can be ferromagnets/ferrimagnets (Co, Fe, Ni, CoFe, NiFe, and X_2YZ and XYZ alloys, such as Co_2FeAl, Mn_3Ga), in which a wide range of saturation magnetization and magnetic anisotropy are feasible to meet the dimensionality and retention requirements. In each of these four classes of materials, considerable development is required to improve the material interfaces for integrated devices, the operating temperature range, the processing temperature compatibility and, most importantly, the performance metrics.

Conclusion

In conclusion, we propose a scalable beyond-CMOS spintronic logic device with non-volatility and an energy-efficient charge-based interconnect. The proposed device allows (a) continued scaling in energy per operation towards attojoule-level switching energy (about 30 times below that of advanced CMOS devices) at 100 mV (more than 5 times below the operating voltage of advanced CMOS devices), (2) substantial improvement in logic density (about 5 times compared to advanced CMOS devices), enabled by majority-gate circuits implemented with a collective switching device, (3) improved scalability for interconnects due to the small impact of the resistivity, which is up to 1 mΩ cm, and (4) a path to seamless monolithic integration with CMOS technology (see Supplementary Fig. 19). The development of a beyond-CMOS device with an advantageous scaling method using quantum materials, highly compact majority logic[14] and non-volatile logic[15] can open up a potentially new technology paradigm for improving energy efficiency in beyond-CMOS computing devices. Combined with non-volatility and ultra-low energy, MESO logic may enable entirely new computer architectures that may avoid the trade-offs of the Turing and von Neumann architectures and of Amdahl's law. A combination of quantum materials, novel integration and new logic architectures may thus enable computing beyond advanced CMOS technology.

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METHODS

Uniform benchmarking to beyond-CMOS logic options. We adopted the uniform, beyond-CMOS benchmarking method[12] to compare beyond-CMOS options. This method describes the impact of material improvements, device parameters, circuit topology and interconnects on the performance of computing devices. The model is adopted in beyond-CMOS research and includes the following spin-logic devices: (1) spin-torque devices[32,56–58] (spin-transfer-torque domain-wall device, all-spin-logic device, charge spin logic, spin-torque oscillator logic), (2) dipole-field devices (nanomagnetic logic)[59], and (3) magnetoelectric devices (MESO, spin majority gate, spin-wave device[60]). We evaluated several digital logic circuits[12] (a fanout-4 inverter, a two-input NAND adder, a 32-bit ripple-carry adder and a 32-bit ALU) to compare the MESO logic with leading beyond-CMOS logic options. We also considered tunnelling field-effect transistors[61,62], ferroelectric and piezoelectric integration in transistors[63,64] and Mott transistors[65]. See Supplementary Information section F, for a detailed explanation of the benchmarking.

Vector spin circuit modelling of MESO logic. We verify the functionality of MESO spin logic using an equivalent spin circuit model that describes the magnetization dynamics of the nanomagnet, vector spin injection, spin-to-charge transduction and magnetoelectric switching. The equivalent circuit model is based on vector spin circuit theory (magnetoelectric circuit analysis); see Supplementary Information section B.

The intrinsic resistance of the ISOC current source is derived from the conductivity of the interconnect and the ISOC conversion layers. The nanomagnet is connected to a control transistor operating as a power supply and shared among several MESO devices. We have also included the resistance and capacitance parasitics of the ground contact. The conductance across the magnet to the spin injection layer is modelled as a 4×4 matrix that relates the four-component charge and spin voltages to the injected four-component charge and spin currents[31,32,66]. The current injected at the nanomagnet–ferromagnet interface is given by

$$\begin{bmatrix} I_c \\ I_{sx} \\ I_{sy} \\ I_{sz} \end{bmatrix} = R^{-1}(\hat{\boldsymbol{m}}) \begin{bmatrix} G_{11} & \alpha G_{11} & 0 & 0 \\ \alpha G_{11} & G_{11} & 0 & 0 \\ 0 & 0 & G_{SL} & G_{FL} \\ 0 & 0 & -G_{FL} & G_{SL} \end{bmatrix} R(\hat{\boldsymbol{m}}) \begin{bmatrix} V_N - V_F \\ V_{sx} \\ V_{sy} \\ V_{sz} \end{bmatrix} \quad (3)$$

where R is the rotation matrix that accounts for the magnetization direction of the nanomagnet, and I_{si} and V_{si}, $i = \{x, y, z\}$, are the components of the spin current and voltage, respectively. G_{SL}, G_{FL}, G_{11}, V_N and V_F are the conductance elements for the Slonczewski torque, field-like torque, conductance, voltage at the normal metal and voltage at the ferromagnet, correspondingly. See Supplementary Information sections B and C for a detailed explanation of the model.

Stochastic behaviour of magnetoelectric switching versus spin-torque switching. We modelled the magnetization dynamics of the nanomagnet using the Landau–Lifshitz–Gilbert equation[50] and the Fokker–Planck equation[67,68]. The modified Landau–Lifshitz–Gilbert equation, a phenomenological equation that describes the dynamics of a nanomagnet with magnetic moment unit vector $\hat{\boldsymbol{m}}$, was used for Monte Carlo simulations (see Supplementary Table 1 for parameters). We used the Fokker–Planck equation for uniaxial anisotropy parameterized with the angle of the magnetization, which was validated versus the Monte Carlo simulations of the nanomagnets. See Supplementary Information sections C and O for a detailed explanation of the stochastic modelling.

Complete logic family and state elements. The proposed device family is readily extended to a general-purpose computing state machine. A state machine and complete Boolean logic family are the prerequisites for a Turing machine[69]. Majority logic operation can be readily demonstrated because the input of a capacitive node is added to the charge currents converging at the node via the Kirchhoff law. Spin-logic devices with multiple switching inputs (domain-wall, spin-wave or spin-current) have been shown to facilitate the development of majority logic[70] and spin state machines[71]. Combined with a random access memory (RAM), a state machine enables general-purpose computing.

CMOS compatibility, memory and control logic. The proposed magnetoelectric-logic scalable spintronic logic device has several desirable features that are compatible with CMOS nanoelectronics. First, the MESO device can be integrated in the backend of the CMOS process (that is, between the interconnect layers), allowing CMOS devices to be used for clocking, control and power supply (Supplementary Fig. 19). Second, MESO devices can serve as elements of an embedded memory with 'logic-compatible speed' (known as large-signal memory, commonly implemented with a static RAM), making them usable as on-chip non-volatile memories. Third, the MESO device allows stacking of several layers of magnetic logic in a three-dimensional architecture. Fourth, because the state variable of the interconnect between MESO gates is the charge, MESO logic can be readily interfaced with CMOS circuitry to implement clocking control and power delivery. Owing to its low supply voltage, the MESO device is efficient even with interconnects with high metal resistivity of $>100\ \mu\Omega\ \mathrm{cm}$[72,73].

Code availability. The MATLAB codes used to benchmark the circuit performance are available under 'Benchmarking of devices' from the Nanoelectronics Research Initiative, at https://nanohub.org/tools/nribench/browser/trunk/src.

Data availability

The data that support the findings of this study are available from the corresponding author on reasonable request.

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