**Midterm Exam -- (Take Home 30%) Due: Nov. 21**

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1. Describe three synchronization methods of CPU with I/O devices.

* Programmed I/O method; CPU waits for I/O device. Lots of CPU time is wasted, because the CPU has to wait for the I/O Device
* Interrupt driven I/O method; I/O device informs the CPU of it’s status by using an interrupt.
* Direct Memory Access; CPU sends I/O requests to the Direct Memory Access controller, which is managing the entire transaction

1. What is the difference between CISC and RISC architecture?

CISC stands for Complex Instruction Set Computer. It’s a CPU design based on single commands, which are good at executing multi-step operations.

They generally have small programs. Due to the high amount of compound instructions, it takes long to perform. It is considered less efficient than RISC.

RISC stands for Reduced Instruction Set Computer. It’s a CPU design based on simple orders and acts fast.

They usually have a small set of instructions. The instructions are expected to be very simple. Due to the simplicity of the instructions, the CPU is inexpensive to make,

RISC CISC

Focus on software Focus on hardware

More registers Less registers

Code size is large Code size is small

Instructions in single clock cycle Instructions take multiple cycles

No trouble pipelining Trouble with pipelining

1. What is the difference between a *von Neumann* architecture and a *Harvard* architecture?

von Neumann is associated with using a single path to access a main memory that holds both instruction and data. Harvard is associated with having separate memories and access paths for instruction and data, allowing transfers to be performed at the same time.