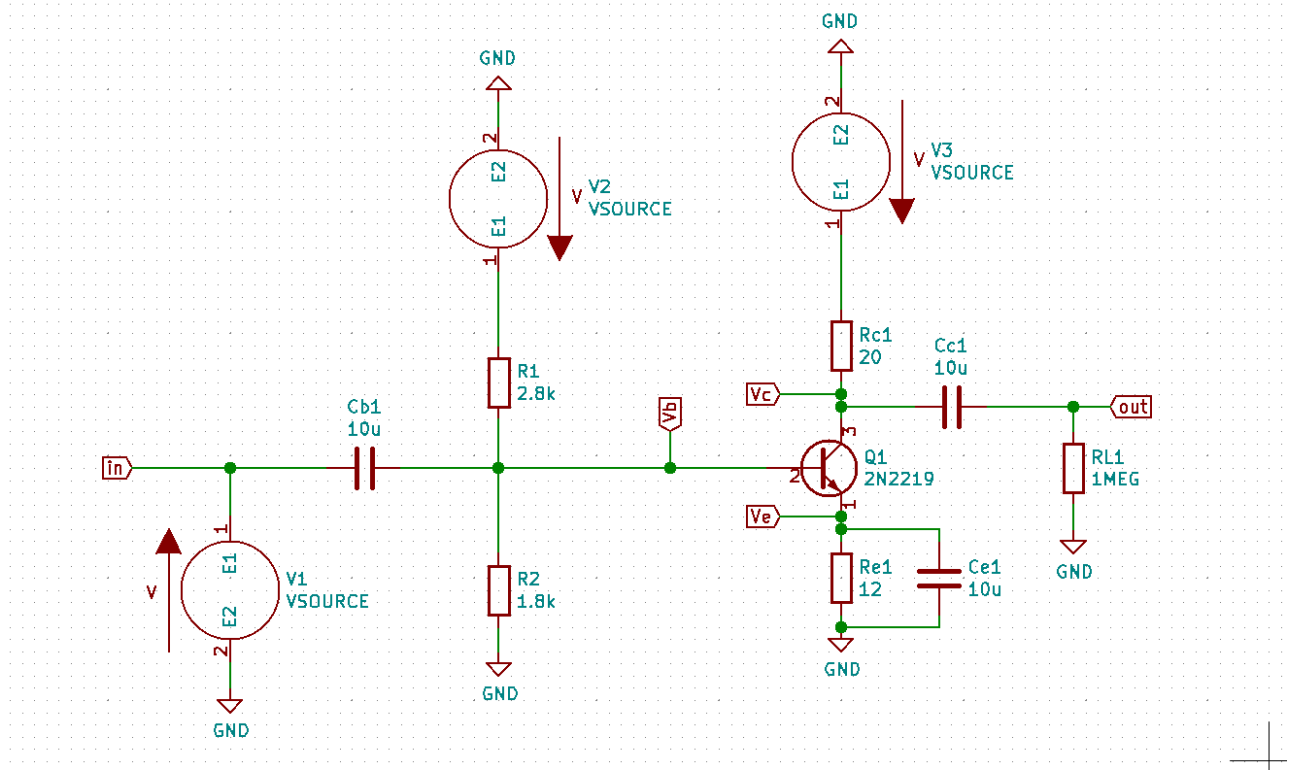
Simple amplifier using the open source software Kicad

I have been asked in a 1st approach for the project to design a simple class A amplifier.
A class A amplifier is bascically a common emitter. Here is the schematic below :



A few words about this schematic : Cb1 and Cc1 are coupling capacitors, used to make a connection between the AC and the DC, but with no perturbation from one on the other.

Ce1 is a bypass capacitor. As our goal is to design an amplifier in high frequencies, this cap will short circuit the emitter resistance in this frequencies to keep a large voltage gain.

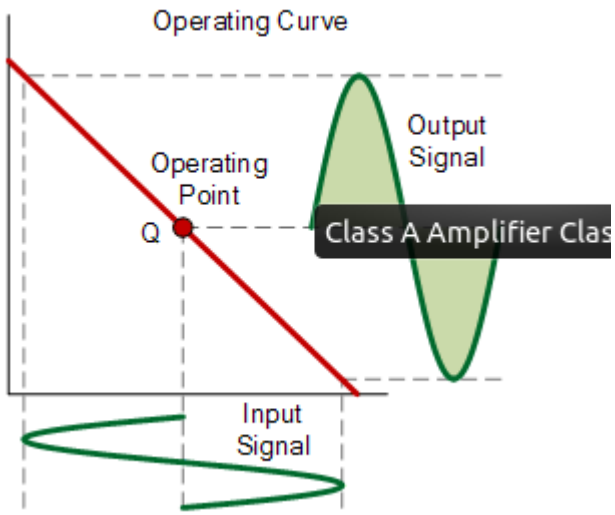
This emitter resistance is here to counter any changes into the collector current that could occur.

The volage divider at the input is here to apply a stable bias voltage on the base (e.g does not depend on the current gain Beta, which can varies a lot because of the temperature).

V2 and V3 are two constant voltage sources set up at 10V. V1 reprensents the input signal (for example the output of the AD9364) which is a 100mV sinusoid at 3MHz.
RL1 is the load. A very high load resistance is the same as if nothing were connected at all at the output.

In a class A amplifier, a single transistor is processing the input signal (in class B, there is 2).
It takes this signal, increase or decrease its magnitude and apply a minus sign (e.g phase shifting of 180°). In order to properly output this signal, the transistor has to be biased in a way that it is linear. And for this, a common rule is to set the voltage between the collector and the emitter at Vcc/2. If it is not properly biased, the output signal will be distorted compared to the input signal.
In a transistor, there is 3 region : the saturation, cutoff and the active region. The latter is the one which interests us, as it is corresponds to a linear region.

Should the transistor has been properly biased, the input signal will be held into this linear region, resulting as non distortion on the output signal. Vcc/2 matches the middle voltage value of this region. A screenshot to illustrate it :



The DC analysis (or operating point analysis)

This analysis will allow us to see if the transistor is properly biased.
A good tool to use is called « ngspice » and works great with Kicad.
To make the DC analysis, go to your schematic file, then « Tools », « Spice » tab and « generate Netlist ». A .cir file should apppear in the project's folder. Open it with a text editor and add « .OP » line before the « .end ». It is to achieve a dc analysis. Then open a terminal and go to your project's folder. Type « ngspice filename.cir », then when ngspice is on, type « run ».It will then perform the DC analysis.

So, with the circuit showed earlier, here the result I get :

Concerning the Vbe voltage, we know it must be somewhere around 0.7/0.8V :

```
ngspice 1 -> print v(Vb) - v(Ve)
v(vb) - v(ve) = 8.679160e-01
```

Concerning Vce voltage, we know it must be equal to Vcc/2 (here Vcc = 10V) :

```
ngspice 1 -> print v(Vc) - v(Ve)
v(vc) - v(ve) = 4.937329e+00
```

We can also check the bias voltage of the transistor, which corresponds to Vb :

```
ngspice 1 -> print v(Vb)
v(vb) = 2.774213e+00
```

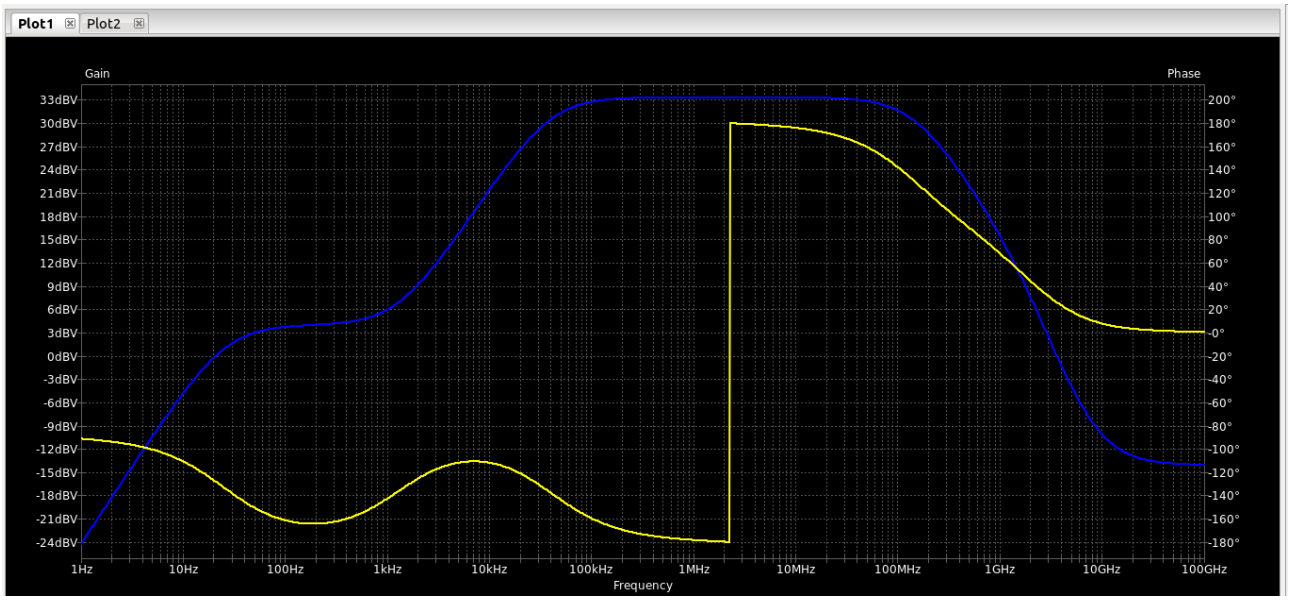
We can also check if collector current and emitter current are merely equal :
20 is the value of the collector resistor and 12 the emittor resistor

```
gspice 1 -> print (v(V3) - v(VC)) / 20
(v(v3) - v(vc)) / 20 = 1.578187e-01
gspice 1 -> print (v(Ve) / 12)
(v(ve) / 12) = 1.588581e-01
```

We can see they are both equal to approximately 158 mA. Because base current is much smaller than collector current. And if it is low enough, collector current and emitter current are virtually equal.

The frequency response

Kicad allows us to make the simulation of such an amplifier.
Here is a plot of the frequency response :

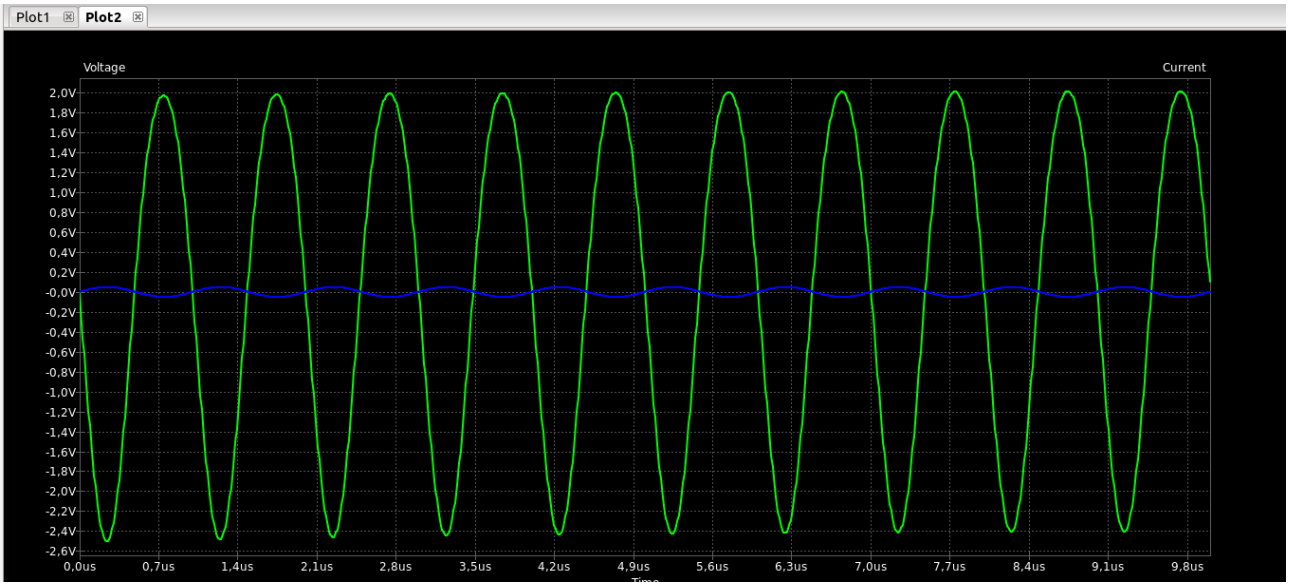


In blue it is the magnitude and in yellow the phase. This bode diagram looks like a bandpass filter.Let's focus on the magnitude curve.
On the contrary of a bandpass filter , the two cutoff frequencies are not wanted. They come from capacitances.
In low frequencies, they are caused by the 3 coupling capacitors. However, only 1 is really responsible for this cutoff frequency, and it is the emitter bypass capacitor. If its capacitance value is high, the bandwith will be stretched and a small value will narrow the bandwith.

The high frequency cutoff is provoked by the internals caps of the BJT and nothing can be done about it. We can only look in the datasheet and search for the « Transition frequency » to see at which frequency the current gain is equal to 1. (a.k.a GBW).
The most important thing to know from this diagram is that the maximum gain (33.3 dB) will be obtained from 100 kHz to 40 MHz. So our input signal must be a sinusoid which has a frequency between these 2 boundaries.Obviously, this transistor is therefore not good for our main project.

The transient response

This response plots the voltage/current against the time.



The blue sinusoid corresponds to the input and the green one to the ouput.
The input is a 100 mV peak to peak voltage.
So for a gain of 33.3 dB, we should have a voltage ouput peak to peak of 0.100*(10^(33.3/20)) = 4.62V.
On the simulation output, we can read : 2V + 2.41V = 4.41V.
I mentionned earlier that this amplifier is a « common emitter » transistor. It is one of the 3 fundamentals configuration of a transistor.
This one is used to make an « inverting amplifier ». The 2 main caracteristics of this amplifier is to increase/decrease the voltage's amplitude and to apply a phase shifting of 180°.
This beheviour can be seen on the screenshot. When there is a peak for the input, the ouput have a hollow, and vice versa.

If I increase the input voltage, the output voltage saturates and eventually starts oscillating (on the peak of the output sinusoid, an oscillation can be observed) . I finally found what is wrong. I have plotted the voltage between collector and ground (before the cap) and in fact the voltage has reached the supply voltage for the positive peak voltage. This is why it saturates.

The footprint

Now that the simulation is done, we can make the PCB.
For it, we need the footprint. I created a very simple footprint for the transistor, just need to be careful with the pad dimensions.

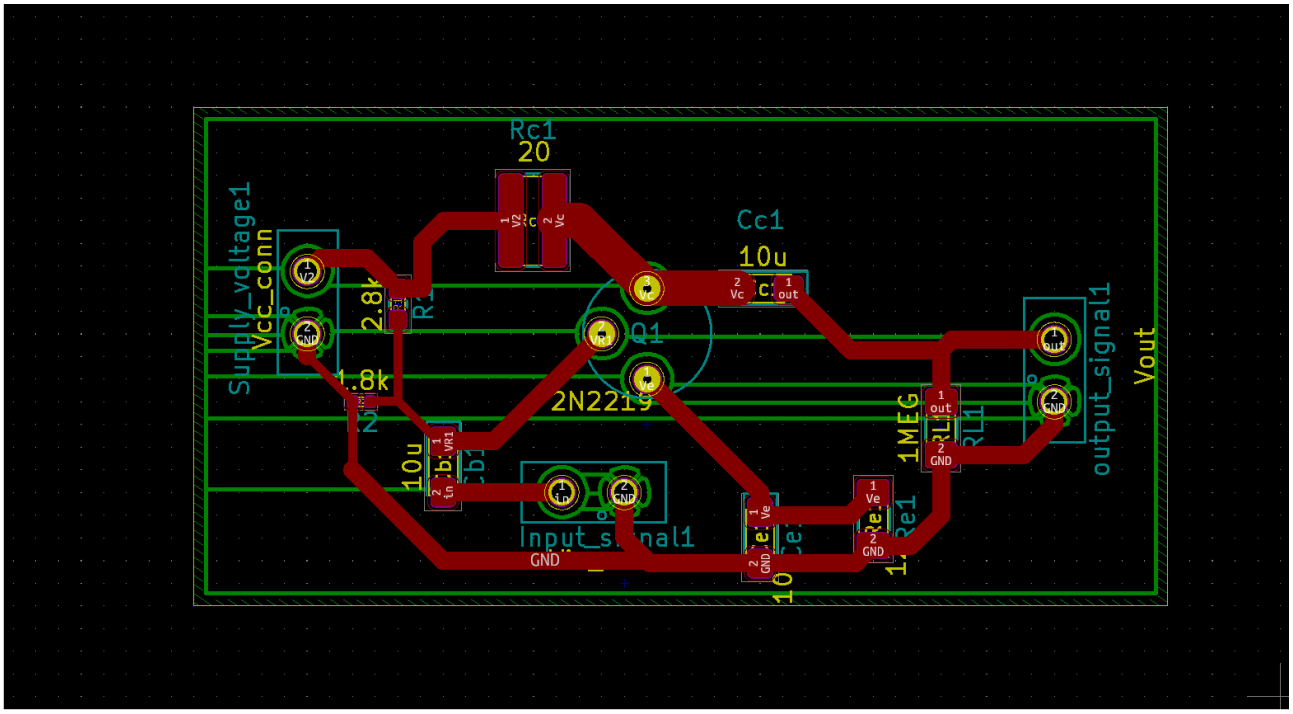
While desiging the circuit's footprint, care must be taken when choosing the right component's footprint : pay attention to the box's dimension. Which kind of box is used for the choosen component ? For example , the 2.74 kOhms (used in our voltage divider) that I saw (CRCW06032K74FKEA) uses a 1608 box using metric units (mm). This box is already made in kicad, so it is good !

For the R2 resistor, we want a 1.78 kOhms, in the datasheet we can see that many packages can be used, depending on the caracteristics we are seeking.

As the current flowing into the base is very low, we can take a resistor regardless of its maximum power dissipation.
However, when choosing collector resistor, we have to be careful. Using ngspice, we can know the current flowing into Rc : (V3 – Vc) / Rc => 157 mA (we call it Ic)
So the power is this current multiplied by the voltage accross Rc : Ic * (V3 – Vc) => 0.5W
So we have to take a resistor with a power dissipation higher than the usual 1/4 W.
For the emitter resistor, let's do the same thing : Ie = 157 mA (same as Ic)
ngspice says that Ve = 1.90V, so P = 0.3 W
The usual 1/4 W would not be good as well.

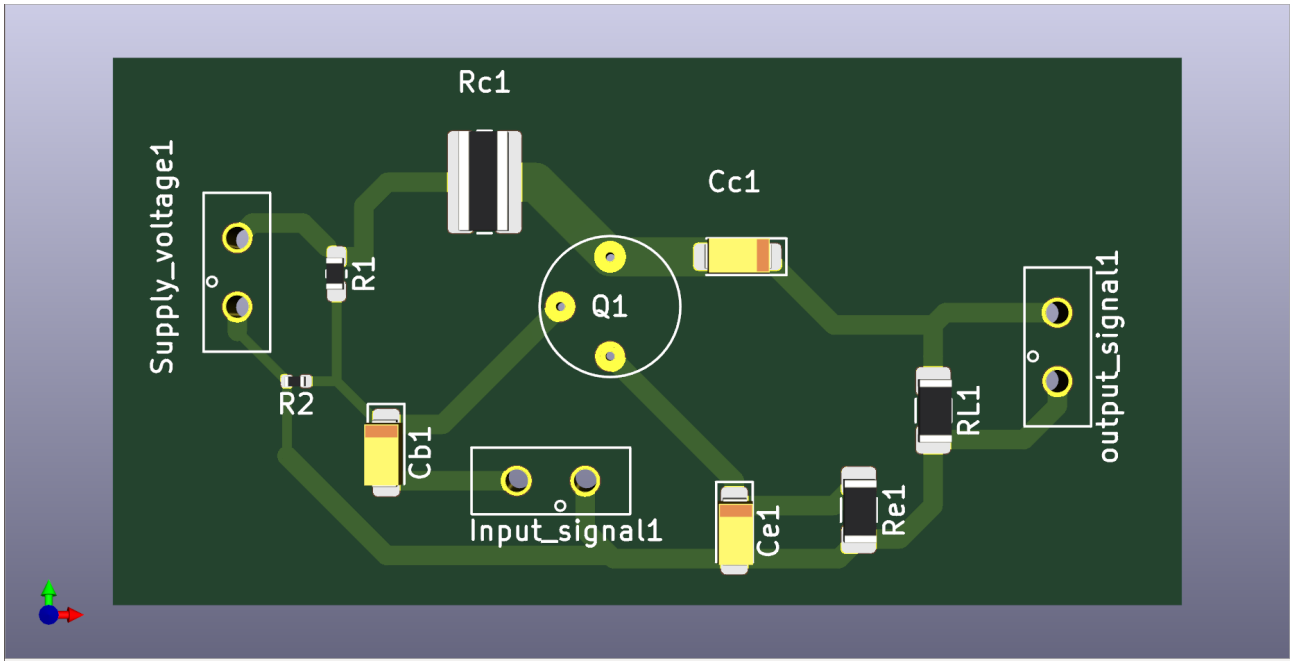
Now let's look at the capacitors. All 3 have the same value, so I will be using the exact same one capacitor for the 3 footprints.

Here is the screenshot of the footprint :

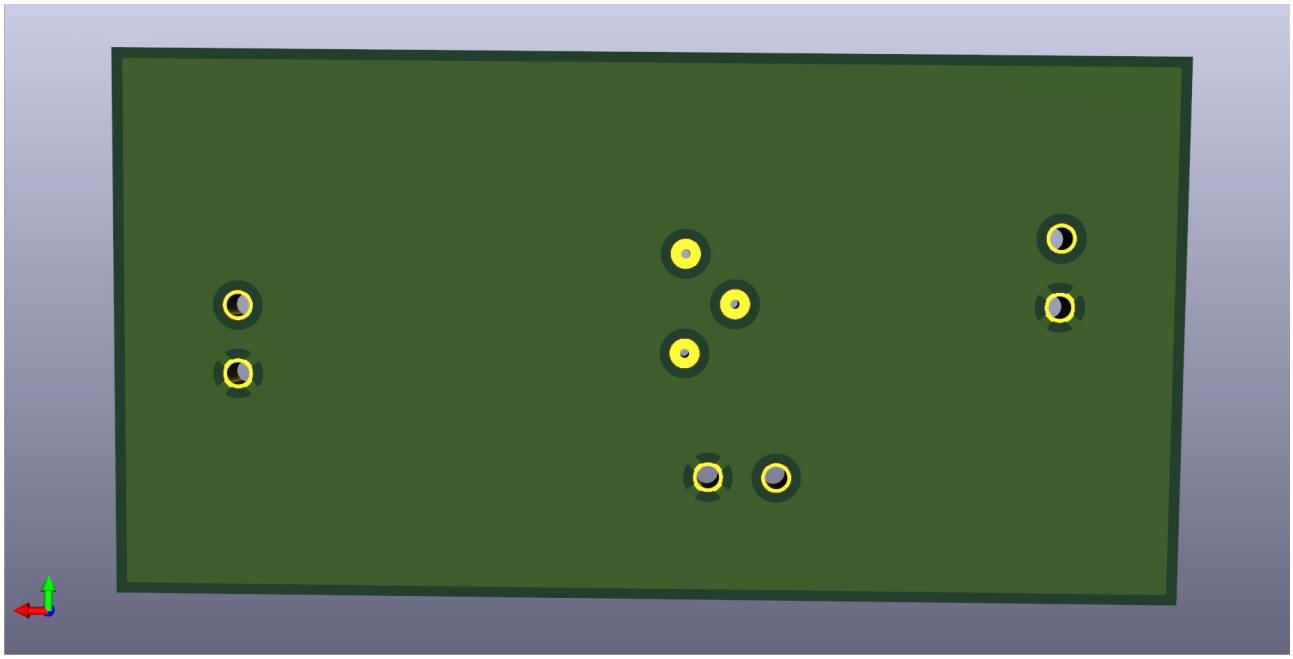


The red and the green colors are representing 2 differents layers of the PCB. One is used to make the connection between the component's pads, and the other is used to make the ground connection. The ground (green layer) is covering the whole rear of the PCB.

And here 2 screenshots of what would looks like the manufactured PCB :

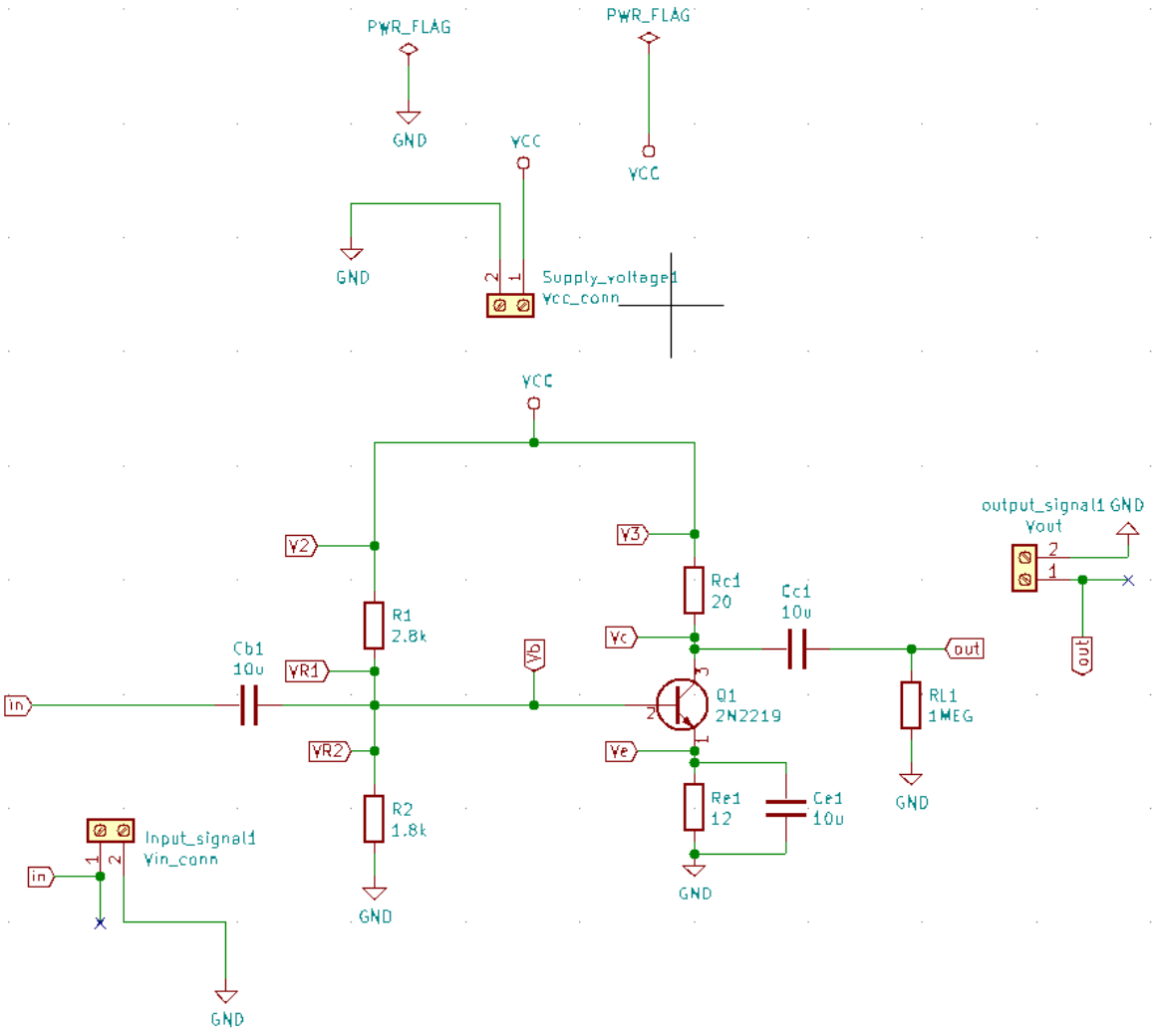


And a screenshot which reprensents the rear of the PCB to illustrate the ground connection :



Of course, the power 2 terminal will have to be solder on the BOTTOM layer !

And a last sreenshot to show the modified electric shematic in order to create the PCB :



All the voltages sources has been removed as they were useful only for a simulation purpose. To create the PCB, we won't solder voltages sources to the PCB, but use external ones instead. This is why some screw terminals just appeared on the schematic.
A « PWR_FLAG » appeared as well, and is connected to VCC as well as ground. Now kicad knows that « VCC » is a supply voltage.

Everything presented above has been done with Kicad.
However, I used as well LTSpice (with wine) to double check my simulation results. And in the end it was a good idea, as at first I had strange results with kicad.
For example, the transistor's SPICE model (the kind of file which describes a component's behaviour) I found on internet inversed 2 of the transistor's pads. Fortunately, it is very easy in Kicad to change the pad's order of a transistor.

What is also great about Kicad, is that it provides as well a « PCB calculator » which will be useful in high frequencies for impedance matching and biasing. Indeed, in high frequencies I won't use resistors but inductors, and the latter can be designed with a portion of a track (called transmission line) . This calculator will allow me to quickly determine the right width and length for an RF inductor.