School of Electrical Engineering
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ELEC3251
Assignment 1

Practical and Theoretical Analysis of Buck Converter and Flyback Converter

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1 Buck Converter

1.1 Ideal Calculations

The duty cycle required to achieve an output voltage of $V_o = 5$ V for an input supply voltage of $V_d = 12$ V can be determined using the DC transfer function of the Buck converter, see Equation 1. The resulting duty cycle required for the ideal circuit is $D \approx 41.67\%$.

$$\frac{V_o}{V_d} = D \tag{1}$$

The output voltage ripple (ΔV_o) of an ideal Buck converter is given by Equation 2. This equation can be rearranged, see Equation 3, to find the required capacitance for the low pass filter, provided that the duty cycle (D), filter inductance (L), and switching period (T_s) are known. For $T_s = 1/f_s = 10$ μs, $L = 1$ mH, $D = 41.67\%$, $\Delta V_o = 25$ mV, and $V_o = 5$ V, the required capacitance is $C = 1.458$ μF.

$$\frac{\Delta V_o}{V_o} = \frac{1}{8}\frac{T_s^2(1-D)}{LC} \tag{2}$$

$$C = \frac{V_o}{\Delta V_o}\frac{T_s^2(1-D)}{8L} \tag{3}$$

The output power of the converter will be limited by the ratings of the components in the circuit. As the output voltage of the converter is required to remain constant at 5 V, only the output current can be adjusted to suit the ratings of the components. The inductor selected for the circuit is the Murata #1410516C, which has a maximum DC current of 1.6 A [**?**]. A IRFZ24NPbF MOSFET has been selected for the switch, this component has a maximum DC current rating of 17 A [**?**]. The selected diode is an SB120 which has a maximum DC current of 1.0 A [**?**]. The inductor current will equal the output current, assuming the voltage across the capacitor remains constant. Therefore, the output current must be less than 1.6 A, to avoid causing damage to the inductor. The diode will only conduct when the switch is off, therefore the DC current flowing through the diode is $I_D = (1-D)I_o$. For $I_o = 1.6$ A the diode current is 0.93 A, which is less than the maximum rating of the device. Therefore, the load resistance must be selected such that $I_o \leq 1.6$ A. Using Ohm's law this inequality is equivalent to $R_{Load} \geq 3.125$ Ω. The smallest resistor provided in the laboratory kit is 3.9 Ω so this resistance will be used for the load.

The continuous conduction mode (CCM) and discontinuous conduction mode (DCM) boundary occurs when the current flowing through the inductor reaches 0 A. For the ideal Buck converter this will occur for a DC output current (I_{oB}) which can be found using Equation 4. For the designed converter the minimum DC output current is $I_{oB} = 14.6$ mA, which is equivalent to an output load of 342 Ω.

$$I_{oB} \approx \frac{T_s V_o}{2L}(1-D) \tag{4}$$

1.2 Ideal Simulations

Wolfram System Modeller (Wolfram) was used to simulate the performance of the designed converter. The model used for the simulations is shown in Figure **??**. The output voltage of the ideal Buck converter is shown in Figure **??**. The average output voltage, at steady state, is close to 5 V which lies close to the theoretically expected value of 5 V. The slight discrepancy between the simulated value and the expected value may be the result of truncating the duty cycle to 2 decimal places ($5/12 \approx 0.4167$). It may also be a result of the numerical methods used by the Wolfram software to simulate the system. An output voltage ripple of 6.7 mV is observed from the simulations and is shown in Figure **??**.

Figure 1 (A) displays the inductor current for a load resistance of 342 Ω. The current reaches a minimum value of 120 μA, which indicates that the converter is close to the CCM-DCM boundary. Figure 1 (b) displays the current for a load resistance of 345 Ω. Slight distortion is observed in the waveform near the zero crossing which indicates that the converter has entered DCM. This suggests that the CCM-DCM boundary lies in the range $342 \leq R_{Load} \leq 345$ Ω which agrees with the theoretically expected value of 342 Ω. The boundary may not lie exactly at 342 Ω because of the assumption, made in Equation 4, that the inductor current and the output current are equal. This assumption is not correct as a small amount of current also flows through the capacitor.

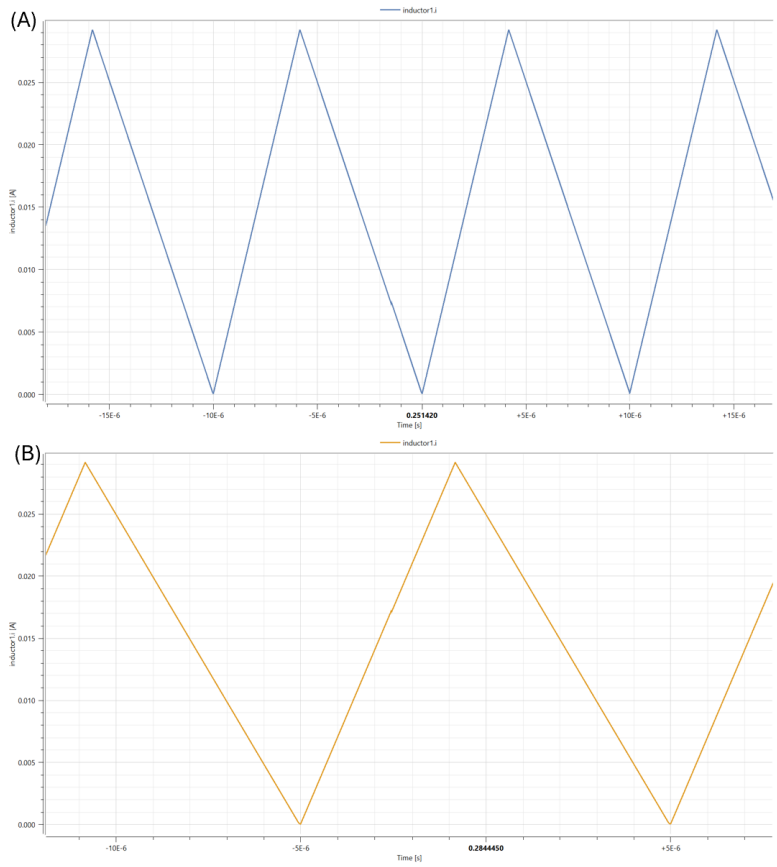

Figure 1: Buck converter inductor current for a load resistance of (A) 342 Ω, and (B) 345 Ω. A small amount of distortion is present in (B) which indicates that the CCM-DCM boundary lies in the range $342 \leq R_{Load} \leq 345\ \Omega$.

1.3 Non Ideal Calculations

The previous calculations and simulations neglect many real-world effects that will affect the circuit's performance. Previously, no voltage losses were assumed to occur across the switch. This assumption is invalid as real switches are often implemented using transistors that have finite on resistances. Furthermore, it was assumed that no voltage drop occurs across the diode. All diodes have a non-zero voltage drop, which is required to overcome the potential barrier formed at the P-N junction of these devices. In addition, the windings of an inductor are not perfect conductors and hence have resistance. These effects will result in the output voltage of the converter being lower than the theoretically expected value. Figure **??** displays equivalent circuit models which can be used to account for these effects when (A) the switch is on and (B) when the switch is off. Applying Kirchoff's voltage law (KVL) to the outer loop of each circuit, results in Equations 5 and 6.

$$V_{L,on} = V_d - V_o - V_{loss,on} = V_d - V_o - (R_{DS} + R_L)i_L \tag{5}$$

$$V_{L,off} = -V_o - V_f - V_{loss,off} = V_o - V_f - R_L i_L \tag{6}$$

Where R_{DS} is the on resistance of the switch, R_L is the inductor resistance, and V_f is the forward voltage of the diode.

If it is assumed that the circuit is in steady state, then the zero volt-seconds assumption can be applied which yields,

$$V_{L,on}t_{on} + V_{L,off}t_{off} = 0$$

If the inductor current is assumed to be equal to the load current then,

$$i_L \approx i_{Load} = \frac{V_o}{R_{Load}}$$

Which can be used with the previous equation to obtain Equation 7.

$$V_o = \frac{R_{Load}}{(1+2D)R_{Load} - R_L - DR_{DS}} \{DV_d - (1-D)V_f\} \tag{7}$$

For the ideal duty cycle ($D = 41.67\%$) with the parameters $R_{DS} = 0.07\ \Omega$, $R_L = 1.6\ \Omega$, $V_f = 0.7$ V and a load current of $i_L = 1.28$ A ($R_{Load} = 3.9\ \Omega$), the expected output voltage of the converter is $V_o = 3.24$ V [**? ? ?**]. The duty cycle required to obtain an output of 5 V is $D = 61.44\%$.

INCLUDE EFFECTS OF INDUCTOR TOLERENCE AND LOAD TOLERENCE, MENTION PARASITICS

1.4 Non Ideal Simulations

The output voltage of the non-ideal converter for the ideal duty cycle is shown in Figure **??**. Applying a 2nd order low pass filter, with a cutoff frequency of 10 kHz, to the output voltage results in average output voltage of 3.22 V which lies close to the theoretically predicted value of 3.24 V. Figure **??** displays the output voltage for a duty cycle of 61.44 %, an average voltage of 5.00 V is observed which matches the theoretically predicted value.

MISSING GRAPHICS

2 Flyback Converter

2.1 Ideal Calculations

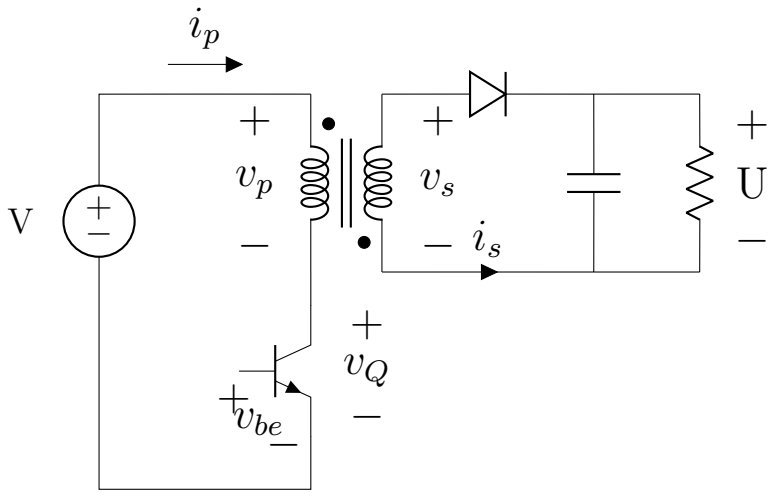

Figure 2: Ideal Flyback Converter

To determine the required duty cycle for the ideal flyback converter the zero volt seconds rule is applied. It is assumed that no lossed occur at the transformer, switches and diodes. It also assumed that the transform turns ratio is 1:1. For the case in which the switch is closed,

$$V_d - V_L = 0 \tag{8}$$

The secondary side has no influence, as the inductor is assumed to be in steady state. For the case where the switch is open,

$$-V_L - V_o = 0 \tag{9}$$

The application of the zero-volts second rule,

$$DT_s \cdot V_{L\,on} + (1 - D)T_s \cdot V_{L\,off} = 0 \tag{10}$$

Cancel out T_s, then substitute equations V_L equations,

$$D \cdot V_d + (1 - D) \cdot -V_o = 0 \tag{11}$$

Therefore, the duty cycle becomes,

$$D = \frac{V_o}{V_d + V_o} \tag{12}$$

The design specifications desire V_o to be 10V but specifys the input, V_d, to be a range of [5,12]V For $V_{d\,min}$, the duty cycle ends up being,

$$D = \frac{10}{5 + 10} = 66.6\% \tag{13}$$

and for $V_{d\,max}$,

$$D = \frac{10}{12 + 10} = 45.45\% \tag{14}$$

2.2 Non-Ideal Calculations

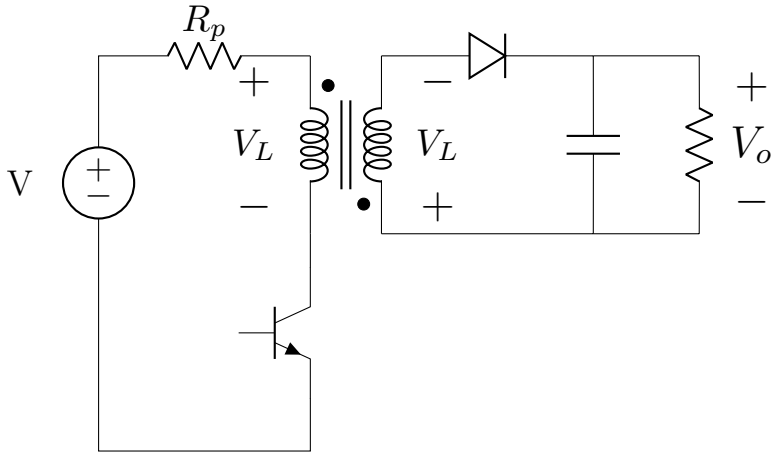

Figure 3: Non-Ideal Flyback Converter

The non-ideal components of the current flyback converter can be modelled like this. This included resistances represent the internal

2.3 Ideal Simulations

2.4 Non-Ideal Simulations

2.5 Results

References