



School of Electrical Engineering
University of Newcastle

ELEC3251

Assignment 1

**Practical and Theoretical Analysis of
Buck Converter and Flyback Converter**

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1 Buck Converter

1.1 Ideal Calculations

The duty cycle required to achieve an output voltage of $V_o = 5$ V for an input supply voltage of $V_d = 12$ V can be determined using the DC transfer function of the Buck converter, see Equation 1. The resulting duty cycle required for the ideal circuit is $D \approx 41.67\%$.

$$\frac{V_o}{V_d} = D \quad (1)$$

The output voltage ripple (ΔV_o) of an ideal Buck converter is given by Equation 2. This equation can be rearranged, see Equation 3, to find the required capacitance for the low pass filter, provided that the duty cycle (D), filter inductance (L), and switching period (T_s) are known. For $T_s = 1/f_s = 10 \mu\text{s}$, $L = 1 \text{ mH}$, $D = 41.67\%$, $\Delta V_o = 25 \text{ mV}$, and $V_o = 5 \text{ V}$, the required capacitance is $C = 1.458 \mu\text{F}$.

$$\frac{\Delta V_o}{V_o} = \frac{1}{8} \frac{T_s^2(1 - D)}{LC} \quad (2)$$

$$C = \frac{V_o}{\Delta V_o} \frac{T_s^2(1 - D)}{8L} \quad (3)$$

The output power of the converter will be limited by the ratings of the components in the circuit. As the output voltage of the converter is required to remain constant at 5 V, only the output current can be adjusted to suit the ratings of the components. The inductor selected for the circuit is the Murata #1410516C, which has a maximum DC current of 1.6 A [1]. A IRFZ24NPbF MOSFET has been selected for the switch, this component has a maximum DC current rating of 17 A [2]. The selected diode is an SB120 which has a maximum DC current of 1.0 A [3]. The inductor current will equal the output current, assuming the voltage across the capacitor remains constant. Therefore, the output current must be less than 1.6 A, to avoid causing damage to the inductor. The diode will only conduct when the switch is off, therefore the DC current flowing through the diode is $I_D = (1 - D)I_o$. For $I_o = 1.6 \text{ A}$ the diode current is 0.93 A, which is less than the maximum rating of the device. Therefore, the load resistance must be selected such that $I_o \leq 1.6 \text{ A}$. Using Ohm's law this inequality is equivalent to $R_{Load} \geq 3.125 \Omega$. The smallest resistor provided in the laboratory kit is 3.9 Ω so this resistance will be used for the load.

The continuous conduction mode (CCM) and discontinuous conduction mode (DCM) boundary occurs when the current flowing through the inductor reaches 0 A. For the ideal Buck converter this will occur for a DC output current (I_{oB}) which can be found using Equation 4. For the designed converter the minimum DC output current is $I_{oB} = 14.6 \text{ mA}$, which is equivalent to an output load of 342 Ω .

$$I_{oB} \approx \frac{T_s V_o}{2L} (1 - D) \quad (4)$$

1.2 Ideal Simulations

Wolfram System Modeler (Wolfram) was used to simulate the performance of the designed converter. The model used for the simulations is shown in Figure 1. The output voltage of the ideal Buck converter is shown in Figure 2. The RMS output voltage is 4.9983 V, which lies close to the theoretically expected value of 5 V. The slight discrepancy between the simulated value and the expected value may be the result of truncating the duty cycle to 4 decimal places ($5/12 \approx 0.4167$). It may also be a result of the numerical methods used by the Wolfram software to simulate the system. An output voltage ripple of 6.67 mV is observed. This ripple is smaller than the expected ripple of 25 mV, this may be the result of the assumption that the output ripple is independent of the load impedance. The addition of the load resistance results in an RLC filter at the output of the converter. This resistance dampens the resonant peak of the LC combination which is likely to result in larger amounts of attenuation for the high frequency components of the output voltage.

Figure 3 (A) displays the inductor current for a load resistance of 342Ω . The current reaches a minimum value of $120 \mu\text{A}$, which indicates that the converter is close to the CCM-DCM boundary. Figure 3 (b) displays the current for a load resistance of 345Ω . Slight distortion is observed in the waveform near the zero crossing which indicates that the converter has entered DCM. This suggests that the CCM-DCM boundary lies in the range $342 \leq R_{Load} \leq 345 \Omega$ which agrees with the theoretically expected value of 342Ω . The boundary may not lie exactly at 342Ω because of the assumption, made in Equation 4, that the inductor current and the output current are equal. This assumption is not correct as a small amount of current also flows through the capacitor.

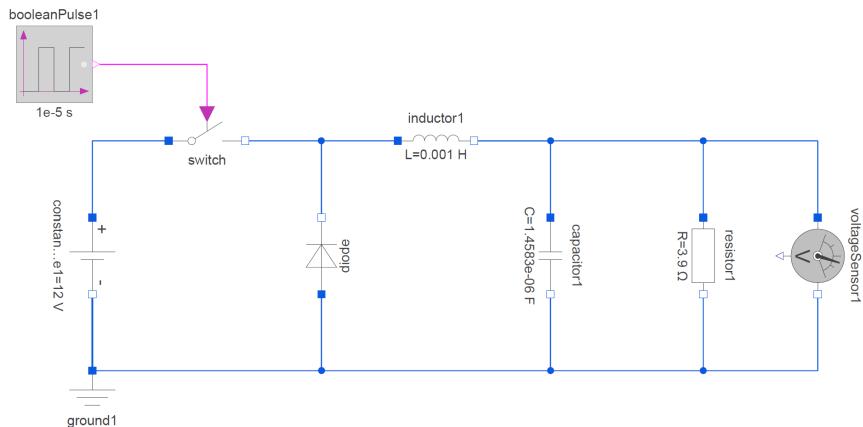


Figure 1: Modelica model used to simulate the operation of the ideal Buck converter.

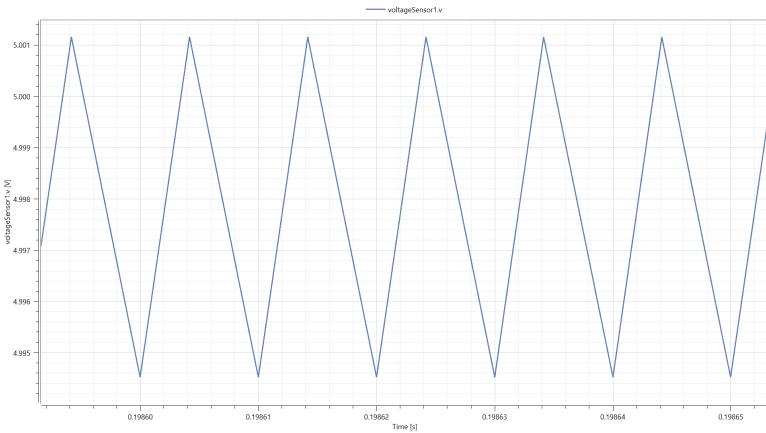


Figure 2: Ideal Buck converter output voltage in steady state. An RMS value of 4.9983 V and a voltage ripple of 6.67 mV are observed.

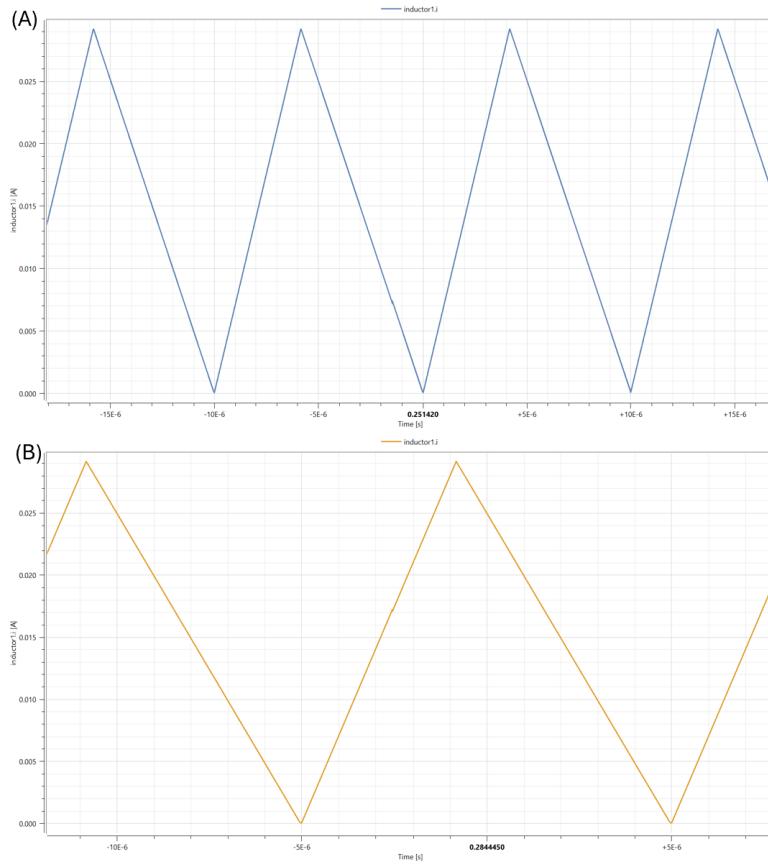


Figure 3: Buck converter inductor current for a load resistance of (A) 342Ω , and (B) 345Ω . A small amount of distortion is present in (B) which indicates that the CCM-DCM boundary lies in the range $342 \leq R_{Load} \leq 345 \Omega$.

1.3 Non Ideal Calculations

The previous calculations and simulations neglect many real-world effects that will affect the circuit's performance. Previously, no voltage losses were assumed to occur across the switch. This assumption is invalid as all switches have non-zero on resistances. Furthermore, it was assumed that no voltage drop occurs across the diode. All diodes have a non-zero voltage drop, which is required to overcome the potential barrier formed at the P-N junction of these devices. In addition, the windings of an inductor are not perfect conductors and hence have resistance. These effects will result in the output voltage of the converter being lower than the theoretically expected value. Applying Kirchoff's voltage law (KVL) when the switch is on and when the switch is off results in Equations 5 and 6.

$$V_{L,on} = V_d - V_o - V_{loss,on} = V_d - V_o - (R_{DS} + R_L)i_L \quad (5)$$

$$V_{L,off} = -V_o - V_f - V_{loss,off} = V_o - V_f - R_L i_L \quad (6)$$

Where R_{DS} is the on resistance of the switch, R_L is the inductor resistance, and V_f is the forward voltage of the diode.

If it is assumed that the circuit is in steady state, then the zero volt-seconds assumption can be applied which yields,

$$V_{L,on}t_{on} + V_{L,off}t_{off} = 0$$

If the inductor current is assumed to be equal to the load current then,

$$i_L \approx i_{Load} = \frac{V_o}{R_{Load}}$$

Which can be used with the previous equation to obtain Equation 7.

$$V_o = \frac{R_{Load}}{(1+2D)R_{Load} - R_L - DR_{DS}} \{DV_d - (1-D)V_f\} \quad (7)$$

For the ideal duty cycle ($D = 41.67\%$) with the parameters $R_{DS} = 0.07 \Omega$, $R_L = 1.6 \Omega$, $V_f = 0.7 \text{ V}$ and a load current of $i_L = 1.28 \text{ A}$ ($R_{Load} = 3.9 \Omega$), the expected output voltage of the converter is $V_o = 3.24 \text{ V}$ [1, 2, 3]. The duty cycle required to obtain an output of 5 V is $D = 61.44\%$.

The CCM-DCM boundary occurs when the output current is approximately equal to half of the peak current through the inductor. The peak current through the inductor is given by Equation 8.

$$i_{pk} = \frac{1}{L} \int_0^{t_{on}} v_L dt \quad (8)$$

For the ideal case the voltage across the inductor (when the switch is on) is:

$$v_{L,ideal} = V_d - V_o$$

For the non-ideal case the voltage is:

$$v_{L,non-ideal}(t) = V_d - V_o - i_L(t)(R_{DS} + R_L)$$

Where,

$$v_{L,ideal} \geq v_{L,non-ideal}(t)$$

Which implies,

$$i_{pk,ideal} > i_{pk,non-ideal}$$

Thus,

$$I_{oB,ideal} > I_{oB,non-ideal}$$

Therefore, it is expected that a larger load resistance will be required for the non-ideal Buck converter, to observe the CCM-DCM boundary.

1.4 Non Ideal Simulations

Figure 4 displays the Modelica model used to perform the non-ideal simulation. The non ideal switch model from the *InverterParts.NonIdeal_Components* library was used to replicate the IRFZ24NPbF MOSFET. The reverse diode voltage (1.3 V), series resistance (0.07Ω), parallel resistance ($2 \text{ M}\Omega$), turn on time (4.9 ns), and turn off time (19 ns) of the MOSFET are included in this model. The 1.6Ω resistor is used to model the series resistance of the inductor and the $1.3 \times 10^{-11} \text{ F}$ capacitor is used to model the self-resonant frequency of the inductor. The non ideal diode model from the *InverterParts.NonIdeal_Components* library was used to replicate the SB120 diode. The worst case forward voltage (0.70 V) and the junction capacitance (110 pF) of the SB120 were included in this model. An output capacitance of $1 \mu\text{F}$ has been used in the simulation. This capacitance was selected as it lies close to the theoretically predicted value and was the largest capacitance that can be achieved with the laboratory kit without placing multiple capacitors in series.

The output voltage of the non-ideal converter for the ideal duty cycle is shown in Figure 5. An RMS voltage of 3.2164 V is observed, which lies close to the theoretically predicted value of 3.24 V. The slight deviation from this value may be the result of assuming that the output current is constant and equal to the current through the inductor. Figure 6 displays the output voltage for a duty cycle of 61.44%, an RMS voltage of 5.0010 V is observed which lies close to the predicted value. A ripple voltage of 27.739 mV is observed which lies close to the specified value of 25 mV. The increase in the voltage ripple for the non-ideal simulation is likely a result of the reducing the size of the output capacitor, increasing the duty cycle, and including the parasitic capacitance of the inductor. This ripple could be reduced through increasing the size of the output capacitor.

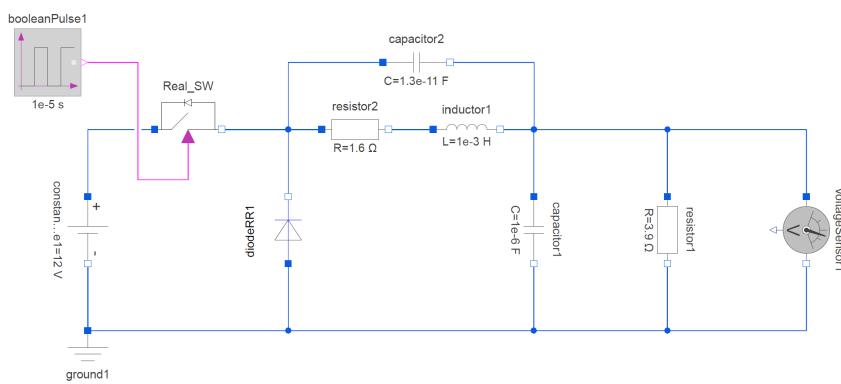


Figure 4: Modelica model used to simulate the operation of the non ideal Buck converter.

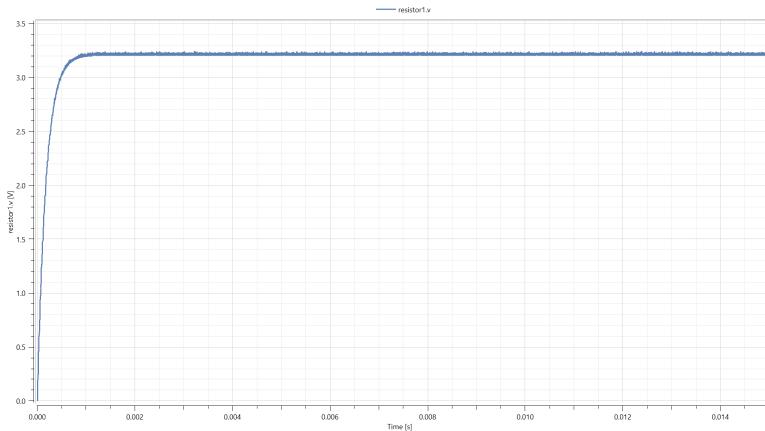


Figure 5: Non-ideal Buck converter output voltage for duty cycle of 41.67% and a load of 3.9Ω . An average voltage of 3.2164 V is observed.

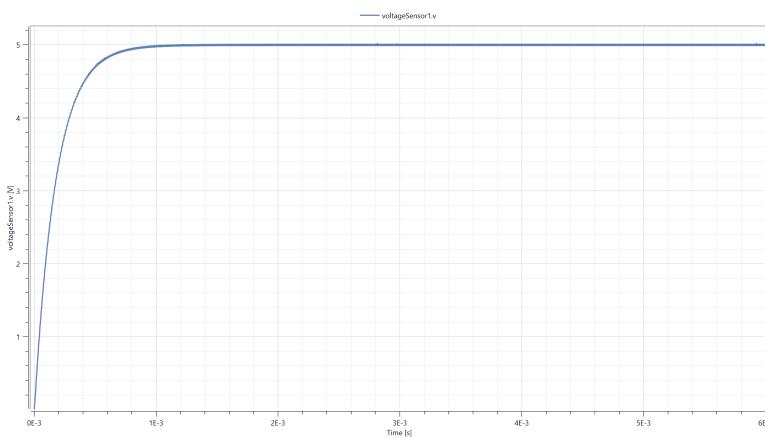


Figure 6: Non-ideal Buck converter output voltage for duty cycle of 61.44% and a load of 3.9Ω . An average voltage of 5.0010 V and a ripple voltage of 27.739 mV is observed.

The current through the inductor for $D = 61.44\%$ (rated power conditions) is shown in Figure 7. An RMS current of 1.2847 A is observed which matches the theoretically predicted value and does not exceed the maximum ratings of the devices. The inductor current for a load of (A) 470Ω and (B) 475Ω is shown in Figure 8. The inductor current for the 475Ω passes through the 0 A crossing for a period of time. This indicates that the circuit has entered DCM. The 470Ω load results in a current which gets close to the 0 A crossing. Therefore the load resistance for the CCM-DCM boundary is expected to lie in the range $470 \leq R_{Load} \leq 475 \Omega$.

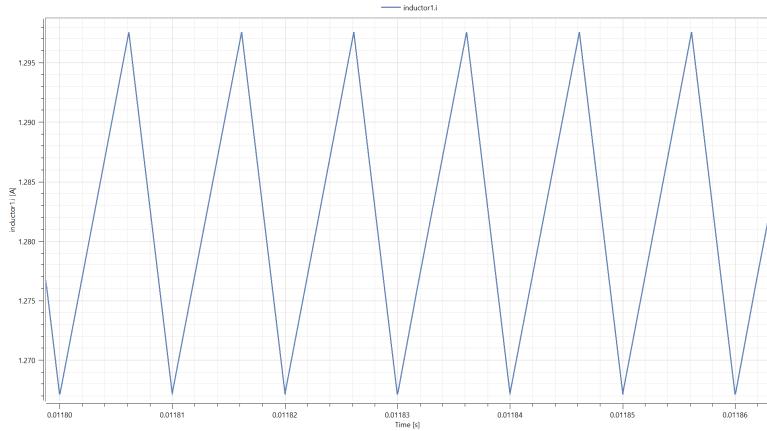


Figure 7: Inductor current for the non ideal Buck converter under rated power conditions.

1.5 Results

The constructed Buck converter is shown in Figure 9. The circuit was constructed on a breadboard and multicore twisted wires were used. The PWM input signal for the gate driver was generated using a signal generator and the output voltage was monitored using an oscilloscope. The observed output voltage of the Buck converter for a duty cycle of $D = 62\%$ is shown in Figure 10. The blue waveform is the output voltage, and the yellow waveform is the PWM input signal to the gate driver. An RMS output voltage of 5.081 V is observed which lies close to the simulated value of 5.0010 V. A peak to peak voltage of 2.000 V is observed which does not align with the simulated ripple voltage of 27.739 mV. This large peak to peak voltage is a result of the large transients that occur when the PWM signal switches. These transients arise from the parasitic inductances of the wires and the parasitic capacitances of the breadboard. As the PWM signal has infinite bandwidth, some of the components of the signal resonant with the parasitic inductances and capacitances which results in large transient responses that are visible in the output waveform. This ripple can only be mitigated through minimizing the parasitic impedances of the device. This could be achieved through designing a printed circuit board (PCB) for the device. This would reduce the parasitic capacitance of the design, as the capacitance formed by the parallel conductive strips on the breadboard would not be present. The designed PCB would need to feature short trace lengths with tight ground loops to minimize parasitic inductance.

To explore the output ripple of the converter once the large transients are no longer present, Figure 11 displays the steady state output voltage of the Buck converter for $D = 62\%$. A maximum voltage of 5.14 V and a minimum voltage of 5.02 V is observed which results in an output voltage ripple of 120 mV. This output ripple is much larger than the specified ripple of 25 mV and is larger than the simulated ripple of 27.739 mV. This is likely due to the parasitic inductances of the wires used. This ripple could be reduced through minimizing the length of the wires and by using a larger output capacitor. A larger output capacitor will result in more attenuation of these high frequency ripple components.

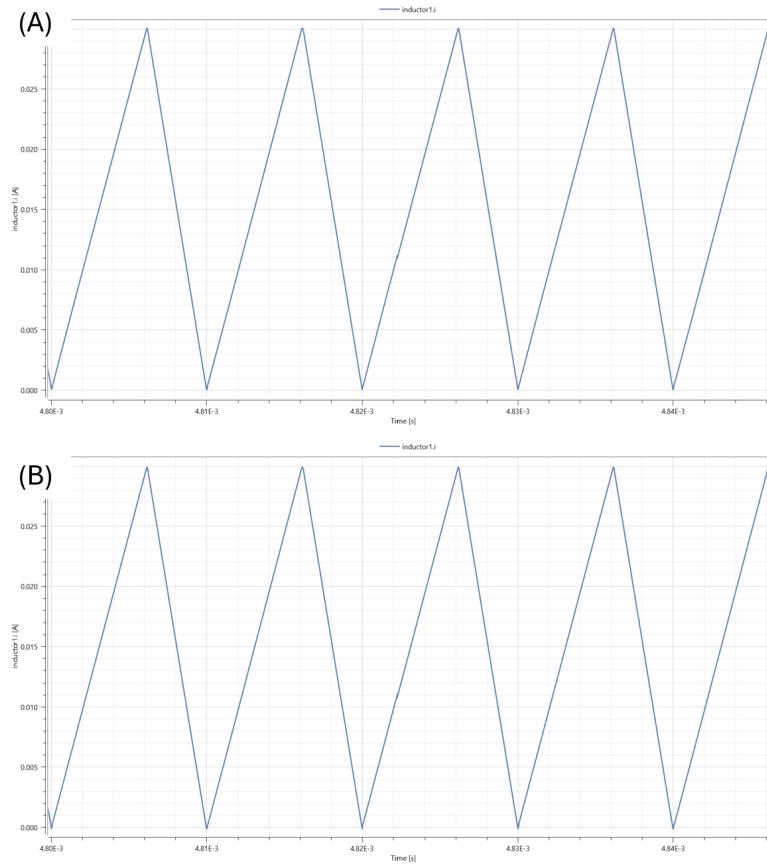


Figure 8: Inductor current for the non ideal Buck converter under rated power conditions.

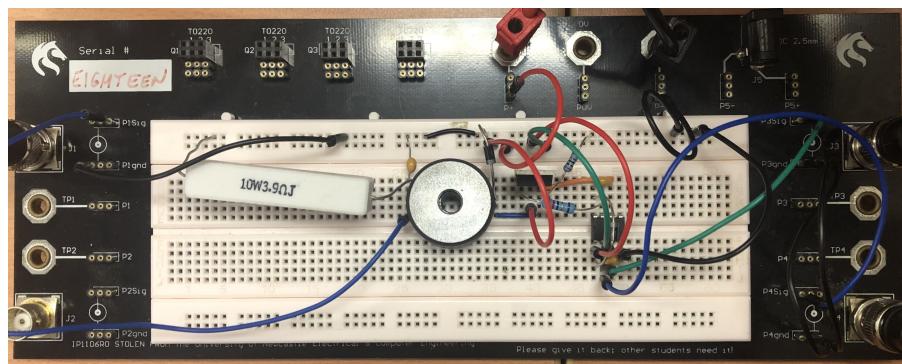


Figure 9: Constructed Buck converter.

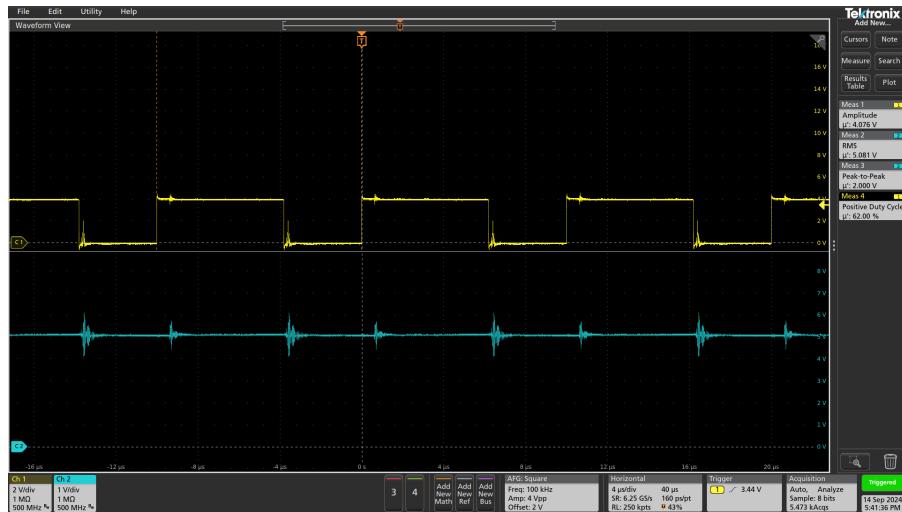


Figure 10: Output voltage of the Buck converter (blue) for a duty cycle of 62%. The yellow waveform is the input PWM signal to the gate driver. An RMS voltage of 5.081 V is observed.

Figure 12 displays the inductor current (green waveform) close to the rated output power conditions ($D = 62\%$). An RMS current of 1.11 A is observed which does not agree with the simulated value of 1.2847 A. This is likely a result of the designed converter not accounting for variation in the resistance of the load. This is evidenced by the RMS output voltage (blue waveform) of 4.75 V which implies the load resistance is 4.27Ω instead of 3.90Ω . This was likely not observed in Figure 10 as the circuit had been running for a longer period of time when the current was measured, compared to when the voltage was measured. This longer operating period likely resulted in the temperature of the load increasing which leads to a larger number of collisions between the electrons and the ions in the load and hence a larger resistance. The dependence of the output voltage on the load could be removed through the use of a closed loop control system with integral action.

Figure 13 (A) displays the inductor (green waveform) for a load of 470Ω and $D = 62\%$. The inductor current is observed to reach 0 A but does not remain there for a considerable amount of time, which indicates that the device is on the cusp of DCM. This result aligns with the simulation results. Figure 13 (B) displays the inductor current inductor current (green waveform) and output voltage (blue waveform) for a load resistance of 600Ω . The current spends a larger amount of time near the zero crossing which indicates that the circuit is in DCM mode.

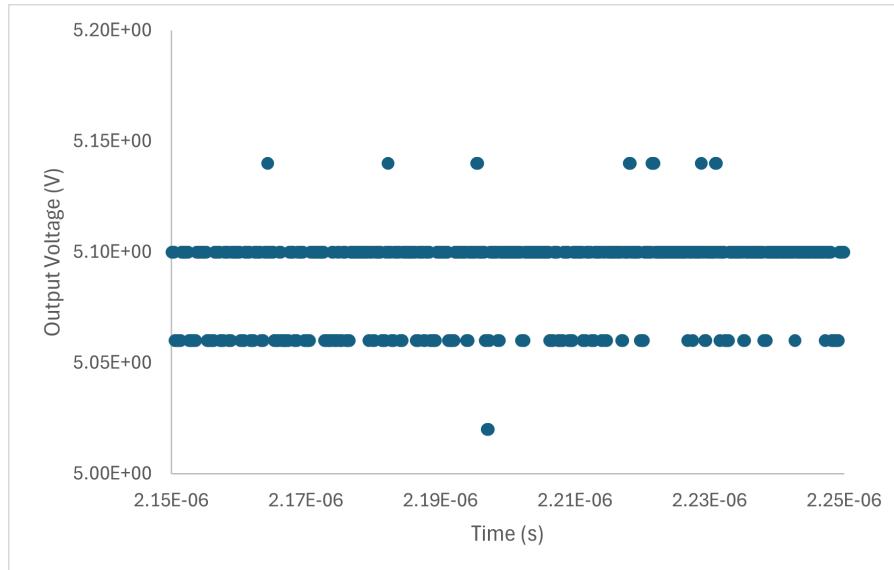


Figure 11: Output voltage of the Buck converter in steady state. A ripple voltage of 120 mV is observed.

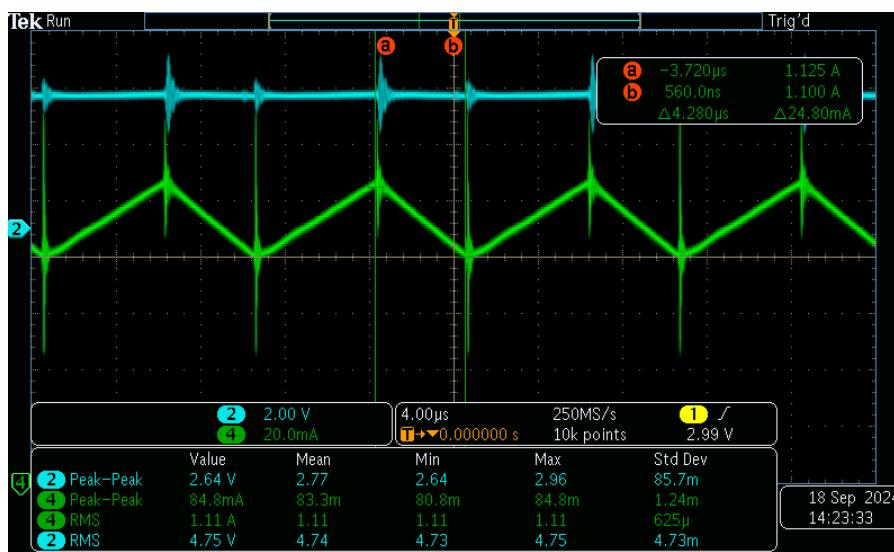


Figure 12: Output current of the Buck converter under rated power conditions.

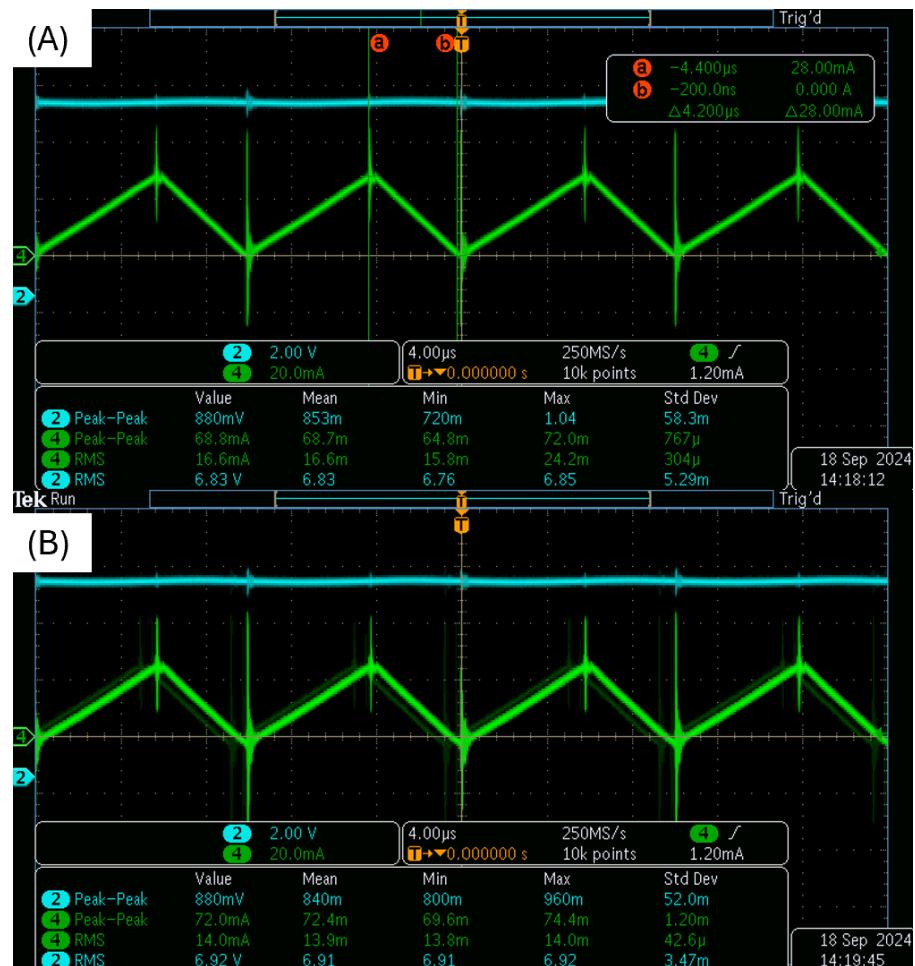


Figure 13: Output current of the Buck converter under rated power conditions.

2 Flyback Converter

2.1 Ideal Calculations

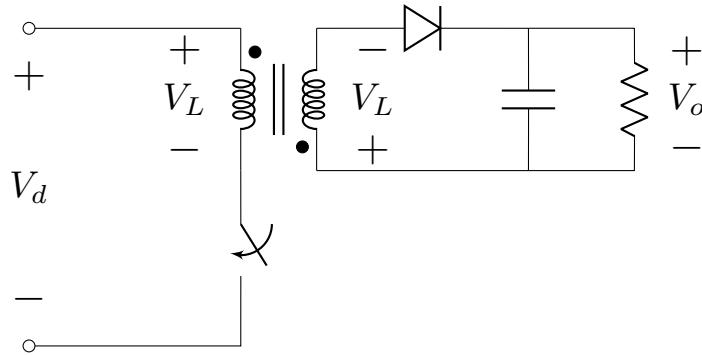


Figure 14: Ideal Flyback Converter

To determine the required duty cycle for the ideal flyback converter, the zero volt seconds rule is applied. It is assumed that no losses occur at the transformer, switches and diodes. In this instance, it is also assumed that the transformer turns ratio is 1:1. For the case in which the switch is closed,

$$V_d - V_L = 0 \quad (9)$$

The secondary side has no influence, as the inductor is assumed to be in steady state. For the case where the switch is open,

$$-V_L - V_o = 0 \quad (10)$$

The application of the zero-volts second rule,

$$DT_s \cdot V_{L\,on} + (1 - D)T_s \cdot V_{L\,off} = 0 \quad (11)$$

Cancel out T_s , then substitute equations V_L equations,

$$D \cdot V_d + (1 - D) \cdot -V_o = 0 \quad (12)$$

Therefore, the duty cycle becomes,

$$D = \frac{V_o}{V_d + V_o} \quad (13)$$

The design specifications desire V_o to be 10V but specifies the input, V_d , to be a range of [5,12]V. For $V_{d\,max}$,

$$D = \frac{10}{12 + 10} = 45.45 \% \quad (14)$$

and for $V_{d\,min}$,

$$D = \frac{10}{5 + 10} = 66.67 \% \quad (15)$$

For the ideal flyback converter, the load resistance can be calculated from the desired output power and desired output voltage,

$$R_L = \frac{V_o^2}{P_o} \quad (16)$$

Therefore, if $V_o = 10$ V and $P_o = 0.5$ W then $R_L = 200 \Omega$. To ensure CCM and a reasonable voltage ripple, the output capacitor, C, is calculated from the voltage ripple equation for the flyback, the same equation as the buck-boost converter.

$$\Delta V_o = \frac{DT_s}{CR_L} V_o \quad (17)$$

If the switching frequency is 100 kHz, then $T_s = 10 \mu\text{s}$. Then rearranging to make C the subject and substituting relevant parameters,

$$C = \frac{DT_s}{\Delta V_o R_L} V_o \quad (18)$$

Hence, for $V_{d\max}$, $C = 1.136 \mu\text{F}$ and for $V_{d\min}$, $C = 1.56 \mu\text{F}$

2.2 Ideal Simulations

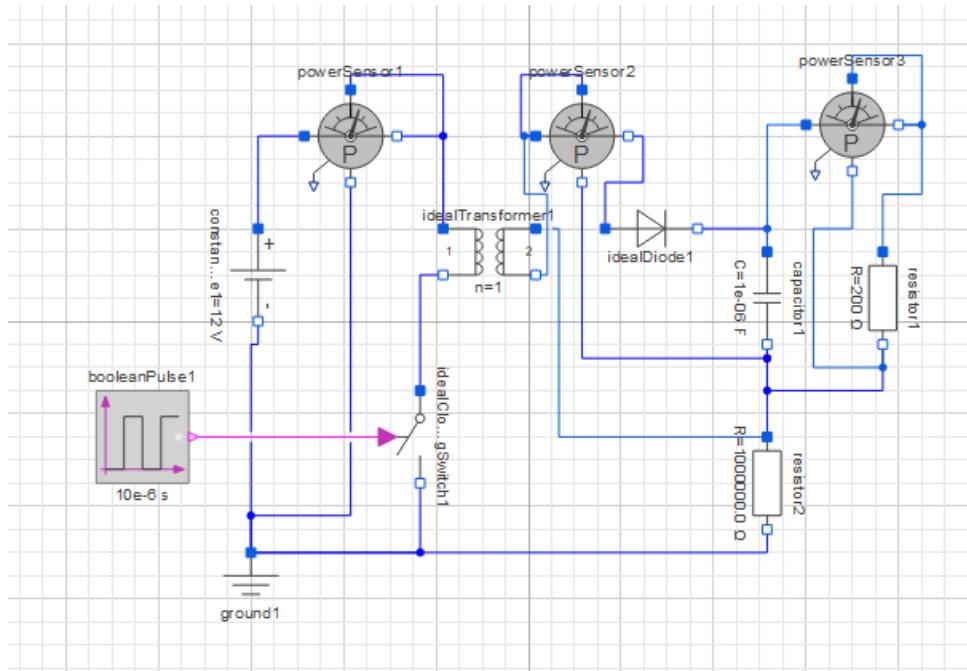


Figure 15: Ideal Flyback, Output Voltage $V_o = 10$ V, ($V_d = 12$ V, $D = 0.4545$)

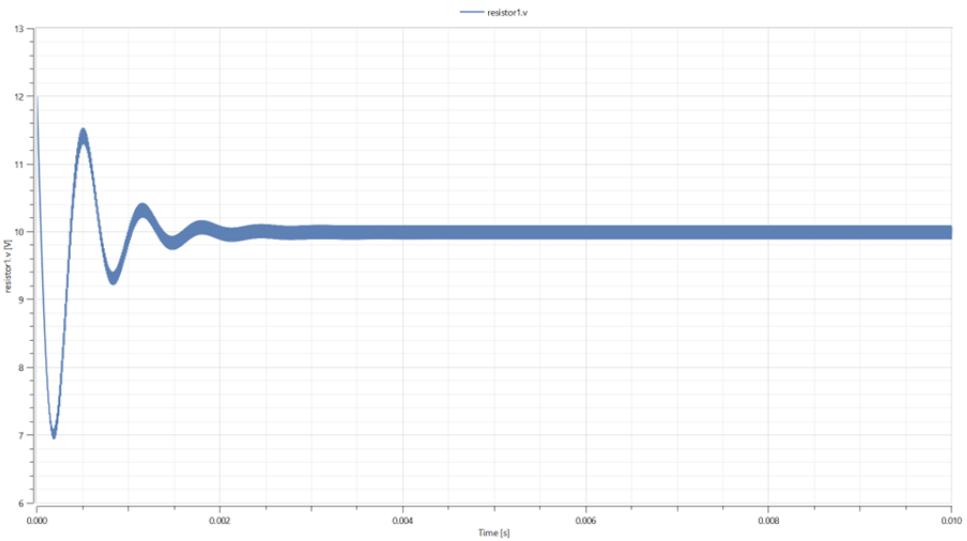


Figure 16: Ideal Flyback, Output Voltage $V_o = 10$ V, ($V_d = 12$ V, $D = 0.4545$)

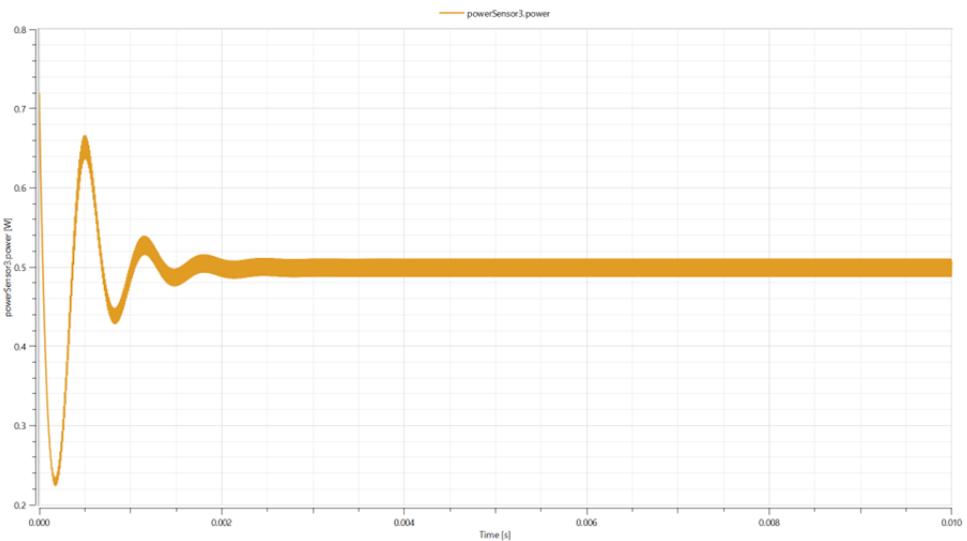


Figure 17: Ideal Flyback, Output Power $P_o = 0.5$ W, ($V_d = 12$ V, $D = 0.4545$)

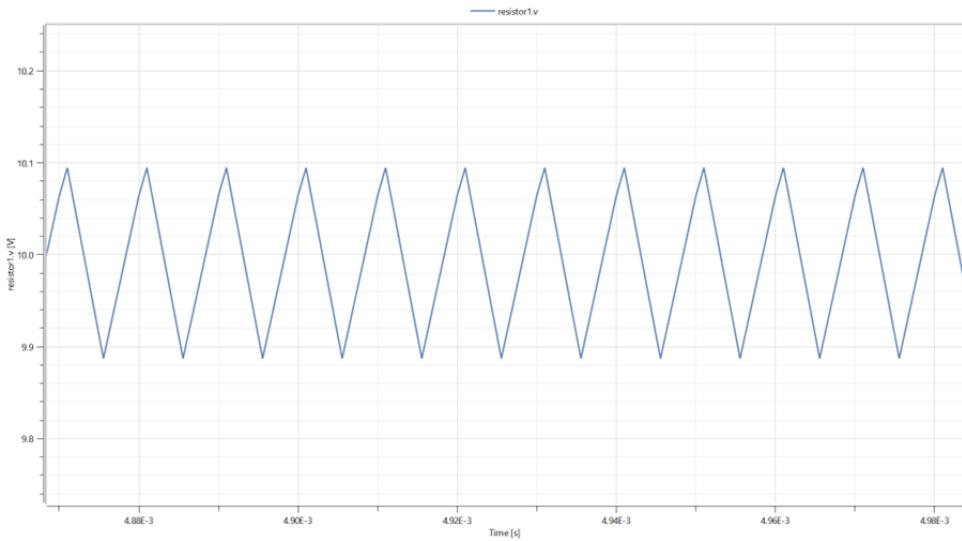


Figure 18: Ideal Flyback, Output Ripple $\Delta V_o = 200 \text{ mV}$, ($C = 1 \mu\text{F}$, $V_d = 12 \text{ V}$, $D = 0.4545$)

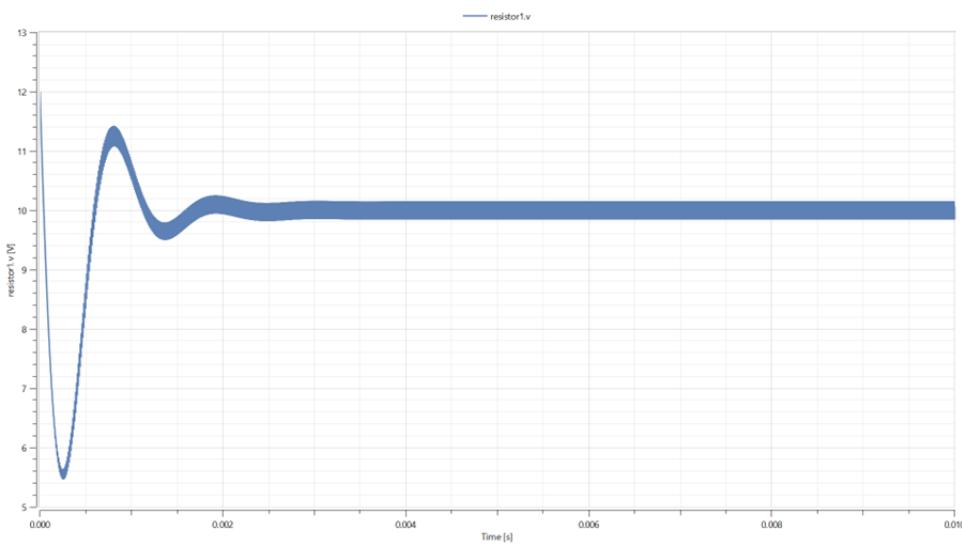


Figure 19: Ideal Flyback, Output Voltage $V_o = 10 \text{ V}$, ($V_d = 5 \text{ V}$, $D = 0.6667$)

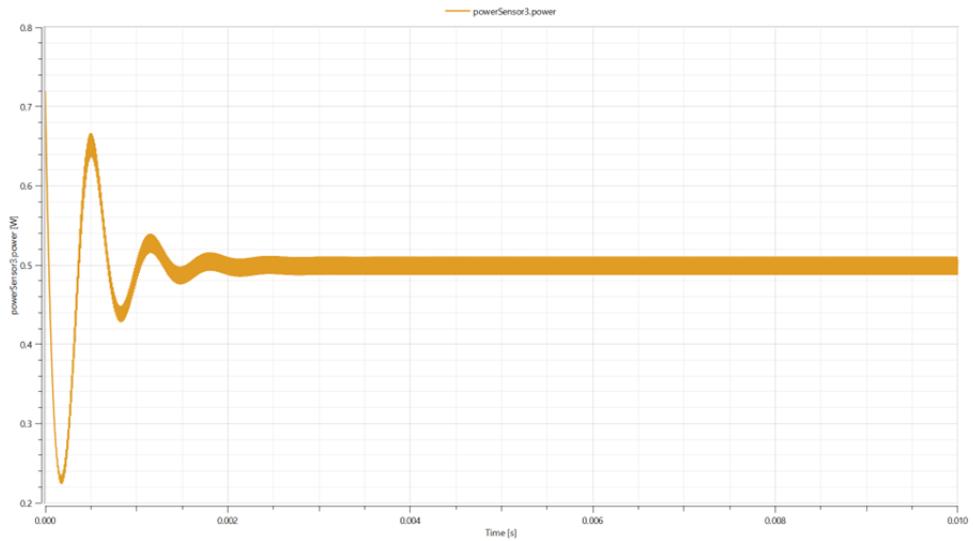


Figure 20: Ideal Flyback, Output Power $P_o = 0.5$ W, ($V_d = 5$ V, $D = 0.6667$)

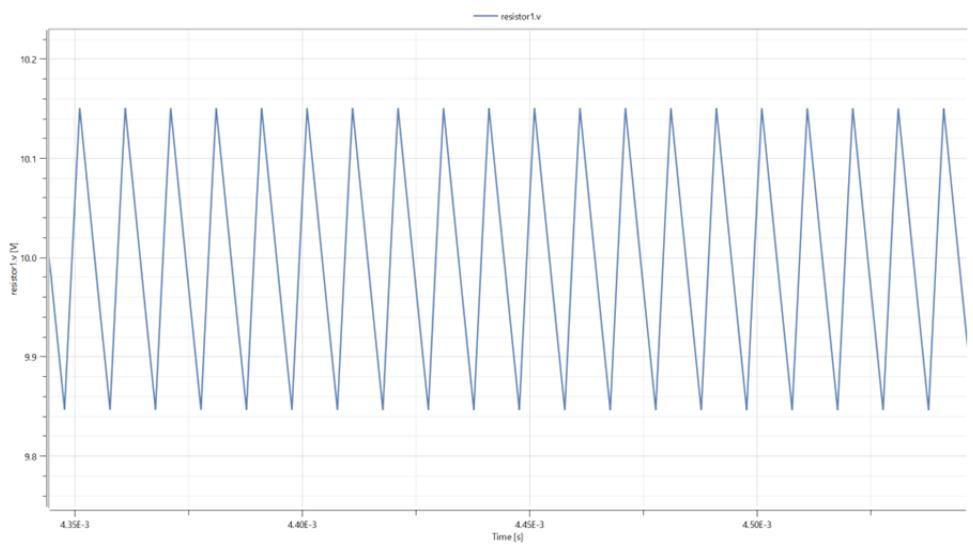


Figure 21: Ideal Flyback, Output Ripple $\Delta V_o = 300$ mV, ($C = 1 \mu\text{F}$, $V_d = 5$ V, $D = 0.6667$)

2.3 Non-Ideal Calculations

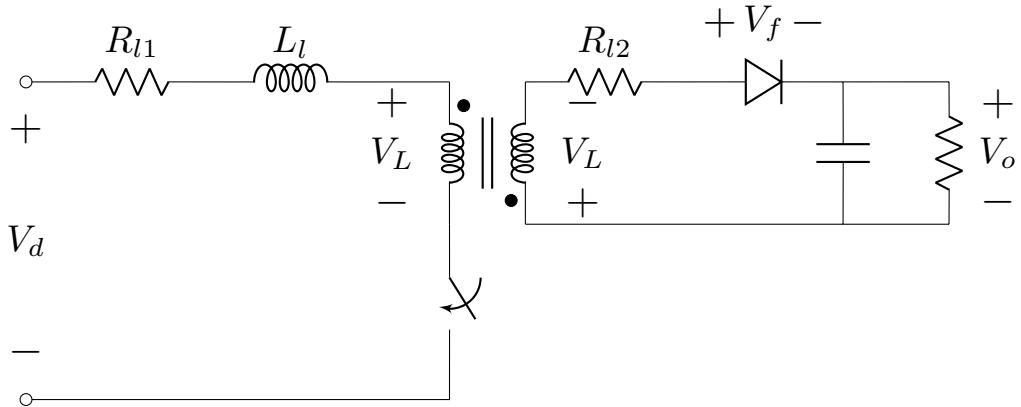


Figure 22: Non-Ideal Flyback Converter

The specifications for the flyback converter ask for an output of 10 V at 0.5 W. To achieve this, an average current can be calculated using ohm's law of power,

$$P = IV \quad (19)$$

which gives $I_{avg} = 50$ mA. This can be used to determine the load resistance with ohm's law,

$$V = IR \quad (20)$$

Therefore, the load resistance, R_L is 200Ω . The closest available load resistor is 220Ω which can be reversed to get the average current, $I_{avg} = 45.45$ mA and output power, $P = 0.4545$ W which is now the standard and will be used for further calculations. The non-ideal components of the current flyback converter can be modelled like this. The primary side is the only active when the switch is on, this means the internal MOSFET resistance and the internal transformer resistance can be added together like this,

$$R_{l1} = R_{mosfet} + R_{transformer} \quad (21)$$

For the case when switch is closed,

$$V_d - V_{Rl1} - V_{Ll} - V_L = 0 \quad (22)$$

The voltage across the leakage inductance cannot be known, instead the leakage inductance will be ratioed in terms of the magnetising inductance. From the transformer datasheet, [4], the magnetising inductance is 3 mH and the leakage inductance at the primary side is $9 \mu\text{H}$. Therefore the case when the switch is closed is simplified to,

$$V_d - V_{Rl1} - V_L = 0 \quad (23)$$

Therefore the case for the switch is open,

$$-\frac{3}{3.009}V_L - V_{Rl2} - V_f - V_o = 0 \quad (24)$$

Applying the zero volt seconds rule, 11, and cancelling out Ts,

$$D \cdot (V_d - V_{Rl1}) + (1 - D) \cdot \frac{3.009}{3}(-V_{Rl2} - V_f - V_o) = 0 \quad (25)$$

rearranging to make duty cycle the subject,

$$D = \frac{\frac{3.009}{3}(V_{Rl2} + V_f + V_o)}{V_d - V_{Rl1} + \frac{3.009}{3}(V_{Rl2} + V_f + V_o)} \quad (26)$$

Equation 21, is used to calculate $R_{l1} = 1.47$. It is known that the average current, $I_{avg} = 45.45$ mA, 20. The forward biased voltage drop across the diode is 0.7 V,[2]. The duty cycle can be calculated for the maximum and minimum of the desired V_d range [5,12]V. For $V_{d max}$,

$$D = \frac{\frac{3.009}{3}(1.7 \cdot I_{avg} + 0.7 + 10)}{12 - 1.47 \cdot I_{avg} + \frac{3.009}{3}(1.7 \cdot I_{avg} + 0.7 + 10)} = 47.53 \% \quad (27)$$

and for $V_{d min}$,

$$D = \frac{\frac{3.009}{3}(1.7 \cdot I_{avg} + 0.7 + 10)}{5 - 1.47 \cdot I_{avg} + \frac{3.009}{3}(1.7 \cdot I_{avg} + 0.7 + 10)} = 68.66 \% \quad (28)$$

2.4 Non-Ideal Simulations

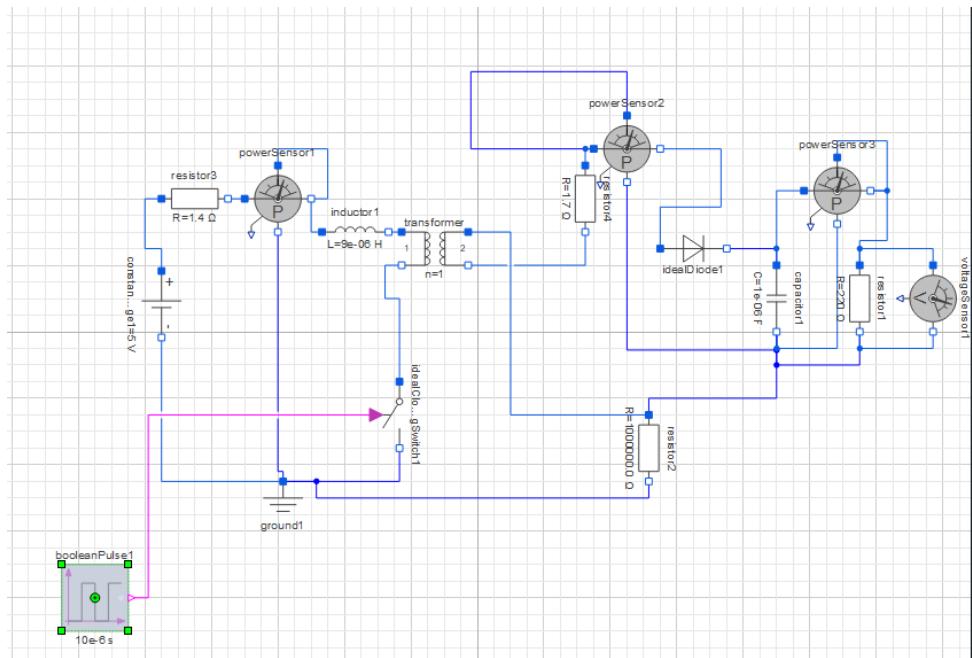


Figure 23: Non Ideal Flyback, Output Voltage $V_o = 9.21 \text{ V}$, ($V_d = 5 \text{ V}$, $D = 0.6667$)

In all non-ideal simulations, the capacitance is set to $1 \mu\text{F}$. This is less than what was calculated, 18, and it should be noted.

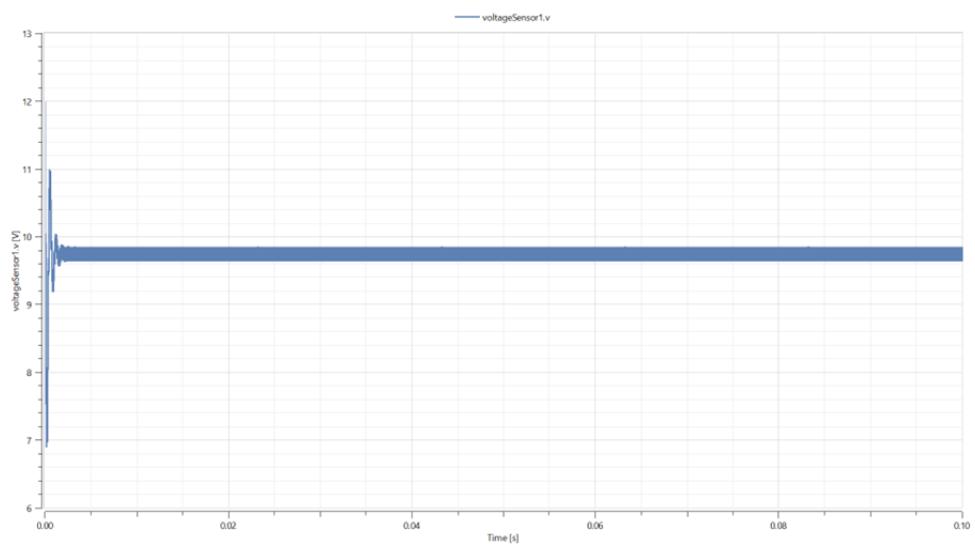


Figure 24: Non Ideal Flyback, Output Voltage $V_o = 9.746$ V, ($V_d = 12$ V, $D = 0.4753$)

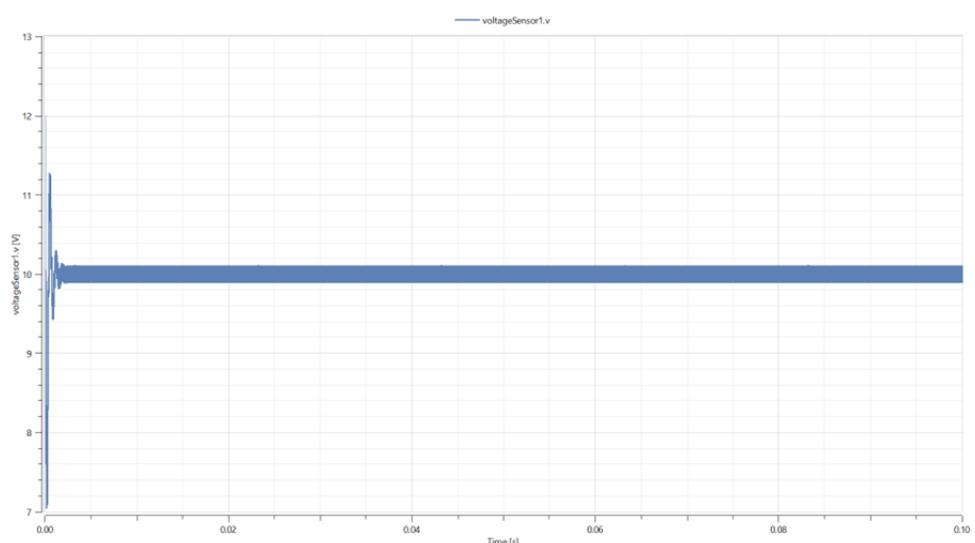


Figure 25: Non Ideal Flyback, Output Voltage $V_o = 10$ V, ($V_d = 12$ V, $D = 0.4815$)

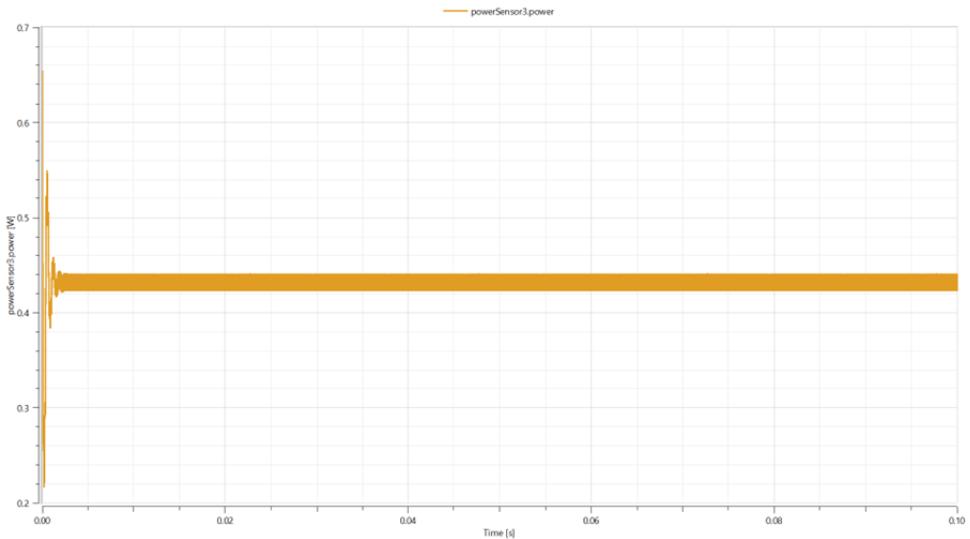


Figure 26: Non Ideal Flyback, Output Power $P_o = 0.432$ W, ($V_d = 12$ V, $D = 0.4753$)

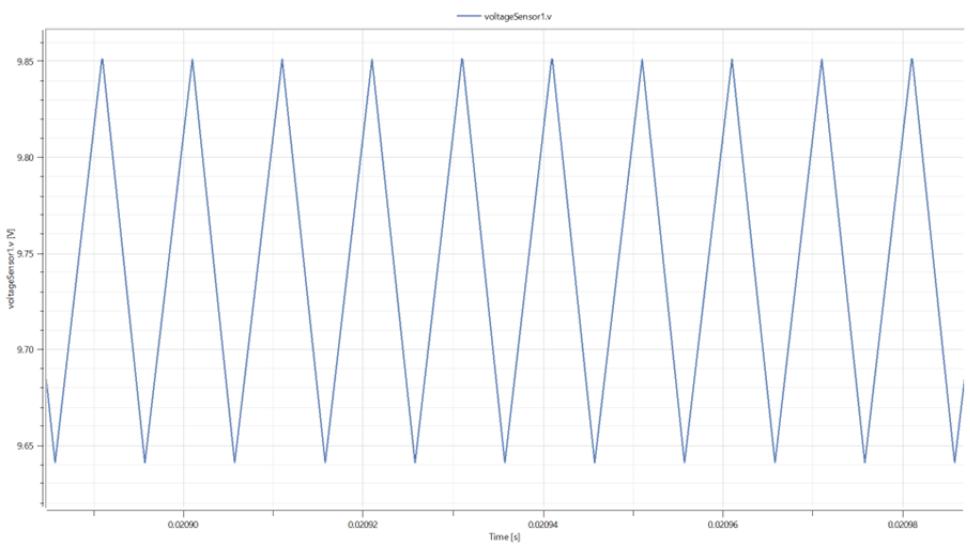


Figure 27: Non Ideal Flyback, Output Ripple $\Delta V_o = 210$ mV, ($V_d = 12$ V, $D = 0.4753$)

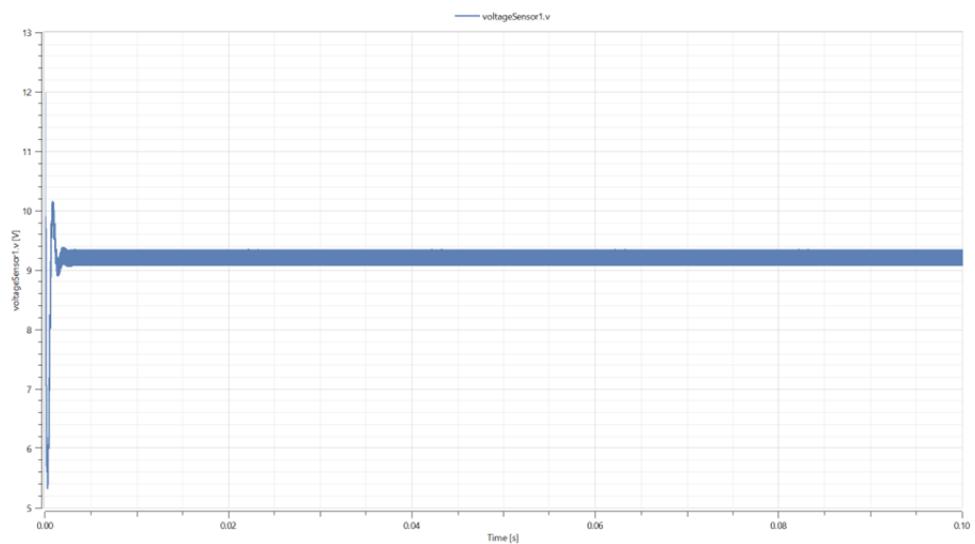


Figure 28: Non Ideal Flyback, Output Voltage $V_o = 9.21$ V, ($V_d = 5$ V, $D = 0.6866$)

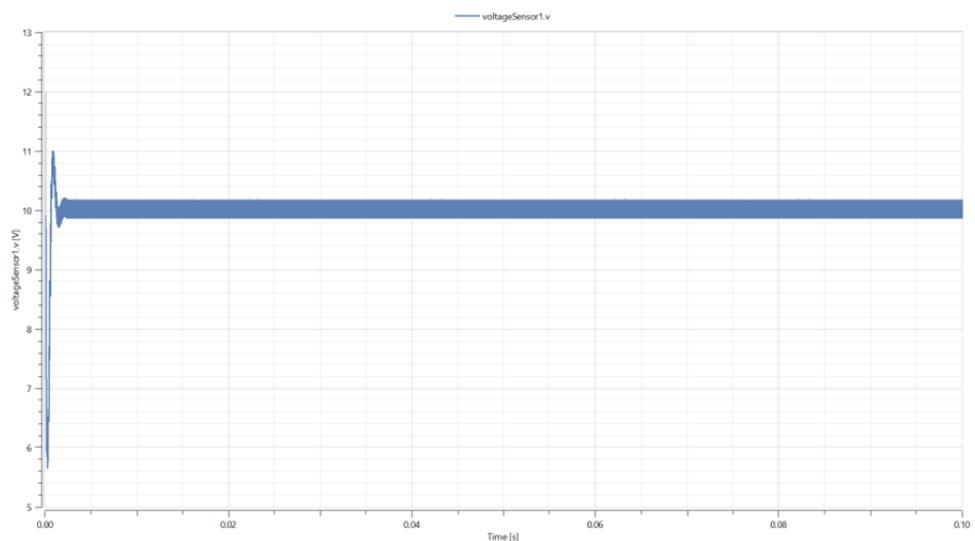


Figure 29: Non Ideal Flyback, Output Voltage $V_o = 10.02$ V, ($V_d = 5$ V, $D = 0.7055$)

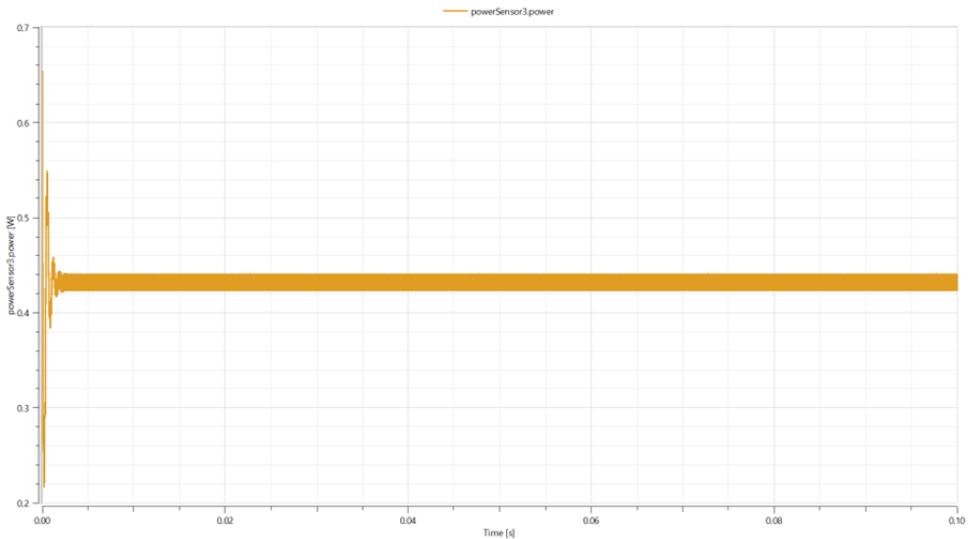


Figure 30: Non Ideal Flyback, Output Power $P_o = 0.385$ W, ($V_d = 5$ V, $D = 0.6667$)

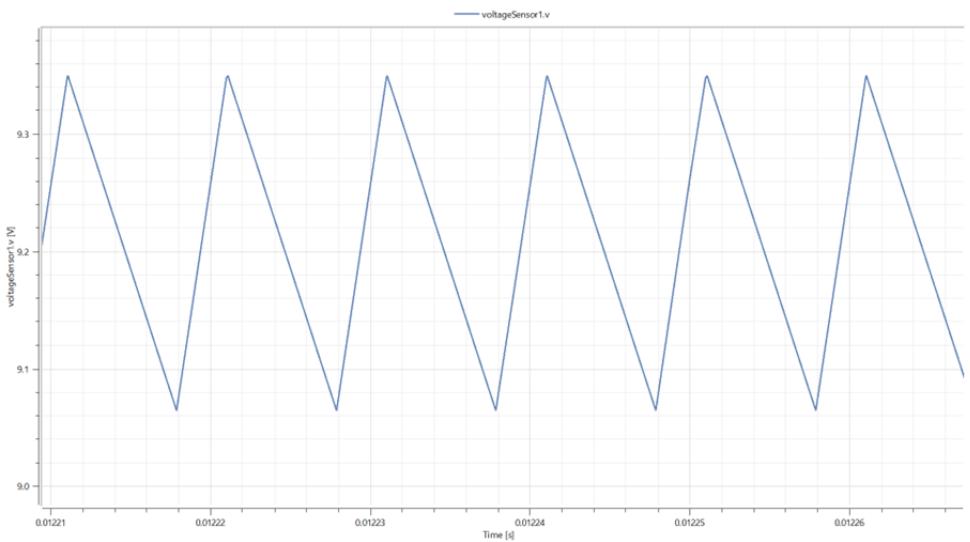


Figure 31: Non Ideal Flyback, Output Ripple $\Delta V_o = 290$ mV, ($V_d = 5$ V, $D = 0.6667$)

2.5 Results

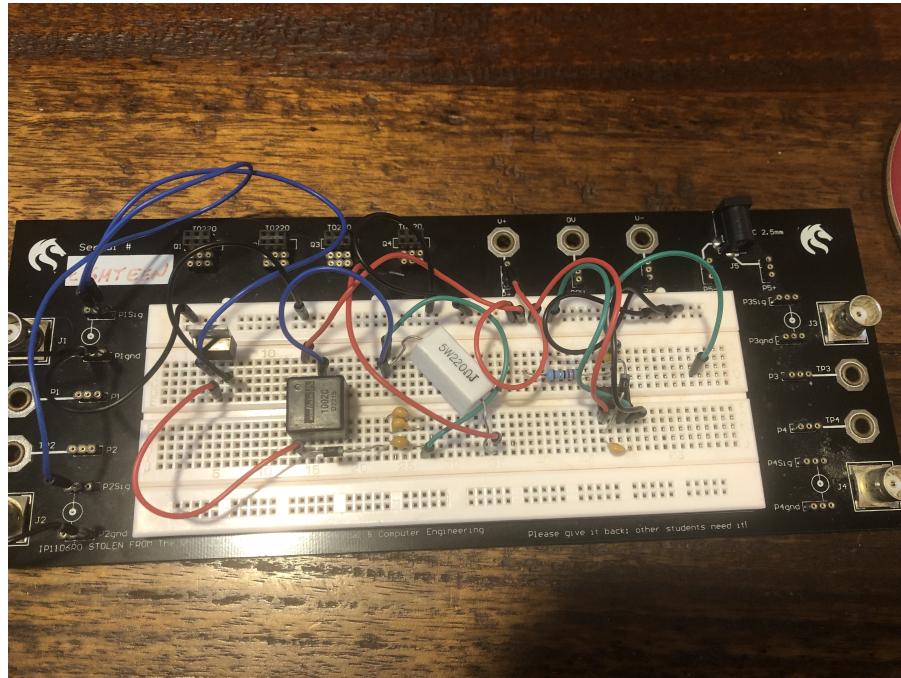


Figure 32: Practical Flyback, $C = 2.68 \mu\text{F}$

Table 1: Comparison of Duty Cycles (D) required to produce $V_o = 10 \text{ V}$

V_d	12V	5V
Calculated D	0.4753	0.6866
Simulated D	0.4815	0.7055
Practical D	0.491	0.734

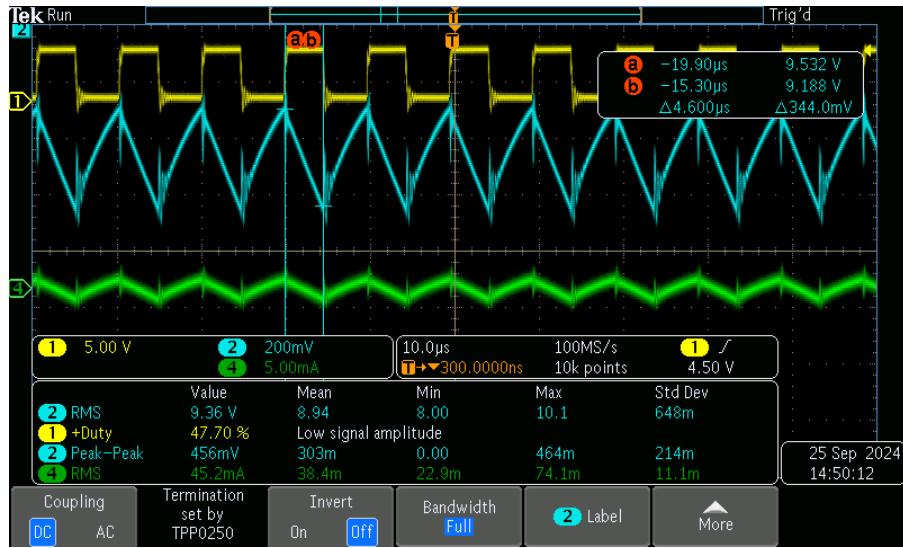


Figure 33: Practical Flyback, Ripple $\Delta V_o = 344$ mV, ($C = 1 \mu\text{F}$, $V_d = 12$ V, $D = 0.477$)

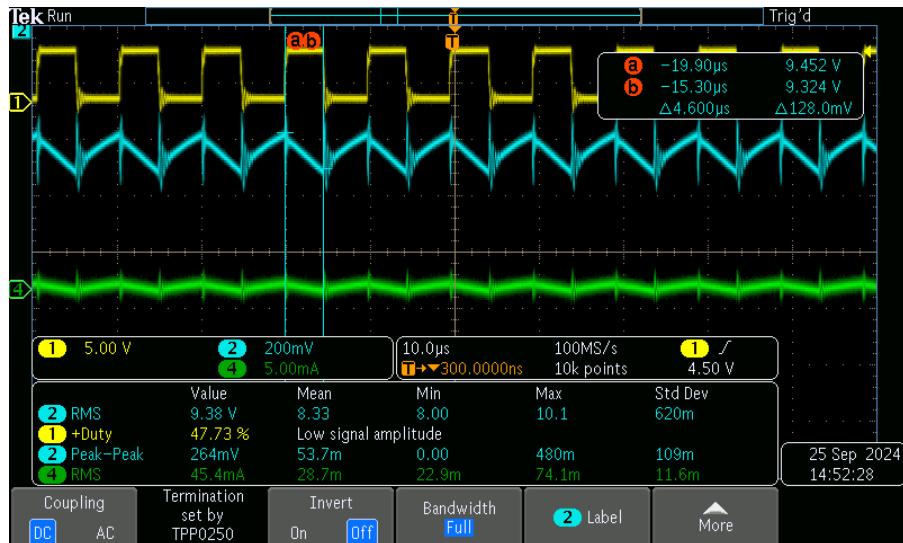


Figure 34: Practical Flyback, Ripple $\Delta V_o = 128$ mV, ($C = 2.68 \mu\text{F}$, $V_d = 12$ V, $D = 0.477$)



Figure 35: Practical Flyback, Output Voltage $V_o = 8.32$ V, ($C = 2.68 \mu\text{F}$, $V_d = 5$ V, $D = 0.688$)



Figure 36: Practical Flyback, Output Voltage $V_o = 10$ V, ($C = 2.68 \mu\text{F}$, $V_d = 5$ V, $D = 0.734$)

2.6 Conclusion

The flyback was successfully built and could meet all specifications including the input voltage range, $V_d = [5,12]V$. Some non-ideal behaviour and theory differences was observed. These include the practical procedure to meet specifications, the gate-driver noise and the mistake with the non-ideal transformer model which will be discussed.

The built flyback needed to be adjusted to meet specifications. To reduce the voltage ripple 33, the capacitance was increased from $1 \mu F$ to $2.68 \mu F$ by placing capacitors in parallel 32, which is known to reduce the output voltage ripple from 17. This is expected to create an output ripple of 76 mV. Implementing this greatly reduces the output voltage ripple from 344 mV to 128 mV, 34. While it does not match the expected ΔV_o , it does match the linear relationship between capacitance and voltage ripple. The output voltage did not match the desired specification, $V_o = 10 V$, 35. To fix this, the duty cycle was increased until output voltage specification was met, see 36. This increased the duty cycle, from 0.688 to 0.734 and does not meet theory expectations.

The output voltage noise was much greater in the buck converter. This is seen by comparing the buck converter peak-peak measurement, Figure 13 to the flyback converter peak-peak measurement, Figure 33. This is because the gate driver was plugged into a breadboard, 32 which creates 20 pF between the pins on each side. This is amplified by switching harmonics, similar to bipolar vs unipolar. In the buck converter, the gate driver must drive the gate of the MOSFET to a greater voltage because it is set up in the high side configuration. In the flyback converter, the MOSFET is setup in a low side configuration, which means the gate voltage doesn't require more than 5 V logic high.

The transformer calculations did not correctly model the simulation and practical behaviour. From the theory in equation 11, a ratio was used to determine power lost at the primary. This however does not accurately reflect lost power, which increases with a higher duty cycle. This relationship is viewed by comparing Figure (24, 25) to (28, 29) and considering Table 1. This occurs because the average current at the primary side will increase with respect to the duty cycle. A better relationship would be to use the voltage inductor law,

$$V_{Ll} = L_l \frac{di}{dt} \quad (29)$$

which can be converted to discrete time,

$$V_{Ll} = L_l \frac{\Delta I_p}{T_s} \quad (30)$$

It is assumed that the power is conserved across transformer,

$$V_p I_p = V_s I_s \quad (31)$$

therefore the change in current at the primary side is estimated by considering the voltage ripple.

$$\Delta I_p = \frac{V_s}{V_p} \cdot \frac{\Delta V_o}{R_L} \quad (32)$$

Therefore, the average voltage drop across the leakage inductance can be calculated from the inductor relationship, 30. Then, $V_{Ll} = 3.27 \text{ mV}$ for $V_d = 5 \text{ V}$ and $V_{Ll} = 1.36 \text{ mV}$ for $V_d = 12 \text{ V}$. The transformer current rule can also be used to adjust the voltage drop across the primary side internal resistance. This would more accurately reflect the power losses due to the transformer as the calculations will be using the primary side current to determine voltage drops.

References

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