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Majority Vote

November 13, 2024

Project: Majority Vote Design Brief

Client:	Board of Directors
Designer:	Liam West
Problem Statement:	At the heart of the controversy was using antiquated and unreliable paper ballots. The use of these paper ballots resulted in an unacceptable amount of overvotes and undervotes. An overvote occurs when someone's vote is counted more than once, and an undervote occurs when someone's vote is not counted at all.
Design Statement:	To ensure that this type of controversy does not occur at your company, the board of directors has asked you to design an electronic voting machine. The voting machine will allow the four board members to cast their ballots and will display the pass/fail status of each of their decisions.
Constraints:	• In this project, you will use only 2-input AND, 2-input OR, 2-input NAND, 2-input NOR, and Inverter logic gates to design, simulate, and build a Majority Vote voting machine that meets these design specifications. • Four members: president (P), vice-president (V), secretary (S), and treasurer (T). Each member has a single yes(1)/no(0) vote. • For a decision (D) to pass (1), a majority of the board members must vote yes. • In the event of a tie, the president's vote is used to break the tie (if the president votes yes, the decision passes; If the president votes no, the decision fails).

Deliverables:	The Google Doc should include documentation of the following items: ● Design brief ● Definition of this circuit's inputs/outputs ● Truth table ● Unsimplified logic expression ● Karnaugh map ● Steps of Boolean algebra ● Simplified logic expression ● Simplified AOI circuit implementation (Multisim) ● NAND circuit implementation (Multisim) ● NOR circuit implementation (Multisim) ● Photo of breadboard prototype

Project Overview

We need to create a ballot system for four users, one with a higher weighted vote than the others.

P	V	S	T	D
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Truth Table:

The truth table considers the president's vote to be used as a tiebreaker.

Unsimplified Logic Expression:

$$\overline{P}VST + P\overline{V}\,\overline{S}T + P\overline{V}S\overline{T} + P\overline{V}ST + PV\overline{S}\,\overline{T} + PV\overline{S}T + PVS\overline{T} + PVST$$

Karnough Mapping:

	S'T'	S'T	ST	ST'
P'V'	0	0	0	0
P'V	0	0	1	0
PV	1	1	1	1
PV'	0	1	1	1

We use the Karnough Method to simplify our logic expressions.

New Logic Expressions:

PT+SP+PV+STV

Boolean Simplification:

We use Boolean Algebra to simplify it down to our most simple expression.

1. Fd = $F_D = \bar{P}VST + P\bar{V}\,\bar{S}T + P\bar{V}S\bar{T} + P\bar{V}ST + PV\bar{S}\,\bar{T} + PV\bar{S}T + PVS\bar{T} + PVST$
2. $F_D = VST(\bar{P} + P) + P\bar{V}\,\bar{S}T + P\bar{V}S\bar{T} + P\bar{V}ST + PV\bar{S}\,\bar{T} + PV\bar{S}T + PVS\bar{T}$
3. $F_D = VST(1) + P\bar{V}\,\bar{S}T + P\bar{V}S\bar{T} + P\bar{V}ST + PV\bar{S}\,\bar{T} + PV\bar{S}T + PVS\bar{T}$
4. $F_D = VST + P\bar{V}T(\bar{S} + S) + P\bar{V}S\bar{T} + PV\bar{S}\,\bar{T} + PV\bar{S}T + PVS\bar{T}$
5. $F_D = VST + P\bar{V}(S\bar{T} + T) + PV\bar{S}\,\bar{T} + PV\bar{S}T + PVS\bar{T}$
6. $F_D = VST + P\bar{V}(S + T) + PV\bar{S}\,(\bar{T} + T) + PVS\bar{T}$
7. $F_D = VST + P\bar{V}(S + T) + PV\bar{S} + PVS\bar{T}$
8. $F_D = P\bar{V}(S + T) + PV\bar{S} + VS(P\bar{T} + T)$
9. $F_D = P\bar{V}(S + T) + PV\bar{S} + VS(P + T)$
10. $F_D = P\bar{V}S + P\bar{V}T + PV\bar{S} + VSP + VST)$
11. $F_D = PS(\bar{V} + V) + P\bar{V}T + PV\bar{S} + VST)$
12. $F_D = P\bar{V}T + P(V\bar{S} + S) + VST)$
13. $F_D = P\bar{V}T + PV + PS + VST)$
14. $F_D = P\bar{V}T + PV + PS + VST)$
15. $F_D = P(\bar{V}T + V) + PS + VST)$
16. $F_D = P(T + V) + PS + VST)$
17. $F_D = PT + PV + PS + VST$