University of Illinois at Urbana-Champaign Dept. of Electrical and Computer Engineering

ECE 120: Introduction to Computing

Counting to Ten (LC-3 Style!)

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What is an Instruction Set Architecture (ISA)?

An ISA answers three questions:

- 1. What operations are possible with instructions?
- 2. On what operands can each operation be performed?
- 3. What bits/representation is used to encode instructions?

The answers to these questions define the ISA.

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We Discussed Five Aspects of the LC-3 ISA

- 1. opcodes: AND, AND, NOT LD/ST, LDI/STI, LDR/STR, LEA BR, JMP, TRAP
- 2. data types: 2's complement (only)
- 3. addressing modes: register, immediate, PC-relative, indirect, base+offset
- 4. condition codes: negative, zero, positive
- 5. encoding: see P&P p. 119, back of P&P, or LC-3 handout

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Let's Count to Ten Together (Using LC-3)

Let's do something exciting with LC-3.

Let's count to 10!

The handout has three versions:

- PC-relative addressing (LD/ST),
- indirect addressing (LDI/STI), and
- base+offset addressing (LDR/STR).

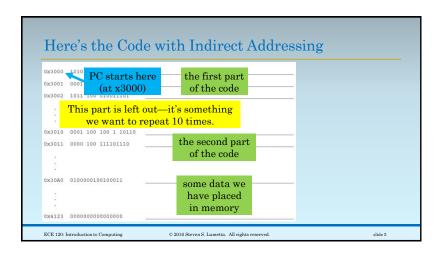
Let's do the **indirect** addressing version together.

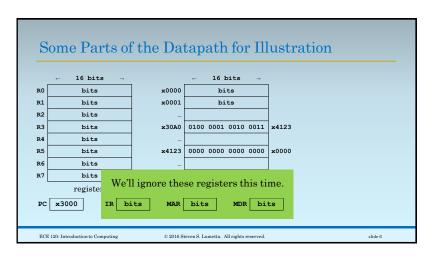
Do the others on your own.

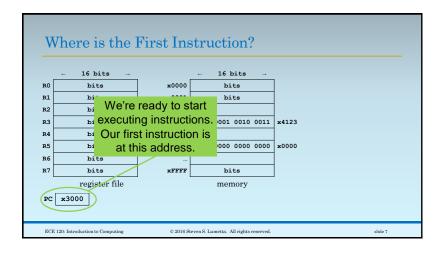
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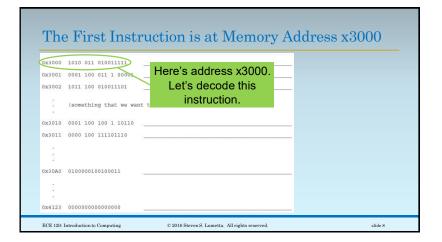
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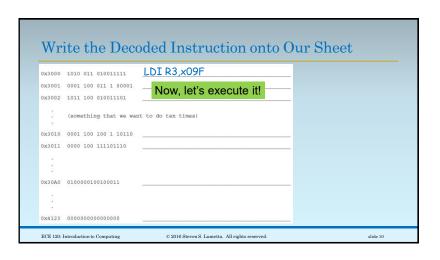




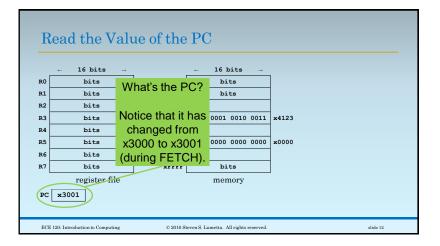


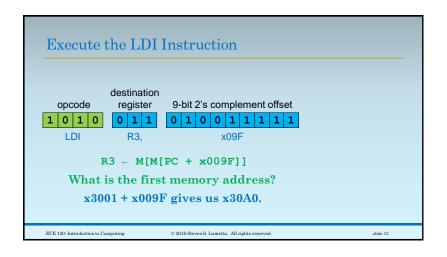


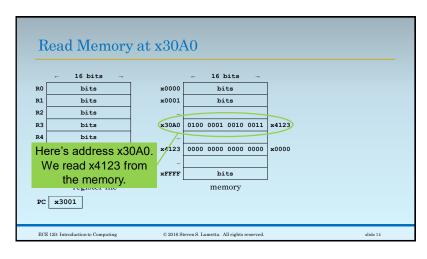
Decode the Instruction at $x300$ opcode register 9-bit 2's complement of the second	nent offset
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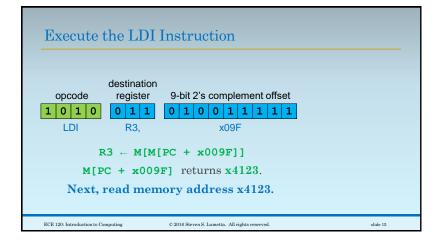


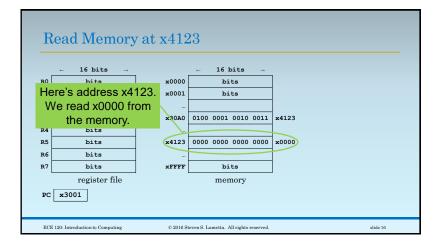
Execute the LDI Instruction opcode register 9-bit 2's complement offset	
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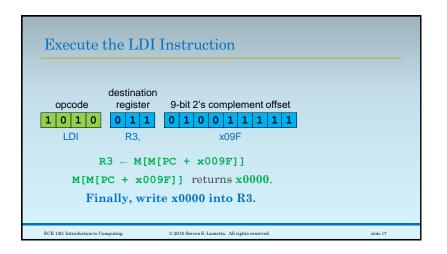


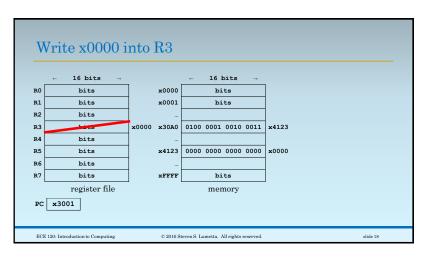


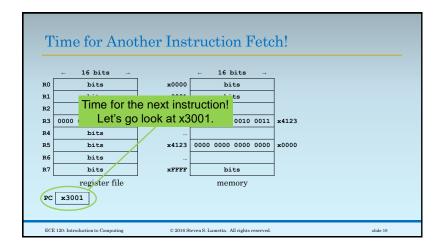


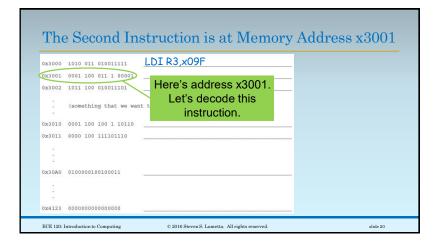






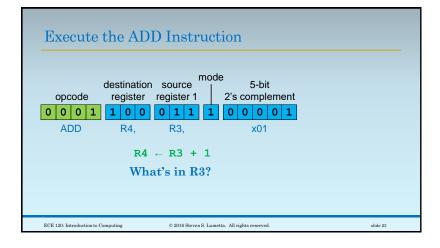


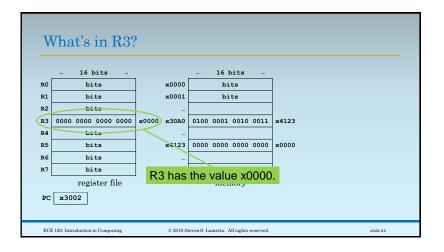


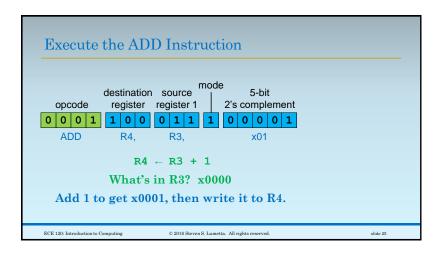


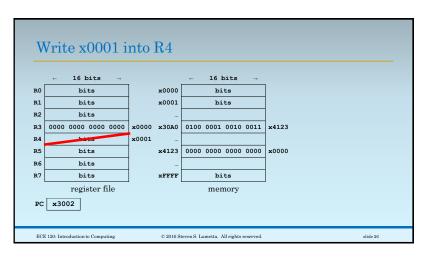
Decode the Instruction at x3001 destination source mode				
ADD R4, R3, \times 01 $\mathbf{R4} \leftarrow \mathbf{R3} + 1$				
ECE 120: Introduction to Computing	$\ensuremath{\mathbb{C}}$ 2016 Steven S. Lumetta. All rights reserved.	slide 21		

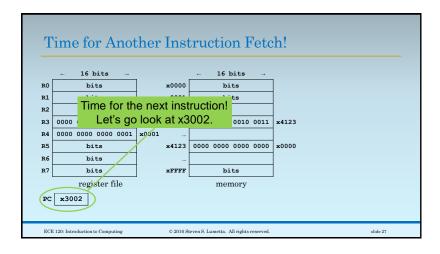
Wr	ite the Deco	oded Instruction onto C	our Sheet
**1.			
0x3000	1010 011 010011111	LDI R3,x09F	
0x3001	0001 100 011 1 00001	ADD R4,R3,x01	
0x3002	1011 100 010011101	Now, let's execute it!	
	(something that we wan	t to do ten times)	
0x3010	0001 100 100 1 10110	<u></u>	
0x3011	0000 100 111101110		
0x30A0	0100000100100011		
1			
0x4123	000000000000000		
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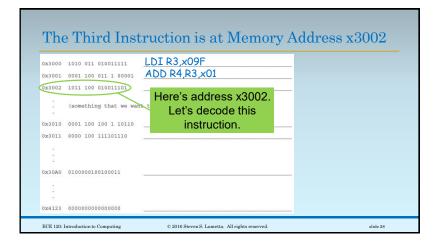


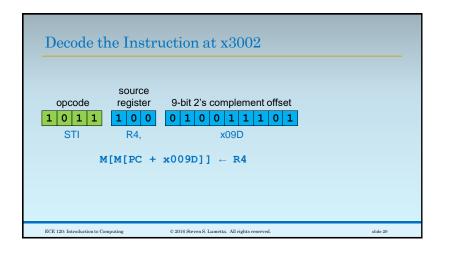


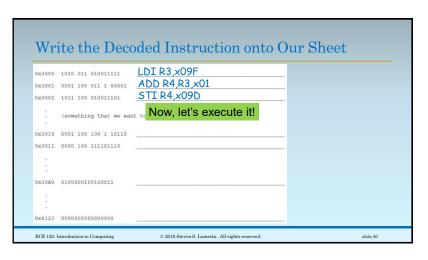


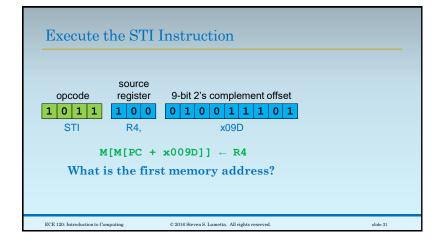


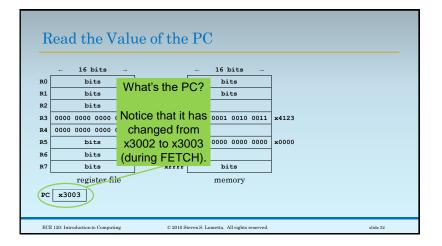


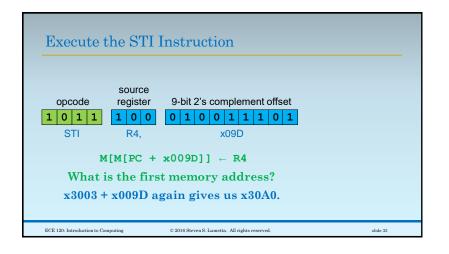


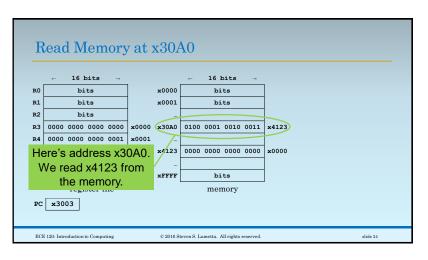


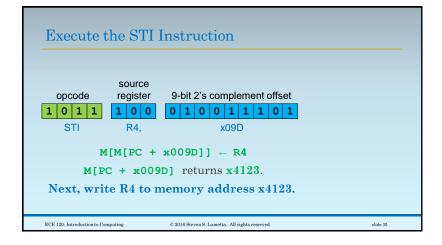


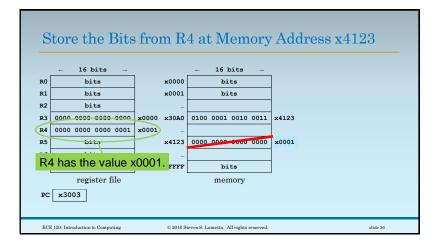


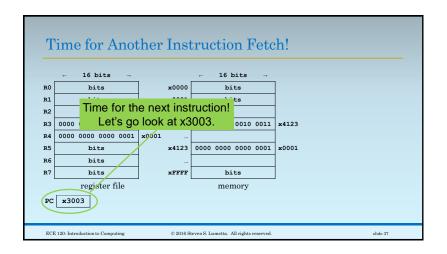


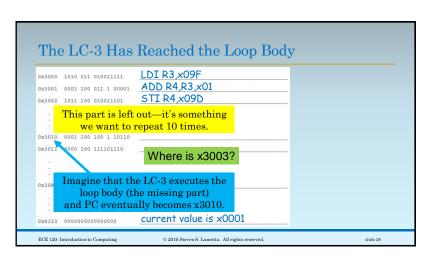


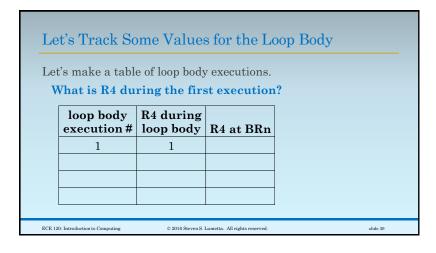


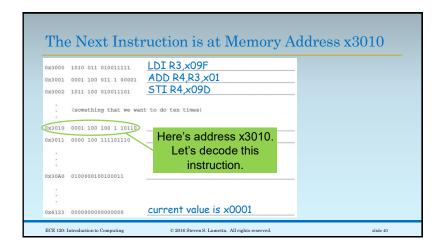


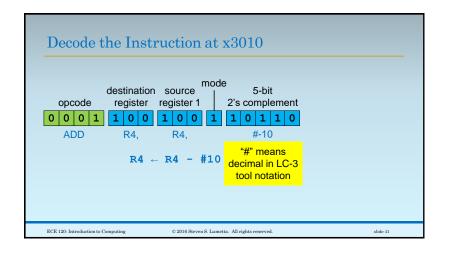


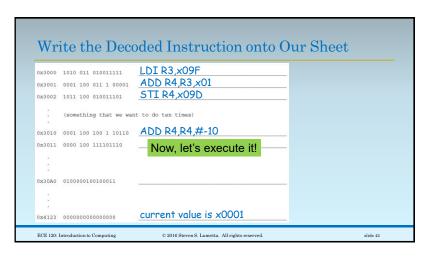


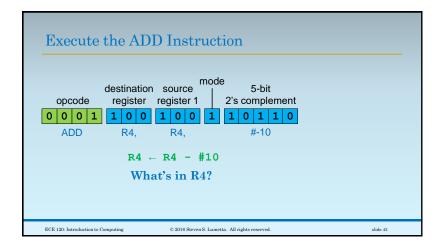


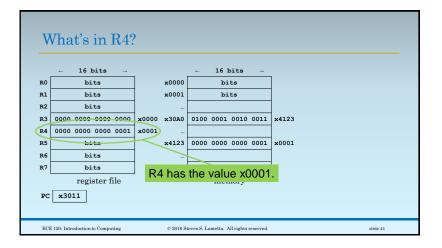


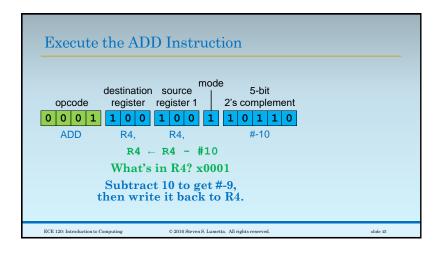


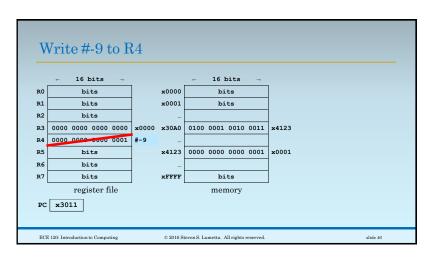


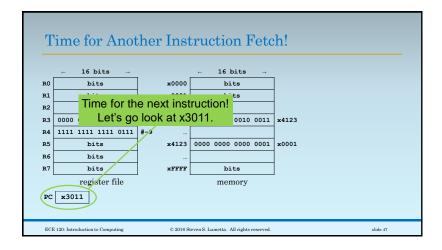


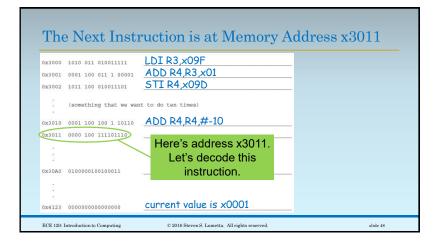


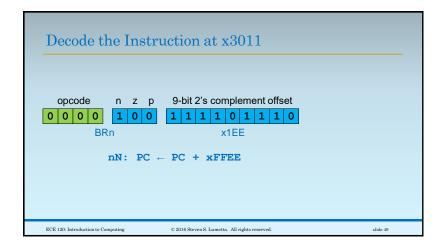


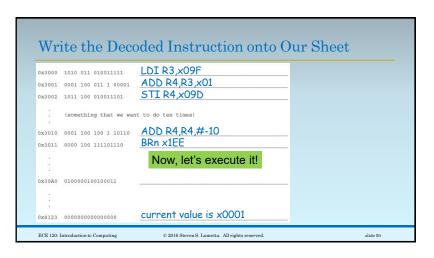


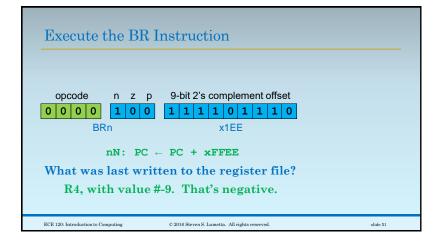


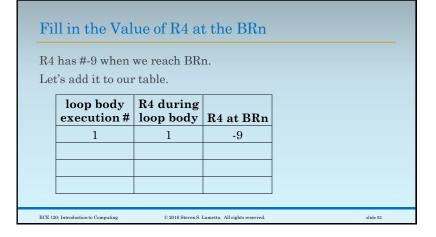


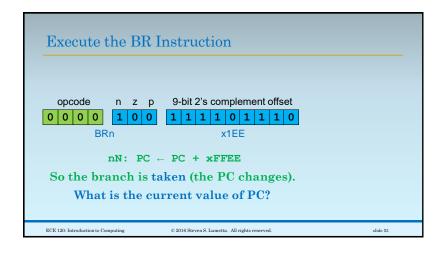


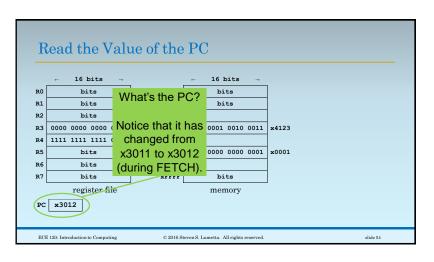


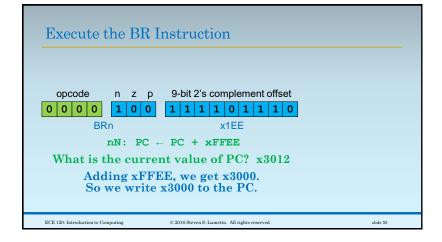


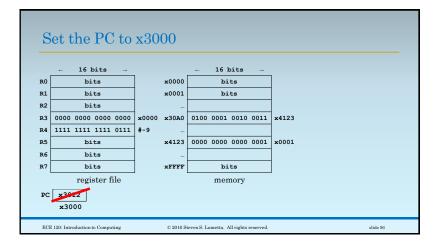


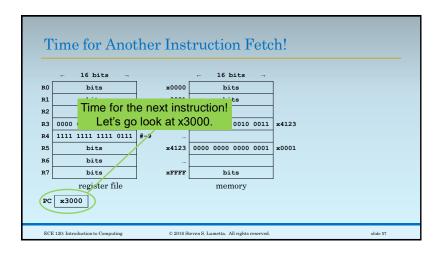


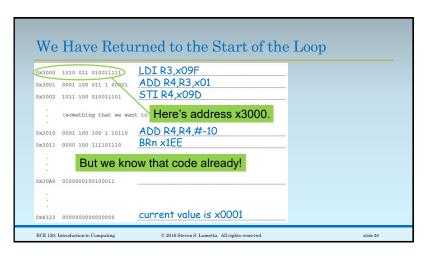












The PC-Relative Addresses Do Not Change Here is the RTL for the first three instructions. **3000 R3 - M[M[PC + **x009F]] **3001 R4 - R3 + 1 **3002 M[M[PC + **x009D]] - R4 Since the values of PC • depend on the instruction addresses, • the same calculations are performed • each time this code executes.

```
Assume that Nothing Changed Address x30A0

Thus, we can simplify the RTL slightly.

x3000 R3 - M[M[x30A0]]

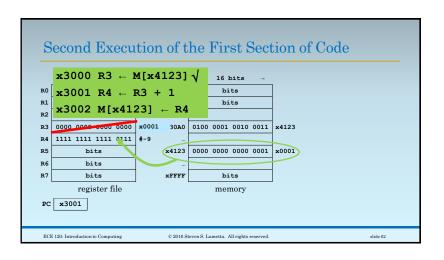
x3001 R4 - R3 + 1

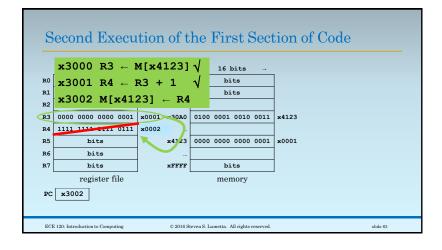
x3002 M[M[x30A0]] - R4

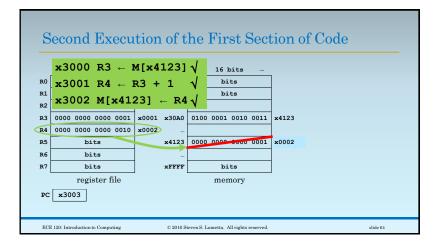
Let's assume that the bits stored at memory address x30A0 have not changed.

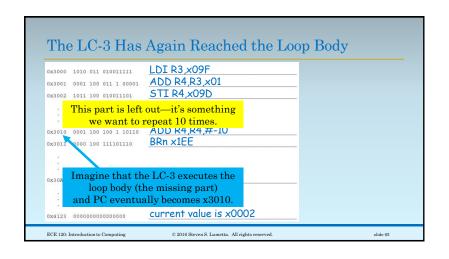
So we can also simplify by replacing M[x30A0] with x4123 in both LDI and STI.
```

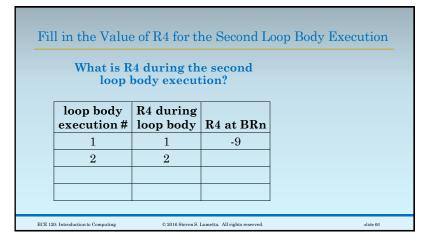
Ready to Execute the RTL on the Datapath Simplifying the RTL again, we obtain: x3000 R3 - M[x4123] x3001 R4 - R3 + 1 x3002 M[x4123] - R4 Let's go execute these three instructions on the datapath now.











The PC-Relative Addresses Do Not Change

Here is the RTL for the code after the loop body.

 $x3010 R4 \leftarrow R4 - #10$

x3011 nN: PC \leftarrow PC + xFFEE

Again, the value of PC (on the right)

- $^{\circ}\,\text{depends}$ on the instruction address, so
- \circ the same calculation is performed
- each time this code executes.

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Ready to Execute the RTL on the Datapath

Thus, we can simplify the RTL slightly.

x3010 R4 ← R4 - #10 x3011 nN: PC ← x3000

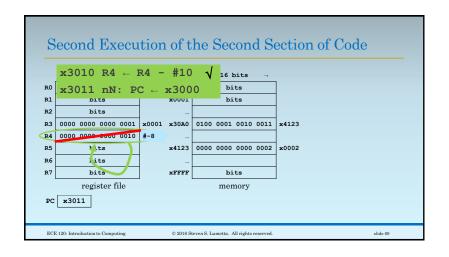
Let's go execute these two instru

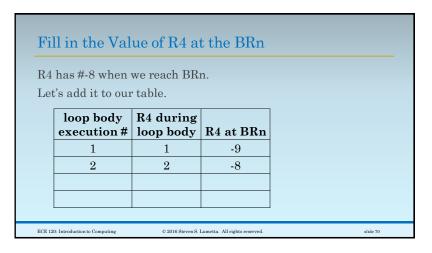
Let's go execute these two instructions on the datapath now.

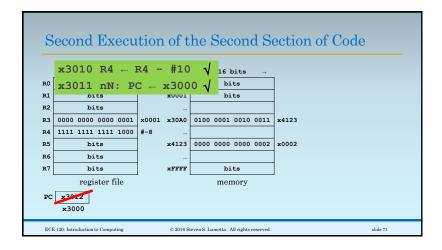
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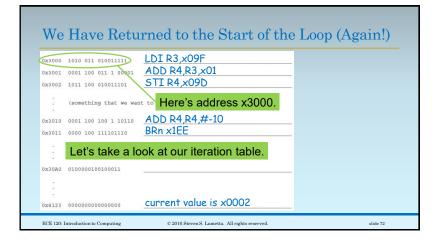
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Let's Generalize Our Table Values

R4 counts up with the loop body execution #.

When does R4 get to 0 (non-negative)?

loop body execution #		R4 at BRn
1	1	-9
2	2	-8
10	10	0

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The Loop Ends After Ten Iterations

In other words,

- after the tenth loop body iteration
- the branch is not taken,
- and the PC remains x3012.

Guess what the LC-3 does.

Executes another instruction!

But we're going to stop.

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Some Questions for You

- 1. Why is there a 0 stored at x4123?
- 2. How many times does the loop body execute if we start M[x4123] at 5?
- 3. How many times does the loop body execute if we start M[x4123] at -5?
- 4. How many times does the loop body execute if we start M[x4123] at 25?

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More Questions for You

- 5. What if we leave M[x4123] as "bits" (set no value there)?
- 6. What happens if we change the value at x30A0 to x3141?
- 7. What happens if the loop body sets R4 to 0?

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```
A Reference Copy of the Code
                           LDI R3,x09F
0x3000 1010 011 010011111
0x3001 0001 100 011 1 00001 ADD R4,R3,x01
                           STI R4,x09D
0x3002 1011 100 010011101
       (something that we want to do ten times)
0x3010 0001 100 100 1 10110 ADD R4,R4,#-10
                           BRn x1EE
0x3011 0000 100 111101110
                           x4123 (data)
0x30A0 0100000100100011
                           x0000 (data)
0x4123 0000000000000000
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```