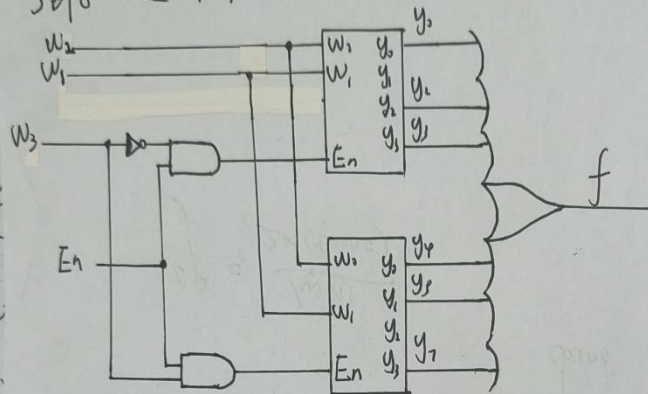


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4.1

解:

3到8=进制译码器的 $y_0, y_1, y_2, y_3, y_4, y_5, y_6, y_7$ 恰好为真时, w_1, w_2, w_3 符合要求



4.5 解: $f(w_1, w_2, w_3) = \sum m(0, 2, 3, 6)$

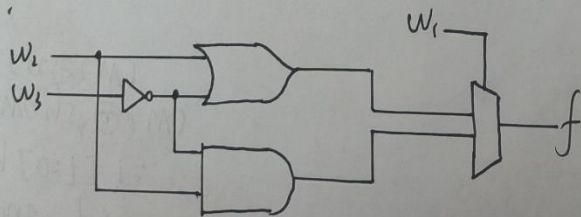
$$= \bar{w}_1 \bar{w}_2 \bar{w}_3 + \bar{w}_1 w_2 \bar{w}_3 + \bar{w}_1 w_2 w_3 + w_1 w_2 \bar{w}_3$$

$$= \bar{w}_1 f w_1 + w_1 f w_1$$

$$= \bar{w}_1 (\bar{w}_2 \bar{w}_3 + w_2 \bar{w}_3 + w_2 w_3) + w_1 w_2 \bar{w}_3$$

$$= \bar{w}_1 (\bar{w}_3 + w_3) + w_1 w_2 \bar{w}_3$$

电路:



4.19 解: 与 4.11 同理

Verilog 代码:

```
module dec3to8andm(w1,w2,w3,f)
```

```
input w1,w2,w3;
```

```
output f;
```

```
reg [0:7] Y;
```

```
always@(w1,w2,w3)
```

```
begin
```

```
Y=8'b00000000;
```

```
case({w1,w2,w3})
```

```
0: Y[0]=1;
```

```
1: Y[1]=1;
```

```
2: Y[2]=1;
```

```
3: Y[3]=1;
```

```
4: Y[4]=1;
```

```
5: Y[5]=1;
```

```
6: Y[6]=1;
```

```
7: Y[7]=1;
```

```
default: Y=8'b00000000;
```

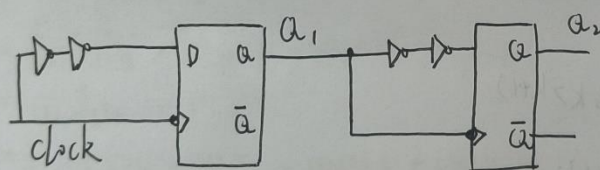
```
endcase
```

```
end
```

```
assign f=Y[1]||Y[2]||Y[3]||Y[5]||Y[6];
```

```
endmodule
```

5.4



clock

D

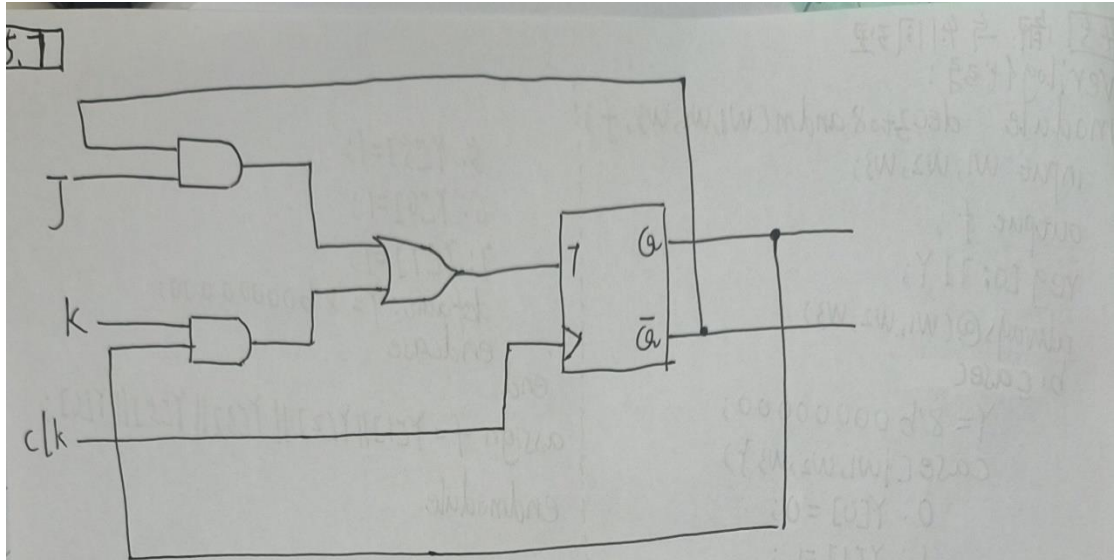
Q₁

Q₂

100 Hz

50 Hz

25 Hz



5.13

module shiftn (D, a, f, Load, clk)

input clk;

input [n-1:0] D; [n-1:0] a; [1:0] Load;

output reg [n-1:0] a;

integer k;

always @ (posedge clk)

begin

if (Load == 2'b00)

begin for (k=0; k<n-1; k=k+1)

begin

a[k] <= a[k+1];

a[n-1] <= D;

end

end if (Load == 2'b01)

begin

for (k=n-1; k>0; k=k-1)

begin

a[k] <= a[k+1];

a[n] <= D;

end

else if (Load == 2'b10)

a <= D;

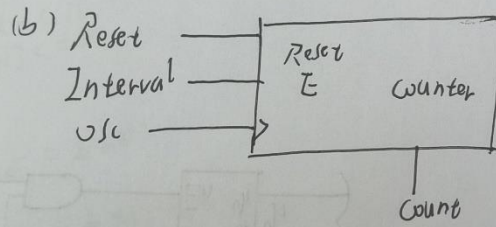
end

endmodule

2)

L
n

(5.24) (a) $f = \frac{1}{2^n \times t_p}$



$$t_p = \frac{100\text{ ns}}{2^n(\text{Count})}$$