Appendix B

B.1. (a)

x_1	x_2	x_3	f
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

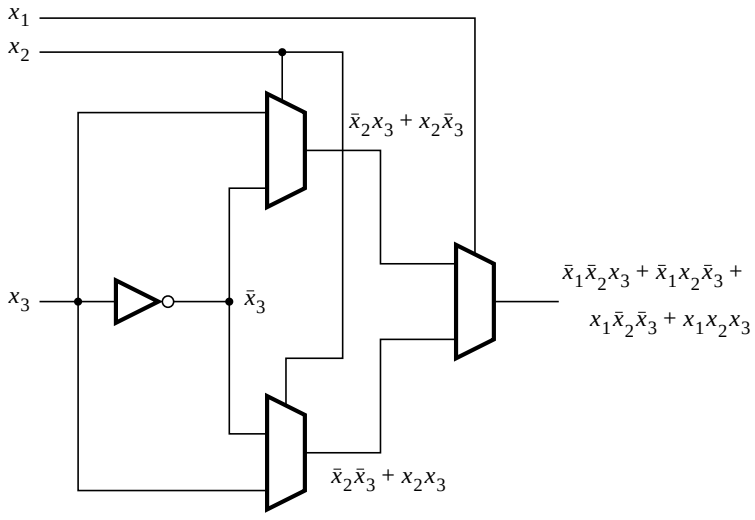
(b)

$$\begin{aligned} \#\text{transistors} &= \text{NOT\_gates} \times 2 + \text{AND\_gates} \times 8 + \text{OR\_gates} \\ &= 3 \times 2 + 4 \times 8 + 1 \times 10 = 48 \end{aligned}$$

B.2. (a) In problem B.1 the canonical SOP for f is

$$f = \overline{x}_1\overline{x}_2x_3 + \overline{x}_1x_2\overline{x}_3 + x_1\overline{x}_2\overline{x}_3 + x_1x_2x_3$$

This expression is equivalent to f in Figure PB.2, as derived below.



(b) Assuming the multiplexers are implemented using transmission gates

$$\begin{aligned} \#\text{transistors} &= \text{NOT\_gates} \times 2 + \text{MUXes} \times 6 \\ &= 1 \times 2 + 3 \times 6 = 20 \end{aligned}$$

B.3. (a) A SOP expression for f in Figure PB.3 is:

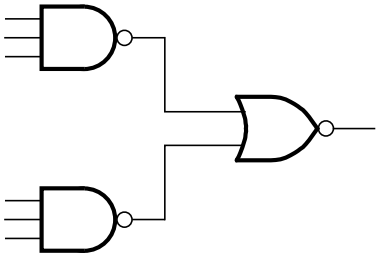
$$\begin{aligned} f &= (x_1 \oplus x_2) \oplus x_3 \\ &= (x_1 \oplus x_2)\overline{x}_3 + \overline{(x_1 \oplus x_2)}x_3 \\ &= x_1\overline{x}_2\overline{x}_3 + \overline{x}_1x_2\overline{x}_3 + \overline{x}_1\overline{x}_2x_3 + x_1x_2x_3 \end{aligned}$$

which is equivalent to the expression derived in problem B.2.

(b) Assuming the XOR gates are implemented as shown in Figure B.61b

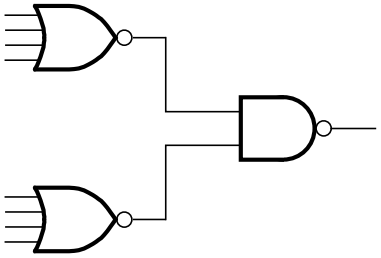
$$\begin{aligned} \#\text{transistors} &= \text{XOR\_gates} \times 8 \\ &= 2 \times 8 = 16 \end{aligned}$$

B.4. Using the circuit



The number of transistors needed is 16.

B.5. Using the circuit



The number of transistors needed is 20.

B.6. (a)

x_1	x_2	x_3	f
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

(*b*) The canonical SOP expression is

$$f = \overline{x}_1\overline{x}_2\overline{x}_3 + \overline{x}_1\overline{x}_2x_3 + \overline{x}_1x_2\overline{x}_3 + \overline{x}_1x_2x_3 + x_1\overline{x}_2\overline{x}_3$$

The number of transistors required using only AND, OR, and NOT gates is

$$\begin{aligned} \#\text{transistors} &= \text{NOT\_gates} \times 2 + \text{AND\_gates} \times 8 + \text{OR\_gates} \times 12 \\ &= 3 \times 2 + 5 \times 8 + 1 \times 12 = 58 \end{aligned}$$

B.7. (*a*)

x_1	x_2	x_3	x_4	f
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0

x_1	x_2	x_3	x_4	f
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

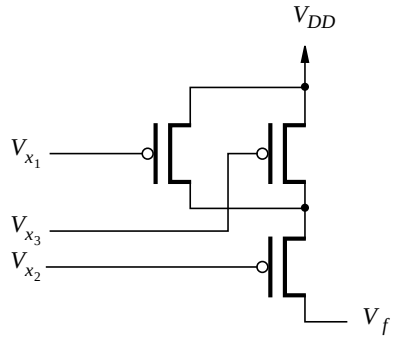
(*b*)

$$\begin{aligned} f &= \overline{x}_1\overline{x}_2\overline{x}_3\overline{x}_4 + \overline{x}_1x_2\overline{x}_3\overline{x}_4 + x_1\overline{x}_2\overline{x}_3\overline{x}_4 \\ &= \overline{x}_1\overline{x}_3\overline{x}_4 + \overline{x}_2\overline{x}_3\overline{x}_4 \end{aligned}$$

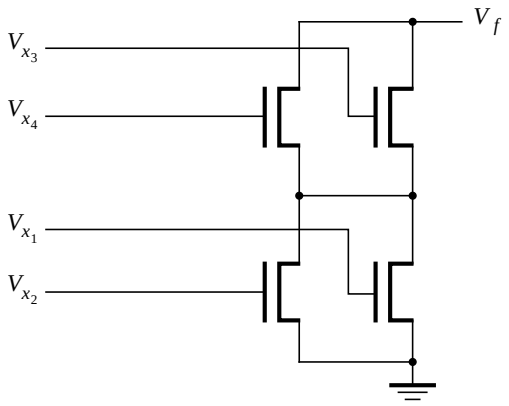
The number of transistors required using only AND, OR, and NOT gates is

$$\begin{aligned} \#\text{transistors} &= \text{NOT\_gates} \times 2 + \text{AND\_gates} \times 8 + \text{OR\_gates} \times 4 \\ &= 4 \times 2 + 2 \times 8 + 1 \times 4 = 28 \end{aligned}$$

B.8.



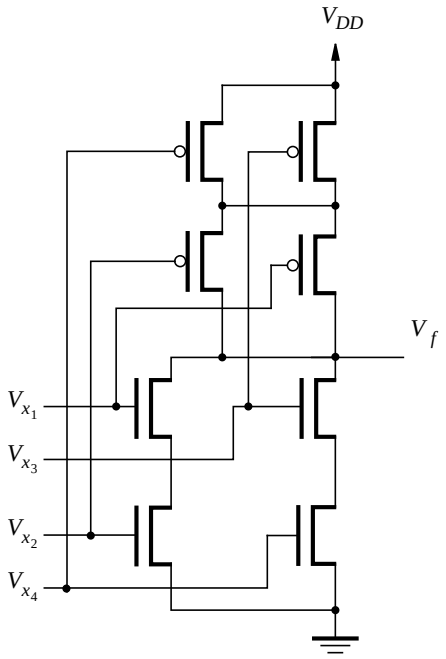
B.9.



B.10. Minimum SOP expression for f is

$$\begin{aligned} f &= \overline{x}_2\overline{x}_3 + \overline{x}_1\overline{x}_3 + \overline{x}_2\overline{x}_4 + \overline{x}_1\overline{x}_4 \\ &= (\overline{x}_1 + \overline{x}_2)(\overline{x}_3 + \overline{x}_4) \end{aligned}$$

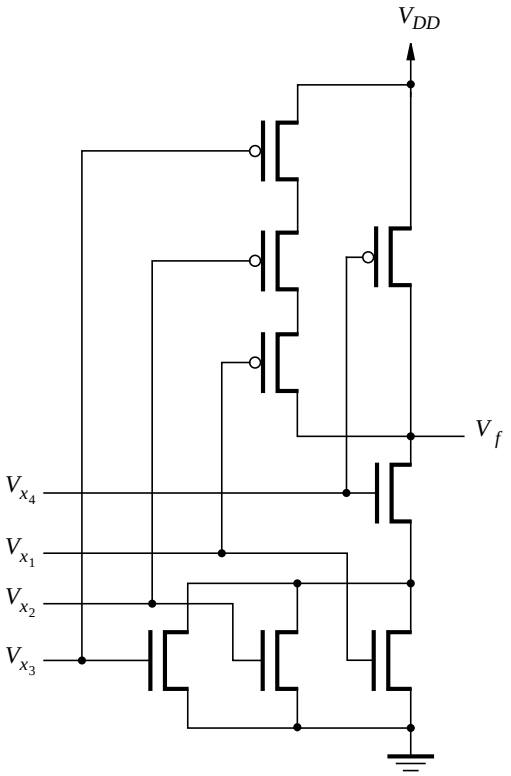
which leads to the circuit



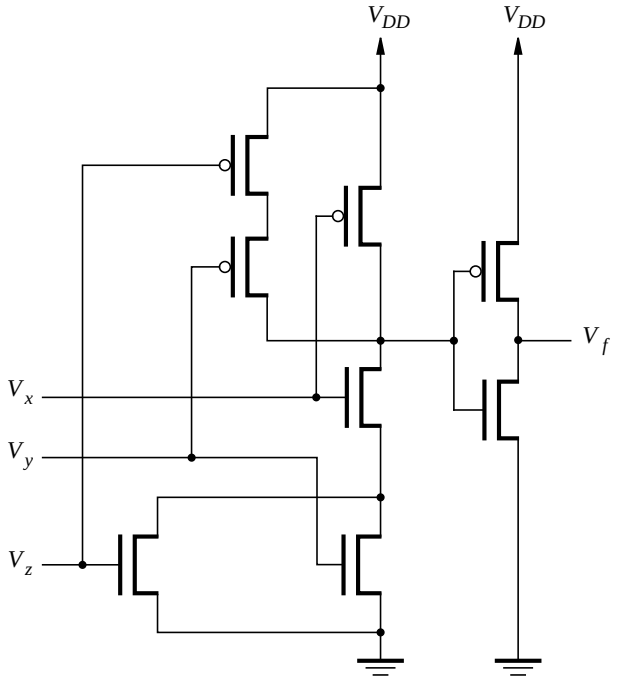
B.11. Minimum SOP expression for f is

$$f = \overline{x}_4 + \overline{x}_1\overline{x}_2\overline{x}_3$$

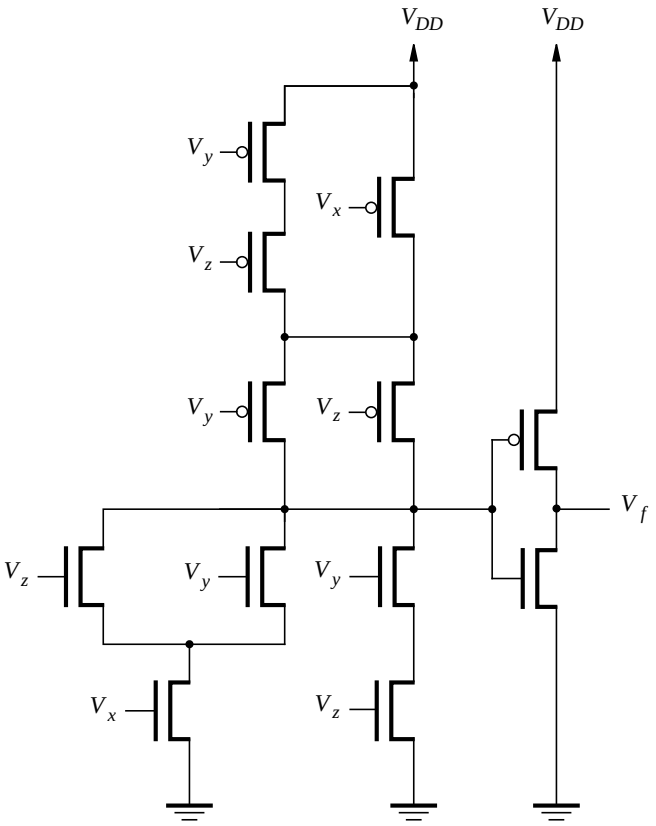
which leads to the circuit



B.12.



B.13.



B.14. (a) Since $V_{DS} \geq V_{GS} - V_T$ the NMOS transistor is operating in the saturation region:

$$\begin{aligned} I_D &= \frac{1}{2}k'_n\frac{W}{L}(V_{GS}-V_T)^2 \\ &= 10\,\frac{\mu\text{A}}{\text{V}^2}\times 5\times(5\text{ V}-1\text{ V})^2 = 800\,\mu\text{A} \end{aligned}$$

(b) In this case $V_{DS} < V_{GS} - V_T$, thus the NMOS transistor is operating in the triode region:

$$\begin{aligned} I_D &= k'_n\frac{W}{L}\left[(V_{GS}-V_T)V_{DS}-\frac{1}{2}V_{DS}^2\right] \\ &= 20\,\frac{\mu\text{A}}{\text{V}^2}\times 5\times\left[(5\text{ V}-1\text{ V})\times 0.2\text{ V}-\frac{1}{2}\times(0.2\text{ V})^2\right] = 78\,\mu\text{A} \end{aligned}$$

B.15. (a) Since $V_{DS} \leq V_{GS} - V_T$ the PMOS transistor is operating in the saturation region:

$$\begin{aligned} I_D &= \frac{1}{2}k'_p\frac{W}{L}(V_{GS}-V_T)^2 \\ &= 5\,\frac{\mu\text{A}}{\text{V}^2}\times 5\times(-5\text{ V}+1\text{ V})^2 = 400\,\mu\text{A} \end{aligned}$$

(b) In this case $V_{DS} > V_{GS} - V_T$, thus the PMOS transistor is operating in the triode region:

$$\begin{aligned} I_D &= k'_p\frac{W}{L}\left[(V_{GS}-V_T)V_{DS}-\frac{1}{2}V_{DS}^2\right] \\ &= 10\,\frac{\mu\text{A}}{\text{V}^2}\times 5\times\left[(-5\text{ V}+1\text{ V})\times(-0.2)\text{ V}-\frac{1}{2}\times(-0.2\text{ V})^2\right] = 39\,\mu\text{A} \end{aligned}$$

B.16.

$$\begin{aligned} R_{DS} &= 1/\left[k_n' \frac{W}{L}(V_{GS} - V_T)\right] \\ &= 1/\left[0.020\,\frac{\text{mA}}{\text{V}^2} \times 10 \times (5\text{ V} - 1\text{ V})\right] = 1.25\,\text{k}\Omega \end{aligned}$$

B.17.

$$\begin{aligned} R_{DS} &= 1/\left[k_n' \frac{W}{L}(V_{GS} - V_T)\right] \\ &= 1/\left[0.040\,\frac{\text{mA}}{\text{V}^2} \times 10 \times (3.3\text{ V} - 0.66\text{ V})\right] = 947\,\Omega \end{aligned}$$

B.18. Since $V_{DS} < (V_{GS} - V_T)$, the PMOS transistor is operating in the saturation region:

$$\begin{aligned} I_{SD} &= \frac{1}{2}k_p' \frac{W}{L}(V_{GS} - V_T)^2 \\ &= 50\,\frac{\mu\text{A}}{\text{V}^2} \times (-5\text{ V} + 1\text{ V})^2 = 800\,\mu\text{A} \end{aligned}$$

Hence the value of R_{DS} is

$$\begin{aligned} R_{DS} &= V_{DS}/I_{DS} \\ &= 4.8\text{ V}/800\,\mu\text{A} = 6\,\text{k}\Omega \end{aligned}$$

B.19. Since $V_{DS} < (V_{GS} - V_T)$, the PMOS transistor is operating in the saturation region:

$$\begin{aligned} I_{SD} &= \frac{1}{2}k_p' \frac{W}{L}(V_{GS} - V_T)^2 \\ &= 80\,\frac{\mu\text{A}}{\text{V}^2} \times (-3.3\text{ V} + 0.66\text{ V})^2 = 558\,\mu\text{A} \end{aligned}$$

Hence the value of R_{DS} is

$$\begin{aligned} R_{DS} &= V_{DS}/I_{DS} \\ &= 3.2\text{ V}/558\,\mu\text{A} = 5.7\,\text{k}\Omega \end{aligned}$$

B.20. The high output voltage of the pseudo-PMOS inverter can be obtained by setting $V_x = 0$ and evaluating the voltage V_f. First we assume that the PMOS transistor is operating in the triode region while the NMOS is operating in the saturation region. For simplicity we will assume that the magnitude of the threshold voltages for both the NMOS and PMOS transistors are equal, so that

$$V_T = V_{TN} = -V_{TP}$$

The current flowing through the NMOS transistor is

$$\begin{aligned} I_D &= \frac{1}{2}k_n' \frac{W_n}{L_n}(V_{GS} - V_{TN})^2 \\ &= \frac{1}{2}k_n(V_{DD} - V_{TN})^2 \\ &= \frac{1}{2}k_n(V_{DD} - V_T)^2 \end{aligned}$$

Similarly, the current going through the PMOS transistor is

$$\begin{aligned} I_D &= k_p' \frac{W_p}{L_p} \left[(V_{GS} - V_{TP}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \\ &= k_p' \frac{W_p}{L_p} \left[((V_x - V_{DD}) - V_{TP})(V_f - V_{DD}) - \frac{1}{2}(V_f - V_{DD})^2 \right] \\ &= k_p \left[((V_x - V_{DD}) - V_{TP})(V_f - V_{DD}) - \frac{1}{2}(V_f - V_{DD})^2 \right] \\ &= k_p \left[(-V_{DD} + V_T)(V_f - V_{DD}) - \frac{1}{2}(V_f - V_{DD})^2 \right] \end{aligned}$$

Since there is only one path for current to flow, we can equate the currents flowing through the NMOS and PMOS transistors and solve for the voltage V_f.

$$k_n (V_{DD} - V_T)^2 = 2k_p \left[(-V_{DD} + V_T)(V_f - V_{DD}) - \frac{1}{2}(V_f - V_{DD})^2 \right]$$

$$k_n (V_{DD} - V_T)^2 - 2k_p (-V_{DD} + V_T)(V_f - V_{DD}) + k_p (V_f - V_{DD})^2 = 0$$

This quadratic equation can be solved by using the standard formula, with the parameters

$$a = k_p,\ b = -2k_p(-V_{DD} + V_T),\ c = k_n (V_{DD} - V_T)^2$$

which gives

$$\begin{aligned} (V_f - V_{DD}) &= \frac{-b}{2a} \pm \sqrt{\frac{b^2}{4a^2} - \frac{c}{a}} \\ &= (-V_{DD} + V_T) \pm \sqrt{(-V_{DD} + V_T)^2 - \frac{k_n}{k_p}(-V_{DD} + V_T)^2} \\ &= (-V_{DD} + V_T) \left[1 \pm \sqrt{1 - \frac{k_n}{k_p}} \right] \end{aligned}$$

Only one of these two solutions is valid, because we started with the assumption that the PMOS transistor is in the triode region while the NMOS is in the saturation region. Thus

$$V_f = V_{DD} - (V_{DD} - V_T) \left[1 - \sqrt{1 - \frac{k_n}{k_p}} \right]$$

B.21. (a)

$$\begin{aligned} I_{stat} &= \frac{1}{2} k_n' \frac{W_n}{L_n} (V_{DD} - V_T)^2 \\ &= 30 \, \frac{\mu\text{A}}{\text{V}^2} \times 1 \times (5\ \text{V} - 1\ \text{V})^2 = 480\, \mu\text{A} \end{aligned}$$

(b)

$$\begin{aligned} R_{DS} &= 1 / \left[k_p' \frac{W_p}{L_p} (V_{GS} - V_T) \right] \\ &= 1 / \left[0.024 \, \frac{\text{mA}}{\text{V}^2} \times 8 \times (5\ \text{V} - 1\ \text{V}) \right] = 768\Omega \end{aligned}$$

(c) Using the expression derived in problem B.20

$$k_p = k'_p \frac{W_p}{L_p} = 192\ \frac{\mu\text{A}}{\text{V}^2}$$
$$k_n = k'_n \frac{W_n}{L_n} = 60\ \frac{\mu\text{A}}{\text{V}^2}$$

$$\begin{aligned} V_{OH} = V_f &= 5\text{ V} - (5\text{ V} - 1\text{ V})\left[1 - \sqrt{1 - \frac{60}{192}}\right] \\ &= 4.3\text{ V} \end{aligned}$$

(d)

$$\begin{aligned} P_D &= I_{stat} V_{DD} \\ &= 480\,\mu\text{A} \times 5\text{ V} = 2.4\,\text{mW} \end{aligned}$$

(e)

$$\begin{aligned} R_{DSN} &= V_{DS}/I_{DS} \\ &= (V_f)/I_{stat} \\ &= (4.3\text{ V})/0.48\,\text{mA} = 9\,\text{k}\Omega \end{aligned}$$

(f) The low-to-high propagation delay is

$$\begin{aligned} t_{p_{LH}} &= \frac{1.7C}{k'_p \frac{W_p}{L_p} V_{DD}} \\ &= \frac{1.7 \times 70\,\text{fF}}{24\ \frac{\mu\text{A}}{\text{V}^2} \times 8 \times 5\text{ V}} = 0.1\,\text{ns} \end{aligned}$$

The high-to-low propagation delay is

$$\begin{aligned} t_{p_{HL}} &= \frac{1.7C}{k'_n \frac{W_n}{L_n} V_{DD}} \\ &= \frac{1.7 \times 70\,\text{fF}}{60\ \frac{\mu\text{A}}{\text{V}^2} \times 1 \times 5\text{ V}} = 0.4\,\text{ns} \end{aligned}$$

B.22. Using the parameters $W_n/L_n = 4.0\ \mu\text{m}/0.5\ \mu\text{m}$, the NMOS and PMOS transistors are the same size. In this case $\frac{k_n}{k_p} > 1$ and the equation produced for Problem B.20 is not valid, because it includes the term $\sqrt{1 - \frac{k_n}{k_p}}$. The pseudo-PMOS inverter does not function properly with these transistor parameters.

B.23. (a)

$$\begin{aligned} I_{stat} &= \frac{1}{2} k'_p \frac{W_p}{L_p} (V_{DD} - V_T)^2 \\ &= 12\ \frac{\mu\text{A}}{\text{V}^2} \times 1 \times (5\text{ V} - 1\text{ V})^2 = 192\,\mu\text{A} \end{aligned}$$

(b) The two NMOS transistors in series can be considered equivalent to a single transistor with twice the length. Thus

$$\begin{aligned} R_{DS} &= 1/\left[k_n' \frac{W_n}{L_n}(V_{GS} - V_T)\right] \\ &= 1/\left[0.060\,\frac{\text{mA}}{\text{V}^2} \times 2 \times (5\text{ V} - 1\text{ V})\right] = 2.08\,\text{k}\Omega \end{aligned}$$

(c) Using the expression derived in problem B.20

$$k_p = k_p' \frac{W_p}{L_p} = 24\,\frac{\mu\text{A}}{\text{V}^2}$$
$$k_n = k_n' \frac{W_n}{L_n} = 120\,\frac{\mu\text{A}}{\text{V}^2}$$

$$\begin{aligned} V_{OL} = V_f &= (5\text{ V} - 1\text{ V})\left[1 - \sqrt{1 - \frac{24}{120}}\right] \\ &= 0.42\text{ V} \end{aligned}$$

(d)

$$\begin{aligned} P_D &= I_{stat} V_{DD} \\ &= 192\,\mu\text{A} \times 5\text{ V} = 960\,\mu\text{W} \approx 1\text{m}W \end{aligned}$$

(e)

$$\begin{aligned} R_{SDP} &= V_{SD}/I_{SD} \\ &= (V_{DD} - V_f)/I_{stat} \\ &= (5\text{ V} - 0.42\text{ V})/0.192\,\text{mA} = 23.9\,\text{k}\Omega \end{aligned}$$

(f) The low-to-high propagation delay is

$$\begin{aligned} t_{p_{LH}} &= \frac{1.7C}{k_p' \frac{W_p}{L_p} V_{DD}} \\ &= \frac{1.7 \times 70\text{ fF}}{24\,\frac{\mu\text{A}}{\text{V}^2} \times 1 \times 5\text{ V}} = 0.99\text{ ns} \end{aligned}$$

The high-to-low propagation delay is

$$\begin{aligned} t_{p_{HL}} &= \frac{1.7C}{k_n' \frac{W_n}{L_n} V_{DD}} \\ &= \frac{1.7 \times 70\text{ fF}}{60\,\frac{\mu\text{A}}{\text{V}^2} \times 2 \times 5\text{ V}} = 0.2\text{ ns} \end{aligned}$$

B.24. (a)

$$\begin{aligned} I_{stat} &= \frac{1}{2} k_p' \frac{W_p}{L_p}(V_{DD} - V_T)^2 \\ &= 12\,\frac{\mu\text{A}}{\text{V}^2} \times 1 \times (5\text{ V} - 1\text{ V})^2 = 192\,\mu\text{A} \end{aligned}$$

(b) The two NMOS transistors in parallel can be considered equivalent to a single transistor with twice the width. Thus

$$\begin{aligned} R_{DS} &= 1/\left[k_n' \frac{W_n}{L_n}(V_{GS} - V_T)\right] \\ &= 1/\left[0.060\,\frac{\text{mA}}{\text{V}^2} \times 8 \times (5\text{ V} - 1\text{ V})\right] = 520\,\Omega \end{aligned}$$

(c) Using the expression derived in problem B.20

$$k_p = k_p' \frac{W_p}{L_p} = 24\,\frac{\mu\text{A}}{\text{V}^2}$$
$$k_n = k_n' \frac{W_n}{L_n} = 480\,\frac{\mu\text{A}}{\text{V}^2}$$

$$\begin{aligned} V_{OL} = V_f &= (5\text{ V} - 1\text{ V})\left[1 - \sqrt{1 - \frac{24}{480}}\right] \\ &= 0.10\text{ V} \end{aligned}$$

(d)

$$\begin{aligned} P_D &= I_{stat} V_{DD} \\ &= 192\,\mu\text{A} \times 5\text{ V} = 960\,\mu\text{W} \approx 1\text{m}W \end{aligned}$$

(e)

$$\begin{aligned} R_{SDP} &= V_{SD}/I_{SD} \\ &= (V_{DD} - V_f)/I_{stat} \\ &= (5\text{ V} - 0.10\text{ V})/0.192\,\text{mA} = 25.5\,\text{k}\Omega \end{aligned}$$

(f) The low-to-high propagation delay is

$$\begin{aligned} t_{p_{LH}} &= \frac{1.7C}{k_p' \frac{W_p}{L_p} V_{DD}} \\ &= \frac{1.7 \times 70\text{ fF}}{24\,\frac{\mu\text{A}}{\text{V}^2} \times 1 \times 5\text{ V}} = 0.99\text{ ns} \end{aligned}$$

The high-to-low propagation delay is

$$\begin{aligned} t_{p_{HL}} &= \frac{1.7C}{k_n' \frac{W_n}{L_n} V_{DD}} \\ &= \frac{1.7 \times 70\text{ fF}}{60\,\frac{\mu\text{A}}{\text{V}^2} \times 8 \times 5\text{ V}} = 0.05\text{ ns} \end{aligned}$$

B.25. (a)

$$NM_H = V_{OH} - V_{IH} = 0.5\text{ V}$$
$$NM_L = V_{IL} - V_{OL} = 0.7\text{ V}$$

(*b*)

$$V_{OL} = 8 \times 0.1\text{ V} = 0.8\text{ V}$$
$$NM_L = 1\text{ V} - 0.8\text{ V} = 0.2\text{ V}$$

B.26. Under steady-state conditions, for an n-input CMOS NAND gate the voltage levels V_{OL} and V_{OH} are 0 V and V_{DD}, respectively. No current flows in a CMOS gate in the steady-state. Thus there can be no voltage drop across any of the transistors.

B.27. (*a*)

$$\begin{aligned} P_{NOT\_gate} &= fCV^2 \\ &= 75\text{ MHz} \times 150\text{ fF} \times (5\text{ V})^2 = 281\,\mu\text{W} \end{aligned}$$

(*b*)

$$P_{total} = 0.2 \times 250,000 \times 281\,\mu\text{W} = 14\text{ W}$$

B.28. (*a*)

$$\begin{aligned} P_{NOT\_gate} &= fCV^2 \\ &= 125\text{ MHz} \times 120\text{ fF} \times (3.3\text{ V})^2 = 163\,\mu\text{W} \end{aligned}$$

(*b*)

$$P_{total} = 0.2 \times 250,000 \times 163\,\mu\text{W} = 8.2\text{ W}$$

B.29. (*a*) The high-to-low propagation delay is

$$t_{p_{HL}} = \frac{1.7C}{k'_n \frac{W_n}{L_n} V_{DD}} = \frac{1.7 \times 150\text{ fF}}{20\ \frac{\mu\text{A}}{\text{V}^2} \times 10 \times 5\text{ V}} = 0.255\text{ ns}$$

(*b*) The low-to-high propagation delay is

$$t_{p_{LH}} = \frac{1.7C}{k'_p \frac{W_p}{L_p} V_{DD}} = \frac{1.7 \times 150\text{ fF}}{8\ \frac{\mu\text{A}}{\text{V}^2} \times 10 \times 5\text{ V}} = 0.638\text{ ns}$$

(*c*) For equivalent high-to-low and low-to-high delays

$$\begin{aligned} t_{p_{HL}} &= t_{p_{LH}} \\ \frac{1.7C}{k'_n \frac{W_n}{L_n} V_D D} &= \frac{1.7C}{k'_p \frac{W_p}{L_p} V_D D} \\ \frac{W_p}{L_p} &= \frac{\frac{k'_n}{k'_p} W_n}{L_n} \\ &= \frac{12.5\,\mu\text{m}}{0.5\,\mu\text{m}} \end{aligned}$$

B.30. (*a*) The high-to-low propagation delay is

$$t_{p_{HL}} = \frac{1.7C}{k'_n \frac{W_n}{L_n} V_{DD}} = \frac{1.7 \times 150\text{ fF}}{40\ \frac{\mu\text{A}}{\text{V}^2} \times 10 \times 3.3\text{ V}} = 0.193\text{ ns}$$

(*b*) The low-to-high propagation delay is

$$t_{p_{LH}} = \frac{1.7C}{k'_p \frac{W_p}{L_p} V_{DD}} = \frac{1.7 \times 150\text{ fF}}{16\ \frac{\mu\text{A}}{\text{V}^2} \times 10 \times 3.3\text{ V}} = 0.483\text{ ns}$$

(c) For equivalent high-to-low and low-to-high delays

$$\begin{aligned} t_{p_{HL}} &= t_{p_{LH}} \\ \frac{1.7C}{k'_n \frac{W_n}{L_n} V_D D} &= \frac{1.7C}{k'_p \frac{W_p}{L_p} V_D D} \\ \frac{W_p}{L_p} &= \frac{\frac{k'_n}{k'_p} W_n}{L_n} \\ &= \frac{8.75\ \mu\text{m}}{0.35\ \mu\text{m}} \end{aligned}$$

B.31. The two PMOS transistors in a CMOS NAND gate are connected in parallel. The worst case current to drive the output high happens when only one of these transistors is turned "ON". Thus each transistor has to have the same dimensions as the PMOS transistor in the inverter, namely $\frac{W_p}{L_p} = 4$.

The two NMOS transistors are connected in series. If each one had the ratio $\frac{W_n}{L_n}$, then the two transistors could be thought of as one equivalent transistor with a $\frac{W_n}{2L_n}$ ratio. Thus each NMOS transistor must have twice the width of that in the inverter, namely $\frac{W_n}{L_n} = 4$.

B.32. The two NMOS transistors in a CMOS NOR gate are connected in parallel. The worst case current to drive the output low happens when only one of these transistors is turned "ON". Thus each transistor has to have the same dimensions as the NMOS transistor in the inverter, namely $\frac{W_n}{L_n} = 2$.

The two PMOS transistors are connected in series. If each of these transistors had the ratio $\frac{W_p}{L_p}$, then the two transistors could be thought of as one transistor with a $\frac{W_p}{2L_p}$ ratio. Thus each PMOS transistor must be made twice as wide as that in the inverter, namely $\frac{W_n}{L_n} = 8$.

B.33. The worst case path in the PMOS network contains two transistors in series. Thus each PMOS transistor must be twice as wide the transistors in the inverter. The worst case path in the NMOS network also contains two transistors in series. Similarly, each NMOS transistor must be twice as wide as those in the inverter.

B.34. The worst case PMOS path contains three transistors in series so each transistor must be three times as wide as the PMOS transistors in the inverter. The worst case NMOS path contains two transistors in series. Thus the NMOS transistors must be two times as wide.

B.35. (a) The current flowing through the inverter is equal to the current flowing through the PMOS transistor. We shall assume that the PMOS transistor is operating in the saturation region.

$$\begin{aligned} I_{stat} &= \frac{1}{2} k'_p \frac{W_p}{L_p} (V_{GS} - V_{Tp})^2 \\ &= 120\ \frac{\mu\text{A}}{\text{V}^2} \times ((3.5\ \text{V} - 5\ \text{V}) + 1\ \text{V})^2 = 30\ \mu\text{A} \end{aligned}$$

(b) The current flowing through the NMOS transistor is equal to the static current I_{stat}. Assume that the NMOS transistor is operating in the triode region.

$$\begin{aligned} I_{stat} &= k'_n \frac{W_n}{L_n} \left[(V_{GS} - V_{Tn}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \\ 30\ \mu\text{A} &= 240\ \frac{\mu\text{A}}{\text{V}^2} \times \left[2.5\ \text{V} \times V_f - \frac{1}{2} V_f^2 \right] \\ 1 &= 20 V_f - 4 V_f^2 \end{aligned}$$

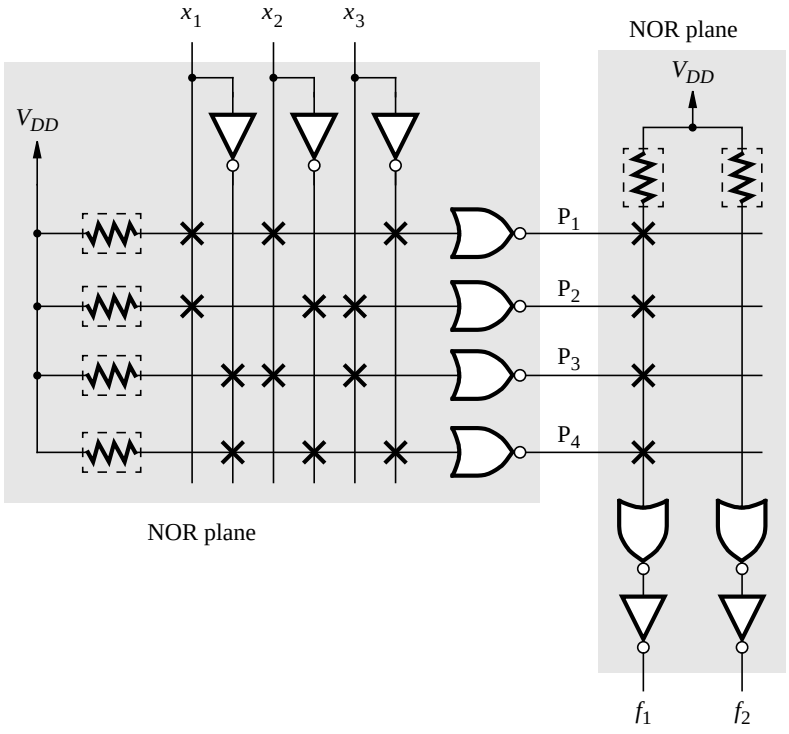
Solving this quadratic equation yields $V_f = 0.05\,\text{V}$. Note that the output voltage V_f satisfies the assumption that the PMOS transistor is operating in the saturation region while the NMOS transistor is operating in the triode region. (c) The static power dissipated in the inverter is

$$P_S = I_{stat} V_{DD} = 30\,\mu\text{A} \times 5\,\text{V} = 150\,\mu\text{W}$$

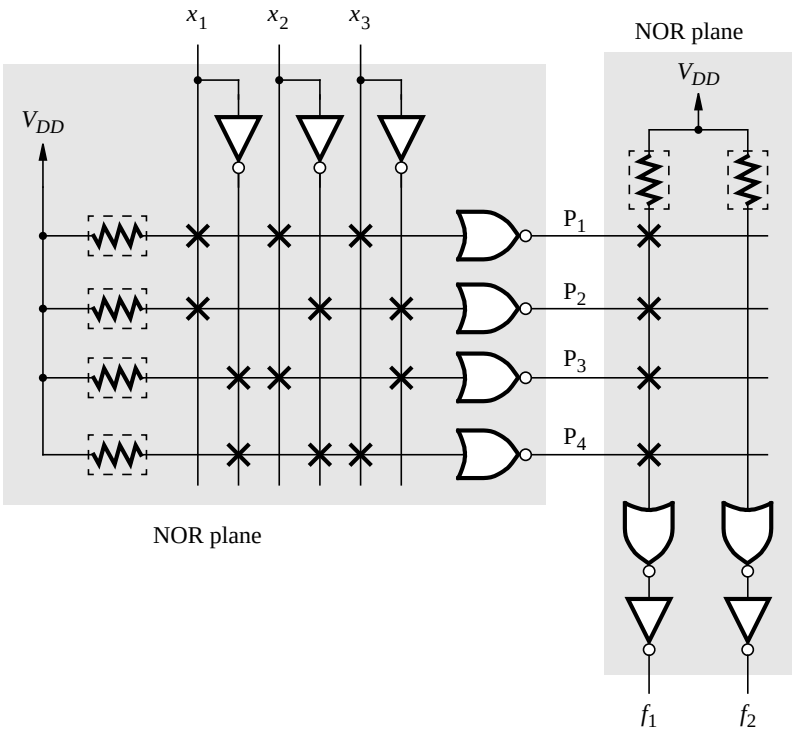
(d) The static power dissipated by 250,000 inverters.

$$250,000 \times P_S = 37.5\,\text{W}$$

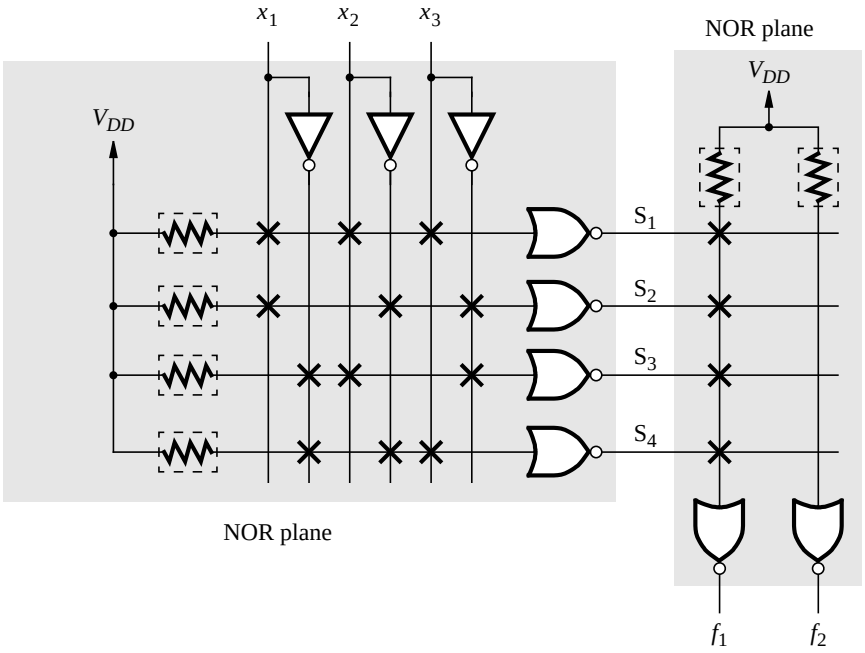
B.36.



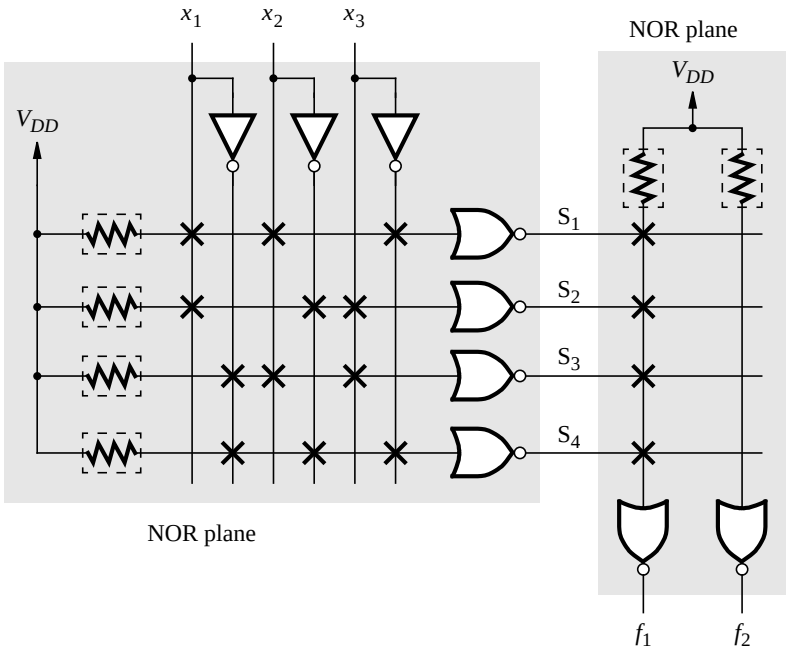
B.37.


x_1
x_2
x_3
NOR plane
V_{DD}
V_{DD}
P_1
P_2
P_3
P_4
NOR plane
f_1
f_2

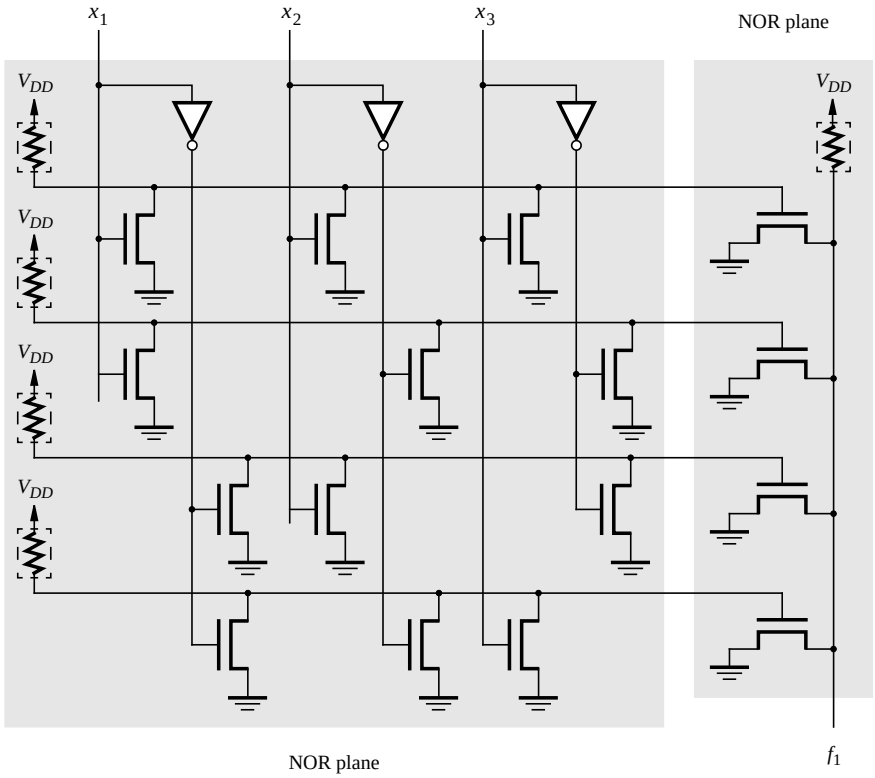
B.38.


x_1
x_2
x_3
NOR plane
V_{DD}
V_{DD}
S_1
S_2
S_3
S_4
NOR plane
f_1
f_2

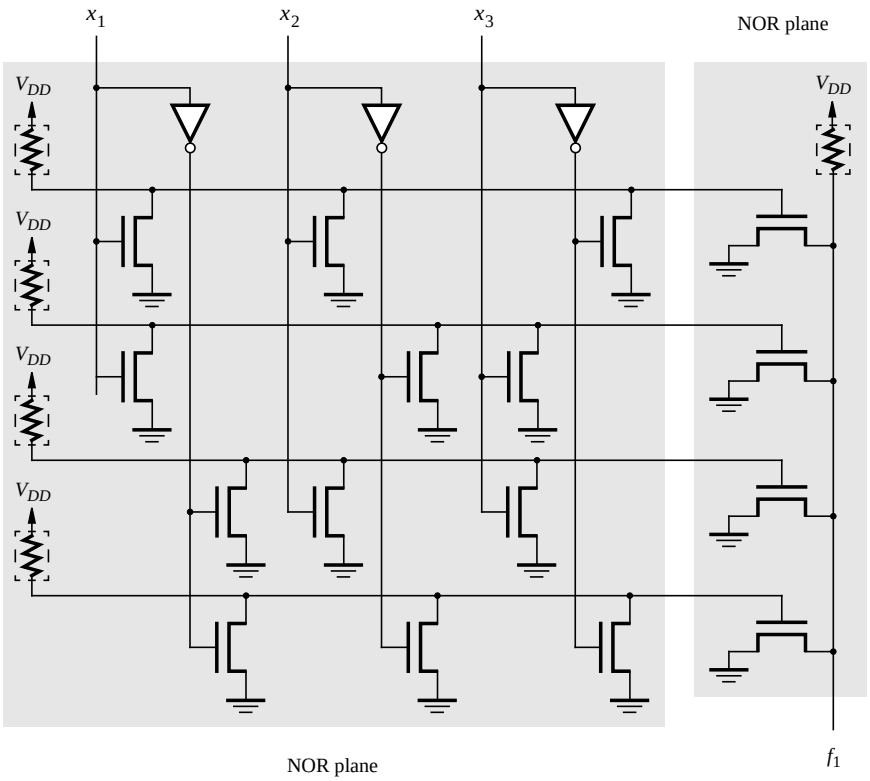
B.39.


x_1
x_2
x_3
NOR plane
V_{DD}
V_{DD}
S_1
S_2
S_3
S_4
NOR plane
f_1
f_2

B.40.


x_1
x_2
x_3
NOR plane
V_{DD}
V_{DD}
V_{DD}
V_{DD}
V_{DD}
NOR plane
f_1

B.41.



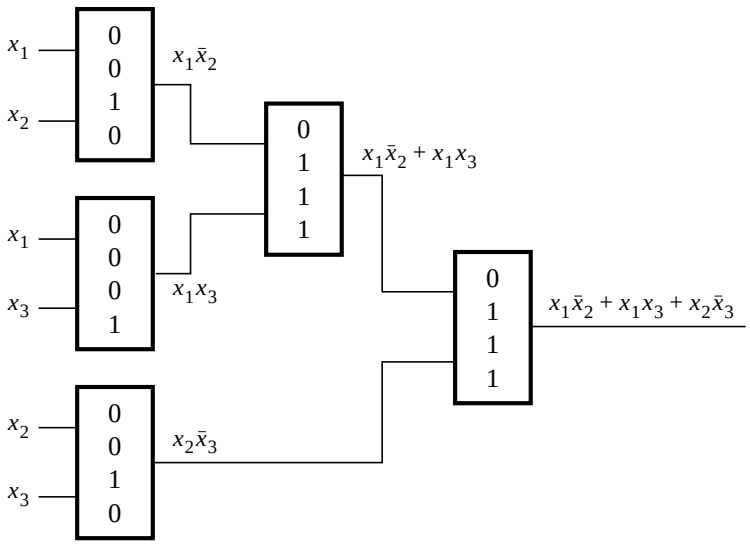
B.42.

$$
\begin{aligned}
f_2 &= m_1 \\
f_2 &= m_2 \\
f_2 &= m_4 \\
f_2 &= m_7 \\
f_2 &= m_1 + m_2 \\
f_2 &= m_1 + m_4 \\
f_2 &= m_1 + m_7 \\
f_2 &= m_2 + m_4 \\
f_2 &= m_2 + m_7 \\
f_2 &= m_4 + m_7 \\
f_2 &= m_1 + m_2 + m_4 \\
f_2 &= m_1 + m_2 + m_7 \\
f_2 &= m_1 + m_4 + m_7 \\
f_2 &= m_2 + m_4 + m_7 \\
f_2 &= m_1 + m_2 + m_4 + m_7
\end{aligned}
$$

B.43.

$$
\begin{aligned}
f_2 &= m_0 \\
f_2 &= m_3 \\
f_2 &= m_5 \\
f_2 &= m_6 \\
f_2 &= m_0 + m_3 \\
f_2 &= m_0 + m_5 \\
f_2 &= m_0 + m_6 \\
f_2 &= m_3 + m_4 \\
f_2 &= m_3 + m_6 \\
f_2 &= m_5 + m_6 \\
f_2 &= m_0 + m_3 + m_5 \\
f_2 &= m_0 + m_3 + m_6 \\
f_2 &= m_0 + m_5 + m_6 \\
f_2 &= m_3 + m_5 + m_6 \\
f_2 &= m_0 + m_3 + m_5 + m_6
\end{aligned}
$$

B.44.



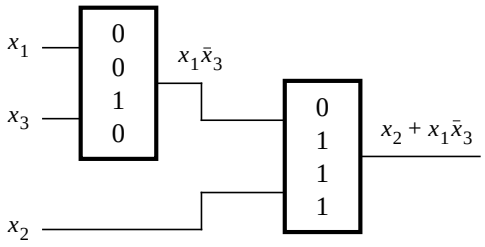
B.45. The canonical SOP for f is

$$f = \overline{x}_1x_2\overline{x}_3 + \overline{x}_1x_2x_3 + x_1\overline{x}_2\overline{x}_3 + x_1x_2\overline{x}_3 + x_1x_2x_3$$

This expression can be manipulated into

$$
\begin{aligned}
f &= \overline{x}_1x_2 + x_1\overline{x}_3 + x_1x_2 \\
&= x_2 + x_1\overline{x}_3
\end{aligned}
$$

The circuit is



B.46. The canonical SOP for f is

$$f = x_1x_2x_4 + x_2x_3\overline{x}_4 + \overline{x}_1\overline{x}_2\overline{x}_3$$

This expression can be manipulated into

$$f = x_2 \cdot (x_1x_4 + x_3\overline{x}_4) + \overline{x}_2 \cdot (\overline{x}_1\overline{x}_3)$$

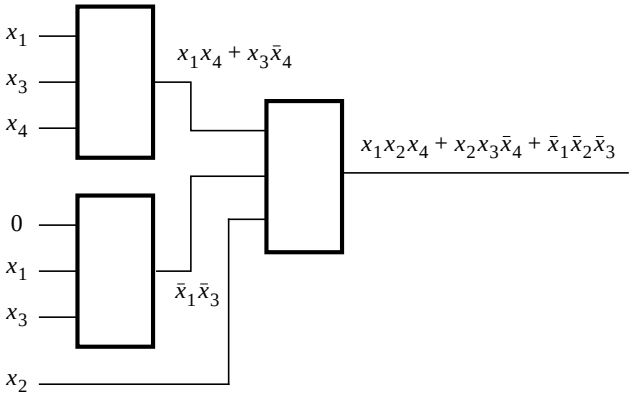
Using functional decomposition we have

$$f = x_2f_1 + \overline{x}_2f_2$$

where

$$\begin{aligned} f_1 &= x_1x_4 + x_3\overline{x}_4 \\ f_2 &= \overline{x}_1\overline{x}_3 \end{aligned}$$

The circuit is



B.47. The canonical SOP for f is

$$f = x_1x_2x_4 + x_2x_3\overline{x}_4 + \overline{x}_1\overline{x}_2\overline{x}_3$$

This expression can be manipulated into

$$f = x_2 \cdot (x_1x_4 + x_3\overline{x}_4) + \overline{x}_2 \cdot (\overline{x}_1\overline{x}_3)$$

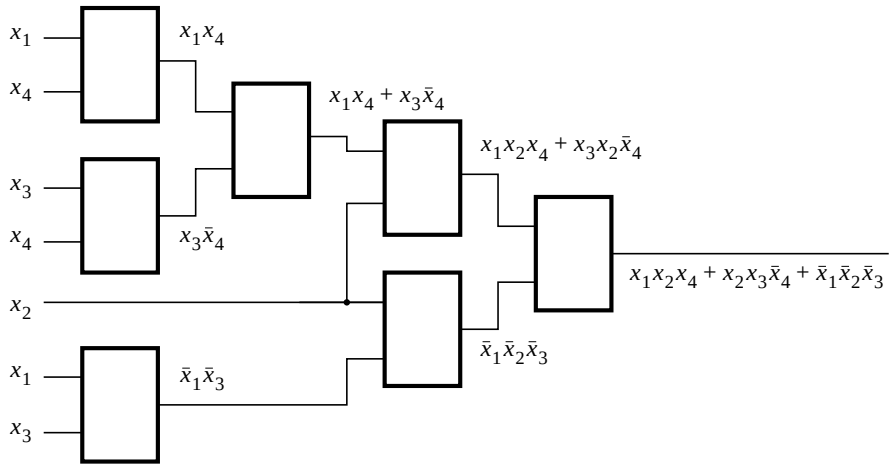
Using functional decomposition we have

$$f = x_2f_1 + \overline{x}_2f_2$$

where

$$\begin{aligned} f_1 &= x_1x_4 + x_3\overline{x}_4 \\ f_2 &= \overline{x}_1\overline{x}_3 \end{aligned}$$

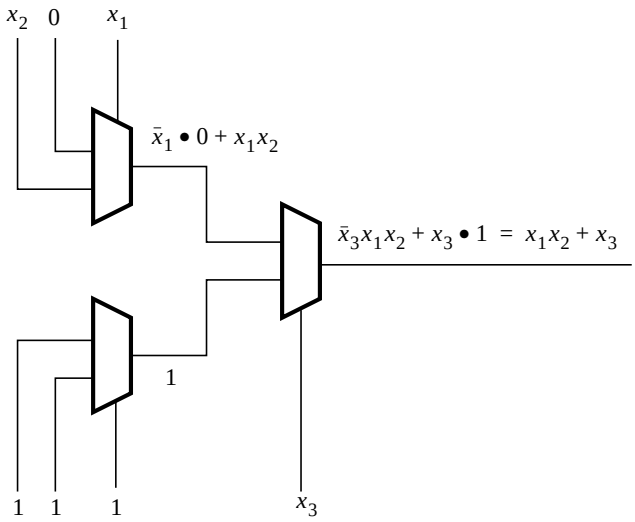
The function f_1 requires one 2-LUT, while f_2 requires three 2-LUTs. We then need three additional 3-LUTs to realize f, as illustrated in the circuit



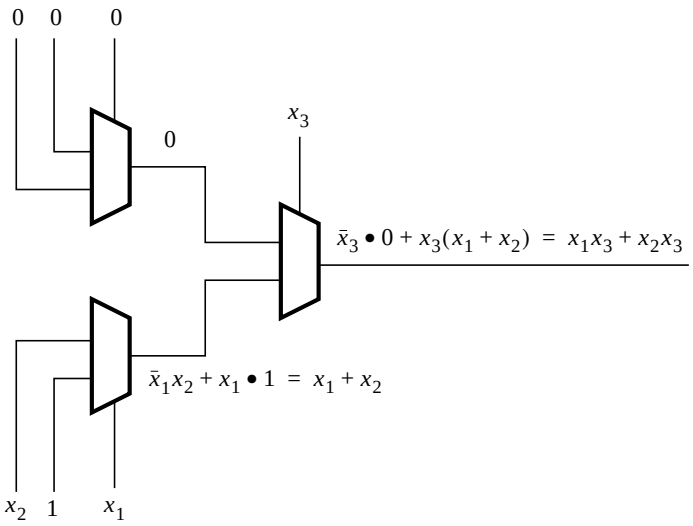
B.48.

$$\begin{aligned} g &= \overline{x}_2 x_3 \\ h &= x_1 \\ j &= x_2 \\ k &= x_3 \end{aligned}$$

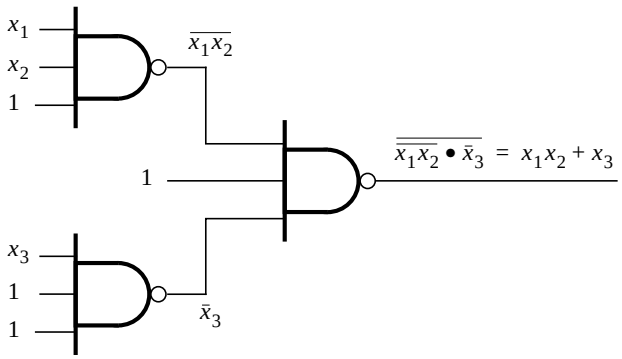
B.49. (a)



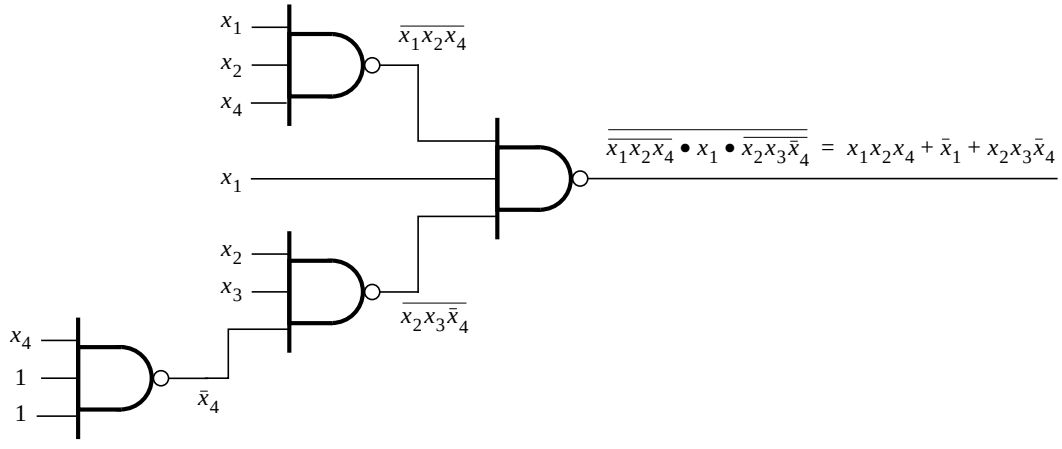
(*b*)


0 0 0
0
x_3
$\bar{x}_3 \bullet 0 + x_3(x_1 + x_2) = x_1x_3 + x_2x_3$
$\bar{x}_1x_2 + x_1 \bullet 1 = x_1 + x_2$
x_2 1 x_1

B.50. (*a*)


x_1
x_2
1
$\overline{x_1x_2}$
$\overline{\overline{x_1x_2} \bullet \bar{x}_3} = x_1x_2 + x_3$
1
x_3
1
1
$\bar{x}_3$

(*b*)


x_1
x_2
x_4
$\overline{x_1x_2x_4}$
$\overline{\overline{x_1x_2x_4} \bullet x_1 \bullet \overline{x_2x_3\bar{x}_4}} = x_1x_2x_4 + \bar{x}_1 + x_2x_3\bar{x}_4$
x_1
x_2
x_3
$\overline{x_2x_3\bar{x}_4}$
x_4
1
1
$\bar{x}_4$

B.51. The circuit in Figure PB.10 is a two-input XOR gate. Since NMOS transistors are used only to pass logic 0 and PMOS transistors are used only to pass logic 1, the circuit does nor suffer from any major drawbacks.

B.52. The circuit in Figure PB.11 is a two-input XOR gate. This circuit has two drawbacks: when both inputs are 0 the PMOS transistor must drive f to 0, resulting in $f = V_T$ volts. Also, when $x_1 = 1$ and $x_2 = 0$, the NMOS transistor must drive the output high, resulting in $f = V_{DD} - V_T$.