Soc Lab – Lab1

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一、簡介

Lab1 所實作的系統是一個乘法器，來實現九九乘法表。

二、觀察與學習

觀察：

1.設定 Directive

#pragma： 可設定 INTERFACE，此 Lab 將 INTERFACE 設定成 AXILite

若沒有#pragma，可直接在 Directive 上設定相關資訊。

加入 Directive 有兩種方式，一種是 inline，即使用#pragma，另一種是使用 directive.tcl 來控制。

使用 inline 方式是當需要將 source code 分享到 github 或給其他人參考時，inline 方法可以更完整的將自己的 design 資訊告訴別人，因為#pragma 也屬於 design 的一部份，可以定義使用到的架構，而別人會比較好懂我設計的方式；而直接使用 directive.tcl 來控制是在一開始需要測試多種不同的 pragma 或 solution，使用起來會較方便，但會相較 inline 起來 design 不完整，不過最後分享出去時還是使用 inline 較佳。

2.跑 C simulation

設定完 Directive 後，可以跑 C simulation 來驗證 source code 的.cpp 檔(C code)是否正確。

3.跑 C synthesis

跑完 C simulation 後確認 code 的運作是正確的，即可跑 C synthesis 來合成。會使用到第一步設定好的 INTERFACE 資訊。

4.跑 Co simulation

需將 ap_ctrl_none 拿掉，因為跑 co simulation 時需要有 block error 來去做 simulation，不然會報錯。

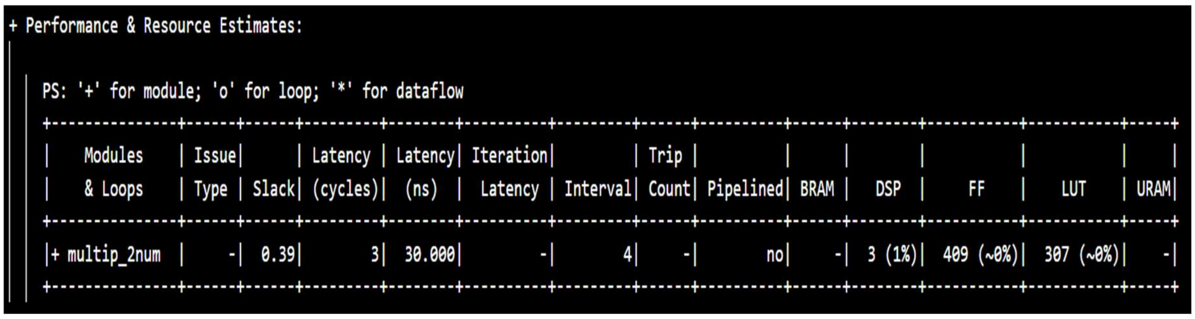
Dump Trace : ALL=可以把所有的波形的 Dump 下來

學習：

學會如何跑一次完整流程，並將.bit/.hwh 檔上傳到 FPGA 板上做驗證。且了解 C simulation、C synthesis、Co simulation 各別的含意和用途。

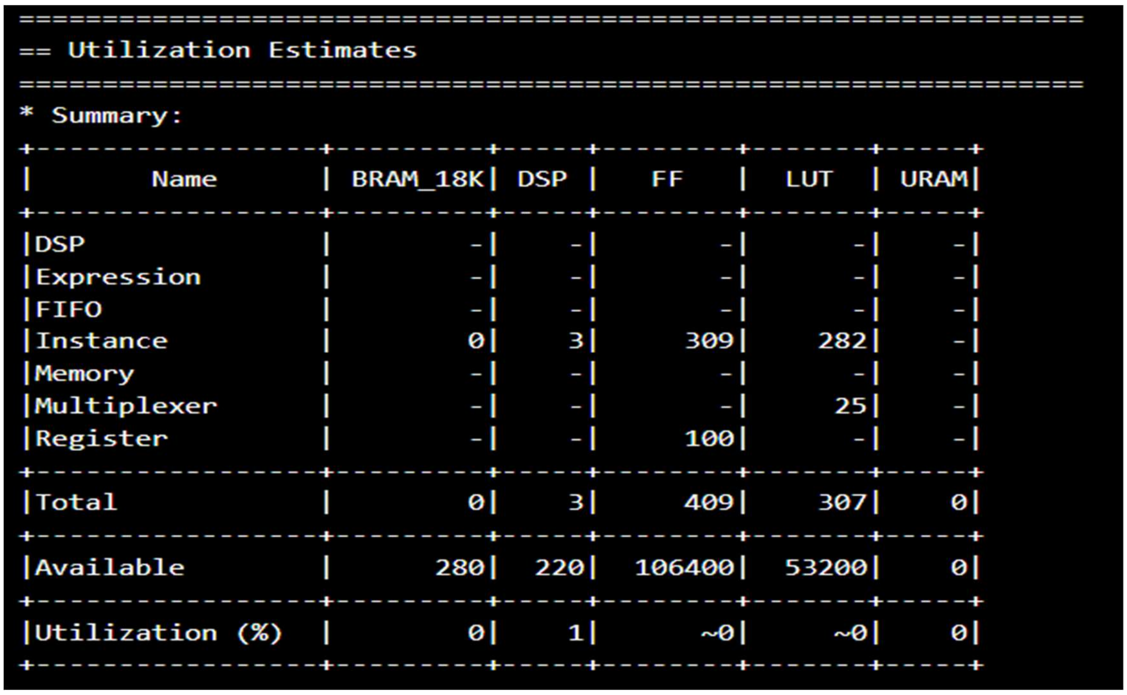
三、截圖

1. Performance

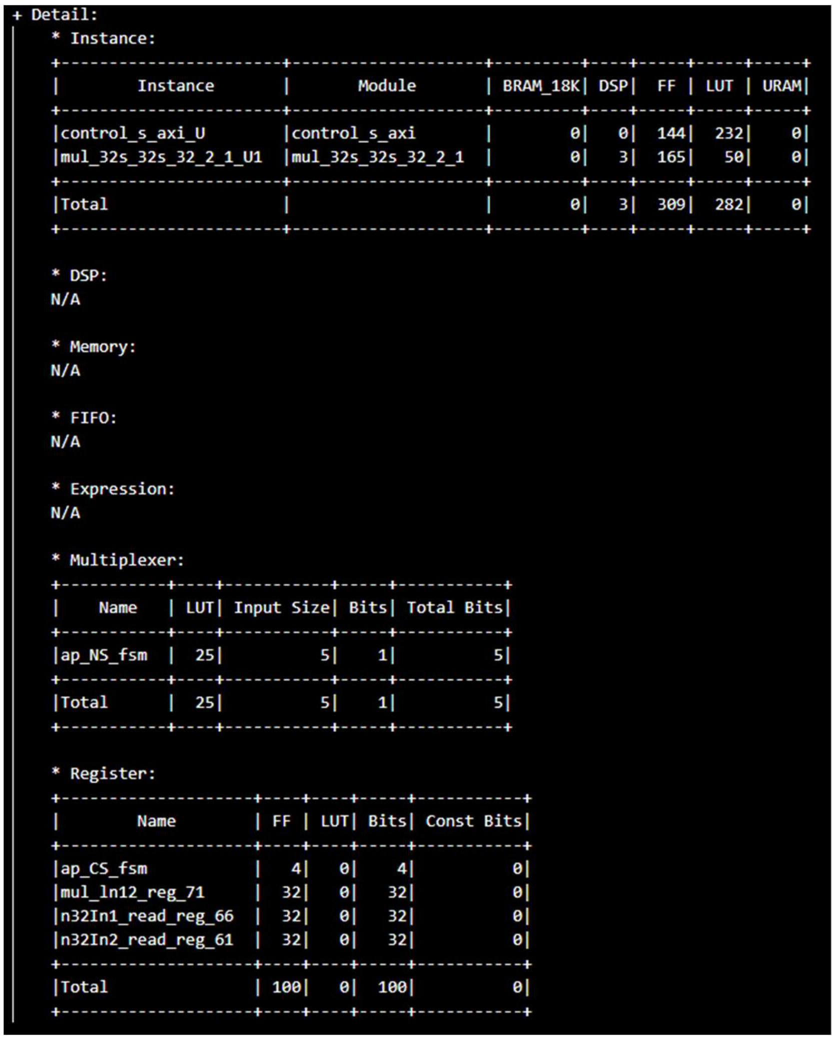


```
+ Performance & Resource Estimates:

    PS: '+' for module; 'o' for loop; '*' for dataflow
    +--------------+-----+-----+--------+-------+---------+--------+-----+---------+-----+--------+----------+----------+-----+
    |    Modules   | Issue|     | Latency | Latency| Iteration|        | Trip |         |     |        |          |          |     |
    |    & Loops   | Type | Slack| (cycles)|  (ns)  |  Latency | Interval| Count| Pipelined| BRAM |   DSP  |    FF    |    LUT   | URAM|
    +--------------+-----+-----+--------+-------+---------+--------+-----+---------+-----+--------+----------+----------+-----+
    |+ multip_2num  |    -|  0.39|       3|  30.000|        -|       4|    -|       no|    -|  3 (1%)|  409 (~0%)|  307 (~0%)|    -|
    +--------------+-----+-----+--------+-------+---------+--------+-----+---------+-----+--------+----------+----------+-----+
```

2. Utilization

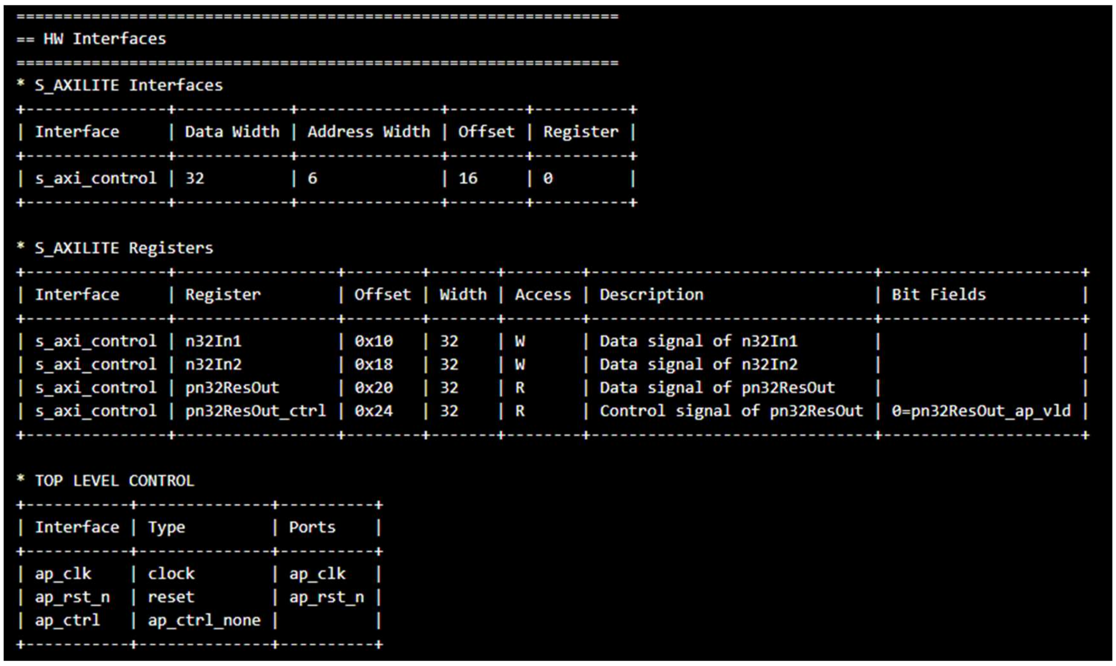


```
================================================================
== Utilization Estimates
================================================================
* Summary:
+-----------------+---------+-----+--------+-------+-----+
|       Name      | BRAM_18K| DSP |   FF   |  LUT  | URAM|
+-----------------+---------+-----+--------+-------+-----+
|DSP              |        -|    -|       -|      -|    -|
|Expression       |        -|    -|       -|      -|    -|
|FIFO             |        -|    -|       -|      -|    -|
|Instance         |        0|    3|     309|    282|    -|
|Memory           |        -|    -|       -|      -|    -|
|Multiplexer      |        -|    -|       -|     25|    -|
|Register         |        -|    -|     100|      -|    -|
+-----------------+---------+-----+--------+-------+-----+
|Total            |        0|    3|     409|    307|    0|
+-----------------+---------+-----+--------+-------+-----+
|Available        |      280|  220|  106400|  53200|    0|
+-----------------+---------+-----+--------+-------+-----+
|Utilization (%)  |        0|    1|      ~0|     ~0|    0|
+-----------------+---------+-----+--------+-------+-----+
```

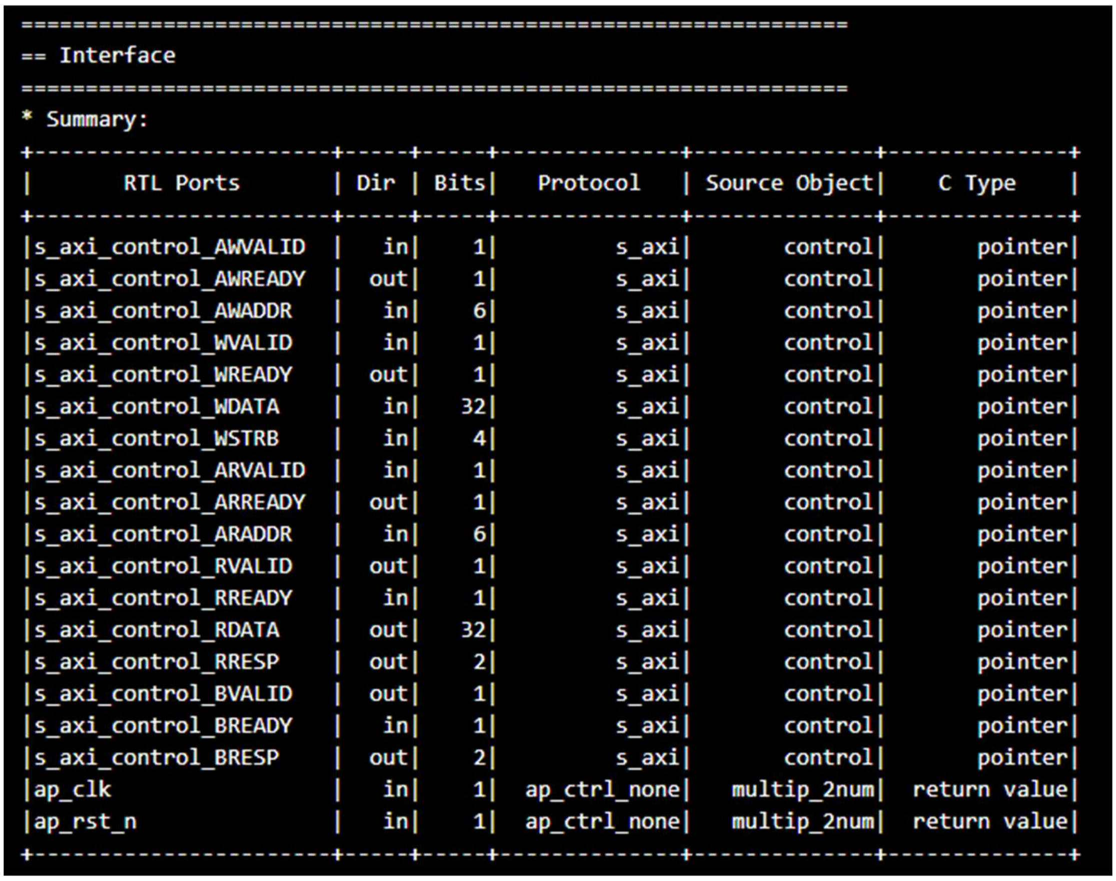


```
+ Detail:
    * Instance:
    +----------------------+-------------------+---------+----+-----+-----+-----+
    |       Instance       |       Module      | BRAM_18K| DSP|  FF | LUT | URAM|
    +----------------------+-------------------+---------+----+-----+-----+-----+
    |control_s_axi_U       |control_s_axi      |        0|   0|  144|  232|    0|
    |mul_32s_32s_32_2_1_U1 |mul_32s_32s_32_2_1 |        0|   3|  165|   50|    0|
    +----------------------+-------------------+---------+----+-----+-----+-----+
    |Total                 |                   |        0|   3|  309|  282|    0|
    +----------------------+-------------------+---------+----+-----+-----+-----+

    * DSP:
    N/A

    * Memory:
    N/A

    * FIFO:
    N/A

    * Expression:
    N/A

    * Multiplexer:
    +-----------+----+-----------+-----+-----------+
    |    Name   | LUT| Input Size| Bits| Total Bits|
    +-----------+----+-----------+-----+-----------+
    |ap_NS_fsm  |  25|          5|    1|          5|
    +-----------+----+-----------+-----+-----------+
    |Total      |  25|          5|    1|          5|
    +-----------+----+-----------+-----+-----------+

    * Register:
    +--------------------+----+----+-----+-----------+
    |        Name        | FF | LUT| Bits| Const Bits|
    +--------------------+----+----+-----+-----------+
    |ap_CS_fsm           |   4|   0|    4|          0|
    |mul_ln12_reg_71     |  32|   0|   32|          0|
    |n32In1_read_reg_66  |  32|   0|   32|          0|
    |n32In2_read_reg_61  |  32|   0|   32|          0|
    +--------------------+----+----+-----+-----------+
    |Total               | 100|   0|  100|          0|
    +--------------------+----+----+-----+-----------+
```

3. Interface

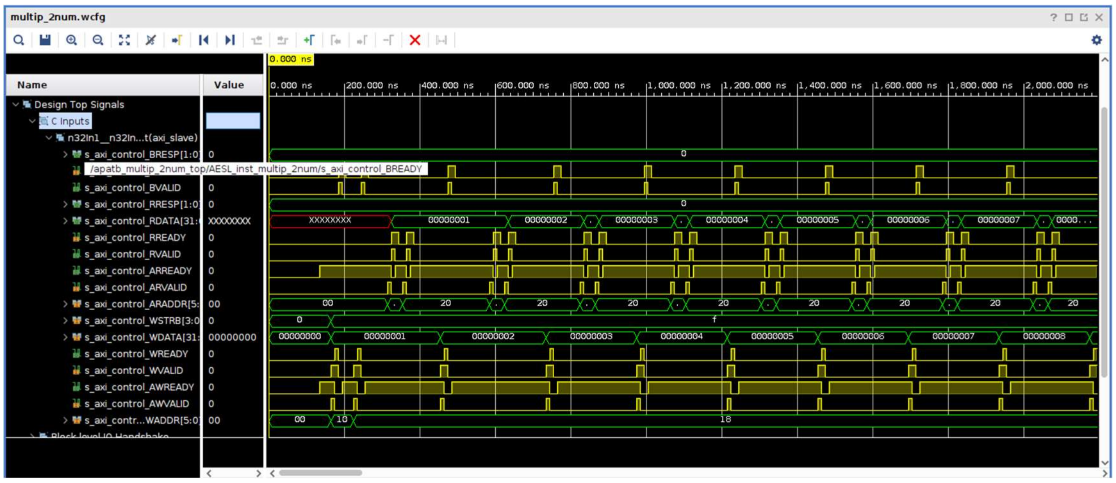


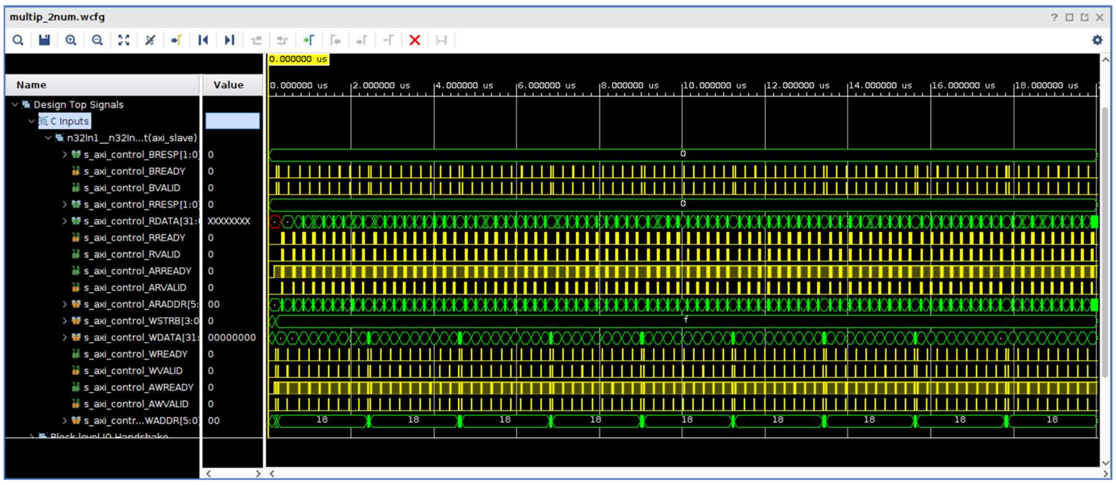
```
================================================================
== HW Interfaces
================================================================
* S_AXILITE Interfaces
+---------------+------------+---------------+--------+----------+
| Interface     | Data Width | Address Width | Offset | Register |
+---------------+------------+---------------+--------+----------+
| s_axi_control | 32         | 6             | 16     | 0        |
+---------------+------------+---------------+--------+----------+

* S_AXILITE Registers
+---------------+-----------------+--------+-------+--------+------------------------------+--------------------+
| Interface     | Register        | Offset | Width | Access | Description                  | Bit Fields         |
+---------------+-----------------+--------+-------+--------+------------------------------+--------------------+
| s_axi_control | n32In1          | 0x10   | 32    | W      | Data signal of n32In1        |                    |
| s_axi_control | n32In2          | 0x18   | 32    | W      | Data signal of n32In2        |                    |
| s_axi_control | pn32ResOut      | 0x20   | 32    | R      | Data signal of pn32ResOut    |                    |
| s_axi_control | pn32ResOut_ctrl | 0x24   | 32    | R      | Control signal of pn32ResOut | 0=pn32ResOut_ap_vld |
+---------------+-----------------+--------+-------+--------+------------------------------+--------------------+

* TOP LEVEL CONTROL
+-----------+--------------+----------+
| Interface | Type         | Ports    |
+-----------+--------------+----------+
| ap_clk    | clock        | ap_clk   |
| ap_rst_n  | reset        | ap_rst_n |
| ap_ctrl   | ap_ctrl_none |          |
+-----------+--------------+----------+
```



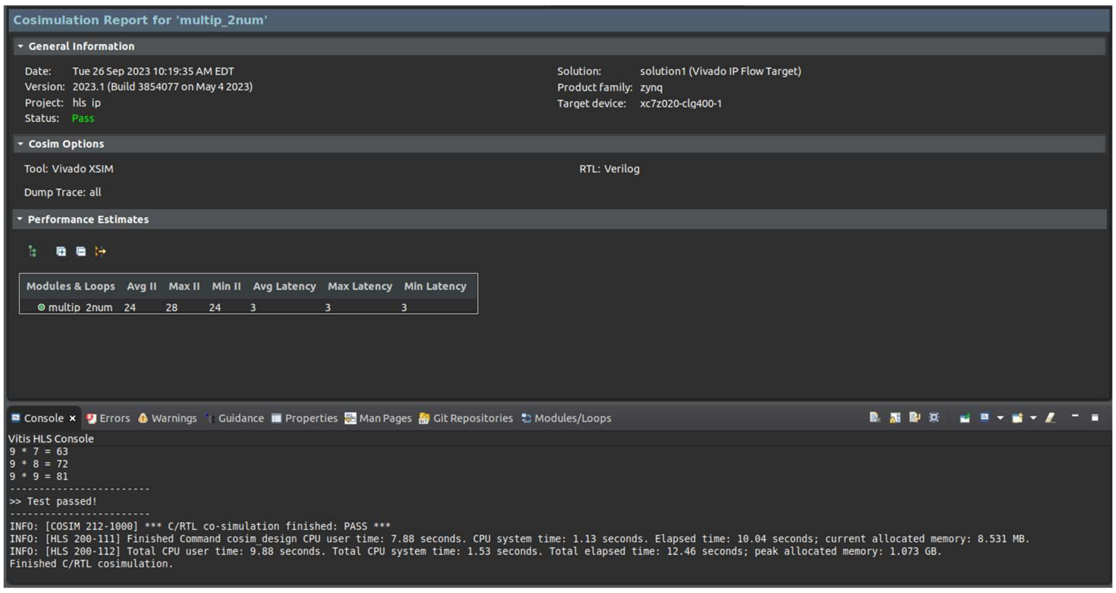
```
================================================================
== Interface
================================================================
* Summary:
+-----------------------+-----+-----+------------+--------------+--------------+
|       RTL Ports       | Dir | Bits|  Protocol  | Source Object|    C Type    |
+-----------------------+-----+-----+------------+--------------+--------------+
|s_axi_control_AWVALID  |   in|    1|       s_axi|       control|       pointer|
|s_axi_control_AWREADY  |  out|    1|       s_axi|       control|       pointer|
|s_axi_control_AWADDR   |   in|    6|       s_axi|       control|       pointer|
|s_axi_control_WVALID   |   in|    1|       s_axi|       control|       pointer|
|s_axi_control_WREADY   |  out|    1|       s_axi|       control|       pointer|
|s_axi_control_WDATA    |   in|   32|       s_axi|       control|       pointer|
|s_axi_control_WSTRB    |   in|    4|       s_axi|       control|       pointer|
|s_axi_control_ARVALID  |   in|    1|       s_axi|       control|       pointer|
|s_axi_control_ARREADY  |  out|    1|       s_axi|       control|       pointer|
|s_axi_control_ARADDR   |   in|    6|       s_axi|       control|       pointer|
|s_axi_control_RVALID   |  out|    1|       s_axi|       control|       pointer|
|s_axi_control_RREADY   |   in|    1|       s_axi|       control|       pointer|
|s_axi_control_RDATA    |  out|   32|       s_axi|       control|       pointer|
|s_axi_control_RRESP    |  out|    2|       s_axi|       control|       pointer|
|s_axi_control_BVALID   |  out|    1|       s_axi|       control|       pointer|
|s_axi_control_BREADY   |   in|    1|       s_axi|       control|       pointer|
|s_axi_control_BRESP    |  out|    2|       s_axi|       control|       pointer|
|ap_clk                 |   in|    1| ap_ctrl_none|   multip_2num|  return value|
|ap_rst_n               |   in|    1| ap_ctrl_none|   multip_2num|  return value|
+-----------------------+-----+-----+------------+--------------+--------------+
```

4. Co-simulation transcript/waveform


multip_2num.wcfg
Name
Value
Design Top Signals
C Inputs
n32In1__n32In...t(axi_slave)
s_axi_control_BRESP[1:0] 0
/apatb_multip_2num_top/AESL_inst_multip_2num/s_axi_control_BREADY
s_axi_control_BVALID 0
s_axi_control_RRESP[1:0] 0
s_axi_control_RDATA[31:0] XXXXXXXX
s_axi_control_RREADY 0
s_axi_control_RVALID 0
s_axi_control_ARREADY 0
s_axi_control_ARVALID 0
s_axi_control_ARADDR[5:0] 00
s_axi_control_WSTRB[3:0] 0
s_axi_control_WDATA[31:0] 00000000
s_axi_control_WREADY 0
s_axi_control_WVALID 0
s_axi_control_AWREADY 0
s_axi_control_AWVALID 0
s_axi_contr...WADDR[5:0] 00
Block-level IO Handshake
0.000 ns
0.000 ns 200.000 ns 400.000 ns 600.000 ns 800.000 ns 1,000.000 ns 1,200.000 ns 1,400.000 ns 1,600.000 ns 1,800.000 ns 2,000.000 ns
XXXXXXXX 00000001 00000002 00000003 00000004 00000005 00000006 00000007 0000...
00 20 20 20 20 20 20 20 20
0 f
00000000 00000001 00000002 00000003 00000004 00000005 00000006 00000007 00000008
00 10 18



Name	Value
Design Top Signals	
C Inputs	
n32In1__n32In...t(axi_slave)	
s_axi_control_BRESP[1:0]	0
s_axi_control_BREADY	0
s_axi_control_BVALID	0
s_axi_control_RRESP[1:0]	0
s_axi_control_RDATA[31:	XXXXXXXX
s_axi_control_RREADY	0
s_axi_control_RVALID	0
s_axi_control_ARREADY	0
s_axi_control_ARVALID	0
s_axi_control_ARADDR[5:	00
s_axi_control_WSTRB[3:0	0
s_axi_control_WDATA[31:	00000000
s_axi_control_WREADY	0
s_axi_control_WVALID	0
s_axi_control_AWREADY	0
s_axi_control_AWVALID	0
s_axi_contr...WADDR[5:0]	00



Cosimulation Report for 'multip_2num'

General Information

Date:	Tue 26 Sep 2023 10:19:35 AM EDT
Version:	2023.1 (Build 3854077 on May 4 2023)
Project:	hls_ip
Status:	Pass
Solution:	solution1 (Vivado IP Flow Target)
Product family:	zynq
Target device:	xc7z020-clg400-1

Cosim Options

Tool: Vivado XSIM

RTL: Verilog

Dump Trace: all

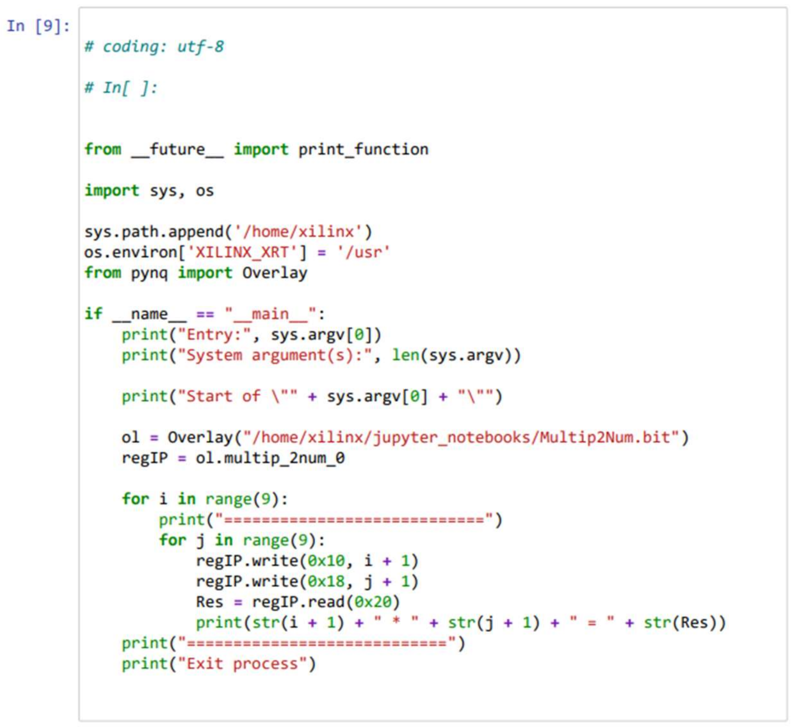
Performance Estimates

Modules & Loops	Avg II	Max II	Min II	Avg Latency	Max Latency	Min Latency
● multip_2num	24	28	24	3	3	3

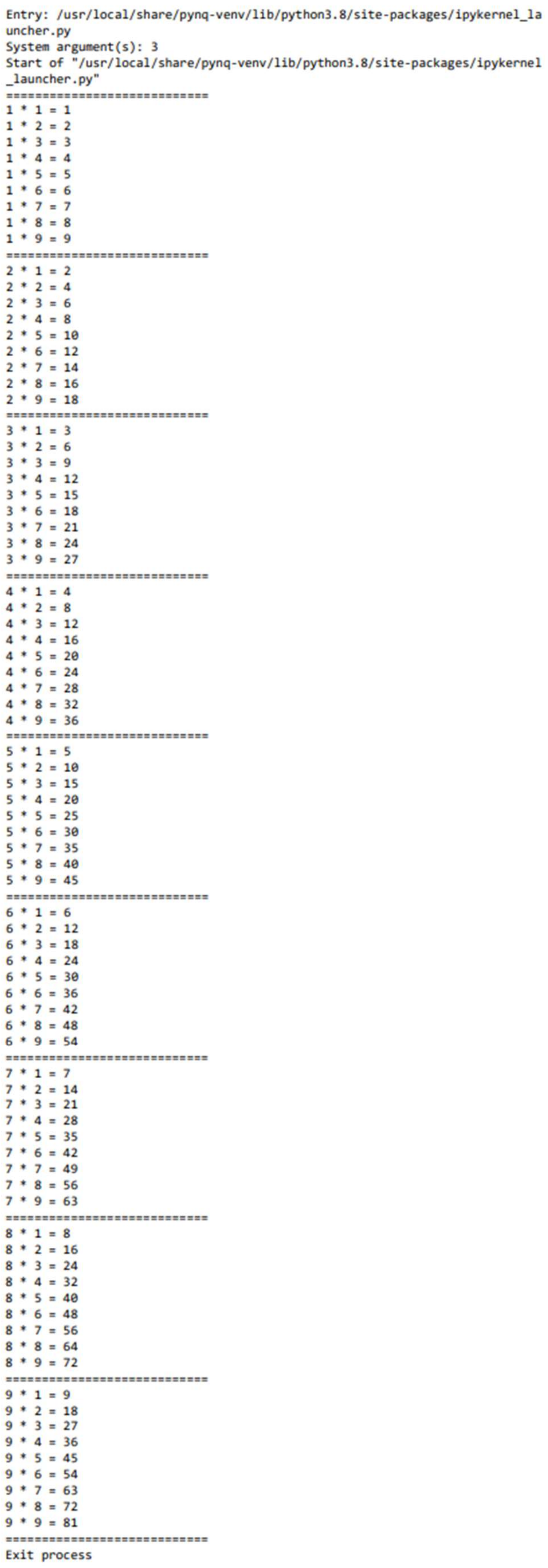
Vitis HLS Console

```
9 * 7 = 63
9 * 8 = 72
9 * 9 = 81
------------------------
>> Test passed!
------------------------
INFO: [COSIM 212-1000] *** C/RTL co-simulation finished: PASS ***
INFO: [HLS 200-111] Finished Command cosim_design CPU user time: 7.88 seconds. CPU system time: 1.13 seconds. Elapsed time: 10.04 seconds; current allocated memory: 8.531 MB.
INFO: [HLS 200-112] Total CPU user time: 9.88 seconds. Total CPU system time: 1.53 seconds. Total elapsed time: 12.46 seconds; peak allocated memory: 1.073 GB.
Finished C/RTL cosimulation.
```

5. Jupyter Notebook execution results



```
In [9]:
# coding: utf-8

# In[ ]:


from __future__ import print_function

import sys, os

sys.path.append('/home/xilinx')
os.environ['XILINX_XRT'] = '/usr'
from pynq import Overlay

if __name__ == "__main__":
    print("Entry:", sys.argv[0])
    print("System argument(s):", len(sys.argv))

    print("Start of \"" + sys.argv[0] + "\"")

    ol = Overlay("/home/xilinx/jupyter_notebooks/Multip2Num.bit")
    regIP = ol.multip_2num_0

    for i in range(9):
        print("===========================")
        for j in range(9):
            regIP.write(0x10, i + 1)
            regIP.write(0x18, j + 1)
            Res = regIP.read(0x20)
            print(str(i + 1) + " * " + str(j + 1) + " = " + str(Res))
    print("===========================")
    print("Exit process")
```



```
Entry: /usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_la
uncher.py
System argument(s): 3
Start of "/usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel
_launcher.py"
===========================
1 * 1 = 1
1 * 2 = 2
1 * 3 = 3
1 * 4 = 4
1 * 5 = 5
1 * 6 = 6
1 * 7 = 7
1 * 8 = 8
1 * 9 = 9
===========================
2 * 1 = 2
2 * 2 = 4
2 * 3 = 6
2 * 4 = 8
2 * 5 = 10
2 * 6 = 12
2 * 7 = 14
2 * 8 = 16
2 * 9 = 18
===========================
3 * 1 = 3
3 * 2 = 6
3 * 3 = 9
3 * 4 = 12
3 * 5 = 15
3 * 6 = 18
3 * 7 = 21
3 * 8 = 24
3 * 9 = 27
===========================
4 * 1 = 4
4 * 2 = 8
4 * 3 = 12
4 * 4 = 16
4 * 5 = 20
4 * 6 = 24
4 * 7 = 28
4 * 8 = 32
4 * 9 = 36
===========================
5 * 1 = 5
5 * 2 = 10
5 * 3 = 15
5 * 4 = 20
5 * 5 = 25
5 * 6 = 30
5 * 7 = 35
5 * 8 = 40
5 * 9 = 45
===========================
6 * 1 = 6
6 * 2 = 12
6 * 3 = 18
6 * 4 = 24
6 * 5 = 30
6 * 6 = 36
6 * 7 = 42
6 * 8 = 48
6 * 9 = 54
===========================
7 * 1 = 7
7 * 2 = 14
7 * 3 = 21
7 * 4 = 28
7 * 5 = 35
7 * 6 = 42
7 * 7 = 49
7 * 8 = 56
7 * 9 = 63
===========================
8 * 1 = 8
8 * 2 = 16
8 * 3 = 24
8 * 4 = 32
8 * 5 = 40
8 * 6 = 48
8 * 7 = 56
8 * 8 = 64
8 * 9 = 72
===========================
9 * 1 = 9
9 * 2 = 18
9 * 3 = 27
9 * 4 = 36
9 * 5 = 45
9 * 6 = 54
9 * 7 = 63
9 * 8 = 72
9 * 9 = 81
===========================
Exit process
```