# Soc Lab – Lab2

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一、簡介

FIR 濾波器是一種數字信號處理濾波器，用於處理離散時間信號。這個特定的函式 fir_n11_maxi 被設計用於處理 32 位整數信號，並且需要一組濾波器係數 an32Coef 以及一個用於指定處理數據長度的參數 regXferLeng。

以下是主要部分的工作流程：

1.初始化一個靜態整數陣列 an32ShiftReg，用作移位寄存器，其大小為 N。

2.計算要處理的數據數量 n32NumXfer4B，這是 regXferLeng 除以 32 位整數大小的向上捨入值。

3.進入主要的循環 XFER_LOOP，該循環將處理每個 32 位整數數據。

在 XFER_LOOP 循環中，以下是每個數據元素的處理步驟：

1.初始化一個累加器 n32Acc 為零，用於存儲輸出數據。

2.從輸入數據陣列 pn32HPInput 中讀取一個 32 位整數 n32Temp。

3.進入內部循環 SHIFT_ACC_LOOP，這是 FIR 濾波器的核心部分，用於計算輸出數據。

4.在 SHIFT_ACC_LOOP 中，對移位寄存器 an32ShiftReg 進行循環移位操作，同時計算移位寄存器的最後一個元素 n32Data。

5.將 n32Data 乘以相應的濾波器係數 an32Coef，並將結果添加到 n32Acc 累加器中。

6.將 n32Acc 的值寫入輸出數據陣列 pn32HPOutput。

最終，XFER_LOOP 循環處理完所有輸入數據後，該函式返回。這個函式的目的是通過 FIR 濾波器處理輸入數據，並將結果存儲在輸出數據陣列中，以達到信號處理的目的。

二、觀察與學習

Differences between MAXI and Stream interface:兩者差別在於有無 address 來做存取，MAXI 有 address、Stream 沒有，因此 Stream 需要使用到 DMA 來幫助連接到 PS side。

Differences between csim and cosim: Csim : 驗證演算法 coding function 是否正確，testbench 和 kernel function 都是 C code，然後將兩者 compile 起來變成.exe 檔，在 host CPU 上跑；Cosim : Testbench 是 C code，kernel function 是 verilog code，且 verilog code 會在 simulator 上跑。

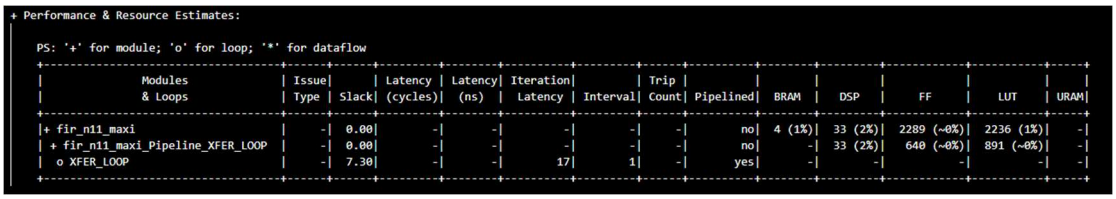
學會如何跑一次完整流程，並將.bit/.hwh 檔上傳到 FPGA 板上做驗證。且了解 C simulation、C synthesis、Co simulation 各別的含意和用途。

Lab2 使用到 KV260 這塊板子，也學會如何設定 KV260 這塊板子上的相關參數，以及如何運作。

三、截圖

1. Performance

MAXI:



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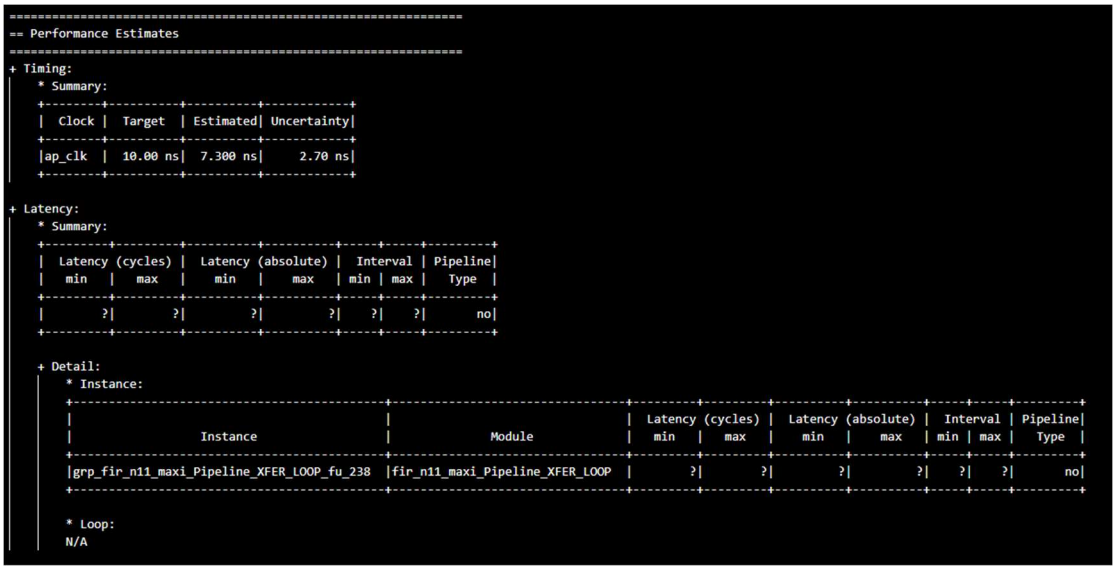
+ Performance & Resource Estimates:

    PS: '+' for module; 'o' for loop; '*' for dataflow
    +-------------------------------+-----+-----+---------+---------+----------+---------+-----+----------+-------+--------+-----------+-----------+-----+
    |             Modules           | Issue|      | Latency | Latency| Iteration|         | Trip |          |       |        |           |           |     |
    |             & Loops           | Type | Slack| (cycles)|  (ns)  |  Latency | Interval| Count| Pipelined| BRAM  |   DSP  |     FF    |    LUT    | URAM|
    +-------------------------------+-----+-----+---------+---------+----------+---------+-----+----------+-------+--------+-----------+-----------+-----+
    |+ fir_n11_maxi                 |     -|  0.00|        -|       -|         -|        -|    -|        no| 4 (1%)| 33 (2%)| 2289 (~0%)| 2236 (1%)|    -|
    | + fir_n11_maxi_Pipeline_XFER_LOOP |     -|  0.00|        -|       -|         -|        -|    -|        no|      -| 33 (2%)|  640 (~0%)|  891 (~0%)|    -|
    |  o XFER_LOOP                  |     -|  7.30|        -|       -|        17|        1|    -|       yes|      -|       -|          -|          -|    -|
    +-------------------------------+-----+-----+---------+---------+----------+---------+-----+----------+-------+--------+-----------+-----------+-----+
```



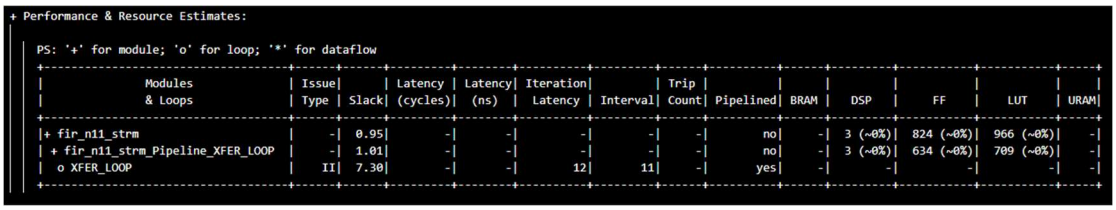
```
================================================================
== Performance Estimates
================================================================
+ Timing:
    * Summary:
    +--------+----------+----------+------------+
    |  Clock |  Target  | Estimated| Uncertainty|
    +--------+----------+----------+------------+
    |ap_clk  |  10.00 ns|  7.300 ns|     2.70 ns|
    +--------+----------+----------+------------+

+ Latency:
    * Summary:
    +---------+---------+----------+----------+-----+-----+---------+
    |  Latency (cycles) |  Latency (absolute) |  Interval | Pipeline|
    |   min   |   max   |    min   |    max   | min | max |   Type  |
    +---------+---------+----------+----------+-----+-----+---------+
    |        ?|        ?|         ?|         ?|    ?|    ?|       no|
    +---------+---------+----------+----------+-----+-----+---------+

    + Detail:
        * Instance:
        +----------------------------------------+--------------------------------+---------+---------+----------+----------+-----+-----+---------+
        |                                        |                                |  Latency (cycles) |  Latency (absolute) |  Interval | Pipeline|
        |                Instance                |             Module             |   min   |   max   |    min   |    max   | min | max |   Type  |
        +----------------------------------------+--------------------------------+---------+---------+----------+----------+-----+-----+---------+
        |grp_fir_n11_maxi_Pipeline_XFER_LOOP_fu_238  |fir_n11_maxi_Pipeline_XFER_LOOP  |        ?|        ?|         ?|         ?|    ?|    ?|       no|
        +----------------------------------------+--------------------------------+---------+---------+----------+----------+-----+-----+---------+

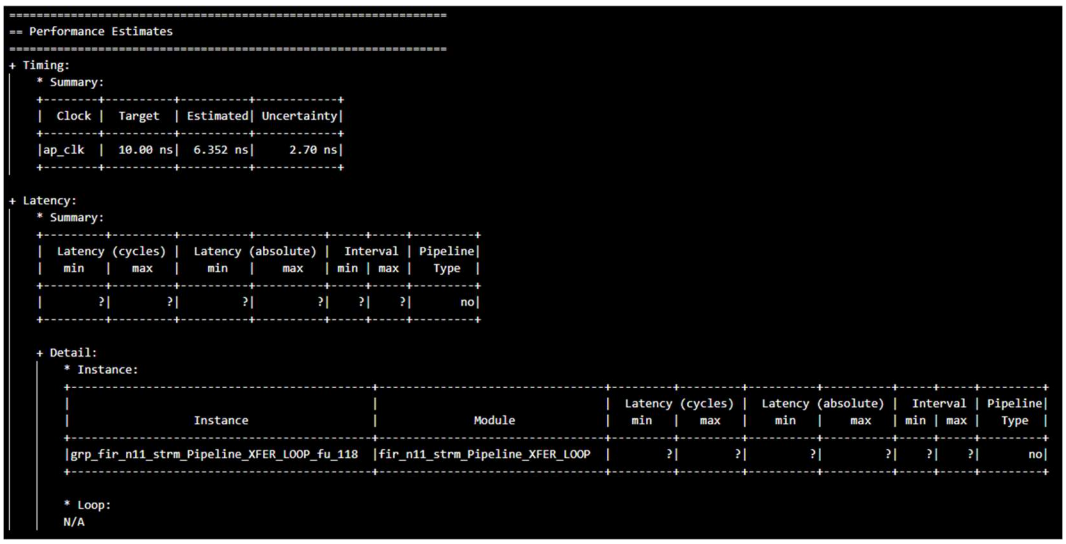
        * Loop:
        N/A
```

Stream:



```
+ Performance & Resource Estimates:

    PS: '+' for module; 'o' for loop; '*' for dataflow
    +-------------------------------+-----+-----+---------+---------+----------+---------+-----+----------+-------+--------+-----------+-----------+-----+
    |             Modules           | Issue|      | Latency | Latency| Iteration|         | Trip |          |       |        |           |           |     |
    |             & Loops           | Type | Slack| (cycles)|  (ns)  |  Latency | Interval| Count| Pipelined| BRAM  |   DSP  |     FF    |    LUT    | URAM|
    +-------------------------------+-----+-----+---------+---------+----------+---------+-----+----------+-------+--------+-----------+-----------+-----+
    |+ fir_n11_strm                 |     -|  0.95|        -|       -|         -|        -|    -|        no|      -| 3 (~0%)|  824 (~0%)|  966 (~0%)|    -|
    | + fir_n11_strm_Pipeline_XFER_LOOP |     -|  1.01|        -|       -|         -|        -|    -|        no|      -| 3 (~0%)|  634 (~0%)|  709 (~0%)|    -|
    |  o XFER_LOOP                  |    II|  7.30|        -|       -|        12|       11|    -|       yes|      -|       -|          -|          -|    -|
    +-------------------------------+-----+-----+---------+---------+----------+---------+-----+----------+-------+--------+-----------+-----------+-----+
```



```
================================================================
== Performance Estimates
================================================================
+ Timing:
    * Summary:
    +--------+----------+----------+------------+
    |  Clock |  Target  | Estimated| Uncertainty|
    +--------+----------+----------+------------+
    |ap_clk  |  10.00 ns|  6.352 ns|     2.70 ns|
    +--------+----------+----------+------------+

+ Latency:
    * Summary:
    +---------+---------+----------+----------+-----+-----+---------+
    |  Latency (cycles) |  Latency (absolute) |  Interval | Pipeline|
    |   min   |   max   |    min   |    max   | min | max |   Type  |
    +---------+---------+----------+----------+-----+-----+---------+
    |        ?|        ?|         ?|         ?|    ?|    ?|       no|
    +---------+---------+----------+----------+-----+-----+---------+

    + Detail:
        * Instance:
        +----------------------------------------+--------------------------------+---------+---------+----------+----------+-----+-----+---------+
        |                                        |                                |  Latency (cycles) |  Latency (absolute) |  Interval | Pipeline|
        |                Instance                |             Module             |   min   |   max   |    min   |    max   | min | max |   Type  |
        +----------------------------------------+--------------------------------+---------+---------+----------+----------+-----+-----+---------+
        |grp_fir_n11_strm_Pipeline_XFER_LOOP_fu_118  |fir_n11_strm_Pipeline_XFER_LOOP  |        ?|        ?|         ?|         ?|    ?|    ?|       no|
        +----------------------------------------+--------------------------------+---------+---------+----------+----------+-----+-----+---------+

        * Loop:
        N/A
```

2. Utilization

MAXI:

```
================================================================
== Utilization Estimates
================================================================
* Summary:
+-----------------+---------+------+--------+--------+-----+
|       Name      | BRAM_18K|  DSP |   FF   |   LUT  | URAM|
+-----------------+---------+------+--------+--------+-----+
|DSP              |        -|     -|       -|       -|    -|
|Expression       |        -|     -|       0|      40|    -|
|FIFO             |        -|     -|       -|       -|    -|
|Instance         |        4|    33|    1764|    2021|    0|
|Memory           |        -|     -|       -|       -|    -|
|Multiplexer      |        -|     -|       -|     175|    -|
|Register         |        -|     -|     525|       -|    -|
+-----------------+---------+------+--------+--------+-----+
|Total            |        4|    33|    2289|    2236|    0|
+-----------------+---------+------+--------+--------+-----+
|Available        |      288|  1248|  234240|  117120|   64|
+-----------------+---------+------+--------+--------+-----+
|Utilization (%)  |        1|     2|      ~0|       1|    0|
+-----------------+---------+------+--------+--------+-----+
```

+ Detail:

* Instance:

| Instance | Module | BRAM_18K | DSP | FF | LUT | URAM |
|---|---|---|---|---|---|---|
| control_s_axi_U | control_s_axi | 0 | 0 | 294 | 436 | 0 |
| grp_fir_n11_maxi_Pipeline_XFER_LOOP_fu_238 | fir_n11_maxi_Pipeline_XFER_LOOP | 0 | 33 | 640 | 891 | 0 |
| gmem_m_axi_U | gmem_m_axi | 4 | 0 | 830 | 694 | 0 |
| Total | | 4 | 33 | 1764 | 2021 | 0 |

* DSP:

N/A

* Memory:

N/A

* FIFO:

N/A

* Expression:

| Variable Name | Operation | DSP | FF | LUT | Bitwidth P0 | Bitwidth P1 |
|---|---|---|---|---|---|---|
| add_ln16_fu_285_p2 | + | 0 | 0 | 40 | 33 | 2 |
| Total | | 0 | 0 | 40 | 33 | 2 |

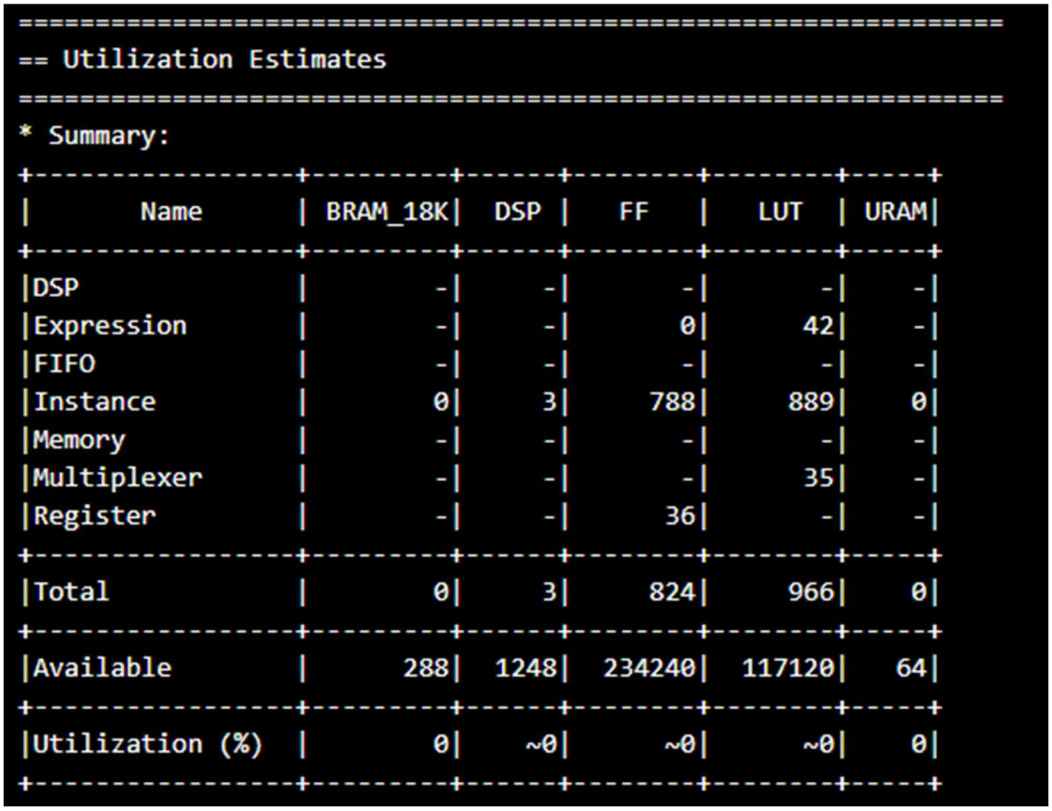
* Multiplexer:

| Name | LUT | Input Size | Bits | Total Bits |
|---|---|---|---|---|
| an32Coef_address0 | 65 | 12 | 4 | 48 |
| ap_NS_fsm | 65 | 14 | 1 | 14 |
| gmem_ARVALID | 9 | 2 | 1 | 2 |
| gmem_AWVALID | 9 | 2 | 1 | 2 |
| gmem_BREADY | 9 | 2 | 1 | 2 |
| gmem_RREADY | 9 | 2 | 1 | 2 |
| gmem_WVALID | 9 | 2 | 1 | 2 |
| Total | 175 | 36 | 10 | 72 |

* Register:

| Name | FF | LUT | Bits | Const Bits |
|---|---|---|---|---|
| an32Coef_load_10_reg_417 | 32 | 0 | 32 | 0 |
| an32Coef_load_1_reg_317 | 32 | 0 | 32 | 0 |
| an32Coef_load_2_reg_327 | 32 | 0 | 32 | 0 |
| an32Coef_load_3_reg_337 | 32 | 0 | 32 | 0 |
| an32Coef_load_4_reg_347 | 32 | 0 | 32 | 0 |
| an32Coef_load_5_reg_357 | 32 | 0 | 32 | 0 |
| an32Coef_load_6_reg_367 | 32 | 0 | 32 | 0 |
| an32Coef_load_7_reg_377 | 32 | 0 | 32 | 0 |
| an32Coef_load_8_reg_387 | 32 | 0 | 32 | 0 |
| an32Coef_load_9_reg_397 | 32 | 0 | 32 | 0 |
| an32Coef_load_reg_307 | 32 | 0 | 32 | 0 |
| ap_CS_fsm | 13 | 0 | 13 | 0 |
| grp_fir_n11_maxi_Pipeline_XFER_LOOP_fu_238_ap_start_reg | 1 | 0 | 1 | 0 |
| pn32HPInput_read_reg_412 | 64 | 0 | 64 | 0 |
| pn32HPOutput_read_reg_407 | 64 | 0 | 64 | 0 |
| tmp_reg_422 | 31 | 0 | 31 | 0 |
| Total | 525 | 0 | 525 | 0 |

Stream:



```
================================================================
== Utilization Estimates
================================================================
* Summary:
+-----------------+---------+------+--------+--------+-----+
|       Name      | BRAM_18K|  DSP |   FF   |   LUT  | URAM|
+-----------------+---------+------+--------+--------+-----+
|DSP              |        -|     -|       -|       -|    -|
|Expression       |        -|     -|       0|      42|    -|
|FIFO             |        -|     -|       -|       -|    -|
|Instance         |        0|     3|     788|     889|    0|
|Memory           |        -|     -|       -|       -|    -|
|Multiplexer      |        -|     -|       -|      35|    -|
|Register         |        -|     -|      36|       -|    -|
+-----------------+---------+------+--------+--------+-----+
|Total            |        0|     3|     824|     966|    0|
+-----------------+---------+------+--------+--------+-----+
|Available        |      288|  1248|  234240|  117120|   64|
+-----------------+---------+------+--------+--------+-----+
|Utilization (%)  |        0|    ~0|      ~0|      ~0|    0|
+-----------------+---------+------+--------+--------+-----+
```

+ Detail:
    * Instance:

| Instance | Module | BRAM_18K | DSP | FF | LUT | URAM |
|---|---|---|---|---|---|---|
| control_s_axi_U | control_s_axi | 0 | 0 | 154 | 180 | 0 |
| grp_fir_n11_strm_Pipeline_XFER_LOOP_fu_118 | fir_n11_strm_Pipeline_XFER_LOOP | 0 | 3 | 634 | 709 | 0 |
| Total | | 0 | 3 | 788 | 889 | 0 |

    * DSP:
    N/A

    * Memory:
    N/A

    * FIFO:
    N/A

    * Expression:

| Variable Name | Operation | DSP | FF | LUT | Bitwidth P0 | Bitwidth P1 |
|---|---|---|---|---|---|---|
| add_ln20_fu_177_p2 | + | 0 | 0 | 40 | 33 | 2 |
| grp_fir_n11_strm_Pipeline_XFER_LOOP_fu_118_pstrmOutput_TREADY | and | 0 | 0 | 2 | 1 | 1 |
| Total | | 0 | 0 | 42 | 34 | 3 |

    * Multiplexer:

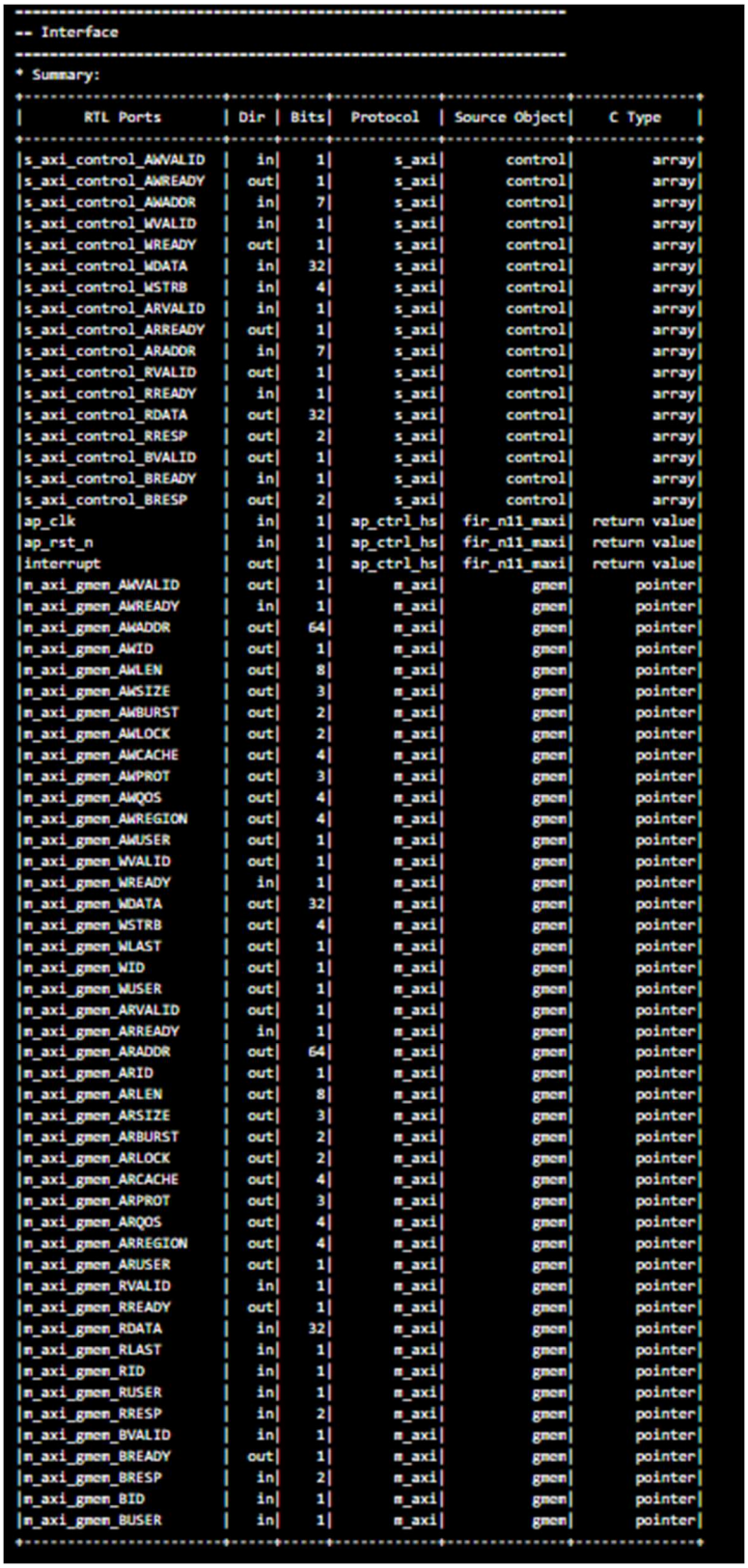
| Name | LUT | Input Size | Bits | Total Bits |
|---|---|---|---|---|
| ap_NS_fsm | 26 | 5 | 1 | 5 |
| pstrmInput_TREADY_int_regslice | 9 | 2 | 1 | 2 |
| Total | 35 | 7 | 2 | 7 |

    * Register:

| Name | FF | LUT | Bits | Const Bits |
|---|---|---|---|---|
| ap_CS_fsm | 4 | 0 | 4 | 0 |
| grp_fir_n11_strm_Pipeline_XFER_LOOP_fu_118_ap_start_reg | 1 | 0 | 1 | 0 |
| tmp_reg_193 | 31 | 0 | 31 | 0 |
| Total | 36 | 0 | 36 | 0 |

3. Interface

MAXI:



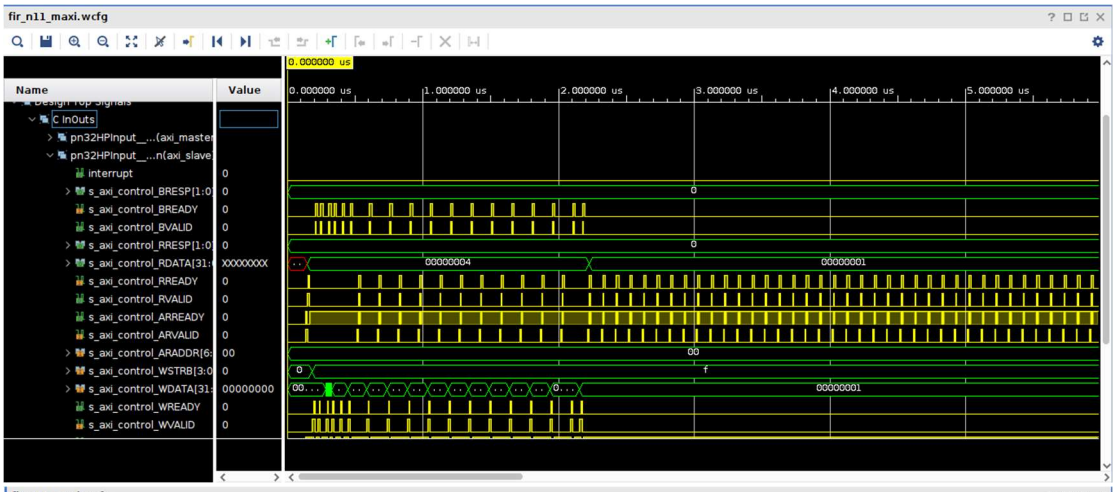
```
================================================================
== Interface
================================================================
* Summary:
+-----------------------+-----+-----+------------+--------------+--------------+
|       RTL Ports       | Dir | Bits|  Protocol  | Source Object|    C Type    |
+-----------------------+-----+-----+------------+--------------+--------------+
|s_axi_control_AWVALID  |   in|    1|       s_axi|       control|         array|
|s_axi_control_AWREADY  |  out|    1|       s_axi|       control|         array|
|s_axi_control_AWADDR   |   in|    7|       s_axi|       control|         array|
|s_axi_control_WVALID   |   in|    1|       s_axi|       control|         array|
|s_axi_control_WREADY   |  out|    1|       s_axi|       control|         array|
|s_axi_control_WDATA    |   in|   32|       s_axi|       control|         array|
|s_axi_control_WSTRB    |   in|    4|       s_axi|       control|         array|
|s_axi_control_ARVALID  |   in|    1|       s_axi|       control|         array|
|s_axi_control_ARREADY  |  out|    1|       s_axi|       control|         array|
|s_axi_control_ARADDR   |   in|    7|       s_axi|       control|         array|
|s_axi_control_RVALID   |  out|    1|       s_axi|       control|         array|
|s_axi_control_RREADY   |   in|    1|       s_axi|       control|         array|
|s_axi_control_RDATA    |  out|   32|       s_axi|       control|         array|
|s_axi_control_RRESP    |  out|    2|       s_axi|       control|         array|
|s_axi_control_BVALID   |  out|    1|       s_axi|       control|         array|
|s_axi_control_BREADY   |   in|    1|       s_axi|       control|         array|
|s_axi_control_BRESP    |  out|    2|       s_axi|       control|         array|
|ap_clk                 |   in|    1|  ap_ctrl_hs|  fir_n11_maxi|  return value|
|ap_rst_n               |   in|    1|  ap_ctrl_hs|  fir_n11_maxi|  return value|
|interrupt              |  out|    1|  ap_ctrl_hs|  fir_n11_maxi|  return value|
|m_axi_gmem_AWVALID     |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWREADY     |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWADDR      |  out|   64|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWID        |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWLEN       |  out|    8|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWSIZE      |  out|    3|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWBURST     |  out|    2|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWLOCK      |  out|    2|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWCACHE     |  out|    4|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWPROT      |  out|    3|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWQOS       |  out|    4|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWREGION    |  out|    4|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWUSER      |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_WVALID      |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_WREADY      |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_WDATA       |  out|   32|       m_axi|          gmem|       pointer|
|m_axi_gmem_WSTRB       |  out|    4|       m_axi|          gmem|       pointer|
|m_axi_gmem_WLAST       |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_WID         |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_WUSER       |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARVALID     |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARREADY     |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARADDR      |  out|   64|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARID        |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARLEN       |  out|    8|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARSIZE      |  out|    3|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARBURST     |  out|    2|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARLOCK      |  out|    2|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARCACHE     |  out|    4|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARPROT      |  out|    3|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARQOS       |  out|    4|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARREGION    |  out|    4|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARUSER      |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_RVALID      |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_RREADY      |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_RDATA       |   in|   32|       m_axi|          gmem|       pointer|
|m_axi_gmem_RLAST       |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_RID         |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_RUSER       |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_RRESP       |   in|    2|       m_axi|          gmem|       pointer|
|m_axi_gmem_BVALID      |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_BREADY      |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_BRESP       |   in|    2|       m_axi|          gmem|       pointer|
|m_axi_gmem_BID         |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_BUSER       |   in|    1|       m_axi|          gmem|       pointer|
+-----------------------+-----+-----+------------+--------------+--------------+
```

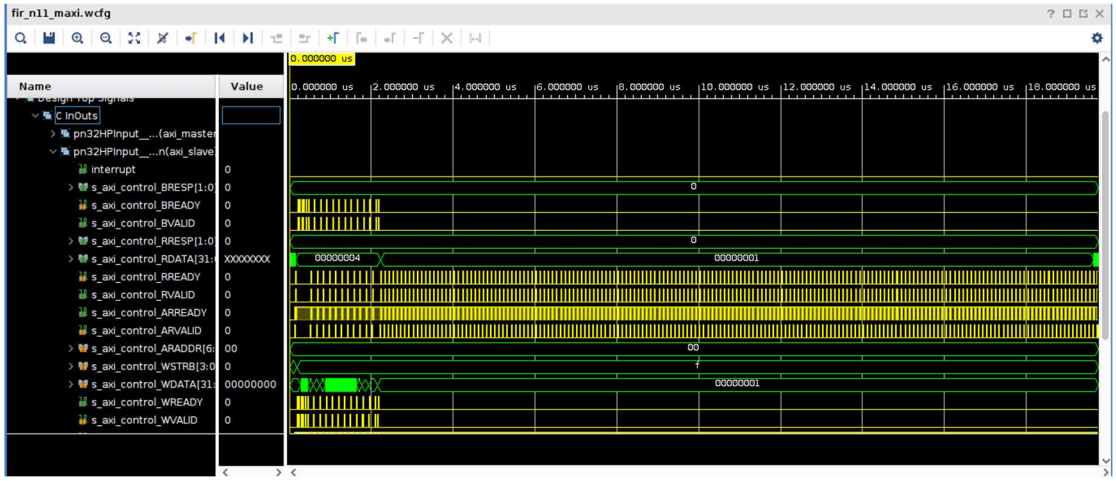
Stream:

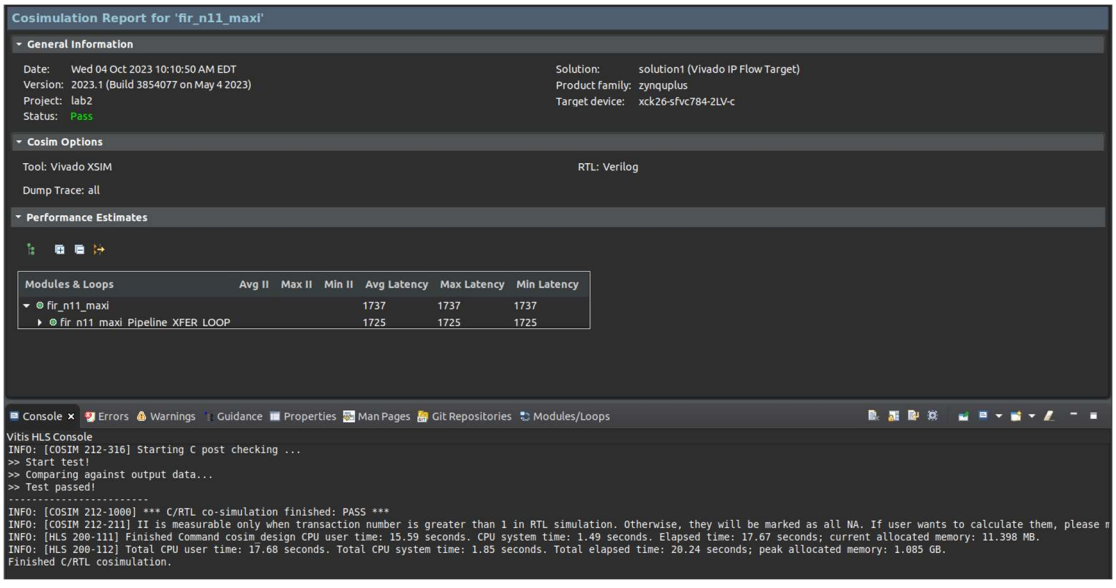
```
================================================================
== Interface
================================================================
* Summary:
+-----------------------+-----+-----+------------+---------------------+-------------+
|       RTL Ports       | Dir | Bits|  Protocol  |     Source Object   |    C Type   |
+-----------------------+-----+-----+------------+---------------------+-------------+
|s_axi_control_AWVALID  |   in|    1|      s_axi|              control|        array|
|s_axi_control_AWREADY  |  out|    1|      s_axi|              control|        array|
|s_axi_control_AWADDR   |   in|    7|      s_axi|              control|        array|
|s_axi_control_WVALID   |   in|    1|      s_axi|              control|        array|
|s_axi_control_WREADY   |  out|    1|      s_axi|              control|        array|
|s_axi_control_WDATA    |   in|   32|      s_axi|              control|        array|
|s_axi_control_WSTRB    |   in|    4|      s_axi|              control|        array|
|s_axi_control_ARVALID  |   in|    1|      s_axi|              control|        array|
|s_axi_control_ARREADY  |  out|    1|      s_axi|              control|        array|
|s_axi_control_ARADDR   |   in|    7|      s_axi|              control|        array|
|s_axi_control_RVALID   |  out|    1|      s_axi|              control|        array|
|s_axi_control_RREADY   |   in|    1|      s_axi|              control|        array|
|s_axi_control_RDATA    |  out|   32|      s_axi|              control|        array|
|s_axi_control_RRESP    |  out|    2|      s_axi|              control|        array|
|s_axi_control_BVALID   |  out|    1|      s_axi|              control|        array|
|s_axi_control_BREADY   |   in|    1|      s_axi|              control|        array|
|s_axi_control_BRESP    |  out|    2|      s_axi|              control|        array|
|ap_clk                 |   in|    1|ap_ctrl_hs|          fir_n11_strm| return value|
|ap_rst_n               |   in|    1|ap_ctrl_hs|          fir_n11_strm| return value|
|interrupt              |  out|    1|ap_ctrl_hs|          fir_n11_strm| return value|
|pstrmInput_TDATA       |   in|   32|      axis|  pstrmInput_V_data_V|      pointer|
|pstrmInput_TVALID      |   in|    1|      axis|  pstrmInput_V_dest_V|      pointer|
|pstrmInput_TREADY      |  out|    1|      axis|  pstrmInput_V_dest_V|      pointer|
|pstrmInput_TDEST       |   in|    1|      axis|  pstrmInput_V_dest_V|      pointer|
|pstrmInput_TKEEP       |   in|    4|      axis|  pstrmInput_V_keep_V|      pointer|
|pstrmInput_TSTRB       |   in|    4|      axis|  pstrmInput_V_strb_V|      pointer|
|pstrmInput_TUSER       |   in|    1|      axis|  pstrmInput_V_user_V|      pointer|
|pstrmInput_TLAST       |   in|    1|      axis|  pstrmInput_V_last_V|      pointer|
|pstrmInput_TID         |   in|    1|      axis|    pstrmInput_V_id_V|      pointer|
|pstrmOutput_TDATA      |  out|   32|      axis| pstrmOutput_V_data_V|      pointer|
|pstrmOutput_TVALID     |  out|    1|      axis| pstrmOutput_V_dest_V|      pointer|
|pstrmOutput_TREADY     |   in|    1|      axis| pstrmOutput_V_dest_V|      pointer|
|pstrmOutput_TDEST      |  out|    1|      axis| pstrmOutput_V_dest_V|      pointer|
|pstrmOutput_TKEEP      |  out|    4|      axis| pstrmOutput_V_keep_V|      pointer|
|pstrmOutput_TSTRB      |  out|    4|      axis| pstrmOutput_V_strb_V|      pointer|
|pstrmOutput_TUSER      |  out|    1|      axis| pstrmOutput_V_user_V|      pointer|
|pstrmOutput_TLAST      |  out|    1|      axis| pstrmOutput_V_last_V|      pointer|
|pstrmOutput_TID        |  out|    1|      axis|   pstrmOutput_V_id_V|      pointer|
+-----------------------+-----+-----+------------+---------------------+-------------+
```

4. Co-simulation transcript/waveform

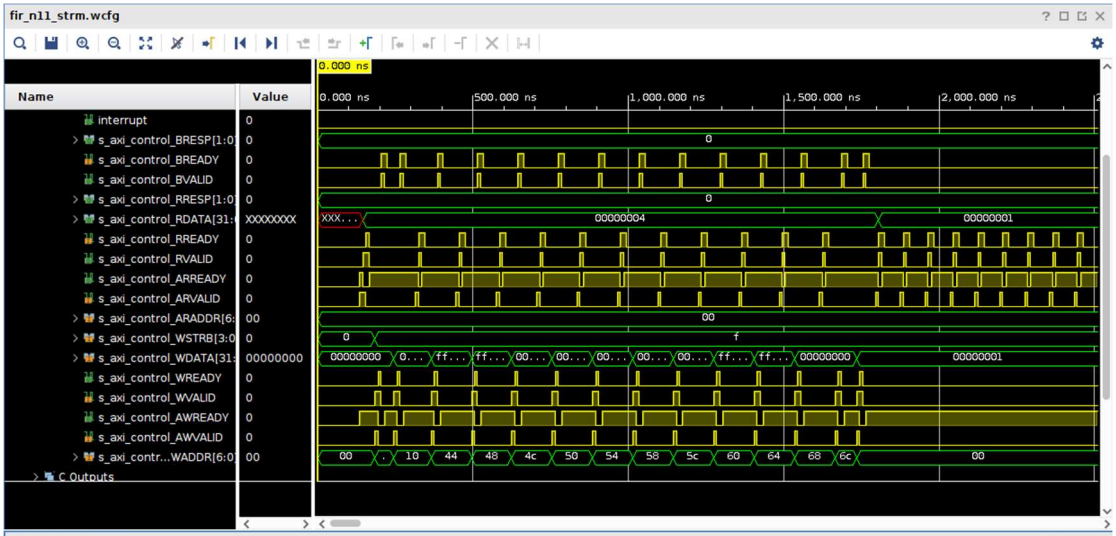
MAXI:

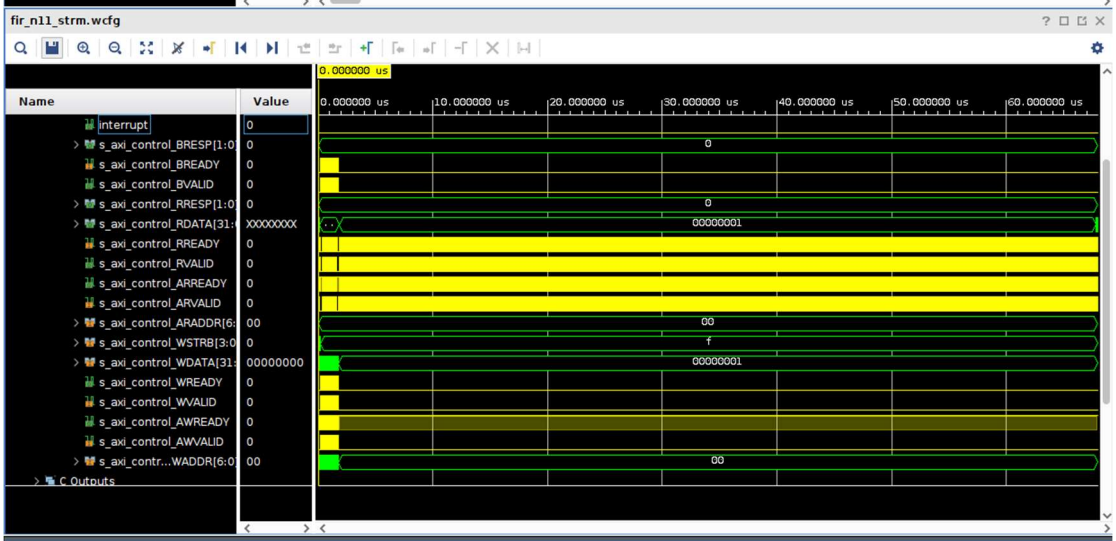


Stream:




**Cosimulation Report for 'fir_n11_strm'**

**General Information**

Date: Wed 04 Oct 2023 09:12:49 AM EDT
Version: 2023.1 (Build 3854077 on May 4 2023)
Project: lab2
Status: Pass

Solution: solution1 (Vivado IP Flow Target)
Product family: zynquplus
Target device: xck26-sfvc784-2LV-c

**Cosim Options**

Tool: Vivado XSIM
RTL: Verilog
Dump Trace: all

**Performance Estimates**

| Modules & Loops | Avg II | Max II | Min II | Avg Latency | Max Latency | Min Latency |
|---|---|---|---|---|---|---|
| fir_n11_strm | | | | 6603 | 6603 | 6603 |
| fir_n11_strm_Pipeline_XFER_LOOP | | | | 6600 | 6600 | 6600 |

Console | Errors | Warnings | Guidance | Properties | Man Pages | Git Repositories | Modules/Loops

23 Guidance-Infos | 7 Guidance-Warnings | 0 Guidance-Errors

| Name | Web Help | Details |
|---|---|---|
| All Categories | | |
| SCHEDULE | | |
| [HLS 200-885] | LINK | The II Violation in module 'fir_n11_strm_Pipeline_XFER_LOOP' (loop 'XFER_LOOP'): Unable to schedule 'load' operation ('an32Coef_load', ../hls_FIRN11Stream/FIR.cpp:35) on array 'an32Coef' due to limited memory ports (II = 1). Please consider using a memory core with more ports or partitioning the array 'an32Coef'. |

solution1

5. Jupyter Notebook execution results

MAXI:

2023/10/4 晚上10:51 FIRN11MAXI - Jupyter Notebook

In [1]:

```
# coding: utf-8

# In[ ]:


from __future__ import print_function

import sys, os
import numpy as np
from time import time
import matplotlib.pyplot as plt

sys.path.append('/home/xilinx')
os.environ['XILINX_XRT'] = '/usr'
from pynq import Overlay
from pynq import allocate

if __name__ == "__main__":
    print("Entry:", sys.argv[0])
    print("System argument(s):", len(sys.argv))

    print("Start of \"" + sys.argv[0] + "\"")

    ol = Overlay("FIRN11MAXI.bit")
    ipFIRN11 = ol.fir_n11_maxi_0

    fiSamples = open("samples_triangular_wave.txt", "r+")
    numSamples = 0
    line = fiSamples.readline()
    while line:
        numSamples = numSamples + 1
        line = fiSamples.readline()

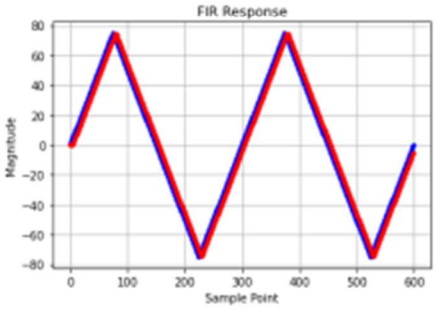
    inBuffer0 = allocate(shape=(numSamples,), dtype=np.int32)
    outBuffer0 = allocate(shape=(numSamples,), dtype=np.int32)
    fiSamples.seek(0)
    for i in range(numSamples):
        line = fiSamples.readline()
        inBuffer0[i] = int(line)
    fiSamples.close()

    numTaps = 11
    n32Taps = [0, -10, -9, 23, 56, 63, 56, 23, -9, -10, 0]
    #n32Taps = [1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1]
    n32DCGain = 0
    timeKernelStart = time()
    for i in range(numTaps):
        n32DCGain = n32DCGain + n32Taps[i]
        ipFIRN11.write(0x40 + i * 4, n32Taps[i])
    if n32DCGain < 0:
        n32DCGain = 0 - n32DCGain
    ipFIRN11.write(0x28, len(inBuffer0) * 4)
    ipFIRN11.write(0x10, inBuffer0.device_address)
    ipFIRN11.write(0x1C, outBuffer0.device_address)
    ipFIRN11.write(0x00, 0x01)
    while (ipFIRN11.read(0x00) & 0x4) == 0x0:
        continue
    timeKernelEnd = time()
    print("Kernel execution time: " + str(timeKernelEnd - timeKernelStart) +
```

```
    plt.title("FIR Response")
    plt.xlabel("Sample Point")
    plt.ylabel("Magnitude")
    xSeq = range(len(inBuffer0))
    if n32DCGain == 0:
        plt.plot(xSeq, inBuffer0, 'b.', xSeq, outBuffer0, 'r.')
    else:
        plt.plot(xSeq, inBuffer0, 'b.', xSeq, outBuffer0 / n32DCGain, 'r.')
    plt.grid(True)
    plt.show() # In Jupyter, press Tab + Shift keys to show plot then redo r

    print("============================")
    print("Exit process")
```

```
Entry: /usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_la
uncher.py
System argument(s): 3
Start of "/usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel
_launcher.py"
Kernel execution time: 0.0002789497375488281 s
```




```
============================
Exit process
```

Stream:

In [1]:

```
# coding: utf-8

# In[3]:


from __future__ import print_function

import sys, os
import numpy as np
from time import time
import matplotlib.pyplot as plt

sys.path.append('/home/xilinx')
os.environ['XILINX_XRT'] = '/usr'
from pynq import Overlay
from pynq import allocate

if __name__ == "__main__":
    print("Entry:", sys.argv[0])
    print("System argument(s):", len(sys.argv))

    print("Start of \"" + sys.argv[0] + "\"")

    ol = Overlay("/home/root/jupyter_notebooks/FIRN11Stream.bit")
    ipFIRN11 = ol.fir_n11_strm_0
    ipDMAIn = ol.axi_dma_in_0
    ipDMAOut = ol.axi_dma_out_0

    fiSamples = open("samples_triangular_wave.txt", "r+")
    numSamples = 0
    line = fiSamples.readline()
    while line:
        numSamples = numSamples + 1
        line = fiSamples.readline()

    inBuffer0 = allocate(shape=(numSamples,), dtype=np.int32)
    outBuffer0 = allocate(shape=(numSamples,), dtype=np.int32)
    fiSamples.seek(0)
    for i in range(numSamples):
        line = fiSamples.readline()
        inBuffer0[i] = int(line)
    fiSamples.close()

    numTaps = 11
    n32Taps = [0, -10, -9, 23, 56, 63, 56, 23, -9, -10, 0]
    #n32Taps = [1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1]
    n32DCGain = 0
    timeKernelStart = time()
    for i in range(numTaps):
        n32DCGain = n32DCGain + n32Taps[i]
        ipFIRN11.write(0x40 + i * 4, n32Taps[i])
    if n32DCGain < 0:
        n32DCGain = 0 - n32DCGain
    ipFIRN11.write(0x10, len(inBuffer0) * 4)
    ipFIRN11.write(0x00, 0x01)
    ipDMAIn.sendchannel.transfer(inBuffer0)
    ipDMAOut.recvchannel.transfer(outBuffer0)
    ipDMAIn.sendchannel.wait()
    ipDMAOut.recvchannel.wait()
    timeKernelEnd = time()
    print("Kernel execution time: " + str(timeKernelEnd - timeKernelSta
```





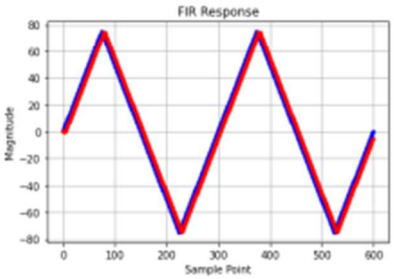
```
    print("Kernel execution time: " + str(timeKernelEnd - timeKernelSta

    plt.title("FIR Response")
    plt.xlabel("Sample Point")
    plt.ylabel("Magnitude")
    xSeq = range(len(inBuffer0))
    if n32DCGain == 0:
        plt.plot(xSeq, inBuffer0, 'b.', xSeq, outBuffer0, 'r.')
    else:
        plt.plot(xSeq, inBuffer0, 'b.', xSeq, outBuffer0 / n32DCGain, '
    plt.grid(True)
    plt.show() # In Jupyter, press Tab + Shift keys to show plot then r

    print("============================")
    print("Exit process")


```

```
Entry: /usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_la
uncher.py
System argument(s): 3
Start of "/usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel
_launcher.py"
Kernel execution time: 0.0008580684661865234 s
```




```
============================
Exit process
```

In [ ]: