FPGA系統設計\_第二章\_訊號定義

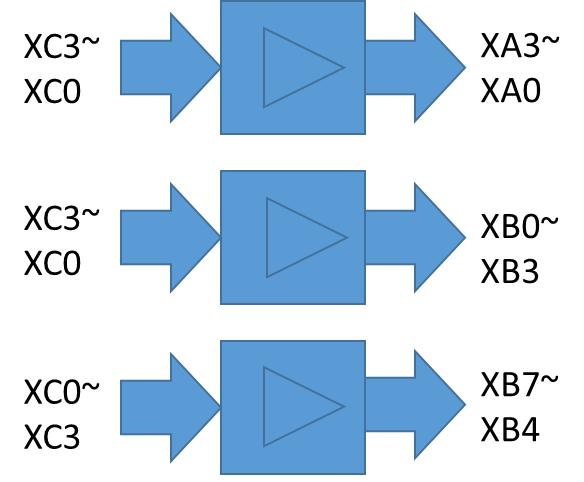
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# **objective- THE PROBLEM AND PURPOSE**

VHDL程式在邏輯訊號和數值訊號兩方面都有豐富和精確的定義，此實驗係練習序列訊號的定義與使用。

# **procedure – DESIGN methods**

## 內部電路設計 :



## 說明 :

XC3~ XC0為輸入，XA0~ XA3 XB0~XB7為輸出，當按鍵OFF時，LED燈滅；當按鍵ON時，LED燈亮。

# **simulation results**

## program codes

### **ch02.vhd**

library IEEE;

use IEEE.std\_logic\_1164.all;

use IEEE.std\_logic\_arith.all;

entity CH02 is

port

( XA : out STD\_LOGIC\_VECTOR (0 to 3);

XB : out UNSIGNED (7 downto 0);

XC : in STD\_LOGIC\_VECTOR (3 downto 0)

);

end CH02;

architecture CH02\_ARCH of CH02 is

begin

XA(3) <= XC(3);

XA(2) <= XC(2);

XA(1) <= XC(1);

XA(0) <= XC(0);

XB(0) <= XC(3);

XB(1) <= XC(2);

XB(2) <= XC(1);

XB(3) <= XC(0);

XB(0) <= XC(7);

XB(1) <= XC(6);

XB(2) <= XC(5);

XB(3) <= XC(4);

end CH02\_ARCH;

### **ch02.ucf**

NET XA<0> LOC = N2;

NET XA<1> LOC = T1;

NET XA<2> LOC = T2;

NET XA<3> LOC = U2;

NET XB<0> LOC = M3;

NET XB<1> LOC = M4;

NET XB<2> LOC = W3;

NET XB<3> LOC = W4;

NET XB<4> LOC = Y3;

NET XB<5> LOC = Y4;

NET XB<6> LOC = W6;

NET XB<7> LOC = Y6;

NET XC<0> LOC = V1;

NET XC<1> LOC = V2;

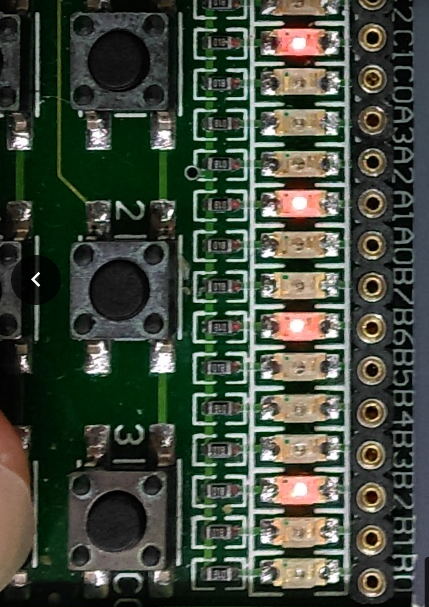
NET XC<2> LOC = W1;

NET XC<3> LOC = W2;

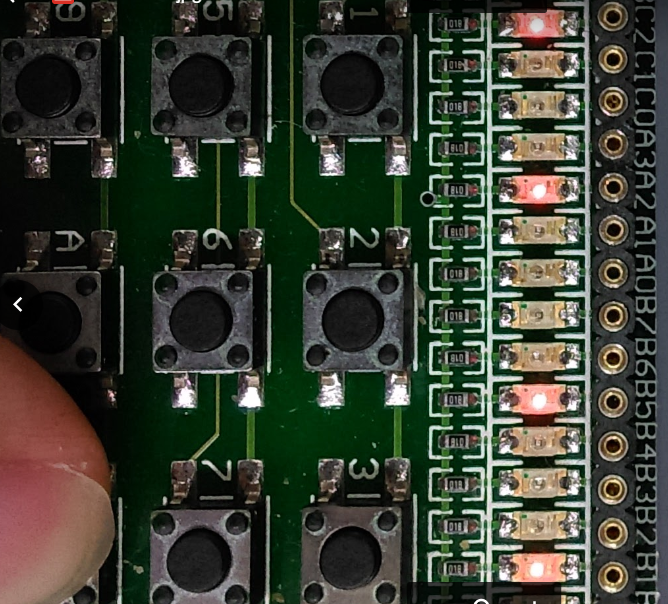
## observations

### 按鍵C0 ON時，A0 B7 B3亮

### 按鍵C1 ON時，A1 B6 B2亮



### 按鍵C2ON時，A2 B5 B1亮



### 按鍵C3 ON時，A3 B4 B0亮

