FPGA系統設計\_第三章\_邏輯處理

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# **objective- THE PROBLEM AND PURPOSE**

本實驗以標準解碼器電路為例，練習基本邏輯的處理方法。

# **procedure – DESIGN methods**

## 內部電路設計(以真值表定義輸入輸出邏輯關係):



輸出為0時，LED燈亮，此真值表輸出1多0少，故採用輸出反向表示法

# **simulation results**

## program codes

### **ch03.vhd**

library IEEE;

use IEEE.std\_logic\_1164.all;

use IEEE.std\_logic\_arith.all;

use IEEE.std\_logic\_unsigned.all;

entity CH03 is

port

( XB : out STD\_LOGIC\_VECTOR (7 downto 0);

XC : in STD\_LOGIC\_VECTOR (3 downto 0)

);

end CH03;

architecture CH03\_ARCH of CH03 is

begin

XB(0) <= not((XC(3) and not XC(2) and not XC(1) and not XC(0)) or (XC(3) and XC(2) and XC(1) and XC(0))); --1000 1111

XB(1) <= not((XC(3) and not XC(2) and not XC(1) and XC(0)) or (XC(3) and XC(2) and XC(1) and not XC(0)); --1001 1110

XB(2) <= not((XC(3) and not XC(2) and XC(1) and not XC(0)) or (XC(3) and XC(2) and not XC(1) and XC(0))); --1010 1101

XB(3) <= not((XC(3) and not XC(2) and XC(1) and XC(0)) or (XC(3) and XC(2) and not XC(1) and not XC(0)); --1011 1100

XB(4) <= not((XC(3) and XC(2) and not XC(1) and not XC(0)) or (XC(3) and not XC(2) and XC(1) and XC(0))); --1100 1011

XB(5) <= not((XC(3) and XC(2) and not XC(1) and XC(0)) or (XC(3) and not XC(2) and XC(1) and not XC(0))); --1101 1010

XB(6) <= not((XC(3) and XC(2) and XC(1) and not XC(0)) or (XC(3) and not XC(2) and not XC(1) and XC(0))); --1110 1001

XB(7) <= not((XC(3) and XC(2) and XC(1) and XC(0)) or (XC(3) and not XC(2) and not XC(1) and not XC(0))); --1111 1000

end CH03\_ARCH;

### **ch03.ucf**

NET XB<0> LOC = M3;

NET XB<1> LOC = M4;

NET XB<2> LOC = W3;

NET XB<3> LOC = W4;

NET XB<4> LOC = Y3;

NET XB<5> LOC = Y4;

NET XB<6> LOC = W6;

NET XB<7> LOC = Y6;

NET XC<0> LOC = V1;

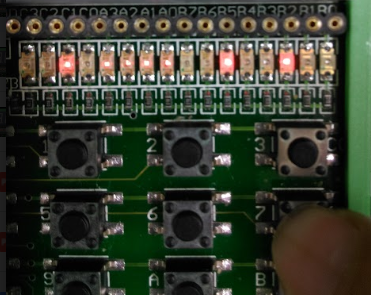
NET XC<1> LOC = V2;

NET XC<2> LOC = W1;

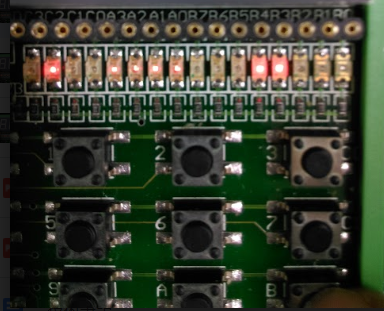
NET XC<3> LOC = W2;

## observations

### 按鍵XC1 ON時，B5 B2亮



### 按鍵XC2 ON時，B3 B4亮



### 按鍵XC0 ON時，B6 B1亮

