FPGA系統設計\_第四章\_序列處理

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# **objective- THE PROBLEM AND PURPOSE**

本實驗以查表邏輯法，將第三章實驗之電路重新設計。

# **procedure – DESIGN methods**

## 內部電路設計(以真值表定義輸入輸出邏輯關係):



輸出為0時，LED燈亮。

# **simulation results**

## program codes

### **ch04.vhd**

library IEEE;

use IEEE.std\_logic\_1164.all;

use IEEE.std\_logic\_arith.all;

use IEEE.std\_logic\_unsigned.all;

entity CH04 is

port

( XB : out STD\_LOGIC\_VECTOR (7 downto 0);

XC : in STD\_LOGIC\_VECTOR (3 downto 0)

);

end CH04;

architecture CH04\_ARCH of CH04 is

begin

XB <= "01111110" when XC="1000" else

"1011101" when XC="1001" else

"11011011" when XC="1010" else

"11100111" when XC="1011" else

"11100111" when XC="1100" else

"11011011" when XC="1101" else

"10111101" when XC="1110" else

"01111110" when XC="1111" else

"11111111";

end CH04\_ARCH;

### **ch04.ucf**

NET XB<0> LOC = M3;

NET XB<1> LOC = M4;

NET XB<2> LOC = W3;

NET XB<3> LOC = W4;

NET XB<4> LOC = Y3;

NET XB<5> LOC = Y4;

NET XB<6> LOC = W6;

NET XB<7> LOC = Y6;

NET XC<0> LOC = V1;

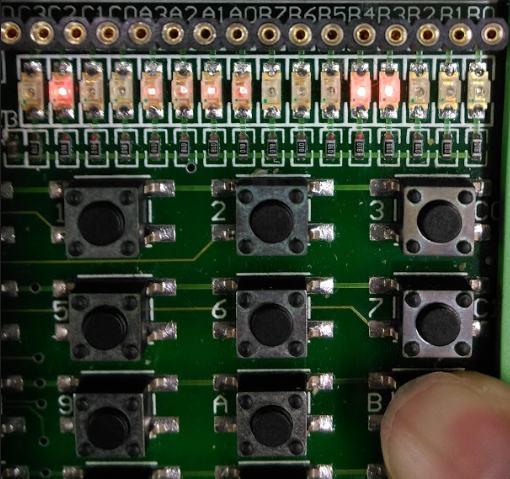
NET XC<1> LOC = V2;

NET XC<2> LOC = W1;

NET XC<3> LOC = W2;

## observations

### 按鍵XC2 ON時，B4 B3亮



### 按鍵XC0 XC1 XC2 ON時，B7 B0亮

