Nand Flash & FTL Introduction

廖偉翔

David Liao

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Outline

Introduction

Introduction

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2D/3D structure

SLC/MLC/TLC/QLC comparison

High ← endurance → Low

Low → capacity → High
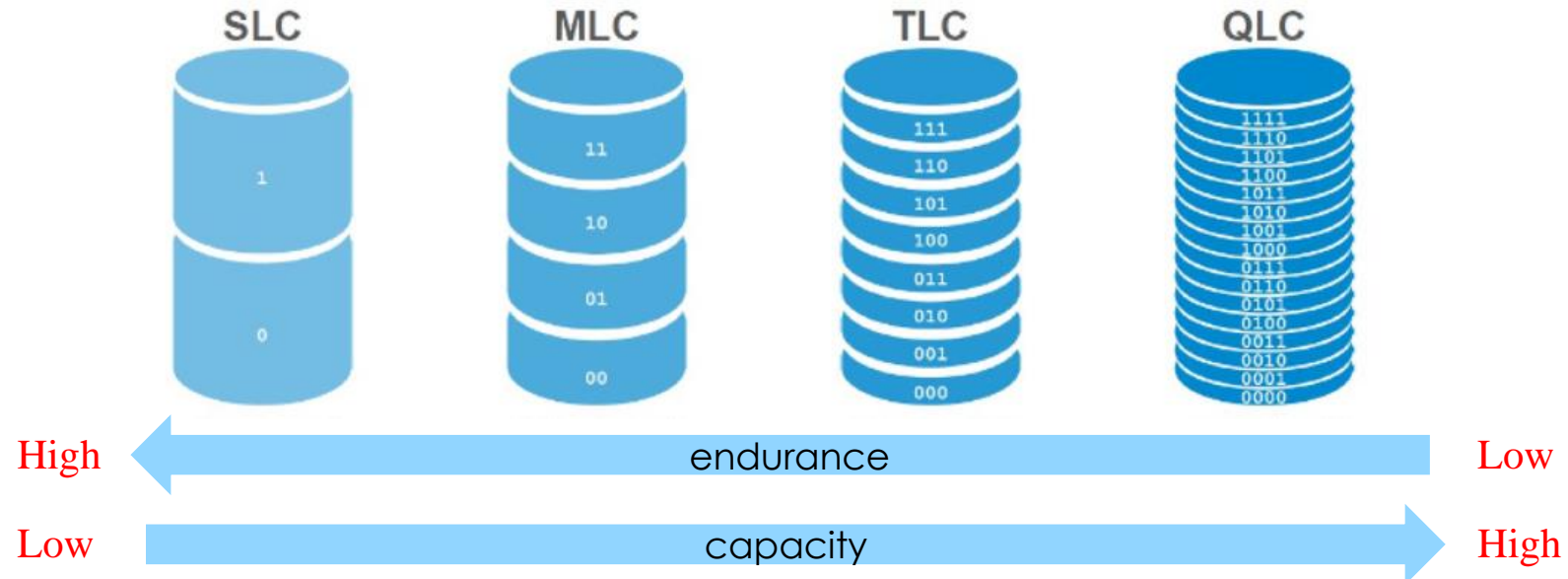
Memory Organization

Memory Organization

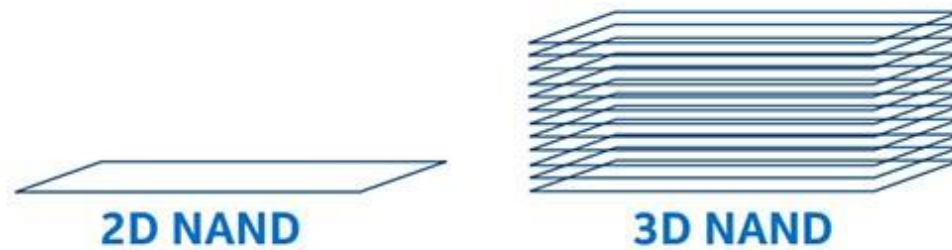**cell** — The smallest storage unit for flash memory.

page — The smallest addressable unit for the read operation.

WL — The smallest addressable unit for the program operation.

block — The smallest addressable unit for the erase operation.

plane — The unit that consists of a number of blocks.

LUN — The minimum unit that can independently execute commands and report status.

target — An independent Flash memory component with its own $\overline{CE}$ signal.

device — The packaged flash memory unit.

Memory Organization

Page size : **18336 bytes** = **16K** + *spare area (Error Correction Coding, ECC)*
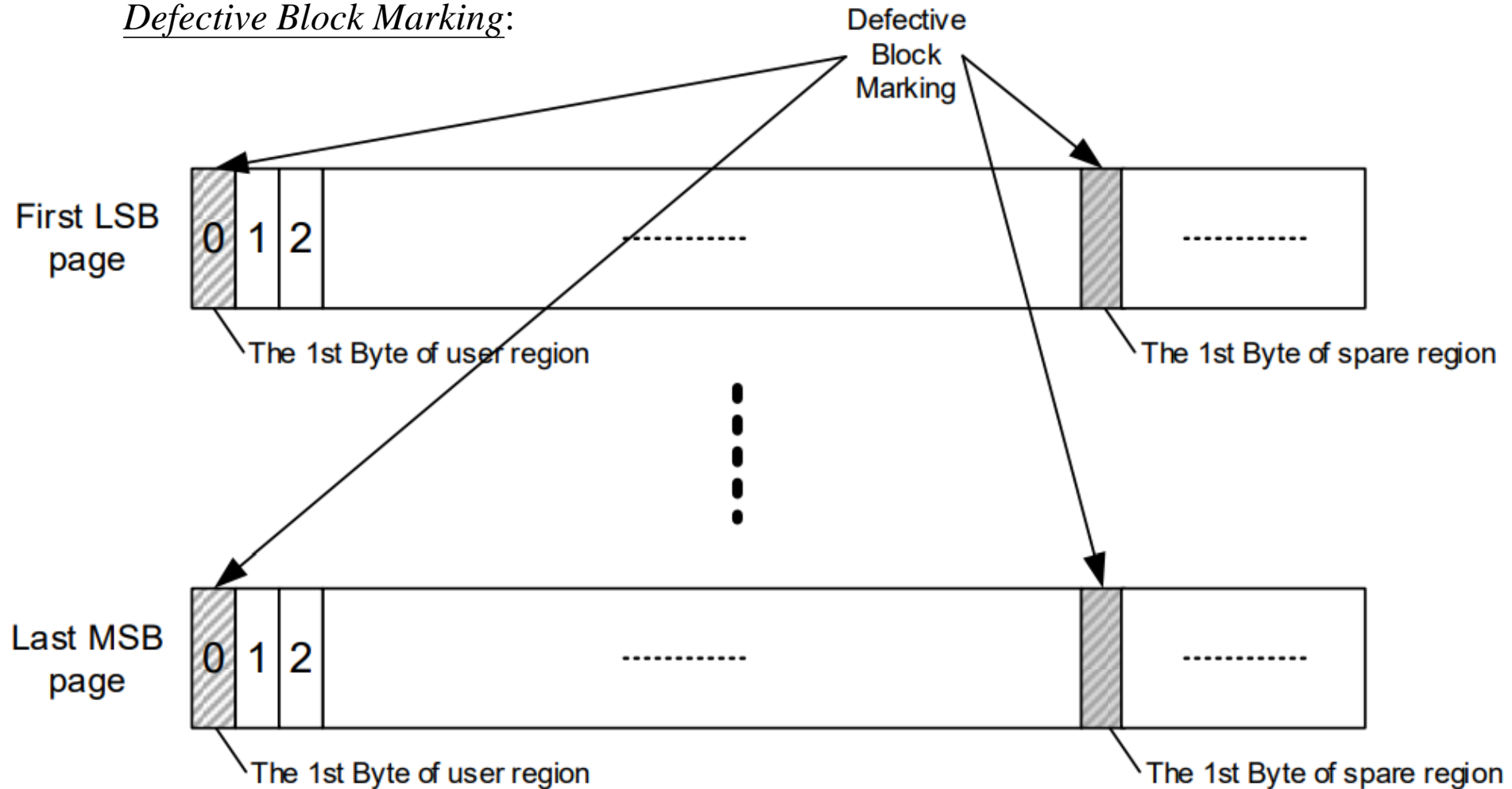
Device capacity **:16K * 768** *(pages)* ***2956** *(blocks)* *** 8** *(bits)* *** 2** *(targets) /* **(1024*1024)** *(Gb)*

= **554 Gb**

Parameter	TH58TFG9V23BA4C
Part number (T_{OPER}: 0~70°C)	TH58TFG9V23BA4C
Device capacity	18336 x 768 x 2956 x 8 x 2 bits
Page size	18336 Bytes
Block size	14082048 Bytes (768 Pages)
Plane size	20,813,266,944 Bytes (1478 Blocks)
Plane per one LUN	2 Planes
LUN per one target	1 LUN
Target per one device	2 targets
Number of valid blocks per a device (Min.)	5548
Number of valid blocks per a device (Max.)	5912
Package weight (Typ.)	0.40 g

Memory Organization

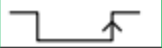*Defective Block Marking*:

Bus Operation

Bus Operation

→ Controller to Flash

← Flash to Controller

Pin Name	Pin Function
DQ[7:0] → ←	**DATA INPUTS/OUTPUTS** The DQ pins are used to input command, address and data and to output data during read operations. The DQ pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE →	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the DQ ports on the rising edge of the $\overline{WE}$ signal.
ALE →	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high.
$\overline{CE}$ →	**CHIP ENABLE** The $\overline{CE}$ input is the device selection control. When the device is in the Busy state, $\overline{CE}$ high is ignored, and the device does not return to standby mode in program or erase operation.
$\overline{RE}$, (RE) →	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active, drives the data onto the DQ bus. Data is valid after t_{DQSRE} of rising edge & falling edge of $\overline{RE}$ which also increments the internal column address counter by each one. The Read Enable $\overline{RE}$ is paired with differential signal RE to provide differential pair signaling to the system during reads.
$\overline{WE}$ →	**WRITE ENABLE** The $\overline{WE}$ input controls writes to the DQ port. Commands, addresses are latched on the rising edge of the $\overline{WE}$ pulse.
$\overline{WP}$ →	**WRITE PROTECT** The $\overline{WP}$ pin provides inadvertent program/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.
R/$\overline{B}$ ←	**READY/BUSY OUTPUT** The R/$\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
DQS, ($\overline{DQS}$) → ←	**DATA STROBE** Output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS is paired with differential signal $\overline{DQS}$ to provide differential pair signaling to the system during reads and writes.

Bus Operation

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	DQS	$\overline{WP}$	Mode	
H	L	L	⌐_⌐	H	X	X	Read Mode	Command Input
L	H	L	⌐_⌐	H	X	X		Address Input(5 cycles)
H	L	L	⌐_⌐	H	X	H	Write Mode	Command Input
L	H	L	⌐_⌐	H	X	H		Address Input(5 cycles)
L	L	L	H	H	⌐_⌐	H	Data Input	
L	L	L	H	⌐_⌐	⌐_⌐	X	Data Output	
X	X	X	X	H	X	X	During Read(Busy)	
X	X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	X	H	During Erase(Busy)	
X	X	X	X	X	X	L	Write Protect	
X	X	H	X	X	X	H/L[3)]	Stand-by	
L	L	L	H	H	H/L	H	Bus Idle	

Bus Operation

Column Address (C1, C2):

Page size = 18336 bytes : 18336 > 2 ^ 14 (16384) , 15 bits are required (C1-0 to C2-6)

Row Address (R1, R2, R3):

WL address : 768 / 3 (TLC) = 256 = 2 ^ 8 (256) , 8 bits are required (R1-0 to R1-7)

**Blocks address** : 1478 per plane , 1478 * 2 = 2956 > 2 ^ 11 (2048) , 12 bits are required (R2-1 to R3-4)

LUN address: 2 , 1 bit is required (R3-5)

	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First cycle (Column address 1)	C1-7	C1-6	C1-5	C1-4	C1-3	C1-2	C1-1	C1-0
Second cycle (Column address 2)	L	C2-6	C2-5	C2-4	C2-3	C2-2	C2-1	C2-0
Third cycle (Row address 1)	R1-7	R1-6	R1-5	R1-4	R1-3	R1-2	R1-1	R1-0
Fourth cycle (Row address 2)	R2-7	R2-6	R2-5	R2-4	R2-3	R2-2	R2-1	R2-0
Fifth cycle (Row address 3)	L	L	L	R3-4	R3-3	R3-2	R3-1	R3-0

R1-0 to R1-7: WL address

R2-0 to R3-3: Block address
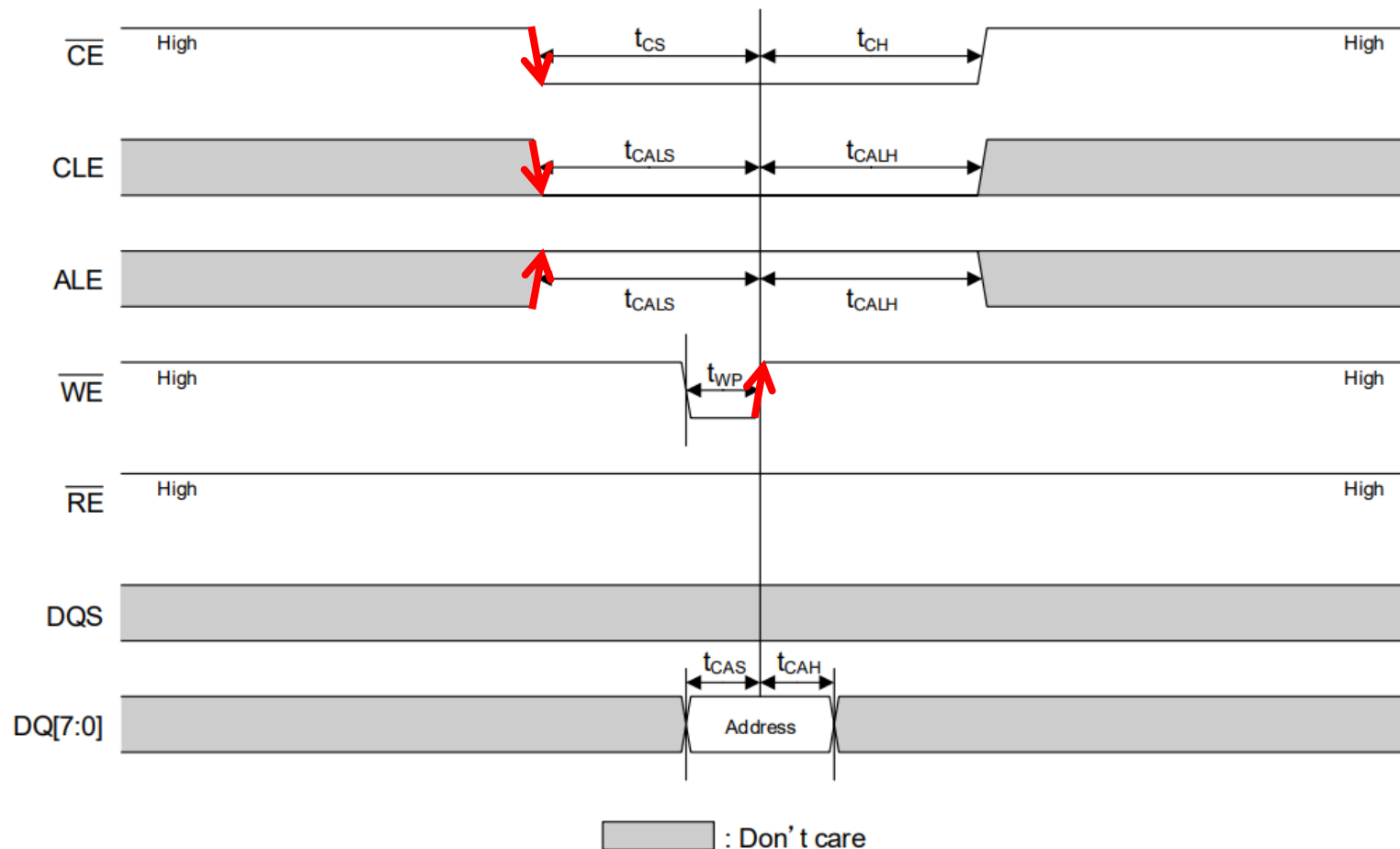
R3-4: LUN address (Note)

Bus Operation

- *Command Latch Cycle*
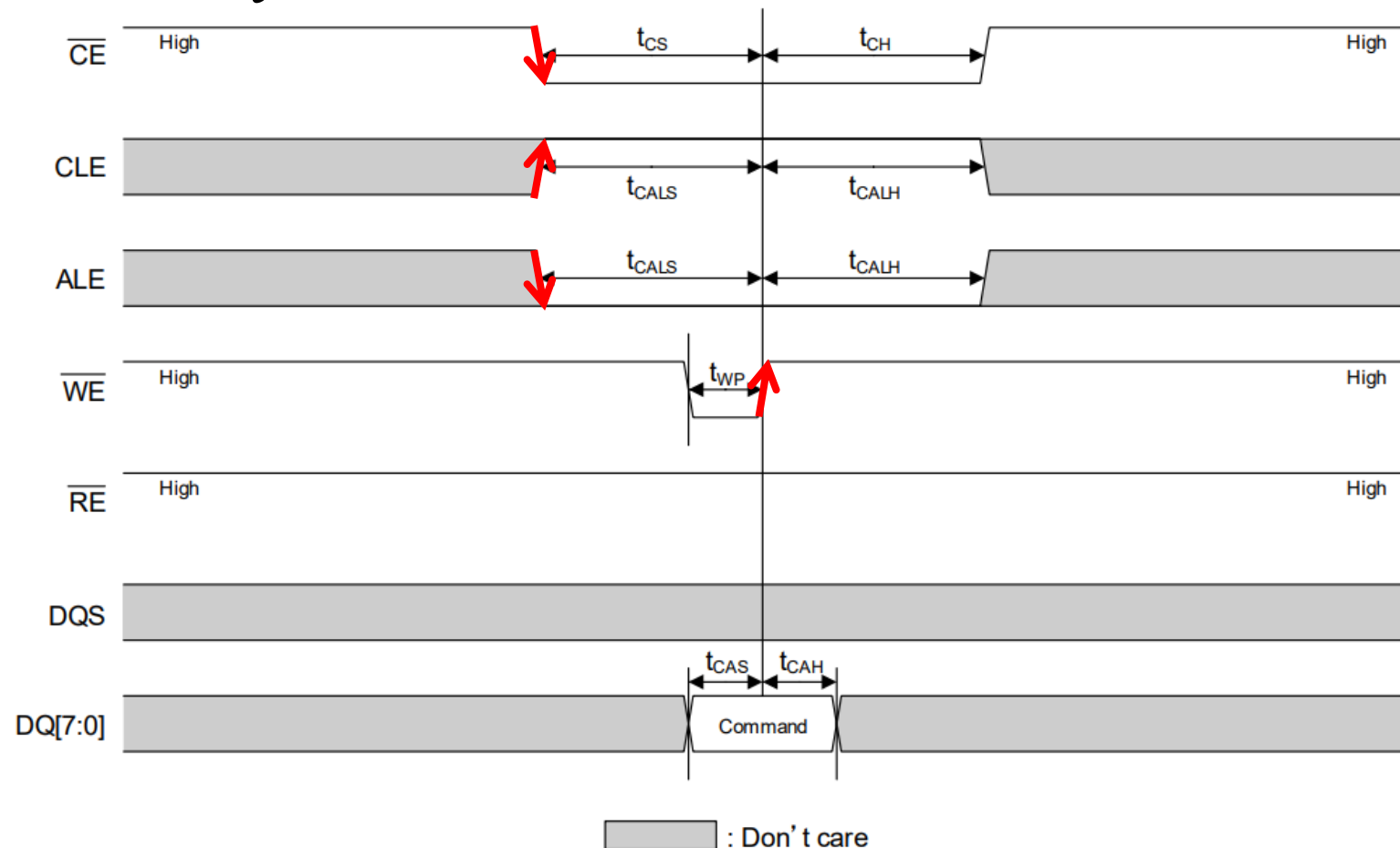
CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	DQS	DQ[7:0]	$\overline{WP}$
H	L	L	⌐_⌐	H	Z	input	X

Bus Operation

■ *Address Latch Cycle*

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	DQS	DQ[7:0]	$\overline{WP}$
L	H	L	⌐_⌐	H	Z	input	X

Bus Operation

- ***Basic Data Input Timing***
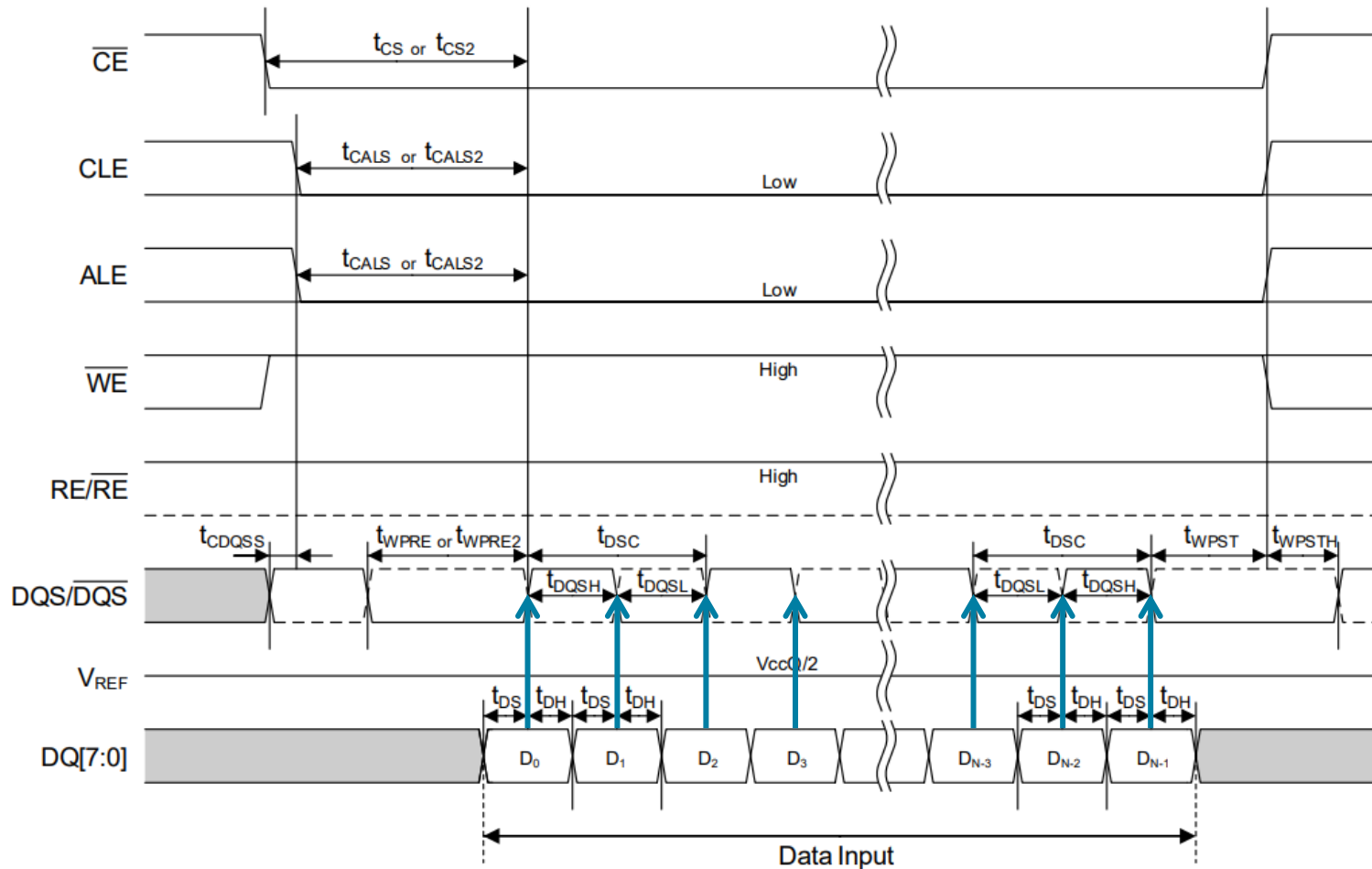
CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	DQS	DQ[7:0]	$\overline{WP}$
L	L	L	H	H	⌐⌐ ⌐⌐	input	H

Bus Operation

Basic Data Output Timing
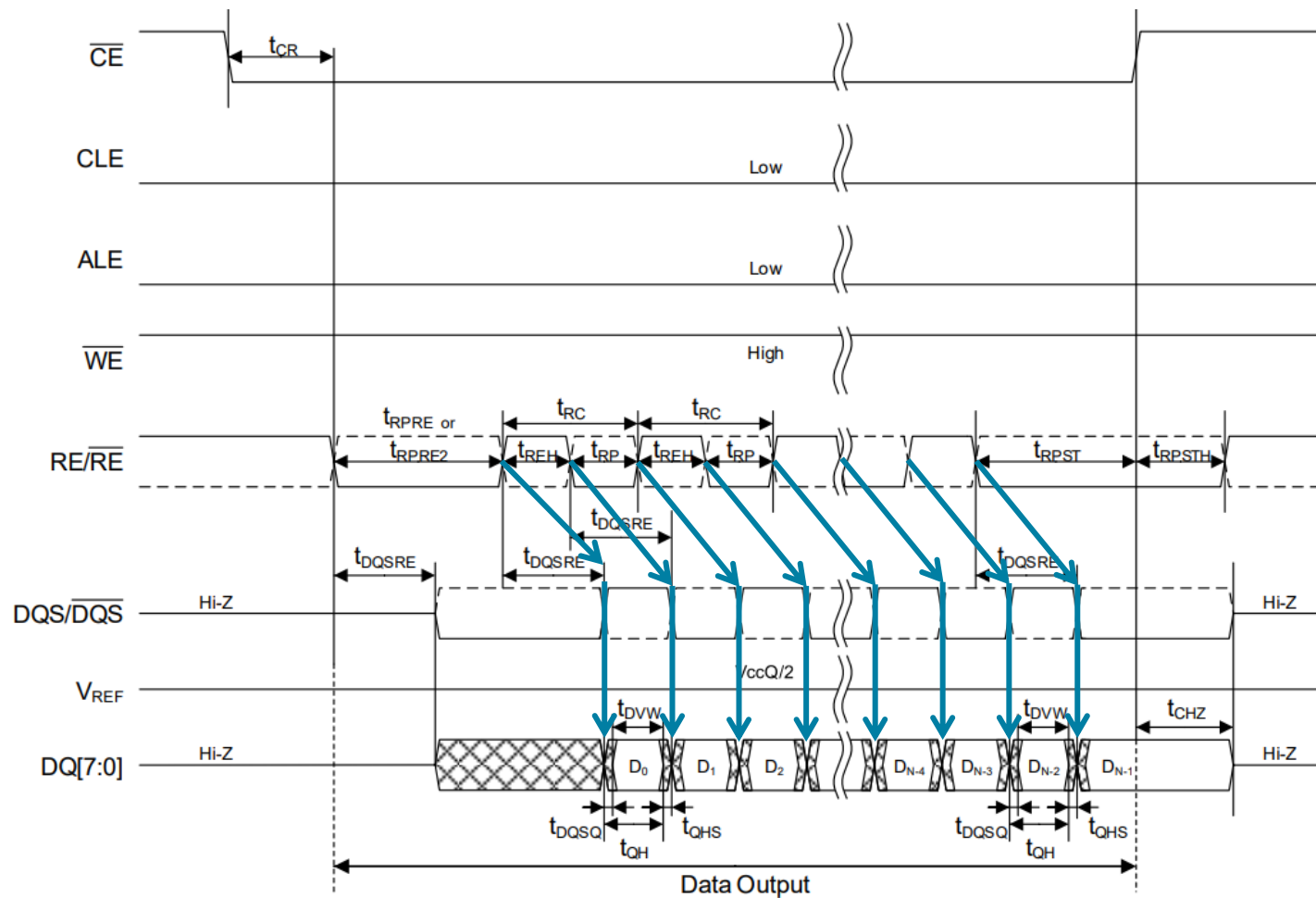
CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	DQS	DQ[7:0]	$\overline{WP}$
L	L	L	H	⎍⎎	⎍⎎	output	H

Device Operation

Device Operation

- **Basic Command Sets**

| Function	Primary or Secondary	1st Set	Address Cycles	2nd Set	Acceptable while Accessed LUN is Busy	Acceptable while Other LUNs are Busy
LSB Page Select [2]	-	01h	-	-		
CSB Page Select [2]	-	02h	-	-		
MSB Page Select [2]	-	03h	-	-		
Page Read	Primary	00h	5	30h		Y
Read Start for Last Page Cache Read	Primary	3Fh	-	-		
Random Cache Read	Primary	00h	5	31h		
Full Sequence Program	N/A	80h-1Ah	5	80h-10h		Y
Cache Full Sequence Program	N/A	80h-1Ah	5	80h-15h or 80h-10h		
Block Erase	Primary	60h	3	D0h		Y
Random Data Input [1]	Primary	85h	5	-		Y
Random Data Output [1]	Primary	05h	5	E0h		Y
Set Feature	Primary	EFh	1	-		
Get Feature	Primary	EEh	1	-		
Read ID	Primary	90h	1	-		
Read Status	Primary	70h	-	-	Y	Y
Read Status 2	Primary	71h	-	-	Y	Y
Read Status 3	Primary	73h	-	-	Y	Y
Reset	Primary	FFh	-	-	Y	Y
Reset LUN	-	FAh	3	-	Y	Y

- *Page Read Operation*
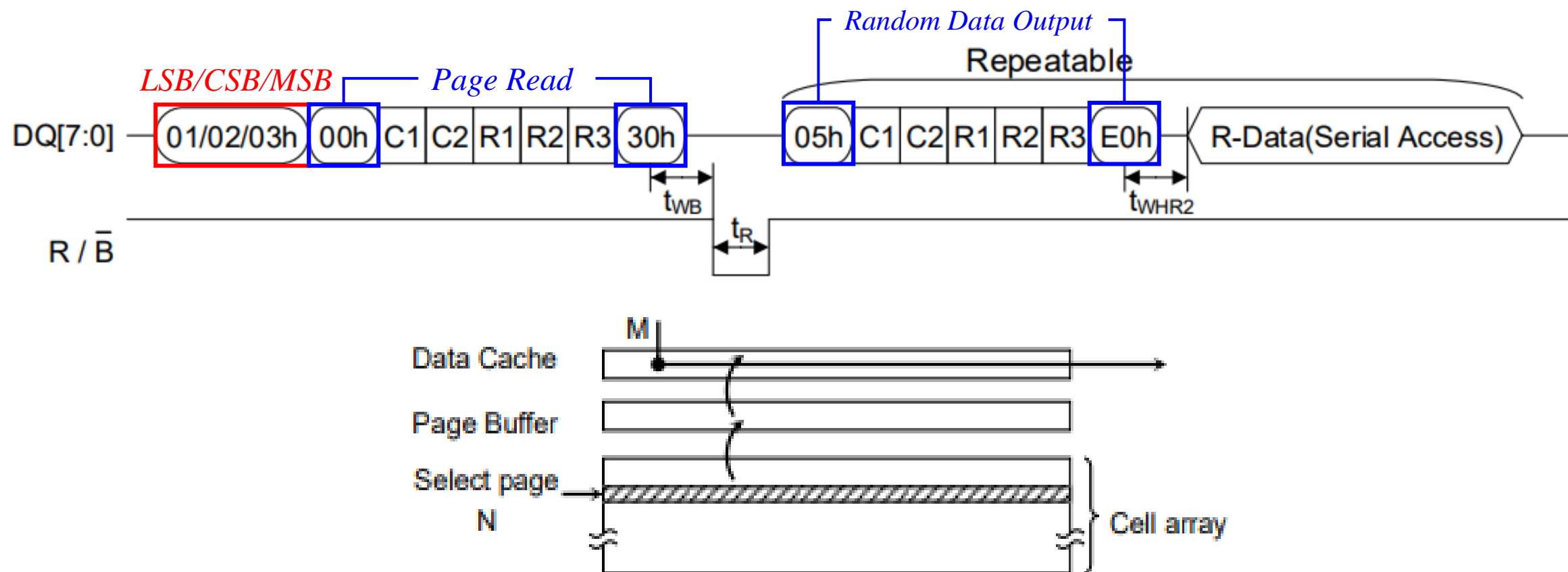
Random Cache Read Operation
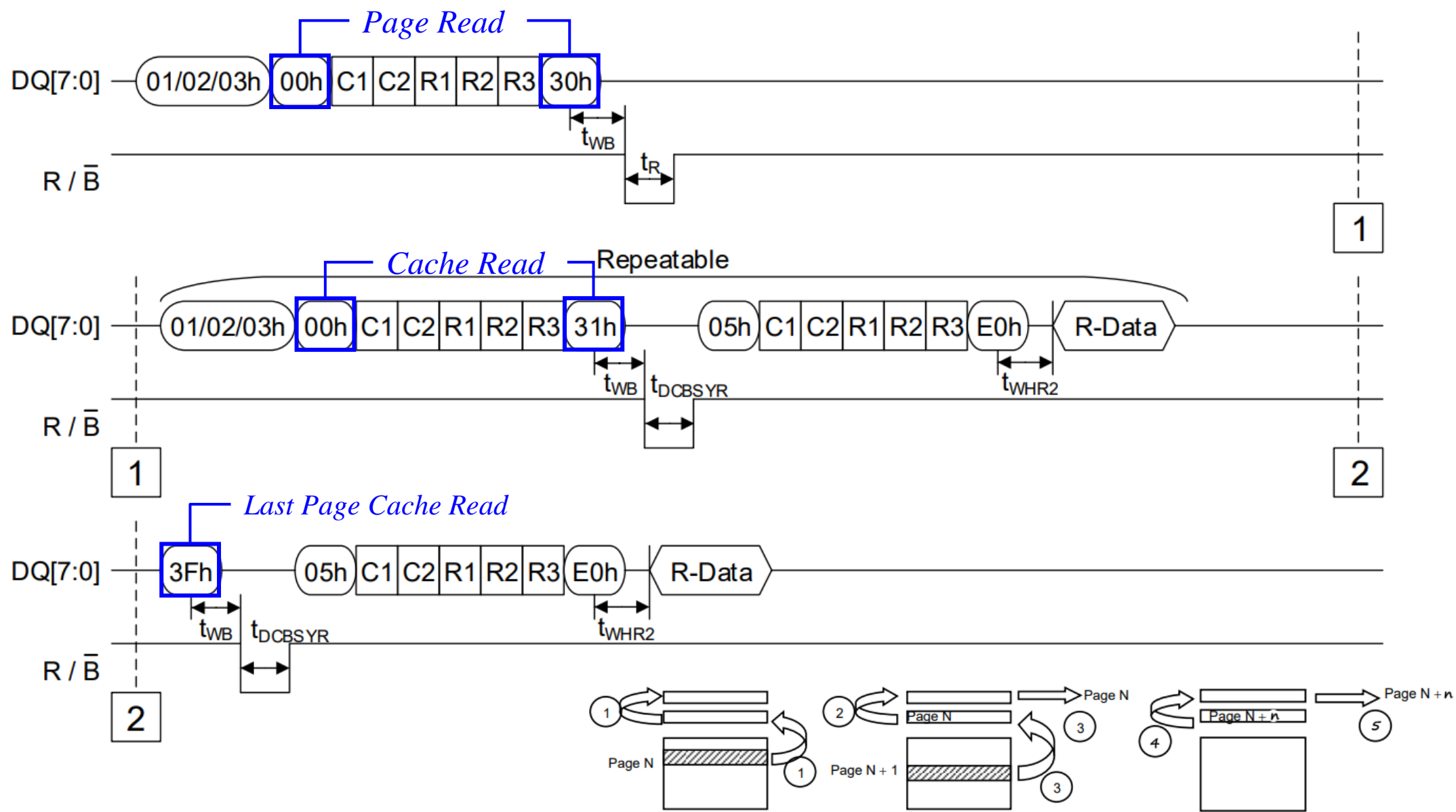
- *Read Status Operation*
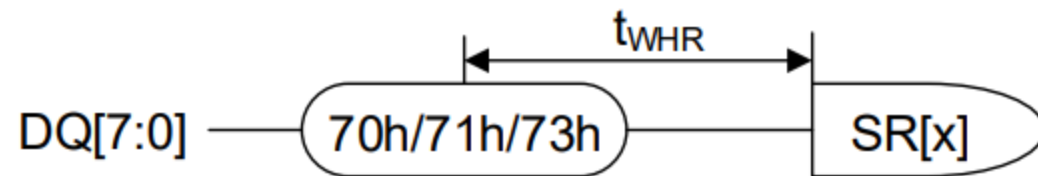
- *Read Status Definition (70h)*

|	DQ 0	DQ 1	DQ 2	DQ 3	DQ 4	DQ 5	DQ 6	DQ 7
Definition of value	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Reserved	Reserved	Reserved	Busy : "0" Ready : "1"	Busy : "0" Ready : "1"	Protected : "0" Not Protected :"1"
Block Erase	Pass/Fail	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Full Sequence Program	Pass/Fail	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Cache FSP	Pass/Fail for the current program	Pass/Fail for the previous program	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Busy/Ready for Host	Write Protect
Read	Not Use	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Cache Read	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Busy/Ready for Host	Write Protect

■ *Full Sequence Program Operation*
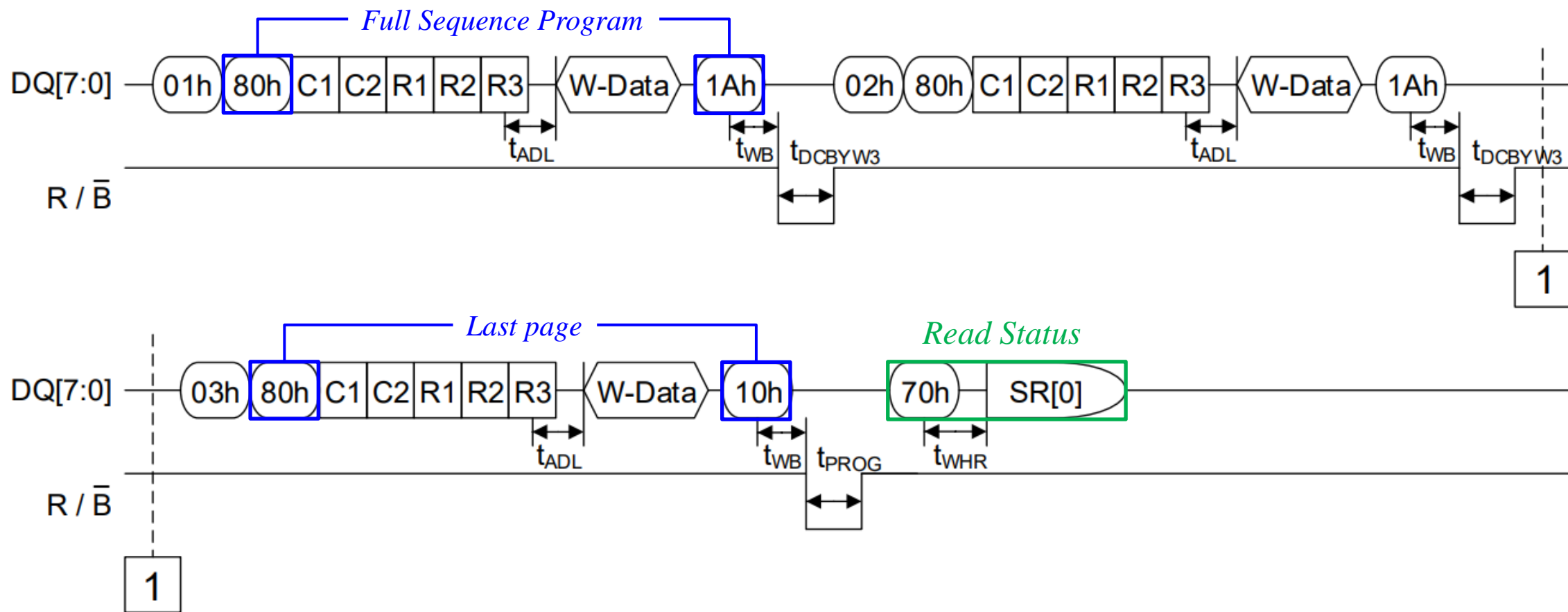
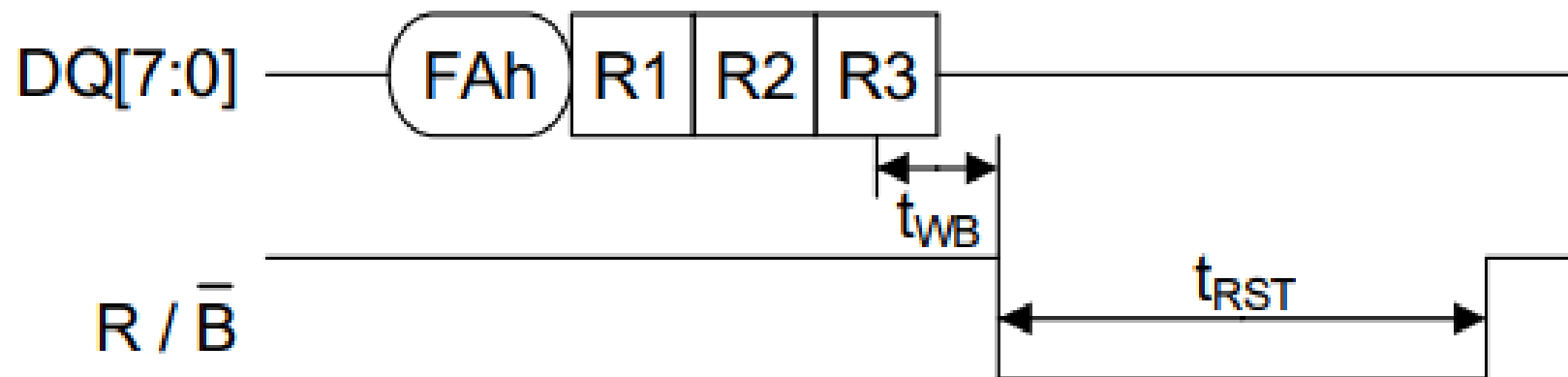# Cache Full Sequence Program Operation
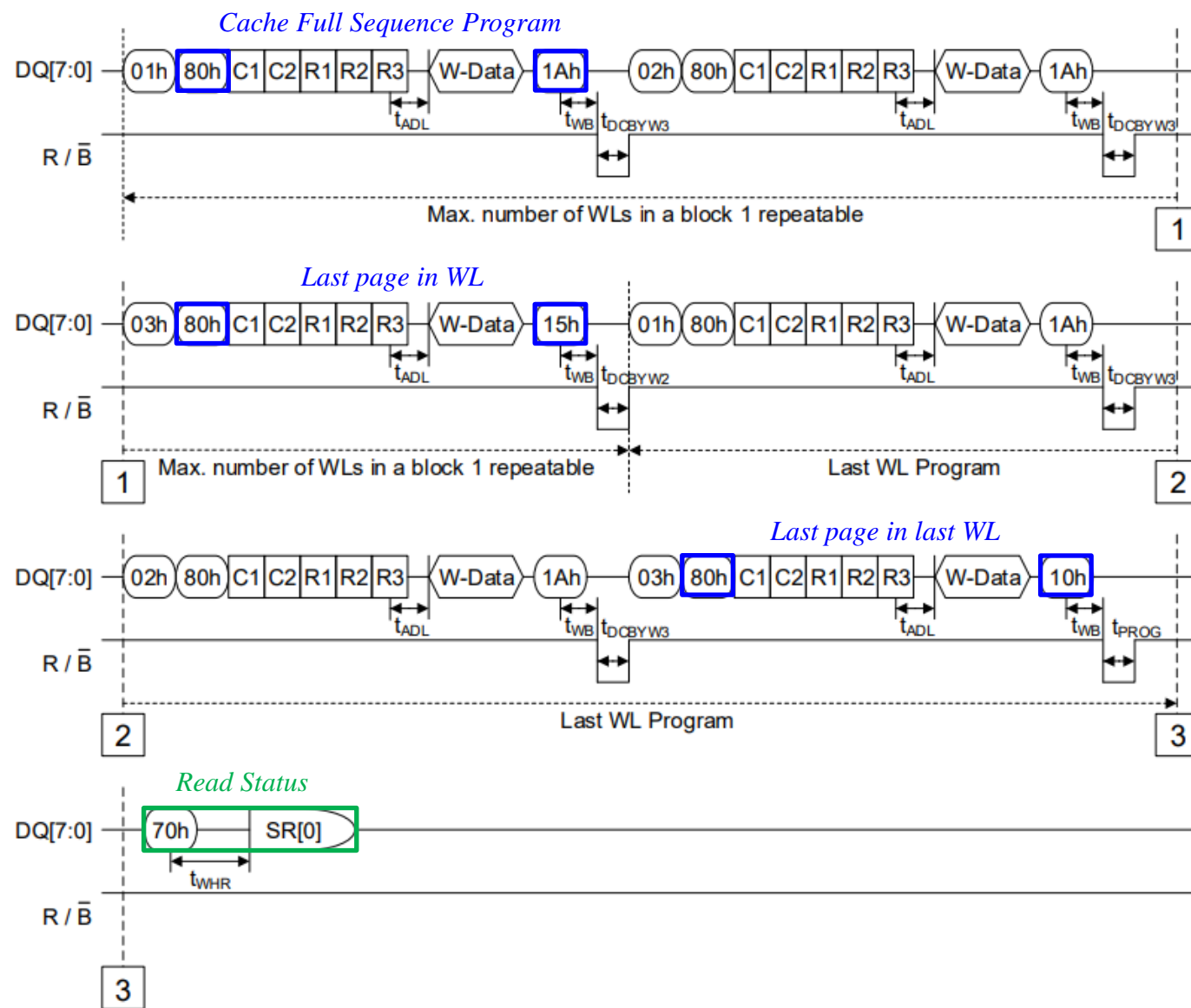
■ ***Block Erase Operation***
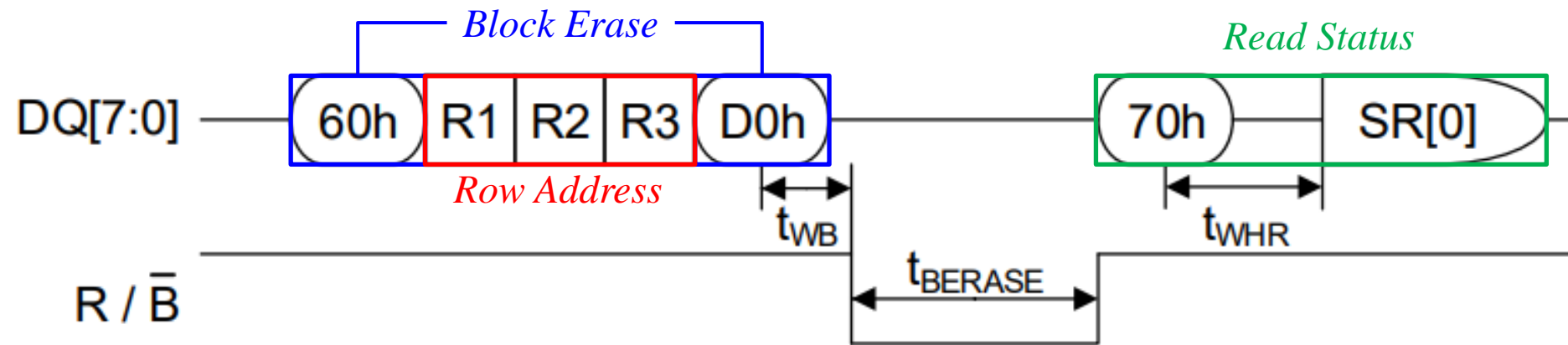
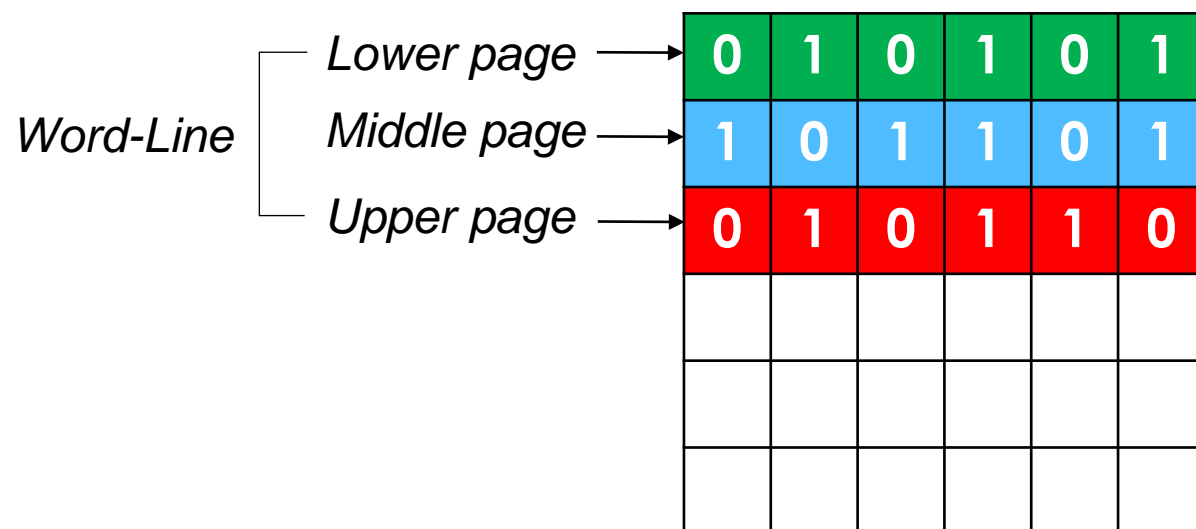- *Reset Operation*
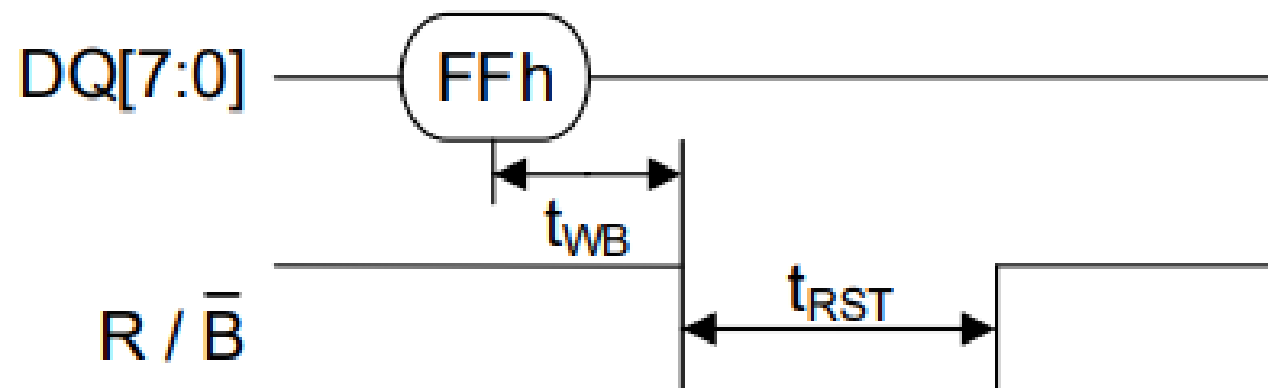
- *Reset LUN Operation*

Flash Translation Layer

- *Logical – Physical mapping*
  - *Page level mapping*
  - *Block level mapping*
  - *Hybrid mapping*
- *磨損均衡(wear-leveling)*
- *ECC（Error-correcting Code）*

- *Logical – Physical mapping*
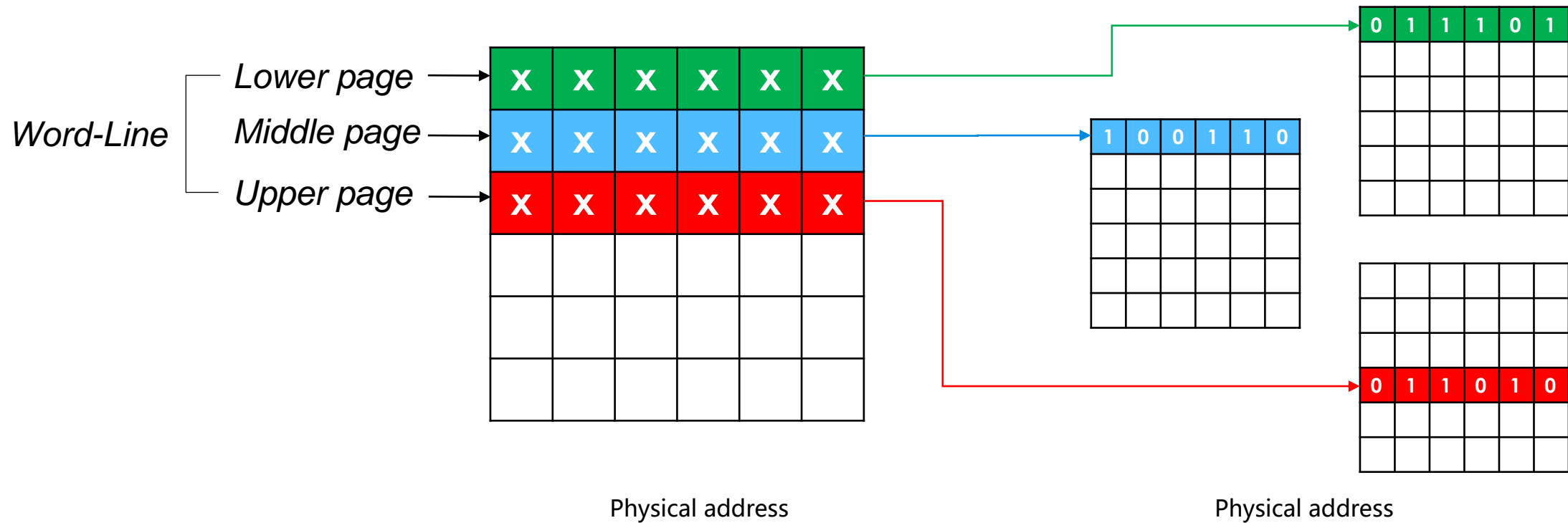 - *Page level mapping*
  - *Block level mapping*
  - *Hybrid mapping*

Word-Line

Lower page →

0	1	0	1	0	1
1	0	1	1	0	1
0	1	0	1	1	0

Lower page → (green row)
Middle page → (blue row)
Upper page → (red row)

Physical address

	Green	**Blue**	**Red**
Logical address	0x00	0x01	0x02
Physical address	0x00	0x01	0x02

■ *Page level mapping*

Program new data to an empty page and update the mapping table.

Physical address   Physical address

	Green	Blue	Red
Logical address	0x00	0x01	0x02
Physical address	0xAF	0x3E	0x6D

- *Page level mapping*
  Erase the block that contains too many invalid pages or when the user region has no space.

Physical address
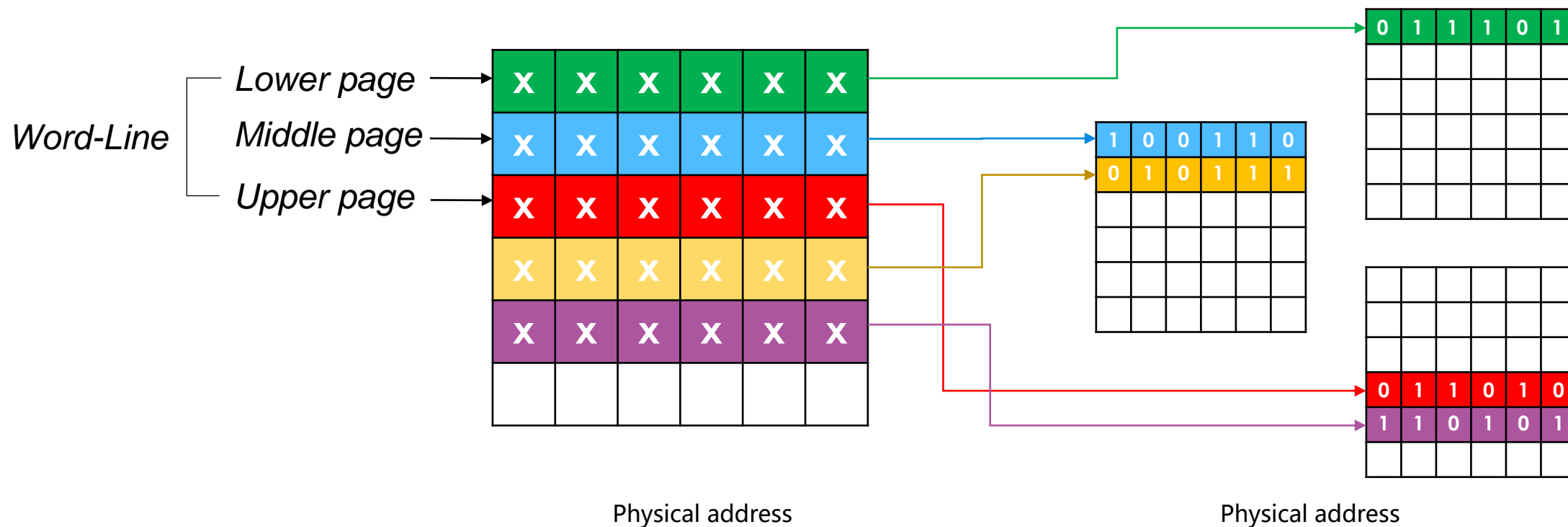
Physical address

	Green	Blue	Red	Yellow	Purple
Logical address	0x00	0x01	0x02	0x03	0x04
Physical address	0xAF	0x3E	0x6D	0x3F	0x6E

■ *Page level mapping*

Move valid pages to another page
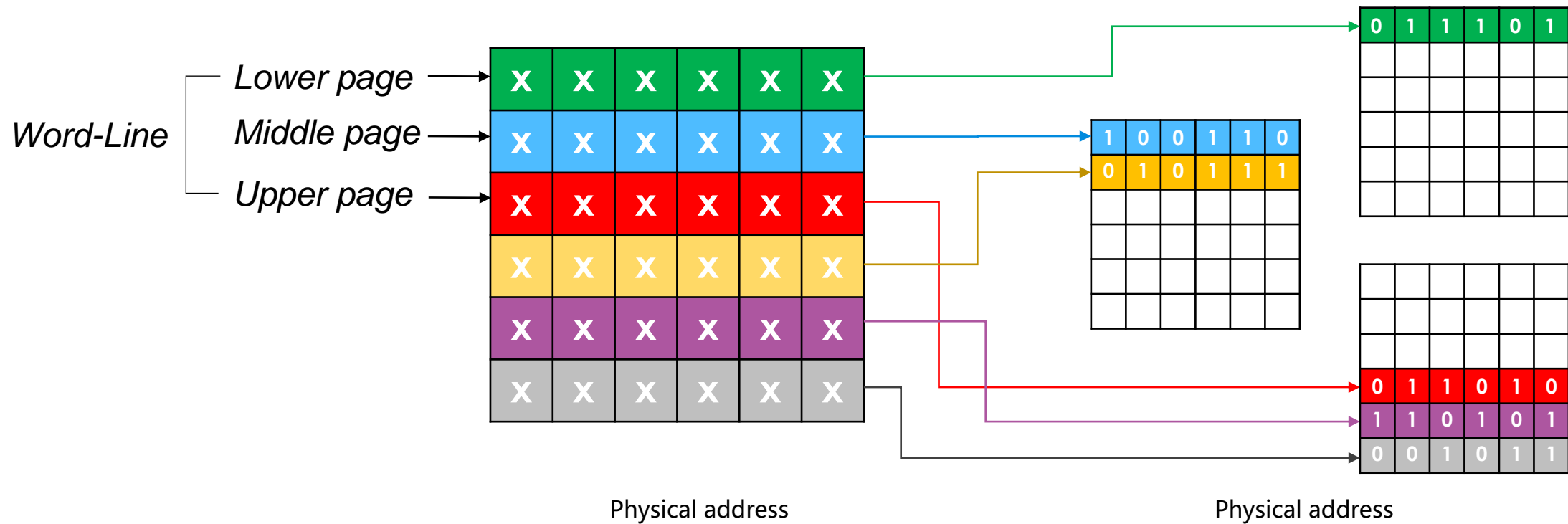
Physical address

Physical address

	Green	Blue	Red	Yellow	Purple	Gray
Logical address	0x00	0x01	0x02	0x03	0x04	0x05
Physical address	0xAF	0x3E	0x6D	0x3F	0x6E	0x6F

■ *Page level mapping*

Erase the invalid block
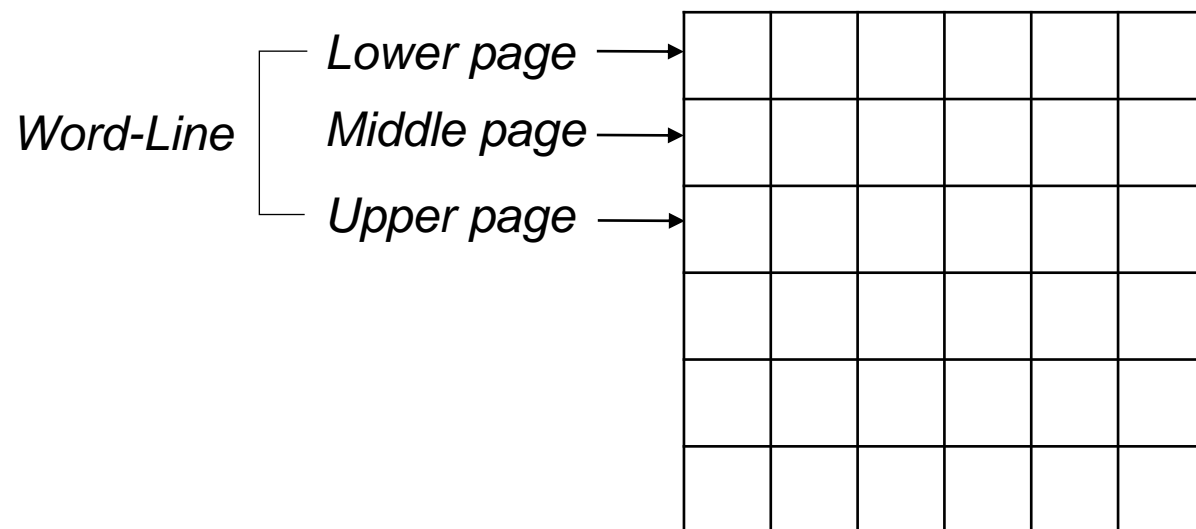
Word-Line
- Lower page →
- Middle page →
- Upper page →

Physical address

Physical address

	Green	Blue	Red	Yellow	Purple	Gray
Logical address	0x00	0x01	0x02	0x03	0x04	0x05
Physical address	0xAF	0x3E	0x6D	0x3F	0x6E	0x6F
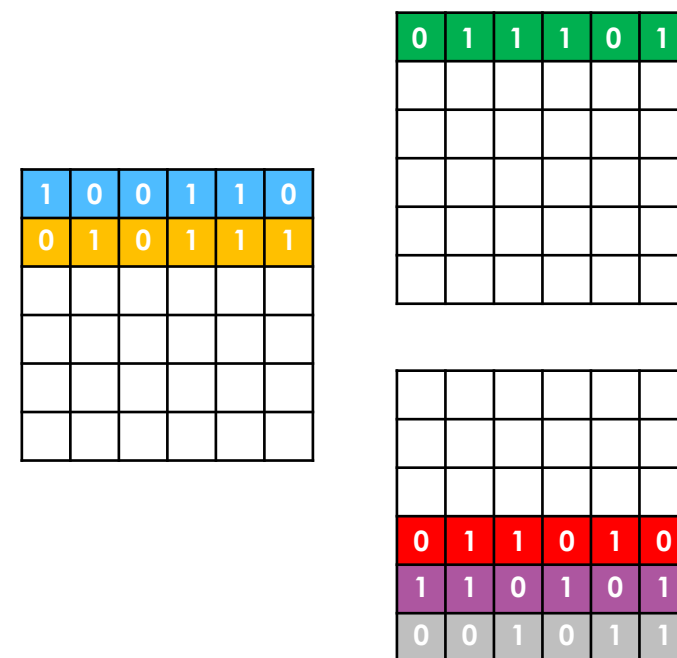
- *Page level mapping*

  *Use to store mapping table: 21 bits(page address requirement) * 768(page number) * 2596(block number) * 1(LUN number)*
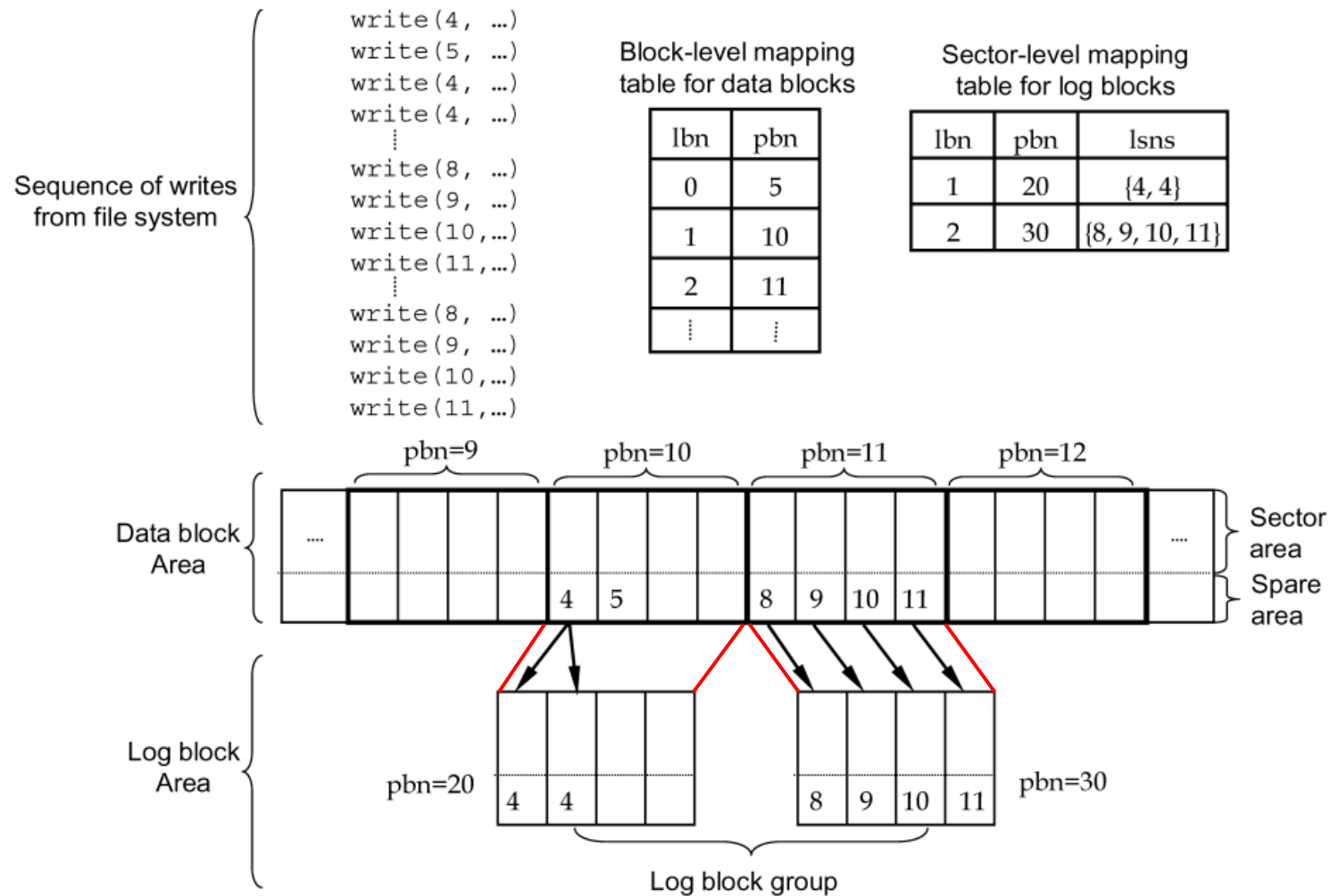
  *= 5.6 * 2 MB(per target)*

- *Block level mapping*

  *Use to store mapping table: 13bits(block address requirement) * 2596 * 1 = 4.69KB * 2 (per target)*
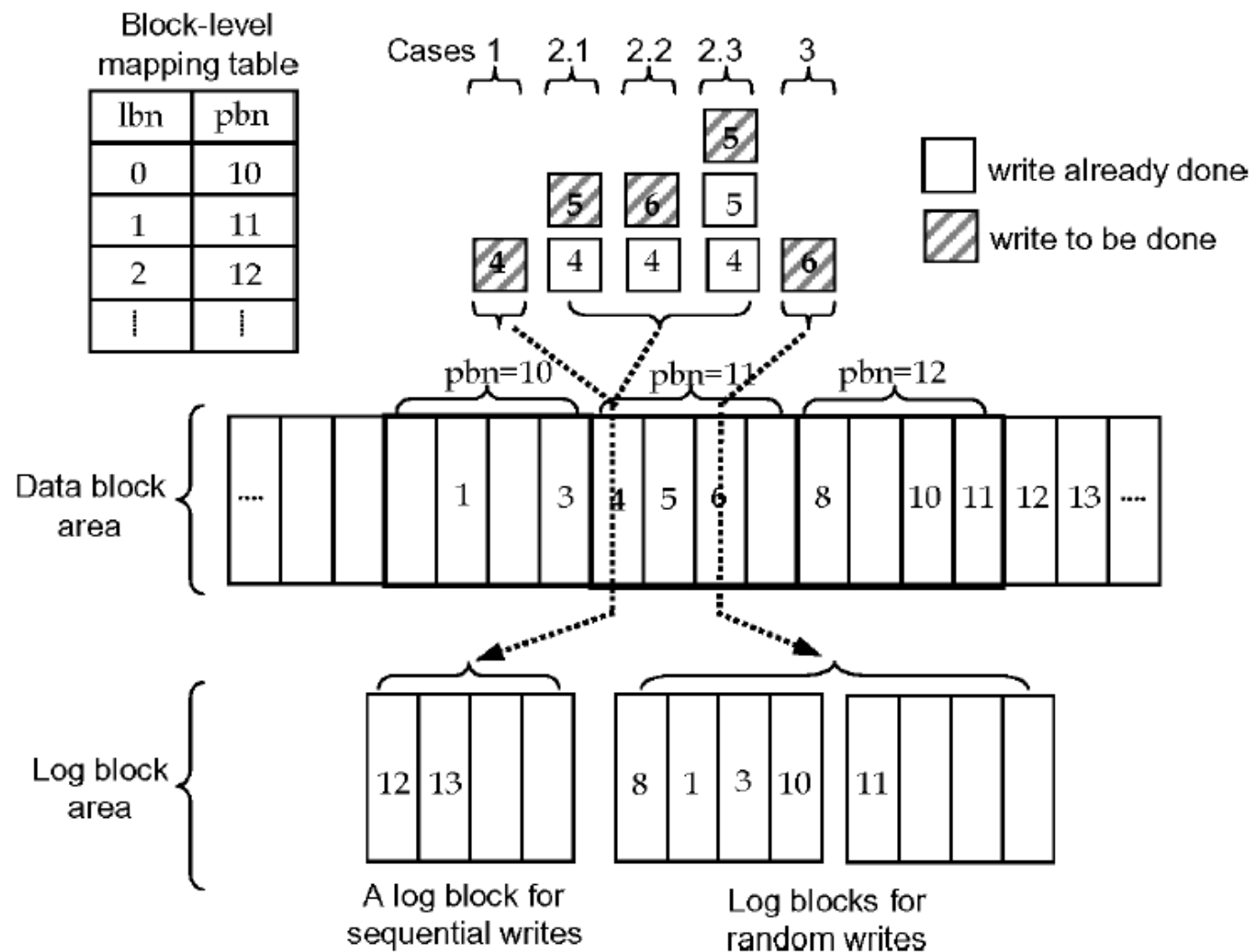
- *Hybrid mapping*

  *Use to store mapping table: 4.69KB * 10(768 pages $\rightarrow$ 2^10) * 2 (per target) = 93.8KB * 2*

■ *BAST Hybrid mapping*

- *FAST Hybrid mapping*

- *Logical – Physical mapping*
  - *Page level mapping*
  - *Block level mapping*
  - *Hybrid mapping*
- *磨損均衡(wear-leveling)*
- *ECC（Error-correcting Code)*

Thanks for Attention

廖偉翔
David Liao

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