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Vishay Siliconix

# P-Channel 60 V (D-S) 175 °C MOSFET

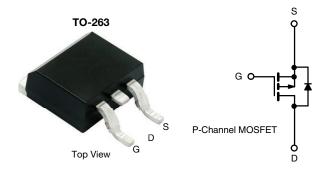
PRODUCT SUMMARY				
V <sub>DS</sub> (V)	$V_{DS}(V)$ $R_{DS(on)}(\Omega)$			
-60	0.0069 at V <sub>GS</sub> = -10 V	-110		
	0.0088 at V <sub>GS</sub> = -4.5 V	-110		

#### **FEATURES**

- TrenchFET® power MOSFET
- Package with low thermal resistance



 Material categorization: for definitions of compliance please see www.vishav.com/doc?99912



#### **Ordering Information:**

SUM110P06-07L-E3 (Lead (Pb)-free)

<b>ABSOLUTE MAXIMUM RATINGS</b> ( $T_C = 25$	5°C, unless otherw	rise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-Source Voltage	V <sub>DS</sub>	-60	V		
Gate-Source Voltage	$V_{GS}$	± 20	] V		
Continuous Drain Current d	T <sub>C</sub> = 25 °C		-110		
$(T_J = 175  ^{\circ}\text{C})$	T <sub>C</sub> = 125 °C	I <sub>D</sub>	-95	1	
Pulsed Drain Current	I <sub>DM</sub>	-240	A		
ralanche Current		I <sub>AS</sub>	-75		
Single Pulse Avalanche Energy <sup>a</sup>	L = 0.1 mH	E <sub>AS</sub>	281	mJ	
Deway Discipation	T <sub>C</sub> = 25 °C °	Б	375	W	
Power Dissipation	T <sub>A</sub> = 25 °C b	P <sub>D</sub>	3.75		
Operating Junction and Storage Temperature Range	•	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C	

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	TYPICAL	UNIT		
Junction-to-Ambient	PCB mount <sup>b</sup>	$R_{thJA}$	40	°C/W		
Junction-to-Case		R <sub>thJC</sub>	0.4	G/VV		

#### Notes

- a. Duty cycle ≤ 1 %.
- b. When mounted on 1" square PCB (FR4 material).
- c. See SOA curve for voltage derating.
- d. Limited by package.



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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-60	-	-	V	
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = -250 \mu A$	-1	-	-3	v	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA	
		$V_{DS} = -60 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	-1	μA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = -60 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125 ^{\circ}\text{C}$	-	-	-50		
		$V_{DS} = -60 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 175 ^{\circ}\text{C}$	-	-	-250		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	-120	-	-	Α	
		$V_{GS} = -10 \text{ V}, I_D = -30 \text{ A}$	-	0.0055	0.0069	Ω	
Drain-Source On-State Resistance a	Ь	$V_{GS} = -10 \text{ V}, I_D = -30 \text{ A}, T_J = 125 \text{ °C}$	-	-	0.0115		
Diain-Source On-State Resistance	R <sub>DS(on)</sub>	$V_{GS} = -10 \text{ V}, I_D = -30 \text{ A}, T_J = 175 \text{ °C}$	ı	-	0.0138		
		$V_{GS} = -4.5 \text{ V}, I_D = -20 \text{ A}$	-	0.0070	0.0088		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	$V_{DS} = -15 \text{ V}, I_{D} = -50 \text{ A}$	20	-	-	S	
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>		-	11 400	-	pF	
Output Capacitance	Coss	$V_{GS} = 0 \text{ V}, V_{DS} = -25 \text{ V}, f = 1 \text{ MHz}$	-	1200	-		
Reverse Transfer Capacitance	$C_{rss}$		-	900	-		
Total Gate Charge <sup>c</sup>	$Q_g$		1	230	345	nC	
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	$V_{DS} = -30 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -110 \text{ A}$	-	50	-		
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$		-	60	-		
Gate Resistance	R <sub>g</sub>	f = 1 MHz	-	3	-	Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>		-	20	30		
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = -30 \text{ V}, R_L = 0.27 \Omega$	-	25	40	ns	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$I_D \cong -110 \text{ A}, V_{GEN} = -10 \text{ V}, R_g = 1 \Omega$	-	110	200		
Fall Time <sup>c</sup>	t <sub>f</sub>		-	50	100		
<b>Drain-Source Body Diode Character</b>	istics (T <sub>C</sub> = 25	5 °C b)					
Continuous Current	IS		-	-	-110	۸	
Pulsed Current	I <sub>SM</sub>		ı	-	-240	Α	
Forward Voltage <sup>a</sup>	$V_{SD}$	I <sub>F</sub> = -85 A, V <sub>GS</sub> = 0 V	-	-1	-1.5	V	
Reverse Recovery Time	t <sub>rr</sub>		-	91	137	ns	
Peak Reverse Recovery Charge	I <sub>RM(REC)</sub>	I <sub>F</sub> = -85 A, dl/dt = 100 A/μs	-	-6	-9	Α	
Reverse Recovery Charge	Q <sub>rr</sub>		-	0.21	0.44	μC	

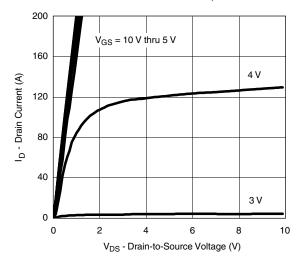
#### Notes

- a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

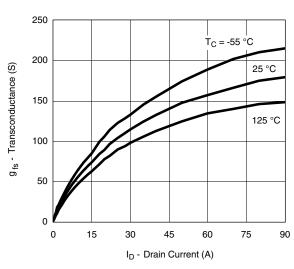
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



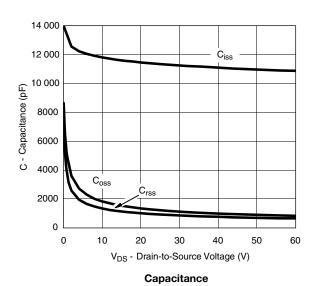
### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

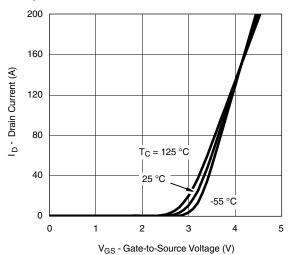


#### **Output Characteristics**

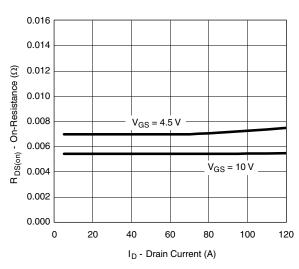


#### Transconductance

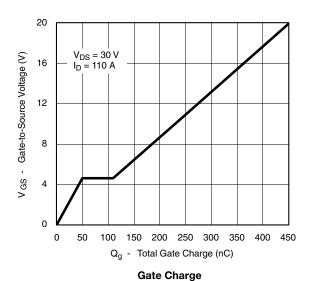




#### **Transfer Characteristics**

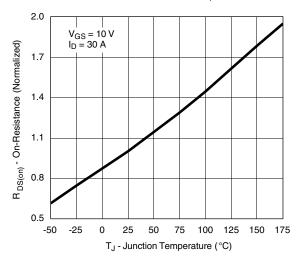


#### On-Resistance vs. Drain Current

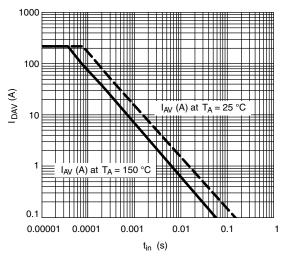




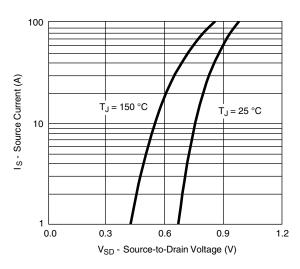
### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



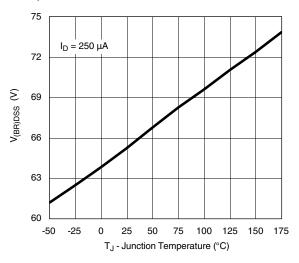
#### On-Resistance vs. Junction Temperature



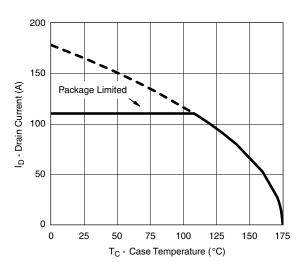
Avalanche Current vs. Time



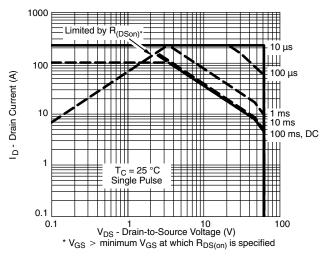
Source-Drain Diode Forward Voltage



**Drain Source Breakdown vs. Junction Temperature** 



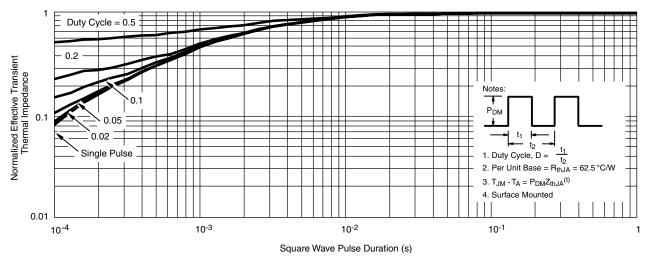
Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72439.



# TO-263 (D<sup>2</sup>PAK): 3-LEAD









DETAIL A (ROTATED 90°)



<u> </u>	b	<b>+</b> +
≥		<u>, o</u>
0	ECTION A	1

- 1. Plane B includes maximum features of heat sink tab and plastic.
- 2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- 3. Pin-to-pin coplanarity max. 4 mils.
- 4. \*: Thin lead is for SUB, SYB. Thick lead is for SUM, SYM, SQM.
- 5. Use inches as the primary measurement.

6 This feature is for thick lead.

		INC	HES	MILLIMETERS		
DIM.		MIN.	MAX.	MIN.	MAX.	
Α		0.160	0.190	4.064	4.826	
	b	0.020	0.039	0.508	0.990	
	b1	0.020	0.035	0.508	0.889	
	b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457	
	Thick lead	0.023	0.028	0.584	0.711	
c1	Thin lead	0.013	0.017	0.330	0.431	
CI	Thick lead	0.023	0.027	0.584	0.685	
	c2	0.045	0.055	1.143	1.397	
	D	0.340	0.380	8.636	9.652	
	D1	0.220	0.240	5.588	6.096	
	D2	0.038	0.042	0.965	1.067	
	D3	0.045	0.055	1.143	1.397	
	D4	0.044	0.052	1.118	1.321	
	Е	0.380	0.410	9.652	10.414	
E1		0.245	-	6.223	-	
E2		0.355	0.375	9.017	9.525	
	E3	0.072	0.078	1.829	1.981	
е		0.100	BSC	2.54 BSC		
K		0.045	0.055	1.143	1.397	
L		0.575	0.625	14.605	15.875	
L1		0.090	0.110	2.286	2.794	
L2		0.040	0.055	1.016	1.397	
L3		0.050	0.070	1.270	1.778	
L4		0.010	BSC	0.254 BSC		
	М	-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13						

DWG: 5843





### RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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