1 Channel Mobile IO-Box Interface Modbus register description v1.2

Contents

Modbus Register Data types

Mobile Telemetry Interface (MTI) provides 3 address spaces in the Input and Holding register spaces
- 16-bit integer variables
- 32-bit integer variables
- 32-bit single precision floating point variables

Modbus protocol provides mean to access 16-bit registers, i.e. read and write. These registers are referred as Input and Holding registers. The Input registers are read only register and the Holding registers are read/write registers. Addition to these 16-bit registers there are also 1-bit accessed Coil and Discrete Input registers. These registers are not implemented to Mobile Telemetry Interface so this document omitted 1-bit registers.

As the Modbus protocol specifies only 16-bit (and 1-bit) registers the access to 32bit data types are implemented as multiple read/write of 16-bit registers. Vendors must specify the protocol to access longer data types. Following chapter describes the means to read and write 32-bit bit variables

Support for 32-bit integer and single precision floating point variables

32-bit variables are accessed as pair of 16-bit register. Although the endianness of the Modbus protocol is big-endian – i.e. the most significant byte of the 16-bit register is transferred first - the endianness of the 32-bit variable in the MTI is little-endian – i.e. the least significant 16-bit (half word) is transferred first.

Table 1 the endianness of the 32-bit word is little-endian. Note following tables present most significant word 16-bit word first

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Register n	least significant 16-bit word															
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Register n + 1	most significant 16-bit word															

As it is possible to access these 32-bit variables with single 16-bit register read/write operation it is responsibility of the Modbus Master (or Client) implement the read/write operations that access the whole 32-bit word in one Modbus frame. Especially the write operation must be performed with one operation – i.e. use the *Write Multiple Registers* function code (16).

Register Map

Radio device common registers

These register are common to all telemetry transmitter devices.

Input Registers (read only registers)

Table 2 Input Register address space

Address				
16-bit integer	***32-bit integer***	***Floating point***	***Description***	***Integer type***
30001	31001	32001	***Battery Voltage***	unsigned
30002	31003	32003	***Battery State of Charge***	unsigned
30003	31005	32005	***Battery Charger State***	unsigned
30004	31007	32007	***CPU Temperature***	signed
30005	31009	32009	***Buttons States***	unsigned
30006	31011	32011	***PWM Module Clock Frequency***	unsigned
30007	31013	32013	***PWM Frequency***	unsigned
30008	31015	32015	***PWM Duty Cycle Channel 1***	unsigned
30009	31017	32017	***PWM Duty Cycle Channel 2***	unsigned
30010	31019	32019	***PWM Duty Cycle Channel 3***	unsigned
30011	31021	32021	***PWM Duty Cycle Channel 4***	unsigned
30012	31023	32023	***Reserved(/Debug)***	
30013	31025	32025	***Reserved(/Debug)***	
30014	31027	32027	***Reserved(/Debug)***	
30015	31029	32029	Reserved	
…	…	…	Reserved	
30025	31049	32049	Reserved	

Battery Voltage Register

Table 3 Battery Voltage Register

Word size	***Address***	***data type***	***Description***
16-bit integer	30001	unsigned	Battery voltage [0.01V]
32-bit integer	31001		
32-bit floating point	32001		Battery voltage [V]

Battery State of Charge Register

Table 4 State of Charge register

Word size	***Address***	***data type***	***Description***
16-bit integer	30002	unsigned	Approximation of the state of charge [0.01%]
32-bit integer	31003		
32-bit floating point	32003		Approximation of the state of charge [%]

Battery Charger State Register

Table 5 Battery Charger State integer register: address 16-bit 30003 and address 32-bit 31005

Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Read	Reserved (only 32-bit register)															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	Reserved														Conn	State

Table 6 Battery Charger State integer field description

Field	Description
15-2 or 31-2 Reserved	Should read 0
1 Conn	0: Charger not connected 1: Charger Connected
0 State	0: Not Charging: charger not connected, battery is full or charging timeout expired 1: Charging

Table 7 Battery Charger State floating point register: address 32005

Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Read	State															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	State															

Table 8 Battery Charger State floating point field description

Field	Description
31-0 State	Convert to unsigned integer and refer to ***Table 6 Battery Charger State integer field*** description

CPU Temperature Register

Table 9 CPU Temperature Register

Word size	***Address***	***data type***	***Description***
16-bit integer	30004	signed	CPU temperature [0.1°C]. Can be used to approximate the ambient temperature.
32-bit integer	31007		
32-bit floating point	32007		CPU temperature [°C]

Buttons States Register

Table 10 Buttons States integer register: address 16-bit 30005 and address 32-bit 31009

Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Read	Reserved (only 32-bit register)															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	Reserved												Button 4	Button 3	Button 1	Button 0

Table 11 Buttons States integer field description

Field	Description
15-4 or 31-4 Reserved	Should read 0
3 Button 4	0: released 1: pressed
2 Button 3	0: released 1: pressed
1 Button 2	0: released 1: pressed
0 Button 1	0: released 1: pressed

Table 12 Buttons States floating point register: address 32009

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read	State															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	State															

Table 13 Buttons State floating point field description

Field	Description
32-0 State	Convert to unsigned integer and refer to ***Table 6 Battery Charger State integer field description***

PWM Module Clock Frequency Register

Table 14 PWM Module Clock Frequency register

Word size	*Address*	*data type*	*Description*
16-bit integer	30006	unsigned	PWM Module Source Clock [10kHz]
32-bit integer	31011		PWM Module Source Clock [Hz]
32-bit floating point	32011		PWM Module Source Clock [Hz]

PWM Frequency Register

Table 15 PWM Frequency register

Word size	*Address*	*data type*	*Description*
16-bit integer	30007	unsigned	PWM output frequency [Hz]
32-bit integer	31013		PWM output frequency [Hz]
32-bit floating point	32013		PWM output frequency [Hz]

PWM Channel Duty Cycle Register

Table 16 PWM Channel Duty Cycle register: ch = 1…4

Word size	*Address*	*data type*	*Description*
16-bit integer	30008 + (ch - 1)	unsigned	PWM channel duty cycle [0.01%]
32-bit integer	31015 + 2 x (ch - 1)		PWM channel duty cycle [0.01%]
32-bit floating point	32015 + 2 x (ch - 1)		PWM channel duty cycle [%]

Reserved (/Debug) Registers

Table 17 Reserved (/Debug) register

Word size	*Address*	*Description*
16-bit integer	30012…30025	Should read 0 (debug register value can differ from 0)
32-bit integer	31023…31049	
32-bit floating point	32023…31049	

Holding Registers (read and write registers)

Table 18 Holding Register address space

Address				
16-bit integer	**32-bit integer**	**Floating point**	**Description**	**Integer type**
40001	41001	42001	***Radio Channel***	unsigned
40002	41003	42003	***On Air Rata Rate***	unsigned
40003	41005	42005	***Radio Device Type***	unsigned
40004	41007	42007	***Device Specific Register 1***	
40005	41009	42009	***Device Specific Register 2***	
40006	41011	42011	***Device Specific Register 3***	
40007	41013	42013	***Device Specific Register 4***	
40008	41015	42015	***Device Specific Register 5***	
40009	41017	42017	Reserved	
…	…	…	Reserved	
40025	41049	42049	***Device Specific Register 6***	

Radio Channel Register

Table 19 Radio Channel register

Word size	***Address***	***data type***	***Description***
16-bit integer	40001	unsigned	Radio Channel: 0...127 Channel frequency = (2400 + Radio Channel) MHz
32-bit integer	41001		
32-bit floating point	42001		

On Air Data Rate Register

Table 20 On Air Data Rate register

Word size	***Address***	***data type***	***Description***
16-bit integer	40002	unsigned	0: 250kpbs 1: 1Mbps 2: 2Mbps (Note! uses 2 radio channels) other: Reserved Note!! Though it is possible to write to the *On Air Data Rate register*, most radio devices will override written value
32-bit integer	41003		
32-bit floating point	42003		

Radio Device Type Register

Table 21 Radio Device Type register

Word size	***Address***	***data type***	***Description***
16-bit integer	40003	unsigned	0: No Device 1: Reserved 2: 16 Channel Thermocouple Transmitter 3: 8 Channel Thermocouple Transmitter 4: Remote Devices (Remote Switch/Mux) 5: 2 Channel Quadrature (Encoder) Transmitter 6: 4 Channel Thermocouple Transmitter others: Reserved Note!! If *reserved type* is written *No Device* is applied
32-bit integer	41005		
32-bit floating point	42005		

Device Specific Registers

See Radio Device Chapters for details.

16 Channel, 8 Channel and 4 Channel Thermocouple Transmitter

As the Modbus implementations of 16 channel, 8 channel and 4 channel thermocouple devices are mostly similar the devices are packed to one device description.

Input Registers (read only registers)

Table 22 Input Register address space

Address				
16-bit integer	**32-bit integer**	**Floating point**	**Description**	**Integer type**
30026	31051	32051	***Rx Timer (16-bit value)***	unsigned
30027	31053	32053	***Radio Rx Status***	unsigned
30028	31055	32055	***Rx Success***	unsigned
30029	31057	32057	***Data Valid***	unsigned
30030	31059	32059	***Data Validation Counter***	unsigned
30031	31061	32061	***Measure Sample Rate***	unsigned
30032	31063	32063	***Reserved***	
…	…	…	…	
30036	31071	32071	***Channel 1 Temperature***	signed
30037	31073	32073	***Channel 2 Temperature***	signed
…	…	…	***…***	…
30051	31101	32101	***Channel 16 Temperature***	signed

Rx Timer Register

Table 23 Rx Timer Index register

Word size	***Address***	***data type***	***Description***
16-bit integer	30026	unsigned	Running 16-bit unsigned index which is incremented when radio packet is expected to be received, i.e. index is incremented even though packet is not received. Index timer is adjusted by PLL locked to radio receive frequency (and phase). The index can be used to give sample times to measurement values. By default sample rate is 100Sps. As the width of the counter is 16-bit the value will overflow at 65536 in all data types, i.e. 65535 -> 0
32-bit integer	31051		
32-bit floating point	32051		

Radio Rx Status Register

Table 24 Radio Rx Status integer register: address 16-bit 30027 and address 32-bit 31053

Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Read	Reserved (only 32-bit register)															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	Reserved														Radio 2	Radio 1

Table 25 Radio Rx Status integer field description

Field	Description
15-2 or 31-2 Reserved	Should read 0
1 Radio 2	0: Packet was not received by radio 2 1: Packet was received by radio 2
0 Radio 1	0: Packet was not received by radio 1 1: Packet was received by radio 1

Table 26 Radio Rx Status floating point register: address 32053

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read	Status															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	Status															

Table 27 Radio Rx Status floating point field description

Field	Description
31-0 Status	Convert to unsigned integer and refer to ***Table 25 Radio Rx Status integer field description***

Rx Success Register

Table 28 Rx Success register

Word size	*Address*	*data type*	*Description*
16-bit integer	30028	unsigned	pps / sps ratio [%]. - pps stands for (received) packets per second - sps stands for samples per second, i.e. sample rate
32-bit integer	31055		
32-bit floating point	32055		

Data Valid Register

Table 29 Data Valid integer register: address 16-bit 30029 and address 32-bit 31057

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read	Reserved (only 32-bit register)															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	Reserved															Valid

Table 30 Data Valid integer field description

Field	Description
15-1 or 31-1 Reserved	Should read 0
0 Valid	0: Data is invalid 1: Data is valid: When data is invalid measured temperatures are not updated to ***Temperature Registers***

Table 31 Data Valid floating point register: address 32057

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read	Status															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	Status															

Table 32 Data Valid floating point field description

Field	Description
31-0 Status	Convert to unsigned integer and refer to ***Table 30 Data Valid integer field*** description

Data Validation Counter Register

Table 33 Data Validation Counter register

Word size	***Address***	***data type***	***Description***
16-bit integer	30030	unsigned	Up/Down counter. If ***Valid***[1] is 0 counter is up counter. When counter reaches ***packets to valid count***[2] bit ***Valid***[1] is set to 1 and counter is updated with ***packets to invalid count*** [3] value If ***Valid***[1] is 1 mode is down counter. When counter reach 0 ***Valid***[1] is cleared to 0 ***Packets to valid count*** and ***packets to invalid count*** can be defined in holding registers, see details ***Table 38 Radio Device Specific Register 1 register***
32-bit integer	31059		
32-bit floating point	32059		

[1] *Valid* refers to Valid bit in ***Data Valid Register***

[2] Counter value is incremented when radio packets are received within the receive window, i.e. *packets to valid count* [2] defines number of consecutive packets that must be received before data is defined valid.

[3] If data have been defined valid (*Valid* = 1*) packets to invalid count* defines the number of consecutively missed packets before data is defined invalid

Measured Sample Rate Register

Table 34 Measured Sample Rate register

Word size	***Address***	***data type***	***Description***
16-bit integer	30031	unsigned	Measure sample rate [0.01Hz].
32-bit integer	31061		
32-bit floating point	32061		Measure sample rate [Hz]

Reserved Register

Table 35 Measured Sample Rate register

Word size	***Address***	***Description***
16-bit integer	30032-30035	Should read 0
32-bit integer	31061-31069	
32-bit floating point	32061-32069	

Temperature Registers

Table 36 Temperature register, ch = 1…16

Word size	***Address***	***data type***	***Description***
16-bit integer	30036 + (ch - 1)	signed	Channel temperature [1/16°C]
32-bit integer	31071 + 2 x (ch - 1)		
32-bit floating point	32071 + 2 x (ch - 1)		Channel temperature [°C]

Channel Temperature description for 16 Channel Thermocouple

Channel	**Description**
1…16	Measured thermocouple temperature for channel 1…16

Channel Temperature description for 8 Channel Thermocouple

Channel	**Description**
1…8	Measured thermocouple temperature for channel 1…8
9…16	Measured cold junction temperature for channel 1…8

Channel Temperature description for 4 Channel Thermocouple

Field	Description
1…4	Measured thermocouple temperature for channel 1…4
5	Measured cold junction temperature for channels 1 and 2
6	Measured cold junction temperature for channels 3 and 4
7…16	Reserved (these registers might not read 0)

Holding Registers (read and write registers)

Table 37 Holding Register address space

Address				
16-bit integer	**32-bit integer**	**Floating point**	**Description**	**Integer type**
40004	41007	42007	***Radio Device Specific Register 1***	unsigned
40005	41009	42009	***Radio Device Specific Register 2***	unsigned
40006	41011	42011	***Radio Device Specific Register 3***	unsigned
40007	41013	42013	Radio Device Specific Register 4[1]	Reserved
40009	41015	42015	Radio Device Specific Register 5[1]	Reserved
…	…	…	…	…
40025	41049	42049	Radio Device Specific Register 6[1]	Reserved

[1] Radio Device Specific Register 4…6 are not used

Radio Device Specific Register 1 Register

Table 38 Radio Device Specific Register 1 register

Word size	***Address***	***data type***	***Description***
16-bit integer	40004	unsigned	If value of register is 49 ***Register 2*** defines *packets to valid count* value ***Register 3*** defines *packets to invalid count* value if Register 1 != 49 data is always valid (both counters are 0)
32-bit integer	41007		
32-bit floating point	42007		

Radio Device Specific Register 2 Register

Table 39 Radio Device Specific Register 2 register

Word size	***Address***	***data type***	***Description***
16-bit integer	40005	unsigned	If ***Register 1*** = 49 this defines *packets to valid count*. Max value is 127
32-bit integer	41009		
32-bit floating point	42009		

Radio Device Specific Register 3 Register

Table 40 Radio Device Specific Register 3 register

Word size	***Address***	***data type***	***Description***
16-bit integer	40006	unsigned	If ***Register 1*** = 49 this defines *packets to invalid count*. Max value is 127
32-bit integer	41011		
32-bit floating point	42011		

2 Channel Quadrature Encoder Telemetry

Input Registers (read only registers)

Table 41 Input Register address space for firmware v1.05 and older

Address				
16-bit integer	**32-bit integer**	**Floating point**	**Description**	**Integer type**
30026	31051	32051	***Rx Timer (16-bit value)***	unsigned
30027	31053	32053	***Radio Rx Status***	unsigned
30028	31055	32055	***Rx Success***	unsigned
30029	31057	32057	***Measured Sample Rate***	unsigned
30030	31059	32059	Reserved	
…	…	…	…	
30036	31071	32071	***Channel 1 (n-4)th Encoder Sample***	signed
30037	31073	32073	***Channel 1 (n-3)th Encoder Sample***	signed
…	….	…		
30040	31079	32079	***Channel 1 nth Encoder Sample***	signed
30041	31081	32081	***Channel 2 (n-4)th Encoder Sample***	signed
…	…	…	***…***	signed
30045	31089	32089	***Channel 2 nth Encoder Sample***	signed

Table 42 Input Register address space for firmware v1.06 and newer

Address				
16-bit integer	**32-bit integer**	**Floating point**	**Description**	**Integer type**
30026	31051	32051	***Rx Timer (16-bit value)***	unsigned
30027	31053	32053	***Radio Rx Status***	unsigned
30028	31055	32055	***Rx Success***	unsigned
30029	31057	32057	***Measured Sample Rate***	unsigned
30030	31059	32059	Reserved	
…	…	…	…	
30035	31069	32069	nth Sample index	unsigned
30036	31071	32071	***Channel 1 nth Encoder Sample***	signed
30037	31073	32073	***Channel 2 nth Encoder Sample***	signed
30038	31075	32075	***Channel 1 (n-1)th Encoder Sample***	signed
30039	31077	32077	***Channel 2 (n-1)th Encoder Sample***	signed
…	…	…	***…***	…
30094	31187	32187	***Channel 1 (n-29)th Encoder Sample***	signed
30065	31189	32189	***Channel 2 (n-29)th Encoder Sample***	signed

Rx Timer Register

Table 43 Rx Timer Index register

Word size	***Address***	***data type***	***Description***
16-bit integer	30026	unsigned	Running 16-bit unsigned index which is incremented when radio packet is expected to be received, i.e. index is incremented even though packet is not received. Index timer is adjusted by PLL locked to radio receive frequency (and phase). The index can be used to give sample times to measurement values. By default packet rate is 2000Hz. As the width of the counter is 16-bit the value will overflow at 65536 in all data types, i.e. 65535 -> 0
32-bit integer	31051		
32-bit floating point	32051		

Radio Rx Status Register

Table 44 Radio Rx Status integer register: address 16-bit 30027 and address 32-bit 31053

Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Read	Reserved (only 32-bit register)															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	Reserved														Radio 2	Radio 1

Table 45 Radio Rx Status integer field description

Field	**Description**
15-2 or 31-2 Reserved	Should read 0
1 Radio 2	0: Packet was not received by radio 2 1: Packet was received by radio 2
0 Radio 1	0: Packet was not received by radio 1 1: Packet was received by radio 1

Table 46 Radio Rx Status floating point register: address 32053

Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Read	Status															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	Status															

Table 47 Radio Rx Status floating point field description

Field	**Description**
31-0 Status	Convert to unsigned integer and refer to ***Table 45 Radio Rx Status integer field description***

Rx Success Register

Table 48 Rx Success register

Word size	***Address***	***data type***	***Description***
16-bit integer	30028	unsigned	pps / sps ratio [%]. - pps stands for (received) packets per second - sps stands for samples per second, i.e. sample rate
32-bit integer	31055		
32-bit floating point	32055		

Measured Sample Rate Register

Table 49 Measured Sample Rate register

Word size	***Address***	***data type***	***Description***
16-bit integer	30029	unsigned	Measure sample rate [Hz]
32-bit integer	31057		
32-bit floating point	32057		

n^{th} Sample Index Register

Table 50 n^{th} Sample Index

Word size	***Address***	***data type***	***Description***
16-bit integer	30035	unsigned	The most recent sample index. This is 24-bit unsigned integer value, i.e. 16-bit register will overflow 65535 -> 0
32-bit integer	31069		
32-bit floating point	32069		

Encoder Sample Register

Table 51 Encoder Sample register, channel ch = 1…2, sample s=0…30 were s=0 is the most recent sample

Word size	***Address***	***Description***
16-bit integer	30036 + (*ch - 1)* + 2 x *s*	(n-s)th quadrature encoder counter sample. Quadrature encoder counter width is 24-bit, i.e. 16-bit register will overflow at 32768 and underflow at -32769.
32-bit integer	31071 + 2 x (*ch - 1)* + 4 x s	
32-bit floating point	32071 + 2 x (*ch - 1)* + 4 x s	

Holding Registers (read and write registers)

Table 52 Holding Register address space

Address				
16-bit integer	**32-bit integer**	**Floating point**	**Description**	**Integer type**
40004	41007	42007	***Radio Device Specific Register 1***	Reserved
…	…	…	**…**	
40009	41015	42015	***Radio Device Specific Register 5***	Reserved
…	…	…	**…**	
40025	41049	42049	***Radio Device Specific Register 6***	Reserved
40026	41051	42051	***PWM Frequency***	unsigned
40027	41053	42053	***RX PLL Control***	unsigned
40028	41055	42055	***Channel 1 PWM Counter Max Value***	signed
40029	41057	42057	***Channel 1 PWM Counter Min Value***	signed
40030	41059	42059	***Channel 1 PWM Counter 50% Value***	signed
40031	41061	42061	***Channel 1 PWM Control Word***	unsigned
40032	41063	42063	***Channel 2 PWM Counter Max Value***	signed
40033	41065	42065	***Channel 2 PWM Counter Min Value***	signed
40034	41067	42067	***Channel 2 PWM Counter 50% Value***	signed
40035	41069	42069	***Channel 2 PWM Control Word***	unsigned

Radio Device Specific Registers

2 Channel Quadrature Encoder Transmitter does not use *Radio Device Specific Registers*

PWM Frequency Register

Table 53 PWM Frequency register

Word size	***Address***	***data type***	***Description***
16-bit integer	40026	unsigned	The nominal PWM frequency [Hz], use 10kHz.
32-bit integer	41051		
32-bit floating point	42051		

RX PLL Control Register

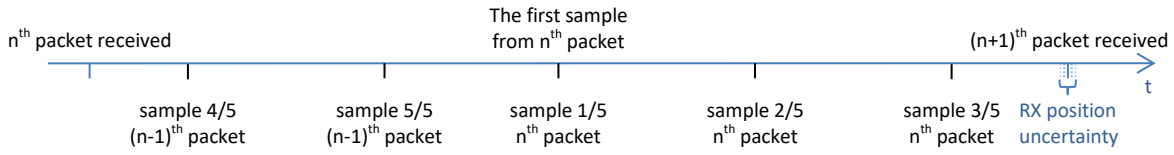

Figure 1 2 Channel Quadrature Encoder RX PLL

When ***Fixed PWM Frequency*** mode is disabled PWM frequency is locked to received packets and ***RX PLL Control Value High*** and ***RX PLL Control Value Low*** defines the amount RX PLL can control the frequency and phase in one RX period (RX PLL tries to delay the PWM by 2 and half samples, see ***Figure 1 2 Channel Quadrature Encoder RX PLL***).

PWM_frequency_true = 1/ (1/***PWM_Frequency*** - *t_control / 5)*
where
t_control = t_RX_{n+1} - $t\_1^{st}\_sample_n$ - measured_rx_period / 2
where
t_RX_{n+1} is time of arrival of $(n+1)^{th}$ packet,
$t\_1^{st}\_sample_n$ is time when first sample of n_{th} packet was updated to PWM generator,
t_control is divided by 5 because one radio packet contains 5 samples / channel,
t_control is limited to *RX PLL Control Value*, i.e. - *RX PLL Control Value* ≤ t_control ≤ *RX PLL Control Value*

Table 54 RX PLL Control Value

Word size	***Address***	***data type***	***Description***
16-bit integer	40027	unsigned	RX PLL Control limit [0.1µs] By default use 1µs
32-bit integer	41053		
32-bit floating point	42053		RX PLL Control limit [1µs]. By default use 1µs

Greater control values are the faster the PLL can shift the phase and better it can deal with variations in the incoming packet times. The disadvantage of greater control values is a bigger deviation in the PWM frequency and in the PWM duty cycles (even if the encoders counter value is constant).

When ***Fixed PWM Frequency*** mode is enabled RX PLL is detached from PWM module and PWM frequency is constant. As PWM module is not locked to the RX PLL the control parameters can be chosen to more aggressive so ***RX PLL Control Value High*** and ***RX PLL Control Value Low*** are ignored - instead the limit are ¼ of the RX period. The Advantage of the ***Fixed PWM Frequency*** is that PWM frequency is constant and the duty cycles are consistent. The disadvantage is that samples might be repeated or samples might be omitted as the clocks of the transmitter and receiver are never exactly the same.

PWM Counter Registers

PWM duty cycle is defined as
DC = (***Counter Value*** – ***PWM 50%***) / range * 100% + 50%
where
range = ***PWM Counter Max*** – ***PWM Counter Min***

Table 55 PWM Counter Max Value register, ch = 1…2

Word size	***Address***	***data type***	***Description***
16-bit integer	40028 + 4 x (ch - 1)	signed	PWM counter max scale value
32-bit integer	41055 + 8 x (ch - 1)		
32-bit floating point	42055 + 8 x (ch - 1)		

Table 56 PWM Counter Min Value register, ch = 1…2

Word size	*Address*	*data type*	*Description*
16-bit integer	40029 + 4 x (ch - 1)	signed	PWM counter min scale value
32-bit integer	41057 + 8 x (ch - 1)		
32-bit floating point	42057 + 8 x (ch - 1)		

Table 57 PWM Counter Duty Cycle 50% Value register, ch = 1…2

Word size	*Address*	*data type*	*Description*
16-bit integer	40030 + 4 x (ch - 1)	signed	PWM 50% duty cycle counter value
32-bit integer	41059 + 8 x (ch - 1)		
32-bit floating point	42059 + 8 x (ch - 1)		

Table 58 PWM Control integer register: address 16-bit 40031 + 4*(ch-1) and address 32-bit 41061 + 8*(ch-1)

Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Read Write	Reserved (only 32-bit register)															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read Write	Reserved								Fixed PWM	Reserved					50% Offset	Saturate

Table 59 PWM Control integer field description

Field	Description
15-8 or 31-8 Reserved	Should read 0
7 Fixed PWM	0: PWM frequency is locked to RX frequency and phase 1: PWM frequency is fixed to ***PWM Frequency register***
6-2 Reserved	Should read 0
1 50% Offset	Use 50% Offset register Should set this 1
0 Saturate	0: PWM saturated mode disabled 1: PWM saturated mode enabled If saturated mode enabled PWM duty cycle will not overflow or underflow, i.e. when quadrature counter value is greater that *Max Value* PWM duty cycle is 100% or is less than *Min Value* PWM duty cycle is 0% If saturated mode disabled PWM duty cycle will overflow or underflow, i.e. when quadrature counter value is *Max Value* + 1 then PWM duty cycle is overflown to 0% and counter value *Min Value* – 1 causes PWM duty cycle to underflow to 100%

Table 60 PWM Control floating point register: address 42061 + 8*(ch-1)

Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Read Write	CTRL															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read Write	CTRL															

Table 61 PWM Control floating point field description

Field	Description
31-0 CTRL	Read: Convert to unsigned integer and refer to ***Table 59 PWM Control integer field description*** Write: Generate unsigned integer according to ***Table 59*** and convert to floating point

Remote Devices

Input Registers (read only registers)

Table 62 Input Register address space

Address				
16-bit integer	**32-bit integer**	**Floating point**	**Description**	**Integer Type**
30026	31051	32051	***Device 1 Type***	unsigned
30027	31053	32053	***Device 1 ID***	unsigned
30028	31055	32055	***Device 1 Timeout***	unsigned
30029	31057	32057	Device 1 Reg 1	
…	…	…	…	
30035	31069	32069	Device 1 Reg 7	
30036	31071	32071	***Device 2 Type***	unsigned
30037	31073	32073	***Device 2 ID***	unsigned
30038	31075	32075	***Device 2 Timeout***	unsigned
30039	31077	32075	Device 2 Reg 1	
…	…	…	…	
30045	31089	32089	Device 2 Reg 7	
…	…	…	**…**	
…	…	…	**…**	
30336	31671	32671	***Device 32 Type***	unsigned
30337	31673	32673	***Device 32 ID***	unsigned
30338	31675	32675	***Device 32 Timeout***	unsigned
30339	31677	32675	Device 32 Reg 1	
…	…	…	**…**	
30345	31689	32689	Device 32 Reg 7	

Device Type Register

Table 63 Device Type register, dev = 1…32 (location in the device table and Modbus register space)

Word size	***Address***	***data type***	***Description***
16-bit integer	30026 + 10 x (dev - 1)	unsigned	Remote Device Type 0: No Device 1: Remote Switch 2: Remote Mux 3: SW and TC 4 Channel
32-bit integer	31051 + 20 x (dev - 1)		
32-bit floating point	32051 + 20 x (dev - 1)		

Device ID Register

Table 64 Device ID register, dev = 1…32 (location in the device table and Modbus register space)

Word size	***Address***	***data type***	***Description***
16-bit integer	30027 + 10 x (dev - 1)	unsigned	Device ID
32-bit integer	31053 + 20 x (dev - 1)		
32-bit floating point	32053 + 20 x (dev - 1)		

Device Timeout Register

Table 65 Device ID register, dev = 1...32 (location in the device table and Modbus register space)

Word size	*Address*	*data type*	*Description*
16-bit integer	30028 + 10 x (dev - 1)	unsigned	Devices have 120s timeout. When packet is received from device timeout counter is loaded with 120s and is decremented every second. If Timeout is 0, Device Type and ID are set to 0 unless device is defined in device mapped to location dev.
32-bit integer	31055 + 20 x (dev - 1)		
32-bit floating point	32055 + 20 x (dev - 1)		

Holding Registers (read and write registers)

Table 66 Input Register address space

Address				
16-bit integer	**32-bit integer**	**Floating point**	**Description**	**Integer Type**
40004	41007	42007	***Global Switch Control***[1]	unsigned
40005	41009	42009	***Radio Device Specific 2***	
…	…	…		
40025	41049	42049	***Global Switch State***[2]	unsigned
40026	41051	42051	***Device 1 Type***	unsigned
40027	41053	42053	***Device 1 ID***	unsigned
40028	41055	42055	***Device 1 Map***	unsigned
40029	41057	42057	***Device 1 Reg 1***	unsigned
40030	41059	42059	reserved	
…	…	…	…	
40035	41069	42069	reserved	
40036	41071	42071	***Device 2 Type***	unsigned
40037	41073	42073	***Device 2 ID***	unsigned
40038	41075	42075	***Device 2 Map***	unsigned
40039	41077	42075	***Device 2 Reg 1***	unsigned
40040	41079	42079	reserved	
…	…	…	…	
40045	41089	42089	reserved	
…	…	…	**…**	
…	…	…	**…**	
40336	41671	42671	***Device 32 Type***	unsigned
40337	41673	42673	***Device 32 ID***	unsigned
40338	41675	42675	***Device 32 Map***	unsigned
40339	41677	42675	***Device 32 Reg 1***	unsigned
40340	41679	42679	reserved	
…	…	…	…	
40345	41689	42689	reserved	

[1] *Radio Device Specific 1*

[2] *Radio Device Specific 6*

Radio Device Specific Registers

Remote Device uses Device Specific registers 1 and 6, Device Specific registers 2, 3, 4 and 5 are unused

Global Switch Control Register

Table 67 Global Switch Control unsigned integer register: address 16-bit 40004 and address 32-bit 41007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read Write	Reserved (only 32-bit register)															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read Write	Reserved														Update	SW / MUX

Table 68 Global Switch Control unsigned integer field description

Field	Description
15-2 or 31-2 Reserved	Should read 0
1 Update	0: Remote device update rate is controlled independently 1: Global Switch State register controls every devices update rate
0 SW/MUX	0: Remote device switches and muxes are controlled independently 1: Global Switch State register controls every devices switches and muxes

Table 69 Global Switch Control floating point register: address 42007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read Write	CTRL															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read Write	CTRL															

Table 70 Global Switch Control floating point field description

Field	Description
31-0 CTRL	Read: Convert to unsigned integer and refer to ***Table 68 Global Switch Control unsigned integer field description*** Write: Generate unsigned integer according to ***Table 68*** and convert to floating point

Global Switch State Register

Table 71 Global Switch State unsigned integer register: address 16-bit 40025 and address 32-bit 41049

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read Write	Reserved (only 32-bit register)															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read Write	Reserved														Update	SW/MUX

Table 72 Global Switch State unsigned integer field description.

Field	Description
15-2 or 31-2 Reserved	Should read 0
1 Update	This bit is valid only if *Update* is set in ***Global Switch Control register*** 0: Devices update rate is fastest 1: Devices update rate is slowest
0 SW/MUX	This bit is valid only if *SW/MUX* is set in ***Global Switch Control register*** 0: Switches are open, muxes select input 1, outputs are disabled 1: Switches are closed, muxes select input 2, outputs are enabled

Table 73 Global Switch State floating point register: address 42007

Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Read Write	State															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read Write	State															

Table 74 Global Switch State floating point field description

Field	Description
31-0 State	Read: Convert to unsigned integer and refer to ***Table 72 Global Switch State unsigned integer field*** description. Write: Generate unsigned integer according to ***Table 72*** and convert to floating point

Device Type Register

Table 75 Device Type register

Word size	***Address***	***data type***	***Description***
16-bit integer	40026 + 10 x (dev - 1)	unsigned	If *Mapped* is set in the ***Device Map register*** this register and ***Device ID register*** defines device mapped to location *dev*
32-bit integer	41051 + 20 x (dev - 1)		
32-bit floating point	42051 + 20 x (dev - 1)		

Device ID Register

Table 76 Device ID register

Word size	***Address***	***data type***	***Description***
16-bit integer	40027 + 10 x (dev - 1)	unsigned	If *Mapped* is set in the ***Device Map register*** this register and ***Device Type register*** defines device mapped to location *dev*
32-bit integer	41053 + 20 x (dev - 1)		
32-bit floating point	42053 + 20 x (dev - 1)		

Device Map Register

Table 77 Device Map unsigned integer register: address 16-bit 40028 + 10*(dev-1) and address 32-bit 41055 + 20*(dev-1)

Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Read Write	Reserved (only 32-bit register)															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read Write	Reserved															Mapped

Table 78 Device Map unsigned integer field description

Field	Description
15-1 or 31-1 Reserved	Should read 0
0 Mapped	0: dev location is allocated dynamically 1: dev location is reserved for device defined by ***Device Type register*** and ***Device ID registers***

Table 79 Device Map floating point register: address 42055 + 20*(dev-1)

Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Read Write	Map															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read Write	Map															

Table 80 Device Map floating point field description

Field	Description
31-0 Map	Read: Convert to unsigned integer and refer to ***Table 78 Device Map unsigned integer*** field description Write: Generate unsigned integer according to Table 78 and convert to floating point

Device Reg 1 Register

Table 81 Device ID register

Word size	***Address***	***data type***	***Description***
16-bit integer	40029 + 10*(dev-1)	unsigned	The 1st device specific register. This register can be used to set switch/mux states and update rate modes. See device specific implementation for details
32-bit integer	41057 + 20*(dev-1)		
32-bit floating point	42057 + 20*(dev-1)		

Remote Switch Device (device type = 1)

Input Registers (read only registers)

Table 82 Input Register address, dev = 1...32 (location in the device table and Modbus register space)

Address				
16-bit integer	**32-bit integer**	**Floating point**	**Description**	**Integer**
30026 + 10*(dev-1)	31051 + 20*(dev-1)	32051 + 20*(dev-1)	***Device Type***	unsigned
30027 + 10*(dev-1)	31053 + 20*(dev-1)	32053 + 20*(dev-1)	***Device ID***	unsigned
30028 + 10*(dev-1)	31055 + 20*(dev-1)	32055 + 20*(dev-1)	***Device Timeout***	unsigned
30029 + 10*(dev-1)	31057 + 20*(dev-1)	32057 + 20*(dev-1)	***Switch and Update State***	unsigned
30030 + 10*(dev-1)	31059 + 20*(dev-1)	32059 + 20*(dev-1)	***Temperature***	signed
30031 + 10*(dev-1)	31061 + 20*(dev-1)	32061 + 20*(dev-1)	***Input Voltage***	unsigned
30032 + 10*(dev-1)	31063 + 20*(dev-1)	32063 + 20*(dev-1)	***SW 1 Output Voltage***	unsigned
30033 + 10*(dev-1)	31065 + 20*(dev-1)	32065 + 20*(dev-1)	***SW 1 Output Current***	unsigned
30034 + 10*(dev-1)	31067 + 20*(dev-1)	32067 + 20*(dev-1)	***SW 2 Output Voltage***	unsigned
30035 + 10*(dev-1)	31069 + 20*(dev-1)	32069 + 20*(dev-1)	***SW 2 Output Current***	unsigned

Switch and Update Rate State Register

Refer to ***Table 88 Switch and Update Rate State integer register*** as read only register.

Temperature Register

Table 83 Temperature register

Word size	*Address*	*data type*	*Description*
16-bit integer	30030 + 10*(dev-1)	signed	Device Temperature [1/128°C]
32-bit integer	31059 + 20*(dev-1)		
32-bit floating point	32059 + 20*(dev-1)		Device Temperature [°C]

Input Voltage Register

Table 84 Input Voltage register

Word size	*Address*	*data type*	*Description*
16-bit integer	30031 + 10*(dev-1)	unsigned	Input Voltage [mV]
32-bit integer	31061 + 20*(dev-1)		
32-bit floating point	32061 + 20*(dev-1)		Input Voltage [V]

Switch Output Voltage and Current Registers

Table 85 Switch Output Voltage register, sw = 1…2

Word size	*Address*	*data type*	*Description*
16-bit integer	30032 + 10*(dev-1) + 2*(ch-1)	unsigned	Output Voltage [mV]
32-bit integer	31063 + 20*(dev-1) + 4*(ch-1)		
32-bit floating point	32063 + 20*(dev-1) + 4*(ch-1)		Output Voltage [V]

Table 86 Switch Output Current register, sw = 1…2

Word size	*Address*	*data type*	*Description*
16-bit integer	30033 + 10*(dev-1) + 2*(sw-1)	unsigned	Output Voltage [mA]
32-bit integer	31065 + 20*(dev-1) + 4*(sw-1)		
32-bit floating point	32065 + 20*(dev-1) + 4*(sw-1)		

Holding Registers (read and write registers)

Table 87 Input Register address, dev = 1…32 (location in the device table and Modbus register space)

Address				
16-bit integer	**32-bit integer**	**Floating point**	**Description**	**Integer**
40026 + 10*(dev-1)	41051 + 20*(dev-1)	42051 + 20*(dev-1)	***Device Type***	unsigned
40027 + 10*(dev-1)	41053 + 20*(dev-1)	42053 + 20*(dev-1)	***Device ID***	unsigned
40028 + 10*(dev-1)	41055 + 20*(dev-1)	42055 + 20*(dev-1)	***Device Map***	unsigned
40029 + 10*(dev-1)	41057 + 20*(dev-1)	42057 + 20*(dev-1)	***Switch and Update State***	unsigned
40030 + 10*(dev-1)	41059 + 20*(dev-1)	42059 + 20*(dev-1)	reserved	
40031 + 10*(dev-1)	41061 + 20*(dev-1)	42061 + 20*(dev-1)	reserved	
40032 + 10*(dev-1)	41063 + 20*(dev-1)	42063 + 20*(dev-1)	reserved	
40033 + 10*(dev-1)	41065 + 20*(dev-1)	42065 + 20*(dev-1)	reserved	
40034 + 10*(dev-1)	41067 + 20*(dev-1)	42067 + 20*(dev-1)	reserved	
40035 + 10*(dev-1)	41069 + 20*(dev-1)	42069 + 20*(dev-1)	reserved	

Switch and Update Rate State Register

Table 88 Switch and Update Rate State integer register

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read Write	Reserved (only 32-bit register)															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read Write	Reserved								Update	Reserved				SW2	SW1	6.5V Supply

Table 89 Switch and Update Rate State integer field description

Field	Description
15-8 or 31-8 Reserved	
7 Update	0: Update interval 20s 1: Update interval 2s
6-3 Reserved	
2 SW2	0: Switch 2 open 1: Switch 2 closed
1 SW1	0: Switch 1 open 1: Switch 1 closed
0 6.5V Supply	0: 6.5V output disabled 1: 6.5V output enabled Note! When 6.5V Output is enabled update interval is 2s

Table 90 Switch and Update Rate State floating point register

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read Write	State															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read Write	State															

Table 91 Switch and Update Rate State unsigned integer field description

Field	Description
31-0 State	Read: Convert to unsigned integer and refer to **Table 89 Switch and Update Rate State integer field description** Write: Create unsigned integer according to **Table** 89 and convert to floating point

Remote Mux Device (device type = 2)

Input Registers (read only registers)

Table 92 Input Register address, dev = 1...32 (location in the device table and Modbus register space)

Address				
16-bit integer	**32-bit integer**	**Floating point**	**Description**	**Integer**
30026 + 10*(dev-1)	31051 + 20*(dev-1)	32051 + 20*(dev-1)	***Device Type***	unsigned
30027 + 10*(dev-1)	31053 + 20*(dev-1)	32053 + 20*(dev-1)	***Device ID***	unsigned
30028 + 10*(dev-1)	31055 + 20*(dev-1)	32055 + 20*(dev-1)	***Device Timeout***	unsigned
30029 + 10*(dev-1)	31057 + 20*(dev-1)	32057 + 20*(dev-1)	***Mux and Update State***	unsigned
30030 + 10*(dev-1)	31059 + 20*(dev-1)	32059 + 20*(dev-1)	***Temperature***	signed
30031 + 10*(dev-1)	31061 + 20*(dev-1)	32061 + 20*(dev-1)	***Input Voltage***	unsigned
30032 + 10*(dev-1)	31063 + 20*(dev-1)	32063 + 20*(dev-1)	reserved	
30033 + 10*(dev-1)	31065 + 20*(dev-1)	32065 + 20*(dev-1)	reserved	
30034 + 10*(dev-1)	31067 + 20*(dev-1)	32067 + 20*(dev-1)	reserved	
30035 + 10*(dev-1)	31069 + 20*(dev-1)	32069 + 20*(dev-1)	reserved	

Mux and Update Rate State Register

Refer to ***Table 96 Mux and Update Rate State unsigned integer register*** as read only register.

Temperature Register

Table 93 Temperature register

Word size	***Address***	***data type***	***Description***
16-bit integer	30030 + 10 x (dev - 1)	signed	Device Temperature [1/128°C]
32-bit integer	31059 + 20 x (dev - 1)		
32-bit floating point	32059 + 20 x (dev - 1)		Device Temperature [°C]

Input Voltage Register

Table 94 Input Voltage register

Word size	***Address***	***data type***	***Description***
16-bit integer	30031 + 10*(dev-1)	unsigned	Input Voltage [mV]
32-bit integer	31061 + 20*(dev-1)		
32-bit floating point	32061 + 20*(dev-1)		Input Voltage [V]

Holding Registers (read and write registers)

Table 95 Input Register address, dev = 1...32 (location in the device table and Modbus register space)

Address				
16-bit integer	**32-bit integer**	**Floating point**	**Description**	**Integer**
40026 + 10*(dev-1)	41051 + 20*(dev-1)	42051 + 20*(dev-1)	***Device Type***	unsigned
40027 + 10*(dev-1)	41053 + 20*(dev-1)	42053 + 20*(dev-1)	***Device ID***	unsigned
40028 + 10*(dev-1)	41055 + 20*(dev-1)	42055 + 20*(dev-1)	***Device Map***	unsigned
40029 + 10*(dev-1)	41057 + 20*(dev-1)	42057 + 20*(dev-1)	***Mux and Update State***	unsigned
40030 + 10*(dev-1)	41059 + 20*(dev-1)	42059 + 20*(dev-1)	reserved	
40031 + 10*(dev-1)	41061 + 20*(dev-1)	42061 + 20*(dev-1)	reserved	
40032 + 10*(dev-1)	41063 + 20*(dev-1)	42063 + 20*(dev-1)	reserved	
40033 + 10*(dev-1)	41065 + 20*(dev-1)	42065 + 20*(dev-1)	reserved	
40034 + 10*(dev-1)	41067 + 20*(dev-1)	42067 + 20*(dev-1)	reserved	
40035 + 10*(dev-1)	41069 + 20*(dev-1)	42069 + 20*(dev-1)	reserved	

Mux and Update Rate State Register

Table 96 Mux and Update Rate State unsigned integer register

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read Write	Reserved (only 32-bit register)															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read Write	Reserved								Update	Reserved			MUX4	MUX3	MUX2	MUX1

Table 97 Mux and Update Rate State unsigned integer field description

Field	Description
15-8 or 31-8 Reserved	
7 Update	0: Update interval 20s 1: Update interval 2s
6-4 Reserved	
3 MUX4	0: Mux 4 Output 1 1: Mux 4 Output 2
2 MUX3	0: Mux 3 Output 1 1: Mux 3 Output 2
1 MUX2	0: Mux 2 Output 1 1: Mux 2 Output 2
0 MUX1	0: Mux 1 Output 1 1: Mux 1 Output 2

Table 98 Switch and Update Rate State floating point register

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read Write	State															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read Write	State															

Table 99 Switch and Update Rate State unsigned integer field description

Field	Description
31-0 State	Read: Convert to unsigned integer and refer to ***Table 97 Mux and Update Rate State unsigned integer field*** description Write: Create unsigned integer according to ***Table*** 97 and convert to floating point

RemoteSWmini (4 Channel TC) (device type = 3)

Input Registers (read only registers)

Table 100 Input Register address, dev = 1...32 (location in the device table and Modbus register space)

Address				
16-bit integer	**32-bit integer**	**Floating point**	**Description**	**Integer**
30026 + 10*(dev-1)	31051 + 20*(dev-1)	32051 + 20*(dev-1)	***Device Type***	unsigned
30027 + 10*(dev-1)	31053 + 20*(dev-1)	32053 + 20*(dev-1)	***Device ID***	unsigned
30028 + 10*(dev-1)	31055 + 20*(dev-1)	32055 + 20*(dev-1)	***Device Timeout***	unsigned
30029 + 10*(dev-1)	31057 + 20*(dev-1)	32057 + 20*(dev-1)	***Switch and Update State***	unsigned
30030 + 10*(dev-1)	31059 + 20*(dev-1)	32059 + 20*(dev-1)	***Temperature***	signed
30031 + 10*(dev-1)	31061 + 20*(dev-1)	32061 + 20*(dev-1)	***Input Voltage***	unsigned
30032 + 10*(dev-1)	31063 + 20*(dev-1)	32063 + 20*(dev-1)	***TC Ch 1 Temperature***	signed
30033 + 10*(dev-1)	31065 + 20*(dev-1)	32065 + 20*(dev-1)	***TC Ch 2 Temperature***	signed
30034 + 10*(dev-1)	31067 + 20*(dev-1)	32067 + 20*(dev-1)	***TC Ch 3 Temperature***	signed
30035 + 10*(dev-1)	31069 + 20*(dev-1)	32069 + 20*(dev-1)	***TC Ch 4 Temperature***	signed

Switch and Update Rate State Register

Refer to ***Table 105 Switch and Update Rate State unsigned integer register*** as read only register.

Temperature Register

Table 101 Temperature register

Word size	***Address***	***data type***	***Description***
16-bit integer	30030 + 10 x (dev - 1)	signed	Device Temperature [1/128°C]
32-bit integer	31059 + 20 x (dev - 1)		
32-bit floating point	32059 + 20 x (dev - 1)		Device Temperature [°C]

Input Voltage Register

Table 102 Input Voltage register

Word size	***Address***	***data type***	***Description***
16-bit integer	30031 + 10 x (dev - 1)	unsigned	Input Voltage [mV]
32-bit integer	31061 + 20 x (dev - 1)		
32-bit floating point	32061 + 20 x (dev - 1)		Input Voltage [V]

Thermocouple (TC) temperature

Table 103 Switch Output Voltage register, ch = 1…4

Word size	***Address***	***data type***	***Description***
16-bit integer	30032 + 10*(dev-1) + (ch-1)	signed	Thermocouple Temperature [1/16°C]
32-bit integer	31063 + 20 x (dev-1) + 2 x (ch-1)		
32-bit floating point	32063 + 20 x (dev-1) + 2 x (ch-1)		Thermocouple Temperature [°C]

Holding Registers (read and write registers)

Table 104 Input Register address, dev = 1...32 (location in the device table and Modbus register space)

Address				
16-bit integer	**32-bit integer**	**Floating point**	**Description**	**Integer**
40026 + 10*(dev-1)	41051 + 20*(dev-1)	42051 + 20*(dev-1)	***Device Type***	unsigned
40027 + 10*(dev-1)	41053 + 20*(dev-1)	42053 + 20*(dev-1)	***Device ID***	unsigned
40028 + 10*(dev-1)	41055 + 20*(dev-1)	42055 + 20*(dev-1)	***Device Map***	unsigned
40029 + 10*(dev-1)	41057 + 20*(dev-1)	42057 + 20*(dev-1)	***Switch and Update State***	unsigned
40030 + 10*(dev-1)	41059 + 20*(dev-1)	42059 + 20*(dev-1)	reserved	
40031 + 10*(dev-1)	41061 + 20*(dev-1)	42061 + 20*(dev-1)	reserved	
40032 + 10*(dev-1)	41063 + 20*(dev-1)	42063 + 20*(dev-1)	reserved	
40033 + 10*(dev-1)	41065 + 20*(dev-1)	42065 + 20*(dev-1)	reserved	
40034 + 10*(dev-1)	41067 + 20*(dev-1)	42067 + 20*(dev-1)	reserved	
40035 + 10*(dev-1)	41069 + 20*(dev-1)	42069 + 20*(dev-1)	reserved	

Switch and Update Rate State Register

Table 105 Switch and Update Rate State unsigned integer register

Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Read Write	Reserved (only 32-bit register)															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read Write	Reserved								Update		Reserved					6V Output

Table 106 Switch and Update Rate State unsigned integer field description

Field	**Description**
15-8 or 31-8 Reserved	
7-6 Update	00: Update interval 20 10: Update interval 2s X1: Update rate 5Hz
5-1 Reserved	
0 6V Output	0: 6V output voltage disabled 1: 6V output voltage enabled Note! When 6V output voltage enabled update interval is a 2s or 5Hz