

# Small-Signal Synchronization Stability of Grid-Forming Converters With Regulated DC-Link Dynamics

Liang Zhao<sup>ID</sup>, Student Member, IEEE, Zheming Jin<sup>ID</sup>, Member, IEEE, and Xiongfei Wang<sup>ID</sup>, Fellow, IEEE

**Abstract**—The dc-link voltage dynamics can be directly used to synchronize grid-forming (GFM) converters with ac grids. However, such control scheme is prone to unstable low-frequency oscillations (LFO), owing to the constant-power dynamics at the dc link. This article analyzes first the small-signal stability of dc-link voltage-synchronized GFM converters, and proposes a control method for enhancing the system stability under different operating scenarios. In the approach, a  $q$ -axis voltage-feedforward control is introduced in parallel with the dc-link voltage control for the grid-synchronization purpose. The LFO problem with the conventional dc-link voltage-synchronization control is mitigated. Compared to conventional cascaded/paralleled dc-link voltage- and active power-based synchronization, the method mitigates the synchronous oscillation problem. Experimental tests are performed for the GFM converter operating in both rectifier and inverter modes and with different grid strengths. The results corroborate theoretical analyses and validate the effectiveness of the approach.

**Index Terms**—Active damping, dc-link voltage control, grid synchronization, small-signal stability, voltage-source converter.

## I. INTRODUCTION

POWER-SYNCHRONIZATION control (PSC) is an attractive method for voltage-source converters (VSCs) in renewable energy integrated power grids [1]. The small-signal stability of VSCs is a key concern and has been extensively studied in recent years. It is shown that the power-synchronized VSC demonstrates robust small-signal stability over the phase-locked loop (PLL)-synchronized VSC under the weak grid [2], while it

Manuscript received 25 August 2022; revised 3 December 2022; accepted 27 December 2022. Date of publication 9 January 2023; date of current version 9 June 2023. This work was supported in part by the Independent Research Fund Denmark under Grant 1032-00375B and in part by the National Natural Science Foundation of China under Grant 52202458. (*Corresponding author: Zheming Jin.*)

Liang Zhao is with the Department of Energy (AAU Energy), Aalborg University, 9220 Aalborg, Denmark (e-mail: lzh@energy.aau.dk).

Zheming Jin is with the School of Electrical Engineering, Beijing Jiaotong University, Beijing 100044, China (e-mail: zhmjn@bjtu.edu.cn).

Xiongfei Wang is with the Division of Electric Power and Energy Systems, KTH Royal Institute of Technology, 11428 Stockholm, Sweden, and also with the Department of Energy (AAU Energy), Aalborg University, 9220 Aalborg, Denmark (e-mail: xiongfei@kth.se, xwa@energy.aau.dk).

Color versions of one or more figures in this article are available at <https://doi.org/10.1109/TIE.2023.3234147>.

Digital Object Identifier 10.1109/TIE.2023.3234147

may suffer from instability issues under stiff grids [3]. Moreover, the PSC may interact with the ac voltage control in stiff grids, causing subsynchronous oscillations [4]. The oscillations caused by the coupling between the outer power control and the inner vector voltage control are revealed in [5]. A power dynamic decoupling control method is reported in [6] to enhance the system damping of grid-forming (GFM) converters in stiff grids.

Recently, a hybrid synchronization control (HSC) approach that merges the voltage-based synchronization control into the PSC is reported [7]. It is found in [8] that the voltage-based synchronization loop essentially mimics the damper winding of synchronous generators, which enhances the transient stability of GFM converters. On the other hand, increasing the proportional gain of the voltage-based synchronization loop may lead to resonance [9]. Further, in those PSC- or HSC-based GFM converters, a constant dc-link voltage source is assumed, which can be maintained by the front-end converter or the energy storage system at the dc link of VSCs.

A constant dc-link voltage source is not always available for grid-connected VSCs, such as the VSCs found in hybrid ac/dc grids [2], railway traction systems [10], and static synchronous compensators [11], where VSCs are required to regulate the dc-link voltage. Since the dc-link voltage dynamics represent the active power balance at the dc link, the dc-link voltage control (DVC) needs to be integrated with the PSC for GFM converters.

Some research works that merge DVC and PSC have been reported in [2], [11], [12], [13], [14], [15], [16], [17], [18], [19]. A common approach is to cascade the DVC and PSC [2], [12], [13]. The DVC generates the active power reference, and the grid synchronization is still realized by the PSC. The impact of this control method on the small-signal dynamics of VSCs is characterized by impedance modeling [13]. It is shown that oscillations are aroused under weak grids if the parameters of DVC and PSC are not properly tuned. Besides, the dc-link voltage dynamics can directly generate the frequency without involving the PSC [11], [14], [15]. This dc-link voltage-synchronization control (DVSC) is also known as the matching control [16]. Moreover, a dual-port GFM control is discussed in [17], which can be regarded as adding a paralleled active power-frequency feedforward (PFF) loop to the DVSC [18]. The oscillations also arise due to the interaction between paralleled control loops [19], yet the tunable range of DVC parameters within the paralleled scheme is wider than that in the cascaded scheme. Meanwhile, the equivalent transformation between cascaded and paralleled configurations

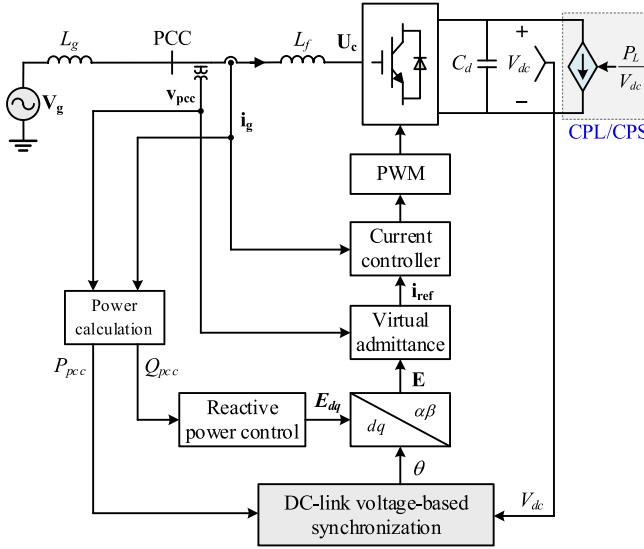


Fig. 1. System block diagram of the GFM converter.

of DVC and PSC is revealed in [18]. Yet, the small-signal stability implications of those different synchronization control loops, considering both rectifier and inverter modes with dc-link constant-power load/source (CPL/CPS), are still unclear.

This article, thus, analyzes the small-signal synchronization stability of dc-link voltage-synchronized VSCs. Two instability issues that challenge the conventional DVC of GFM converters are discussed. A control method that enhances the synchronization stability of GFM converters is proposed. The main contributions are summarized as follows:

- 1) Single-input single-output (SISO) small-signal models of conventional dc-link voltage-synchronization control schemes are developed, through which, instability issues of the system with CPL/CPS at the dc link are identified. They are low-frequency oscillations (LFO) when using the single-loop DVSC scheme and the synchronous oscillations (SO) issue with the paralleled/ cascaded DVC and PSC methods.
- 2) An enhanced synchronization control scheme that introduces a  $q$ -axis voltage feedforward ( $V_q$ FF) loop in parallel with the DVC is proposed. The scheme mitigates the LFO issue of the single-loop DVSC, and the SO issue with the paralleled/cascaded DVC and PSC methods.
- 3) A parameter design guideline for the proposed  $V_q$ FF+DVC method is developed to make GFM converters operate stably in both rectifier and inverter modes with CPL/CPS at the dc link, as well as under different ac grid strengths.

Finally, the effectiveness of theoretical analysis and the proposed method is validated by experimental tests.

## II. SYSTEM DESCRIPTION

Fig. 1 shows the system block diagram of the GFM converter, where different control stages are demonstrated. The single-phase VSC is connected to the point of common coupling (PCC) through an inductor ( $L$ ) filter. The ac grid is represented by

an ideal voltage source  $\mathbf{V}_g$  cascaded with the grid inductance  $L_g$  [20], [21], [22]. The PCC voltage and grid current are represented by  $\mathbf{v}_{pcc}$  and  $\mathbf{i}_g$ , respectively.  $P_{pcc}/Q_{pcc}$  denote the active/reactive power at PCC, where the reference direction of power flow is defined from the grid to the converter.

The CPL and CPS widely exist in dc grids, whose negative resistance characteristics challenge the system stability [23]. Thus, the dc-link CPL/CPS is considered in the GFM converter, which is represented by a controlled current source  $i_{dc}(t) = P_L/V_{dc}(t)$  [23]. Positive and negative values of  $P_L$  denote a CPL and a CPS, respectively.

The GFM converter demonstrates the voltage-source behavior that is represented by the EMF vector. The phase angle of the EMF vector is generated by the dc-link voltage-based synchronization schemes, which will be detailed in subsequent sections. The EMF magnitude is regulated by reactive power control (RPC) loop. The droop control of EMF magnitude versus reactive power ( $Q-E$ ) is adopted. The control law is given by

$$E = E_{ref} - k_q \cdot (Q_0 - Q_{pcc}) \quad (1)$$

where  $Q_0$  denotes the reactive power reference, while  $E_{ref}$  is the reference of EMF magnitude. The EMF vector is then generated through the inverse park transformation, which is given by

$$\mathbf{E} = E \cdot e^{j\theta}. \quad (2)$$

The virtual admittance (VA) control is employed in the intermediate loop, which is utilized for the output impedance regulation and current limitation. The control is given by

$$\mathbf{i}_{ref} = Y_{v\_alpha\beta} \cdot (\mathbf{v}_{pcc} - \mathbf{E}), \quad Y_{v\_alpha\beta} = \frac{1}{s \cdot L_v + R_v} \quad (3)$$

where  $L_v$  and  $R_v$  denote the virtual inductance and the virtual resistance, respectively.

The current control (CC) loop adopts a  $\alpha\beta$ -frame proportional-resonant (PR) controller for the current regulation. The control law is given by

$$\mathbf{E}_c = G_{PR} \cdot (\mathbf{i}_g - \mathbf{i}_{ref}), \quad G_{PR} = k_{pi} + \frac{k_{ri} s}{s^2 + 2\omega_r s + \omega_1^2} \quad (4)$$

where  $k_{pi}$  and  $k_{ri}$  denote the proportional and resonant gains, respectively. The circuit and control parameters of the GFM converter are presented in Table I.

## III. ISSUES WITH CONVENTIONAL DC-LINK VOLTAGE-SYNCHRONIZATION CONTROL

This section is dedicated to analyzing the stability issues of conventional dc-link voltage-synchronization control schemes. The LFO issue with the single-loop DVSC and the SO issue with the cascaded/paralleled DVC+PSC method are identified, respectively.

### A. SISO Small-Signal Model With Single-Loop DVSC

The closed-loop dynamics of the GFM converter are determined by the ac circuit dynamics, the dc-link load/source dynamics, and the used control loops. To evaluate the stability impact of different synchronization loops, a SISO small-signal

**TABLE I**  
PARAMETERS OF THE GFM CONVERTER

Symbol	Description	Value
$P_0$	Rated power	1.6MW (1 p.u.)
$V_g$	Grid voltage RMS	1900V/50Hz (1 p.u.)
$V_{dcref}$	DC-link voltage reference	3300V
$L_f$	Filter inductance	3.3mH (0.46 p.u.)
$C_d$	DC-link capacitor	3.0mF
$\omega_0$	Nominal angular frequency	$100\pi$
$E_{ref}$	Nominal EMF reference	1900V (1 p.u.)
$Q_0$	Reactive power reference	0
$K_p$	DVC proportional gain	0.2 p.u.
$K_i$	DVC integral gain	0 or 1 p.u.
$k_q$	RPC droop gain	$0.1 E_{ref}/P_0$ (0.1 p.u.)
$L_v / R_v$	Virtual admittance	0.15p.u. / 0.1p.u.
$k_{pi} / k_{ri}$	Current controller	4.8/350 (2.1/0.5 p.u.)
$f_s$	Sampling frequency	2800Hz

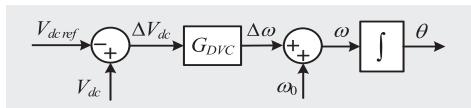


Fig. 2. Block diagram of the single-loop DVSC.

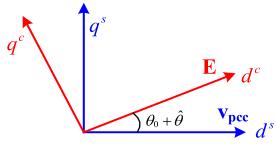


Fig. 3. System and controller  $dq$ -frames.

model is developed to characterize the reference-to-output dynamics of the dc-link voltage. The SISO model highlights different synchronization loops while the rest parts are integrated as a transfer function. In this way, analytical insights into the stability effect of synchronization control loops can be provided through the SISO block diagram [24].

Fig. 2 shows the block diagram of the single-loop DVSC. The dc-link voltage dynamics are utilized to generate the frequency and phase angle of the ac output. The control law is given by

$$\omega = \omega_0 + G_{DVC} \cdot (V_{dc} - V_{dcref}), \quad \theta = \int \omega dt \quad (5)$$

where  $G_{DVC}$  denotes the dc-link voltage controller.

Under small-signal perturbations, the phase angle dynamic of (5) can be represented as

$$\hat{\theta} = \frac{1}{s} \cdot G_{DVC} \cdot (\hat{V}_{dc} - \hat{V}_{dcref}). \quad (6)$$

Fig. 3 shows the two reference frames, which is generated due to the impact of synchronization dynamics. The system and controller  $dq$ -frames are defined by the PCC voltage and the EMF vector, respectively. The superscript  $s$  denotes variables referred to the system  $dq$ -frame, and the superscript  $c$  denotes variables referred to the controller  $dq$ -frame. Moreover, the

steady-state operating points are denoted with subscript “ $0$ ”, e.g.,  $V_{dc0}$  denotes the operating point of dc-link voltage. The small-signal expressions of circuit and control variables are represented with the symbol “ $\hat{\cdot}$ ”, e.g.,  $\hat{V}_{dc}$  denotes the dc-link voltage under the small-signal perturbation.

Fig. 4 shows the overall block diagram of the small-signal model, where the circuit and control dynamics are detailed. The circuit relationship of grid voltage, PCC voltage, and grid current is given by

$$V_{gdq0}^s - (u_{dq0}^s + \hat{u}_{dq}^s) = Z_g (i_{dq0}^s + \hat{i}_{dq}^s) \Rightarrow \hat{u}_{dq}^s = -Z_g \cdot \hat{i}_{dq}^s \quad (7)$$

where the grid impedance is represented by

$$Z_g = \begin{bmatrix} sL_g + R_g & -\omega_1 L_g \\ \omega_1 L_g & sL_g + R_g \end{bmatrix} \quad (8)$$

The terminal voltage behind the L-filter is given by

$$u_{cdq}^s = u_{dq}^s - (sL_f + j\omega_1 L_f) \cdot i_{dq}^s. \quad (9)$$

The active power transferred from ac to dc sides is given by

$$\hat{P}_{dc} = \underbrace{\frac{1}{2} [i_{d0}^s \ i_{q0}^s] \hat{u}_{dq}^s}_{G_{P_{dc}}^u} + \underbrace{\frac{1}{2} [u_{d0}^s - sL_f i_{d0}^s \ u_{q0}^s - sL_f i_{q0}^s] \hat{i}_{dq}^s}_{G_{P_{dc}}^i}. \quad (10)$$

The dc-link power balance with small-signal perturbations is represented by

$$(P_{dc} + \hat{P}_{dc}) - P_L = C_d (V_{dc0} + \hat{V}_{dc}) \cdot d (V_{dc0} + \hat{V}_{dc}) / dt. \quad (11)$$

The dynamic relationship of dc-link voltage versus active power is given by

$$\hat{V}_{dc} = \hat{P}_{dc} / (s C_d V_{dc0}). \quad (12)$$

The PCC reactive power is calculated by

$$\hat{Q}_{pcc} = \underbrace{\frac{1}{2} [-i_{q0}^s \ i_{d0}^s] \cdot \hat{u}_{dq}^s}_{G_Q^u} + \underbrace{\frac{1}{2} [u_{q0}^s \ -u_{d0}^s] \cdot \hat{i}_{dq}^s}_{G_Q^i}. \quad (13)$$

The EMF magnitude is then expressed by

$$\hat{E}_{dq}^c = I_{21} \cdot k_q \cdot \hat{Q}_{pcc}, \quad I_{21} = [1 \ 0]^T. \quad (14)$$

The park transformation of the EMF is given by

$$E_{dq0}^s + \hat{E}_{dq}^s = e^{j(\theta_0 + \hat{\theta})} \cdot (E_{dq0}^c + \hat{E}_{dq}^c). \quad (15)$$

The VA control and the CC are implemented in the stationary  $(\alpha\beta)$  frame with the control law (3) and (4). Through the frequency translation [25], the control laws can be represented in the  $dq$ -frame and are given by

$$\begin{cases} i_{dqref}^s = \underbrace{e^{-j\theta^s} Y_{v_{-\alpha\beta}}(s)}_{Y_{v_{dq}}} \cdot (u_{dq}^s - E_{dq}^s) \\ E_{cdq}^s = \underbrace{e^{-j\theta^s} G_{PR}(s)}_{G_{idq}} \cdot (i_{dq}^s - i_{dqref}^s) \end{cases}. \quad (16)$$

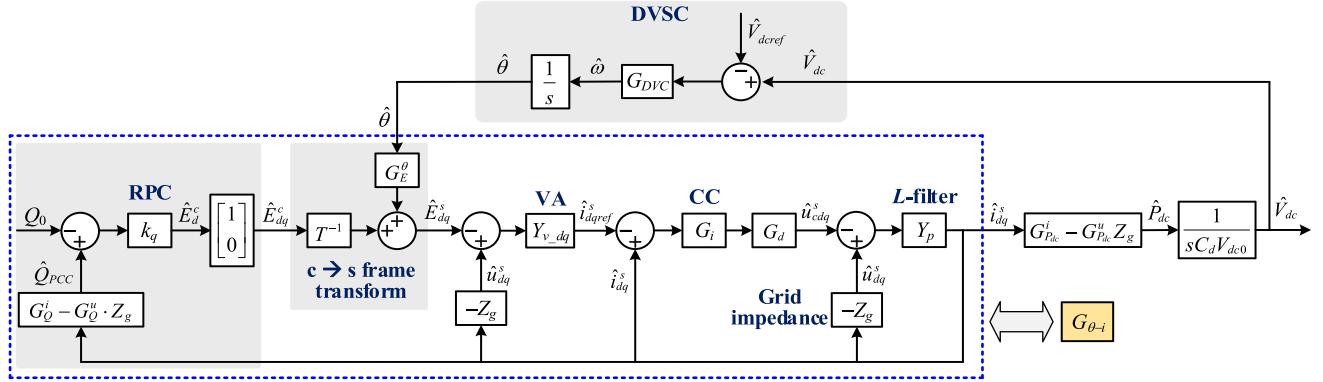


Fig. 4. Block diagram of the small-signal model with single-loop DVSC.

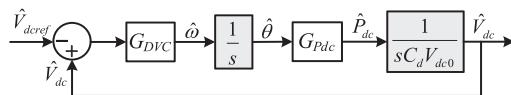


Fig. 5. SISO small-signal model with single-loop DVSC.

In Fig. 4, the dynamics of RPC, frame transformation, VA, CC, and ac *L*-filter can be represented by a transfer function matrix, given by

$$G_{\theta-i} = - \left[ \begin{matrix} Z_g + Z_p + G_d G_i + G_d G_i Y_{v-dq} Z_g \\ + G_d G_i Y_{v-dq} T^{-1} I_{21} k_q (G_Q^i - G_Q^u Z_g) \end{matrix} \right]^{-1} \times G_d G_i Y_{v-dq} G_E^\theta \quad (17)$$

where the input and output signals are the phase angle and the grid current, respectively.

Fig. 5 shows the SISO small-signal model of the single-loop DVSC-VSC, which is equivalent to Fig. 4 but utilizing the representation in (17). The transfer function of dc-link active power versus phase angle is given by

$$G_{P_{dc}} = (G_{P_{dc}}^i - G_{P_{dc}}^u Z_g) G_{\theta-i}. \quad (18)$$

The open-loop and closed-loop transfer functions of reference-to-output of the dc-link voltage are derived as

$$T_{DVSC} = \frac{-G_{P_{dc}} \cdot G_{DVC}}{s C_d V_{dc0} \cdot s},$$

$$T_{closed} = \frac{V_{dc}}{V_{dcref}} (s) = \frac{T_{DVSC}}{1 + T_{DVSC}}. \quad (19)$$

### B. LFO Issue With Single-Loop DVSC

From the SISO model shown in Fig. 5, it is noted that there are two integrators in the closed-loop control diagram of dc-link voltage. The first integrator is served to generate the phase angle from the frequency. The second integrator is included in the transfer function of dc-link voltage versus active power derived in (12), which reflects the dynamics of dc-link CPL/CPS. Those two integrators yield 180° phase lag, which thus deteriorates the phase margin of the closed-loop control. Therefore, the

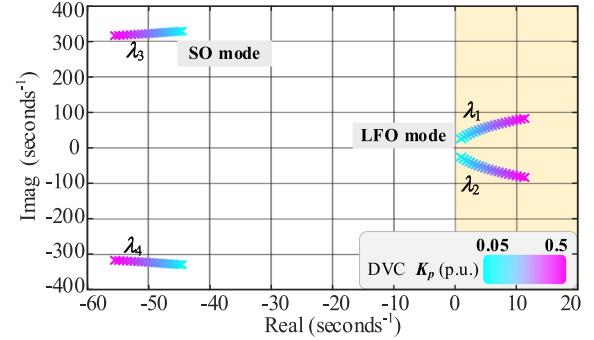


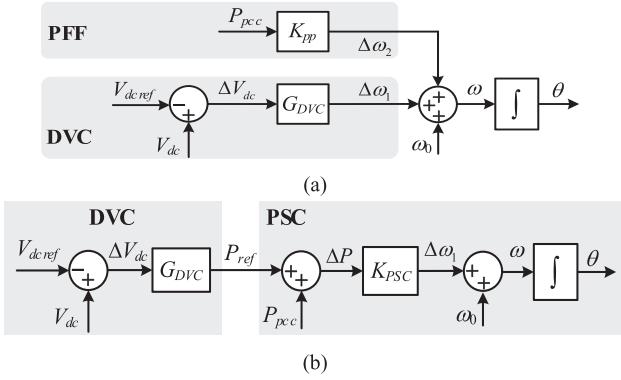
Fig. 6. Closed-loop pole trajectories with single-loop DVSC in the rectifier mode, SCR = 1.2.

DVSC-based GFM converter suffers from the LFO issue when the CPL/CPS is connected to the dc-link.

The small-signal stability is further evaluated through the poles of the closed-loop transfer function (19) [26], [27]. Fig. 6 shows closed-loop pole trajectories with single-loop DVSC method. The GFM converter operates in the rectifier mode with SCR = 1.2. The DVSC adopts a proportional (P) controller that  $K_p$  represents, and  $K_i = 0$ . It is shown that there are two oscillatory modes that determine the system stability. The low-frequency conjugate poles  $\lambda_{1-2}$  denote the LFO mode, and the synchronous-frequency conjugate poles  $\lambda_{3-4}$  denote the SO mode. In Fig. 6, the LFO-mode conjugate poles  $\lambda_{1-2}$  are always located in the right-half plane (RHP) with different DVC proportional gains. Therefore, it proves that the GFM converter with single-loop DVSC suffers from the LFO issue.

### C. LFO Mitigation and SO Issue With Cascaded/Paralleled DVC and PSC Methods

Fig. 7 shows two control schemes that merge DVC and PSC. Compared to the single-loop DVSC, the active power loop is included in those two schemes. In Fig. 7(a), the PFF loop is configured in parallel with the DVC [18]. A PI controller is adopted in  $G_{DVC}$  for the dc-link voltage reference tracking,



**Fig. 7.** Conventional control methods of merging DVC and PSC. (a) Paralleled PFF- and DVC-based synchronization (PFF+DVC) method. (b) Cascaded DVC and PSC method.

given by

$$G_{DVC} = K_p + K_i/s \quad (20)$$

where  $K_p$  and  $K_i$  denote the proportional and integral gains. The PFF loop adopts a P controller represented with  $K_{pp}$  (1 p.u.  $K_{pp} = \omega_0/P_0$ ). Fig. 7(b) shows the cascaded DVC and PSC scheme, where the DVC generates the active power reference for the PSC. It has been reported in [18] that the paralleled control scheme can be equivalently transformed into the cascaded configuration. According to the block diagram algebra [26], the control parameter equivalence is given by

$$G_{DVC\_parallel} = G_{DVC\_cascaded} \cdot K_{PSC}, \quad K_{pp} = K_{PSC} \quad (21)$$

where the subscript *parallel* and *cascaded* refer to controllers in the paralleled and cascaded schemes, respectively. Therefore, the stability analysis in this paper is performed based on the paralleled PFF+DVC method in Fig. 7(a).

Fig. 8(a) shows the SISO small-signal model with the conventional PFF+DVC method, which is derived by integrating the PFF dynamics into the SISO model of single-loop DVSC-VSC shown in Fig. 5. The PCC active power is calculated by

$$\hat{P}_{pcc} = \underbrace{\frac{1}{2} [i_{d0}^s \quad i_{q0}^s] \cdot \hat{u}_{dq}^s}_{G_P^u} + \underbrace{\frac{1}{2} [u_{d0}^s \quad u_{q0}^s] \cdot \hat{i}_{dq}^s}_{G_P^i}. \quad (22)$$

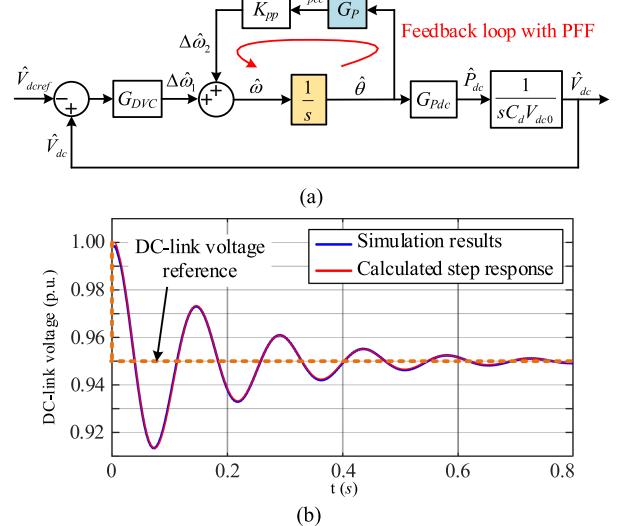
Recalling (7) and (17), The PFF dynamics are given by

$$\begin{cases} \hat{P}_{pcc} = \underbrace{(G_P^i - G_P^u Z_g)}_{G_P} G_{\theta-i} \cdot \hat{\theta} \\ \Delta\hat{\omega}_2 = K_{pp} \cdot G_P \cdot \hat{\theta} \end{cases}. \quad (23)$$

The open-loop and closed-loop transfer functions of reference-to-output of the dc-link voltage are derived as

$$T_{PFF} = \frac{-G_{Pdc} \cdot G_{DVC}}{s C_d V_{dc0} (s - K_{pp} G_P)}, \quad T_{closed} = \frac{T_{PFF}}{1 + T_{PFF}}. \quad (24)$$

Through the closed-loop transfer function, the step response of the dc-link voltage can be derived and is shown in Fig. 8(b).



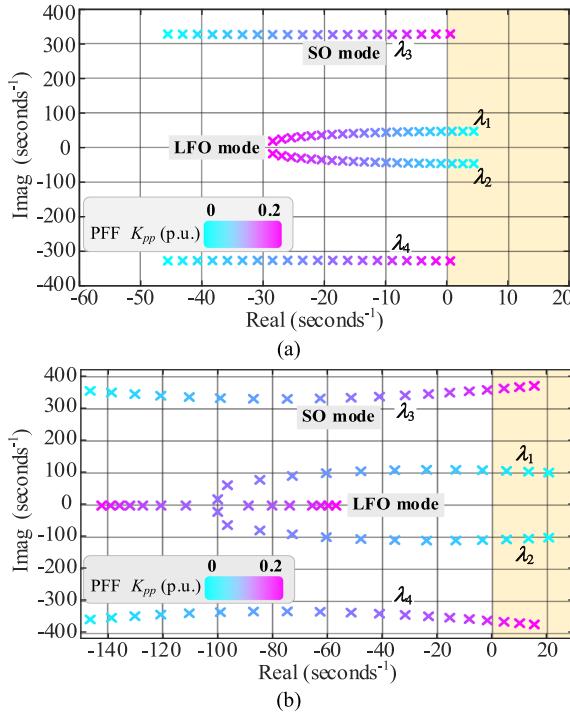
**Fig. 8.** SISO small-signal model of conventional PFF+DVC method and its validation. (a) SISO model. (b) Step response of the dc-link voltage.

It well matches with the time-domain simulation, which thus validates the accuracy of the derived SISO model.

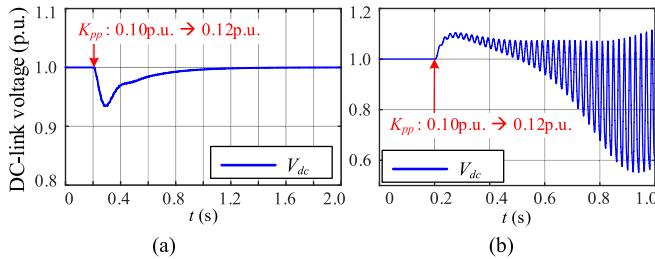
From the SISO model shown in Fig. 8(a), it is observed that the PFF control forms a negative feedback loop from phase angle to frequency ( $G_P$  is with negative gain according to the power-angle relationship). Therefore, active damping is provided to dc-link voltage-frequency control. The LFO issue is thus mitigated. However, it is also noted that the transfer function of active power versus phase angle, i.e.,  $G_P$ , includes a pair of conjugate poles at the synchronous frequency [2]. Therefore, the PFF-formed feedback loop is also a resonant loop at synchronous frequency. A larger resonance peak would be generated with the increase of PFF proportional gain, which may lead to the SO issue.

Fig. 9 shows closed-loop pole trajectories with the proposed PFF+DVC method. The GFM converter operates in both rectifier and inverter modes with dc-link CPL/CPS and under different grid strengths. It is shown that the LFO-mode RHP poles  $\lambda_{1-2}$  from the RHP to the left-half plane (LHP) with the increase of the PFF proportional gain, implying that the PFF control mitigates the LFO issue. However, the SO-mode poles  $\lambda_{3-4}$  move toward an opposite direction from the LFO-mode poles  $\lambda_{1-2}$ . When the PFF proportional gain increases to 0.2 p.u., the SO-mode poles  $\lambda_{3-4}$  move to the RHP, which thus induces the SO. The pole trajectories demonstrate a tradeoff of the stability impact of the DVC+PFF control method. It is expected to increase the PFF proportional gain for the LFO mitigation, whereas increasing it may lead to the SO issue.

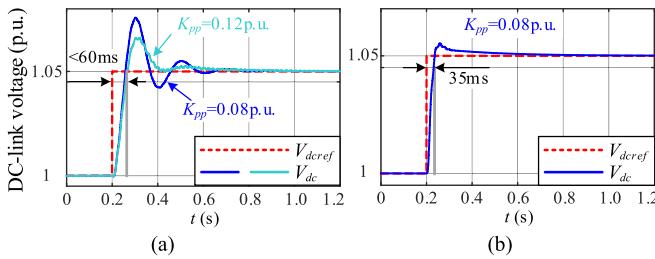
Fig. 10 shows simulation waveforms with the conventional PFF+DVC method. In the rectifier mode with SCR = 1.2 as shown in Fig. 10(a), the GFM converter keeps stable when  $K_{pp}$  equals to 0.1 and 0.12 p.u. However, the GFM converter, with the same control parameters as Fig. 10(a), is subjected to the SO issue when operating in the inverter mode with SCR = 5, as shown in Fig. 10(b). The simulation results show that with the



**Fig. 9.** Closed-loop pole trajectories with PFF+DVC method. (a) Rectifier mode with SCR = 1.2 (b) Inverter mode with SCR = 5.



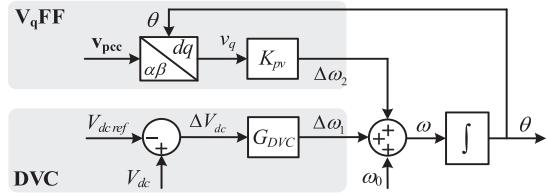
**Fig. 10.** Simulation waveforms with conventional PFF+DVC method. (a) Rectifier mode, SCR = 1.2. (b) Inverter mode, SCR = 5.



**Fig. 11.** Step response of the dc-link voltage with PFF+DVC method. (a) Rectifier mode, SCR = 1.2. (b) Inverter mode, SCR = 5.

conventional PFF+DVC method, the stability robustness against different dc and ac grid conditions is difficult to be guaranteed, owing to the trade-off between the LFO and SO issues.

Fig. 11 shows the step response of the dc-link voltage with PFF+DVC method. The tests are performed in the rectifier mode



**Fig. 12.** Proposed  $V_q$ FF- and DVC-based synchronization ( $V_q$ FF+DVC) method.

with weak grids and the inverter mode with stiff grids. The dc-link voltage well tracks its reference, which indicates that the control accuracy is guaranteed. Besides, the rise time of the dc-link voltage is highlighted to evaluate the dynamic response speed. While it varies with grid conditions, it is within 60 ms in those operation scenarios.

#### IV. PROPOSED SYNCHRONIZATION CONTROL METHOD

##### A. Basic Principle

From Fig. 8(a), it is known that feeding the phase angle dynamics back to the frequency control can essentially dampen the LFO. According to this principle, the  $q$ -axis component of PCC voltage, which can also reflect the phase angle dynamics, is utilized for the provision of damping.

Fig. 12 shows the proposed  $V_q$ FF- and DVC-based synchronization method. The  $V_q$ FF loop is connected in parallel with DVC for the grid-synchronization purpose. A PI controller described in (20) is adopted in DVC. The  $V_q$ FF control adopts a P controller that is represented by  $K_{pv}$ . Moreover, it is known that the PLL commonly utilizes the  $q$ -axis voltage at the PCC for grid synchronization. Yet the  $V_q$ FF control in the proposed method is different from the PLL. It is because the phase angle for the park transformation is generated by paralleled DVC and  $V_q$ FF loops instead of the  $V_q$ FF control loop only.

##### B. Small-Signal Stability Enhancement

Fig. 13(a) shows the SISO model with the proposed  $V_q$ FF+DVC method, which is derived by integrating the  $V_q$ FF dynamics into the SISO model of single-loop DVSC-VSC shown in Fig. 5. The  $q$ -axis voltage dynamics can be derived through the park transformation and is given by

$$u_{dq0}^c + \hat{u}_{dq}^c = e^{-j(\theta_0 + \hat{\theta})} \cdot (u_{dq0}^s + \hat{u}_{dq}^s) \quad (25)$$

$$\hat{u}_q^c = \underbrace{[-\sin \theta_0 \quad \cos \theta_0]}_{G_{Vq}^u} \cdot \hat{u}_{dq}^s - \underbrace{(\cos \theta_0 u_{d0}^s + \sin \theta_0 u_{q0}^s)}_{G_{Vq}^\theta} \cdot \hat{\theta}. \quad (26)$$

Recalling (7) and (17), The  $V_q$ FF dynamics are given by

$$\begin{cases} \hat{u}_q^c = \underbrace{G_{Vq}^\theta - G_{Vq}^u \cdot Z_g \cdot G_{\theta-i} \cdot \hat{\theta}}_{G_{Vq}} \\ \Delta \hat{\omega}_2 = K_{pv} \cdot G_{Vq} \cdot \hat{\theta} \end{cases}. \quad (27)$$

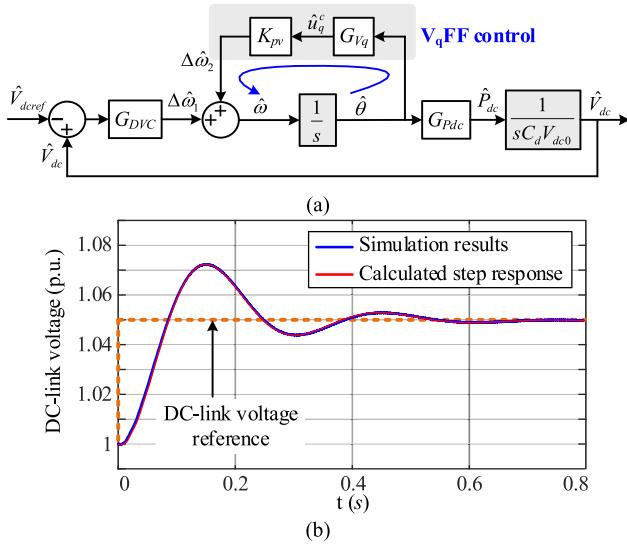


Fig. 13. SISO small-signal model of the proposed  $V_q$ FF+DVC method and its validation. (a) SISO model. (b) Step response of the dc-link voltage.

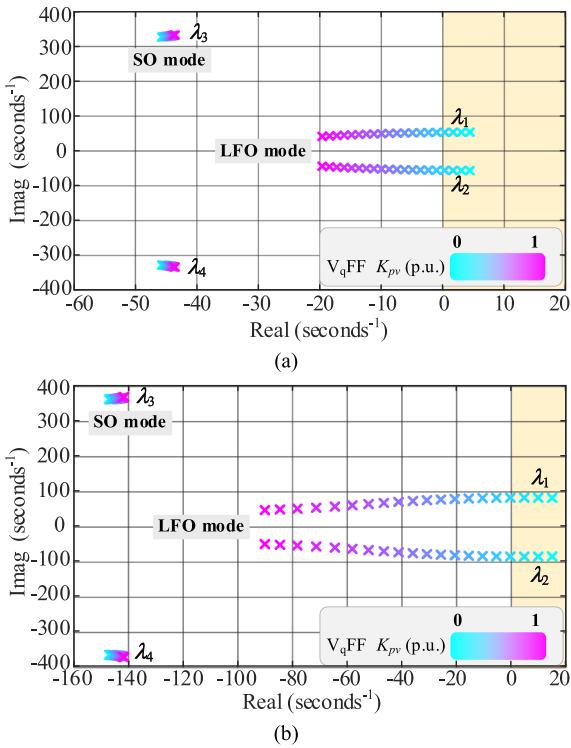


Fig. 14. Closed-loop pole trajectories with proposed  $V_q$ FF+DVC method. (a) Rectifier mode with  $SCR=1.2$  (b) Inverter mode with  $SCR=5$ .

The open-loop and closed-loop transfer functions of reference-to-output of the dc-link voltage are derived as

$$T_{VqFF} = \frac{-G_{Pdc} \cdot G_{DVC}}{s C_d V_{dc0} (s - K_{pv} G_{Vq})}, \quad T_{closed} = \frac{T_{VqFF}}{1 + T_{VqFF}}. \quad (28)$$

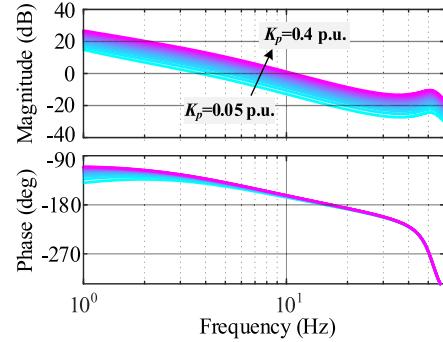


Fig. 15. Bode plots of open-loop transfer function with different DVC proportional gains, rectifier mode with  $SCR = 1.2$ .

The step response of the dc-link voltage can be derived through the closed-loop transfer function and is shown in Fig. 13(b). It matches well with the time-domain simulation, which thus validates the accuracy of the derived SISO model.

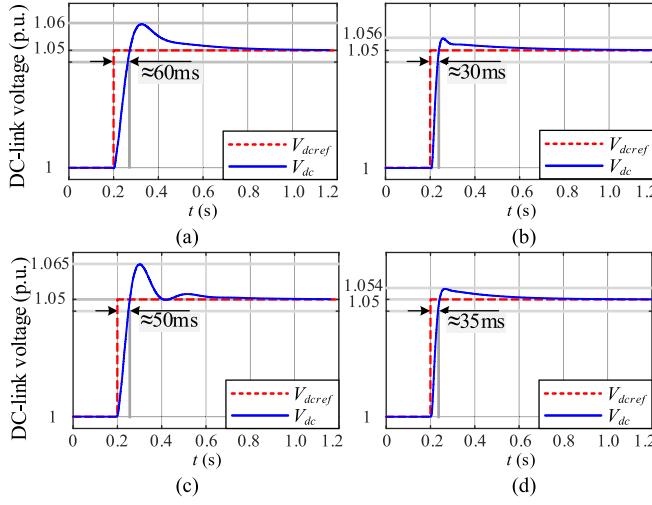
From the SISO model shown in Fig. 13(a), it is observed that the  $V_q$ FF control loop essentially forms a negative feedback loop from the phase angle to frequency ( $G_{Vq}$  is with negative gain), and hence, it provides damping to mitigate the LFO issue. Further, the transfer function from the  $q$ -axis voltage to the phase angle,  $G_{Vq}$ , does not include synchronous-frequency resonant poles. Thus, the  $V_q$ FF control does not lead to additional SO issue.

Fig. 14 shows closed-loop pole trajectories with the proposed  $V_q$ FF+DVC method. The GFM converter operates in the rectifier mode with weak grids and the inverter mode with stiff grids, where the CPL/CPS is connected at the dc link. It is shown that the LFO-mode RHP poles  $\lambda_1$ – $\lambda_2$  move from the RHP to the LHP with the increase of  $V_q$ FF proportional gain, indicating that the LFO issue is damped by the  $V_q$ FF control. Besides, the SO-mode poles  $\lambda_3$ – $\lambda_4$  change a little and are always away from the imaginary axis when the  $V_q$ FF proportional coefficient varies from 0 to 1 p.u. It proves that the  $V_q$ FF control can avoid the adverse stability impact on the SO mode. Moreover, the proposed method and analysis are also applicable to rectifier mode with stiff grids and inverter mode with weak grids due to the same principle.

### C. Parameter Tuning

Considering the small-signal synchronization stability, the transient response of dc-link voltage, and different operating points, the control parameters of the  $V_q$ FF+DVC method are designed with the following procedure.

- 1) Designing DVC parameters based on the dynamic response speed of the dc-link voltage. Given the ac grid condition ( $SCR = 1.2$ ) and the operation mode (rectifier mode with rated power), the Bode plots of the open-loop transfer function (28) are shown in Fig. 15. Given the cut-off frequency  $\omega_{dc}$  equal to 8 Hz as an example, the DVC proportional gain (represented by  $K_p$ ) can be selected as 0.2 p.u. Moreover, making the DVC dynamic dominated by the proportional gain, the integral gain (represented by



**Fig. 16.** Step response of the dc-link voltage with the proposed  $V_q$ FF+DVC method,  $K_{pv}=0.5$  p.u. (a) Rectifier mode, SCR = 1.2. (b) Rectifier mode, SCR = 5. (c) Inverter mode with SCR = 1.2. (d) Inverter mode with SCR = 5.

$K_i$ ) is calculated with  $K_i = K_p \cdot \omega_{dc}/10$ , and selected as 1 p.u.

- 2) Designing the  $V_q$ FF parameter by following the stability analysis in Fig. 14. The  $V_q$ FF proportional gain can be determined by making the LFO-mode conjugate poles located in LHP and well-dampening the dc-link voltage overshoot during the dynamics process [28].
- 3) Evaluating the dynamic performance with the designed parameters under both rectifier and inverter modes, as well as with different ac grid strengths.

Fig. 16 shows the step response of the dc-link voltage with the designed  $V_q$ FF+DVC method. The tests are performed under rectifier and inverter modes with dc-link CPL/CPS, and with different grid SCRs. The dc-link voltage tracks its reference with zero steady-state error. Besides, the rise time of the dc-link voltage is within 60ms in those operation scenarios, which is comparable to the rise time when using conventional PFF+DVC method in Fig. 11. Moreover, the overshoot of the dc-link voltage during the transients is damped [28].

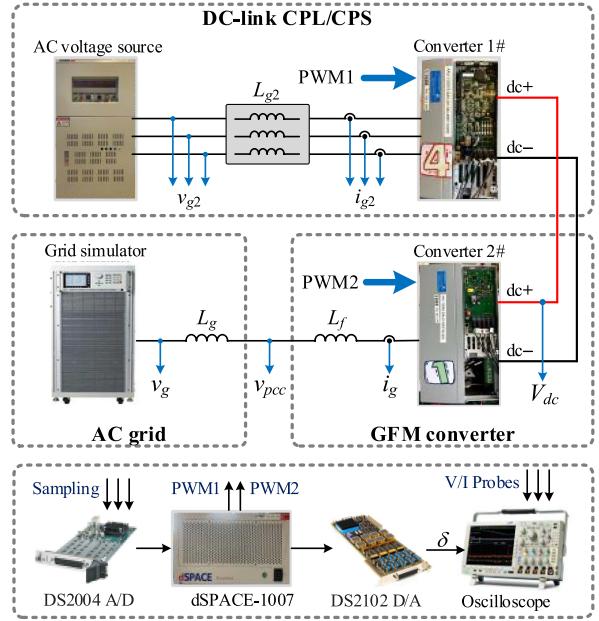
## V. EXPERIMENTAL VERIFICATION

The downscaled experimental tests are carried out with a back-to-back system shown in Fig. 17. The dc-link CPL/CPS is emulated by converter 1#, which is connected to a three-phase ac voltage source through the inductance filter  $L_{g2}$ . A PLL is utilized to synchronize the converter 1# with the ac voltage source. A  $dq$ -frame vector current control is adopted. The current reference is given by

$$i_{dref2} = P_L/v_{gd2}, \quad i_{qref2} = 0. \quad (29)$$

where  $v_{gd2}$  denotes the  $d$ -axis component of  $v_{g2}$ .

Converter 2# regulates the dc-link voltage through the GFM control discussed in this article. Series inductors are served as the  $L$ -filter and the grid impedance. The grid simulator



**Fig. 17.** Downscaled experimental setup.

**TABLE II**  
PARAMETERS OF DOWNSCALED EXPERIMENT

Symbol	Description	Value (p.u.)
$P_0$	Rated power	1kW (1 p.u.)
$V_g$	Grid voltage RMS	150V/50Hz (1 p.u.)
$V_{dcref}$	DC-link voltage reference	400V
$L_f$	Filter inductance	33mH (0.46 p.u.)
$C_d$	DC-link capacitor	1.45mF
$E_{ref}$	Nominal EMF reference	150V (1 p.u.)
$Q_0$	Reactive power reference	0
$K_p$	DVC proportional gain	0.2 p.u.
$K_i$	DVC integral gain	1 p.u.
$k_q$	RPC droop gain	0.1 p.u.
$L_v / R_v$	Virtual admittance	0.15p.u./0.1p.u.
$k_{pi} / k_{ri}$	Current controller	2.1 p.u./0.5 p.u.

(Chroma 61850) generates the grid voltage. The dSPACE DS-1007 platform is utilized to implement the control algorithms of converter 1# and 2#. The DS2004 A/D board is used to transfer circuit variables, including the grid voltage, the PCC voltage and current, and the dc-link voltage. The DS2102 D/A board is adopted to feed the power angle to the oscilloscope. The power angle is defined as  $\delta = \theta_g - \theta$ , where  $\theta_g$  is derived through a fast PLL.  $\theta$  is the output of the synchronization loop. The experimental parameters are listed in Table II. The per-unit values of experimental parameters are the same as those of the theoretical analysis.

Fig. 18 shows experimental results with the conventional PFF+DVC method, where the system stability with and without the PFF loop is evaluated. When zeroing the PFF proportional gain, the control scheme changes to the single-loop DVSC. Low-frequency divergent oscillations arise in dc-link voltage, grid current, and power angle, further blocking the converter 2#.

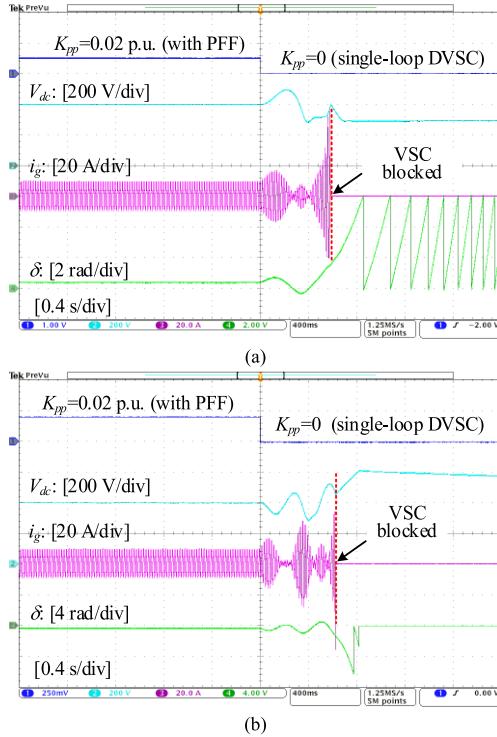


Fig. 18. Experimental waveforms with conventional PFF+DVC method, SCR = 1.2. (a) Rectifier mode. (b) Inverter mode.

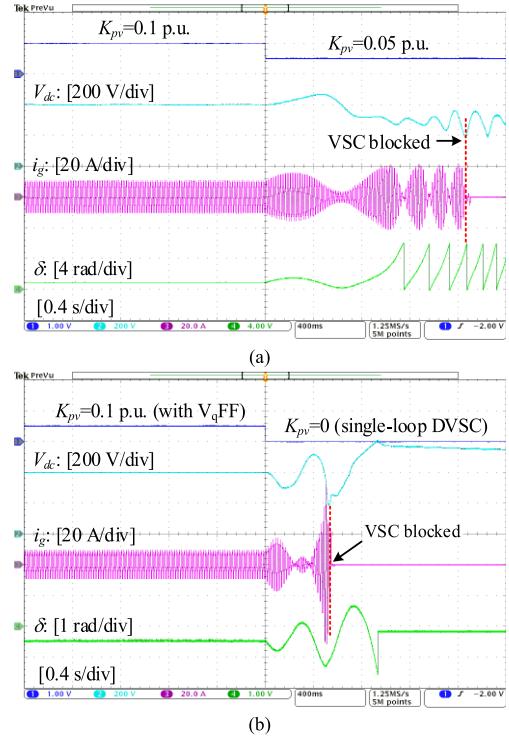


Fig. 20. Experimental waveforms with proposed  $V_q$ FF+DVC method. (a) Rectifier mode with SCR = 1.2. (b) Inverter mode with SCR = 5.

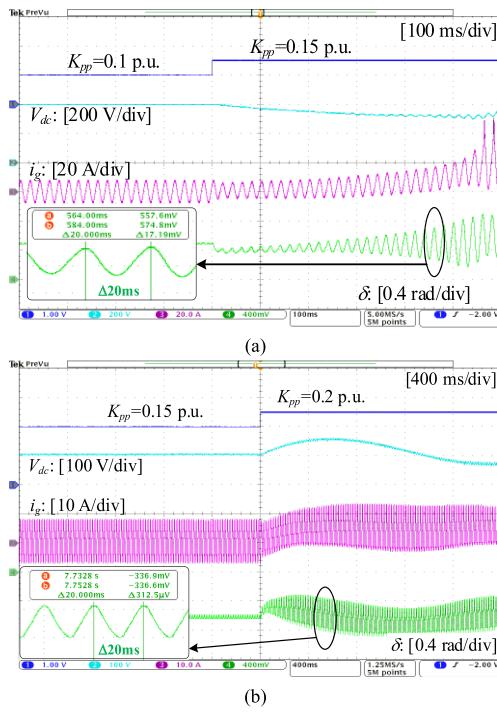


Fig. 19. Experimental waveforms with conventional PFF+DVC method. (a) Rectifier mode with SCR = 5. (b) Inverter mode with SCR = 1.2.

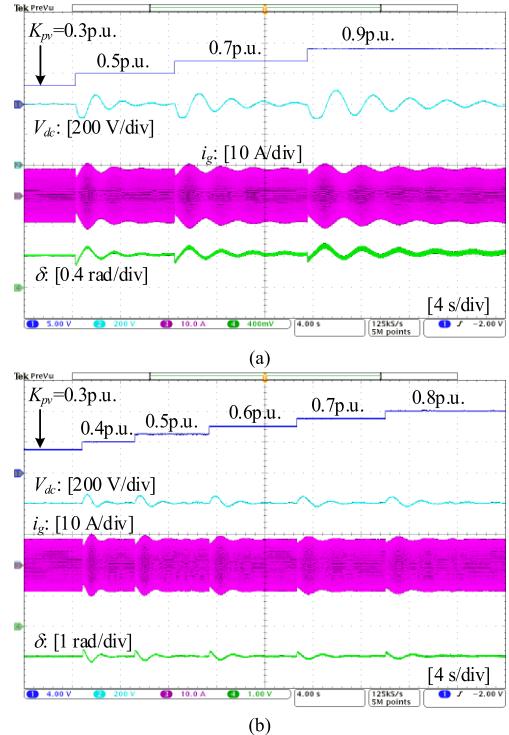
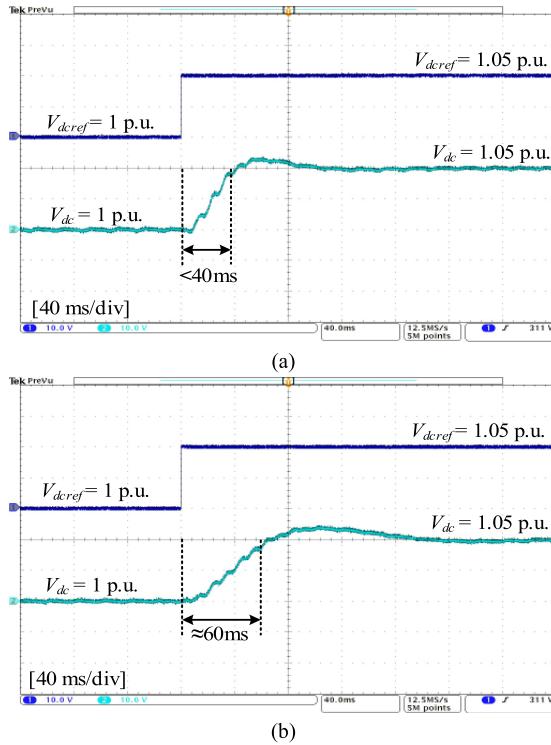


Fig. 21. Experimental waveforms with proposed  $V_q$ FF+DVC method. (a) Rectifier mode with SCR = 5. (b) Inverter mode with SCR = 1.2.



**Fig. 22.** Experimental step response of the dc-link voltage with proposed  $V_q$ FF+DVC method. (a) Rectifier mode with  $SCR = 5$ . (b) Inverter mode with  $SCR = 1.2$ .

The results not only validate the LFO problem with single-loop DVSC, but also validate the active damping effect of the PFF loop to address the LFO. The experimental results corroborate the theoretical analysis in Figs. 6 and 9.

Fig. 19 shows experimental results with conventional parallelized PFF+DVC method, where the adverse effect of the PFF loop is demonstrated. With the increase of PFF proportional gain, the SO of dc-link voltage and power angle is raised in both rectifier and inverter operation modes. A dc component is superimposed on the ac current waveform. Moreover, when  $K_{pp}$  equals to 0.15 p.u., the GFM converter is stable in the inverter mode with  $SCR = 1.2$  while unstable in the rectifier mode with  $SCR = 5$ . It indicates that the stability robustness of the GFM converter against different dc and ac grid conditions is challenged. The experimental results validate the adverse stability effect of conventional PFF+DVC method, which agrees with the theoretical analysis in Fig. 9.

The experimental results of Figs. 18 and 19 further prove that both decreasing and increasing PFF proportional gain would lead to instability issues. The trade-off for the PFF parameter design is thus raised.

Fig. 20 shows experimental results with the proposed  $V_q$ FF+DVC method, where the system stability with and without the  $V_q$ FF loop is evaluated. Both rectifier and inverter operation modes, as well as different ac grid strengths, are considered. To avoid the repetitive presentation, waveforms of two cases, i.e., rectifier mode with weak ac grid and inverter mode with stiff ac grid, are demonstrated. It is shown that the

VSC operates stably with the proposed  $V_q$ FF control, while the LFO issue arises when disabling the  $V_q$ FF control loop. The divergent oscillations of dc-link voltage, ac current, and power angle are manifested, which block the VSC. The experimental results validate the damping effect of the  $V_q$ FF control on the LFO, which is aligned with the theoretical analysis in Fig. 14.

Fig. 21 shows experimental results with the  $V_q$ FF+DVC method, where different  $V_q$ FF proportional gains are tested. The VSC operates stably when the  $V_q$ FF proportional gain is increased from 0.3 to 0.9 p.u. There are no instability issues in both rectifier and inverter modes with different SCRs of ac grid. This result further corroborates the theoretical analysis in Fig. 14.

Fig. 22 shows the experimental step response of the dc-link voltage with the  $V_q$ FF+DVC method. The dc-link voltage reference step changed from 1 to 1.05 p.u. in both rectifier and inverter operation modes. It is shown that the rise time of dc-link voltage is within 60 ms, and the oscillations during dynamic response are also well damped. The experimental results confirm the control-parameter design procedure, and the simulated step response in Fig. 16.

## VI. CONCLUSION

This article has proposed a paralleled DVC- and  $V_q$ FF-based synchronization method for the small-signal synchronization stability enhancement of GFM converters. Theoretical analysis and experimental results have validated that the proposed synchronization control can dampen the LFO problem of VSCs that is induced by dc-link constant-power dynamics. Moreover, the SO problem inherent with conventional PFF+DVC method has also been overcome. Parameter design guidelines are developed, which result in GFM converters operating stably in both inverter and rectifier modes, with CPS/CPL at the dc link, as well as under different ac grid strengths.

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**Liang Zhao** (Student Member, IEEE) received the B.S. and M.S. degrees in power electrical engineering from Harbin Institute of Technology, Harbin, China, in 2018 and 2020, respectively. He is currently working toward the Ph.D. degree in power electronic engineering with Aalborg University, Aalborg, Denmark.

His research interests include the modeling and stability analysis of power electronics systems.



**Zheming Jin** (Member, IEEE) was born in Jilin, China. He received the B.S. degree in electrical engineering and the M.S. degree in power electronics and AC drives from Beijing Jiaotong University, Beijing, China, in 2013 and 2015, respectively, and the Ph.D. degree in power electronic systems from the Department of Energy Technology, Aalborg University, Aalborg, Denmark, in 2018.

In 2019, he joined the Department of Energy Technology, Aalborg University, as a Postdoctoral Researcher, and was subsequently appointed as an Assistant Professor. In 2021, he joined Beijing Jiaotong University, where he is currently an Associate Professor. His research interests include control of power electronic converters, stability of power electronic based power systems, energy storage, dc microgrids, and their applications in transportation electrification.



**Xiongfei Wang** (Fellow, IEEE) received the B.S. degree from Yanshan University, Qinhuangdao, China, in 2006, the M.S. degree from Harbin Institute of Technology, Harbin, China, in 2008, both in electrical engineering, and the Ph.D. degree in energy technology from Aalborg University, Aalborg, Denmark, in 2013.

From 2009 to 2022, he was with Aalborg University where he became an Assistant Professor in 2014, an Associate Professor in 2016, a Professor and Leader of Electronic Power Grid (eGRID) Research Group in 2018. From 2022, he has been a Professor with KTH Royal Institute of Technology, Stockholm, Sweden. His current research interests include modeling and control of power electronic converters and systems, stability and power quality of power-electronics-dominated power systems, and high-power converters.

Dr. Wang serves as Co-Editor-in-Chief for the *IEEE TRANSACTIONS ON POWER ELECTRONICS* and as Associate Editor for the *IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS (JESTPE)*. He was a recipient of 10 IEEE Prize Paper Awards, the 2016 AAU Talent for Future Research Leaders, the 2018 Richard M. Bass Outstanding Young Power Electronics Engineer Award, the 2019 IEEE PELS Sustainable Energy Systems Technical Achievement Award, the 2020 JESTPE Star Associate Editor Award, and the 2022 Isao Takahashi Power Electronics Award.