Principles and Efficient Implementation of Charge Replacement in Hybrid Electrical Energy Storage Systems

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***Abstract*—Hybrid electrical energy storage systems (HEES) are comprised of multiple banks of inhomogeneous EES elements with difference characteristics. They have been proposed to achieve desired performance metrics of an ideal energy storage device, i.e., high energy capacity, high output power level, low self-discharge, low cost, and long service life. Implementation of appropriate charge management policies enables efficient storage and retrieval of the electrical energy, attaining performance metrics that are close to the respective best values across the constituent EES elements in the HEES system. This paper addresses a global charge replacement problem in HEES systems, namely, how to dynamically select a subset of the EES banks and discharge them to meet the load power demand in a prespecified amount of time. Precisely, the global charge replacement optimization problem is formulated as a mixed-integer nonlinear programming problem, and a hierarchical algorithm is presented to efficiently solve this problem. At the top level the proposed algorithm considers the complete discharging process and allocates the load demand among all available EES banks, whereas at the bottom level it employs convex optimization methods to solve for discharging currents and the voltage level of a shared charger transfer interconnect. A prototype HEES system has been built to demonstrate the energy benefits brought by HEES systems and the efficacy of the proposed charge replacement algorithm.**

***Index Terms*—Batteries, charge management, charge replacement, energy efficiency, energy storage system (ESS), hybrid electrical energy storage system (HEES), prototype.**

I. Introduction

ELECTRICAL energy generation and consumption rates are typically not matched with each other. Electrical energy storage (EES) systems store the excessive energy produced at certain times of the day and provide the energy during the peak load times as needed. EES systems [2], [3] increase the availability of the electrical energy, mitigate the supply-demand mismatches, and reduce the power generation capacity required to meet the peak power demand. Conventional EES systems only consist of a single type of EES element. Unfortunately, no available EES element can fulfill all the desired performance metrics of an ideal storage means (e.g., high power/energy density, low cost/weight per unit capacity, high round-trip efficiency, and long cycle life.) An obvious shortcoming of a homogeneous EES system is that the key figures of merit (normalized with respect to capacity) of the system cannot be any better than those of its constituent EES element.

Hybrid EES (HEES) systems [4], [5] are the EES systems that comprise of two or more inhomogeneous EES elements, where each type has its unique strengths and weaknesses. Yet, the HEES system can be designed so that it offers characteristics of an ideal storage, in much the same way that a hybrid memory hierarchy system in today's computer systems provides low access delay, high density, and low cost all at the same time. Based on the characteristics of the HEES system and power demand profiles of load devices (or power sources), charge management policies aiming to achieve near-optimal HEES system performance must be developed. Appropriate charge management policies, including charge migration, charge allocation, charge replacement, and EES bank reconfiguration, can exploit strengths of each type of EES element and achieve performance metrics that are superior to those of any of its individual EES elements [1], [6]–[14].

The charge replacement problem[1] in the HEES system is to adaptively select EES banks and determine discharging currents, from zero to a maximum limit, and voltage level settings on a *charge transfer interconnect* (CTI) so that the given load demand is met and the *charge replacement efficiency* is maximized. Note that the charge replacement efficiency denotes the ratio between the energy requested by load devices and the energy retrieved from the HEES system. In this paper, we provide a mathematical formulation for the *global charge replacement* (GCR) problem and propose an efficient algorithm to solve it near-optimally. Precisely, the GCR problem is formulated as an optimization problem where the objective function is the GCR

[1]Charge replacement implies discharge from EES elements to meet the load demands. This term is borrowed from the terminology used in the computer memory management literature.

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efficiency and constraints are derived from laws of energy and charge conservations. We account for the energy loss due to the internal resistance of batteries, the power conversion energy loss, the rate capacity effect of batteries, and the self-discharge of supercapacitors. We solve the GCR problem using convex optimization methods while imposing an output power bound on battery banks in order to avoid discharging supercapacitor banks too quickly (which could in turn degrade the charge replacement efficiency).

We build a prototype HEES system with the purpose of exploring energy benefits brought by the HEES system and validating the efficacy of the proposed GCR policy. The prototype consists of three EES banks: one supercapacitor bank, one Li-ion battery bank, and one lead-acid battery bank. We connect them to the CTI, which also connects input sources and output loads through appropriate power converters. We first perform a characterization process to obtain characteristics of EES banks and power converters, and then derive the GCR policy based on the characterized information and load demand profiles. We implement the GCR policy to automatically control charging currents and voltage level settings for the CTI. We apply various types of representative load profiles with different durations to test the functionality of implementation and the performance of the proposed charge replacement algorithm. Experiments based on the realistic prototype system show improvements up to 11.1% and 24.7% in terms of the GCR efficiency against other HEES baselines and homogeneous EES baseline, respectively.

II. Notations

Table I lists symbols used in this paper.

TABLE I
Symbols Used in This Paper

S	full set of all EES banks in HEES system
$T_s,\ T_e$	starting and ending time of the discharging process
$S_{on}(t)$	selection set among all EES banks in HEES system
$SoC_k(t)$	state of charge of the kth EES array
$V^{OC}_{array,k}(t)$	open circuit voltage (OCV) of the kth EES array, an essential value obtained using theoretical modeling
$V^{CC}_{array,k}(t)$	closed circuit voltage (CCV) of the kth EES array, measured at the terminal of the EES array
$P_{CTI}(t)$	power delivered in the CTI
$V_{CTI}(t)$	voltage level on the CTI
$P_{load,j}(t)$	power demand of the jth load device
$V_{load,j}(t)$	working voltage of the jth load device
$P_{d,j}(t)$	power loss in DC-DC converter for the jth load device
$P_{c,k}(t)$	power loss in the charger of the kth EES bank
$P_{sd,k}(t)$	power loss due to the self-discharge in the kth EES bank
$P_{array,k}(t)$	output power of the kth EES array
$P_{drawn,k}(t)$	rate of energy decreases in the kth EES array
$I_{bank,k}(t)$	bank discharging current of the kth bank, measured at the downstream of the charger
$I_{array,k}(t)$	array discharging current of the kth array, measured at the upstream of the charger
$I_{eq,k}(t)$	equivalent charging current of the kth EES array, an essential value at which the battery loses charge
$I_{sd,k}(t)$	self-discharge current in the kth EES array
C_b^{full}	nominal capacity of the battery ($A \cdot h$)
C_b	remaining capacity of a battery
γ	Peukert constant of the battery
C_{cap}	capacitance of a supercapacitor bank
τ	self-discharge time constant of a supercapacitor bank
x_c	binary indicator of the charger status (on/off)
η_{GCR}	global charge replacement efficiency
η_{ICR}	instantaneous charge replacement efficiency

III. HEES Systems

A. Related Work

The concept of hybrid power sources (energy storage systems) was first introduced in [15]. Subsequent researchers have invested considerable efforts to find the optimal architecture of a hybrid system. Direct-parallel connections of the battery and supercapacitor [16], [17] are simple but hve a major weakness, that is, the shared terminal voltage of both sources must be kept same. This weakness limits the utilization of supercapacitor capacity and disables the active current distribution control. Cascade dc–dc converters between the battery and supercapacitor [18] can isolate power sources and allow higher supercapacitor utilization. However, this design targeted a specific scenario in which the supercapacitor is used as a buffer of the battery all the time. Connecting both supercapacitor and battery to a dc-bus through distributed converters provides higher design flexibility [19], [20]. However, the previous dc-bus architectures do not change the dc-bus voltage, which prevents them from achieving a higher system efficiency. We generalize the HEES system architecture presented in [21]–[23], which allow individual control of each EES bank and voltage level settings on the DC-bus, to include multiple EES bank, dc inputs and outputs, and ac inputs and outputs.

Proper HEES control policies are crucial to achieve better performance, including higher charging and discharging efficiency, less aging effect, and stronger fault-tolerant capability. A circuit model helps derive a desirable capacity ratio between the battery and supercapacitor to reduce the energy loss during the discharging process [24]. The configuration of supercapacitor and the load demand profiles were considered in optimizing the HEES capacity in [25]. However, none of these previous work is based on the general HEES architectures. The authors in [6], [7], [1], and [9] present the *charge migration*, *charge allocation*, and charge replacement for the HEES system and provide near-optimal solutions to maximize corresponding performance. A charge management policy to extend the battery lifetime using the HEES system is presented in [10]. The authors in [8] present a novel structure to adaptively reconfigure EES elements within an EES bank to achieve better performance. More general HEES architectures, including mesh-network bank connections and multiple CTIs, have been proposed in [11] and [12]. Researchers in [13] consider the capital cost of constructing a HEES system and maximize the return on investment, utilizing price differences during peak hours and off-peak hours. Authors of [14] combine HEES systems with energy-harvesting systems and reduce the overhead in dc–dc converters during the charging process. In this study, we present a near-optimal solution for the GCR problem, design the GCR policy, and implement it in the HEES prototype to explore the energy benefits brought by the HEES systems and validate the efficacy of the designed policy.

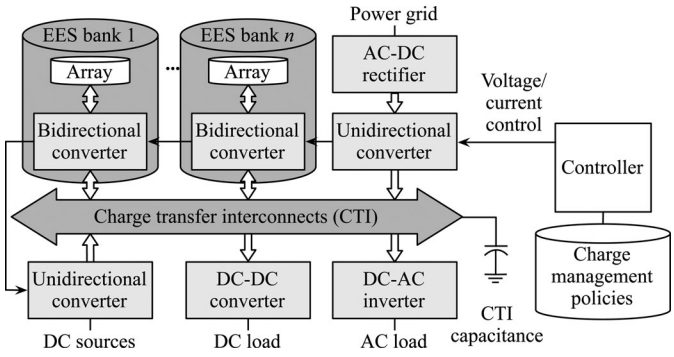

Fig. 1. Architecutre of HEES systems.

B. HEES System Architecture

A conceptual block diagram of the HEES system architecture is provided in Fig. 1. The system is comprised of multiple inhomogeneous *EES banks* connecting to each other through the CTI. Each EES bank contains an*EES elements array* and a *bidirectional charger*, which generates a desirable charging or discharging current of the corresponding EES array. The EES array within an EES bank consists of homogeneous EES elements. Since an individual EES element has low output voltage and small energy capacity, it is necessary to build an EES array with many series- and parallel-connected EES elements, in order to provide the desired output level and energy capacity. We consider a common setup such that each group of series-connected elements has equipped a cell balancer and some monitoring circuity (e.g., Coulomb counter). The cell balancer balances SoCs between those series-connected elements. Lots of work have dedicated to improving cell-balancing techniques [26], [27]. Monitoring circuity monitor and report EES element status (e.g., voltage, temperature, SoC, state-of-health (SoH), and so on). Considerable research efforts have been invested to develop an accurate and low computational-cost online SoC and SoH estimation methods [28]–[31]. Our study focuses on bank-level control in an HEES system and thus we assume that monitoring circuity in the EES array are well designed and provide reliable estimations of SoC and SoH .

All load devices are connected to the HEES system through dc–dc converters (for dc load devices) or dc–ac inverters (for AC load devices) because their terminal voltages are not compatible with the CTI voltage. Similarly, dc and grid power sources are also connected to the HEES system using unidirectional converters to maintain the voltage-level compatibility. We address the stability issue of the CTI voltage by properly designing charge management policies, which balances currents flowing toward and outward the CTI. However, in practice, the CTI voltage may still become unstable due to the discrepancy between incoming and outgoing currents during transient periods when the load or source current changes. In this case, either a dc source or the grid power source can be used to maintain the CTI voltage at the desired level. In the HEES prototype, we use an ac–dc rectifier to convert the grid power to dc power and a dc–dc converter to define the CTI voltage.

The charge management policies, shown by solid arrows in Fig. 1, control the EES bank configuration, EES bank selection, the CTI voltage, and charging or discharging current of each EES bank at each time instance. Charge management policies typically include the charge replacement [1], charge allocation [7], charge migration [6], [9], [12], and EES bank reconfiguration [8] policies. They are carefully designed to achieve better HEES system performance with the consideration of characteristics of EES banks and profiles of the power sources and load devices. For example, batteries typically have high energy capacity, low self-discharge, but rather low output power capacity, while supercapacitors are the opposite. Therefore, the charge allocation and replacement policies use the supercapacitor banks to shave peaks in power supply or load demand, leaving the rest of the power supply or demand to battery banks. According to the specific usage condition, the controller selects and applies appropriate policies among different charge management policies.

C. HEES Prototype

We build an HEES prototype based on the HEES architecture, as shown in Fig. 2. The hardware part of the HEES prototype is comprised of three types of module: the EES bank module, the CTI module, and the converter module. For the software part, the user interface (UI) is designed using the LabVIEW, while control policies are implemented using the Mathscript [32] module of the LabVIEW.

1) EES Bank Module: The EES bank modules store the electrical energy. We install three representative EES bank modules: one supercapacitor bank, one Li-ion battery bank, and one lead-acid battery bank. We select these three types of EES elements as they have very distinct characteristics [4]. A supercapacitor has superior power capacity, but high leakage rate, very low energy capacity and it is very expensive. Li-ion battery is less expensive, but has good power capacity, low leakage rate and ultra-high energy capacity. A lead-acid battery is even cheaper than the Li-ion battery, while its other characteristics are inferior to those of the Li-ion battery.

2) CTI Module: The CTI module is the path for charge transfer between power sources, load devices, and EES banks. The voltage level setting in CTI affects the power conversion efficiency of chargers and power converters. Thus, it is very important to maintain the CTI voltage at a stable and appropriate level. We have used an ac–dc rectifier and unidirectional power converter in our prototype system to keep the CTI voltage stable by using the ac power source (i.e., the Grid). In addition, we also connect a large capacitance of 132,000 μF to the CTI to minimize CTI voltage fluctuations even in the case of a rapid increase in the load demand. We select this CTI capacitance value as it properly maintains a stable CTI voltage when the load demand increases by 240 W. The power used to maintain a stable CTI voltage is negligible compared to HEES system power ratings.

3) Converter Module: This module contains an ac–dc rectifier for the grid power input, which are used to convert ac power into dc power. The dc power is in turn used to charge EES banks and maintain stable CTI voltage level settings. It also contains a

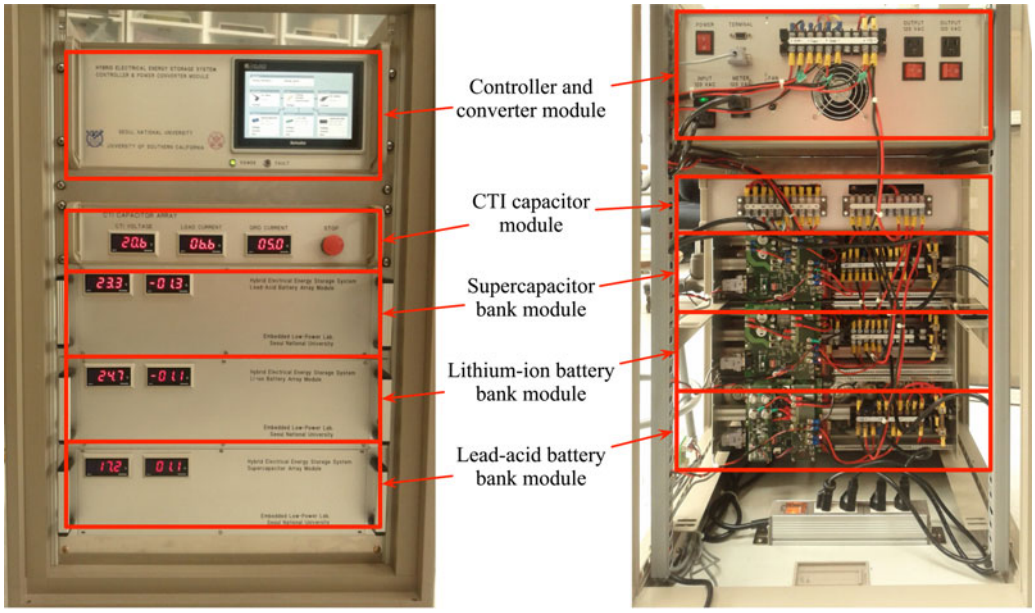

Fig. 2. Prototype of the proposed HEES system. (a) Front. (b) Back.

dc–ac inverter to support ac loads. DC–DC conversion can also be included into the system to provide capability in handling dc inputs and outputs.

4) UI and Control Unit: The UI is designed using the LabVIEW. The LabVIEW UI monitors the runtime status of the HEES prototype, including the CTI voltage, voltage and input/output current for each EES bank, and calculates the instantaneous charging or discharging efficiency using these information. The LabVIEW is also responsible for the top-level power management between the HEES prototype and the external power sources or load devices. In the current version of the prototype, the power management policies are implemented using the LabVIEW MathScript on a PC, which is connected to the HEES prototype through the control area network bus.

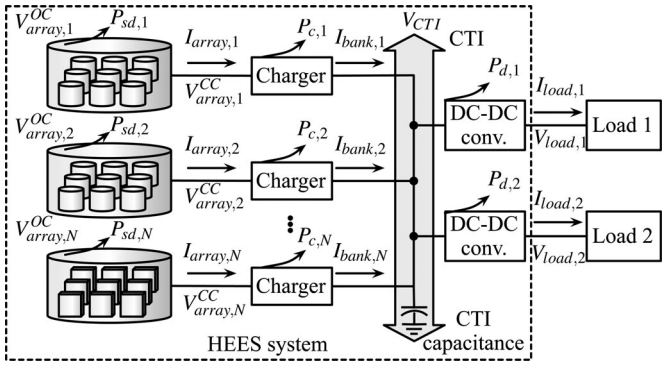

Fig. 3. Block diagram of HEES systems for a charge replacement problem.

IV. Problem Formulation

A. Charge Replacement Problem Description

Charge replacement policy selects EES banks to be discharged and determines the discharging current of each selected EES bank to support a given load demand. Effective charge replacement algorithms need to account for distinct characteristics of EES element arrays, conversion efficiencies of power converters, and load demand profiles. The best-suited EES banks and corresponding discharging currents may vary over time according to load demands and SoCs of storage arrays. The proposed charge replacement algorithm dynamically sets the discharging current of each EES bank to satisfy load demands, as well as maximize the GCR efficiency over the complete discharging process.

Fig. 3 shows the block diagram of HEES systems for the charge replacement problem. The HEES system is comprised of N inhomogeneous EES banks, denoted by a set $S = \{1, 2, \ldots, N\}$. The discharging process starts at time $t = T_s$ and ends at time $t = T_e$. At any time instance, a subset of all EES banks $S_{\rm on}(t) \in S$ are selected to provide power to CTI through their chargers. Note that in this paper, we do not consider charging the HEES system so all EES banks shown in Fig. 3 are discharging. We use $V^{\rm OC}_{{\rm array},k}(t)$ and $V^{\rm CC}_{{\rm array},k}(t)$ to denote the *open-circuit terminal voltage* (OCV) and the *closed-circuit terminal voltage* (CCV) of EES element array in the kth bank, respectively. Because of the internal resistance of the EES array, these two voltages are generally not equal. The discharging rate of each EES array is controlled by the charger in that bank. Each charger sets its downstream current to the desired level determined by the charge replacement policy. We name the downstream current of the kth charger as *bank discharging current*, denoted by $I_{{\rm bank},k}(t)$, as it flows from the EES bank to the CTI. Meanwhile, the upstream current of the kth charger is named *array discharging current*, denoted by $I_{{\rm array},k}(t)$, because it goes from the EES array to the charger inside the EES bank. We account for the self-discharge power loss in the kth supercapacitor bank, $P_{{\rm sd},k}(t)$, conversion power loss in the kth

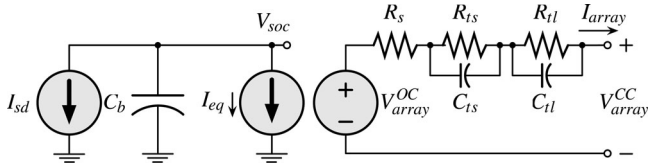

Fig. 4. Equivalent circuit model of Li-ion battery [33] for a discharging process.

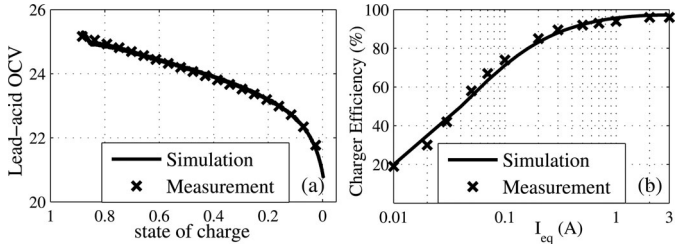

Fig. 5. (a) Comparison of the circuit model simulation results with the measured battery terminal voltage of the lead-acid battery bank in the HEES prototype and (b) the conversion efficiency of a LTM4607 power converter .

charger, $P_{c,k}(t)$, and power loss in a dc–dc converter for the jth load device $P_{d,j}(t)$.

Mapping our HEES prototype in Fig. 2 to the general diagram in Fig. 3, we have three EES banks. The meters on the top left of bank module panels measure CCVs of the corresponding EES element arrays, while the meters on the right is the downstream current of the bidirectional charger of that bank. We distinguish the current direction by using positive values for charging currents and negative values for discharging currents. The energy is drawn from the EES banks, delivered to the CTI, and subsequently retrieved by load devices. We convert ac power into dc power and use a dc–dc converter to set the CTI voltage, which is displayed on the left on the CTI module panel. The middle and right readings on the CTI module panel are the total current flowing out from the CTI and the *grid current* (downstream current of the dc–dc converter, which is on the downstream of the ac–dc rectifier in Fig. 1), respectively. During the discharging process, charge replacement policy sets the discharging current of each EES bank such that the grid current of the ac–dc rectifier is zero, which means that all power requested by load devices is provided by the EES banks. In practice, we may observe transient nonzero, but small, ac–dc rectifier current when CTI voltage setting changes or the load demand fluctuates.

B. Bank Model

1) Battery Bank: The proposed charge replacement framework and optimization technique are general and can be applied to any type of battery banks with accurate battery models. Among the large amount of previous work focusing on the battery models, we adopt a circuit-based battery model [33] because 1) it is more suitable for a mathematical programming formulation and 2) it provides sufficient accuracy for estimating the battery's remaining capacity and OCV. Although this model is proposed for Li-ion battery, the lead-acid battery can be modeled in a similar way with a different set of parameters as well.

Fig. 4 shows a discharging process of a Li-ion battery with the circuit-based model in [33]. In this model, SoC is defined by normalizing the current battery capacity to its nominal capacity: $\mathrm{SoC} = C_b/C_b^{\mathrm{full}}$. The battery OCV is modeled as a nonlinear function of SoC. Other parameters, such as internal resistance and capacitance of the battery, also depend on SoC. The relations are given by

$$V^{\mathrm{OC}} = b_{11}e^{b_{12}\cdot\mathrm{SoC}} + b_{13}(\mathrm{SoC})^3 + b_{14}(\mathrm{SoC})^2 + b_{15}\mathrm{SoC} + b_{16}$$
$$R_s = b_{21}e^{b_{22}\cdot\mathrm{SoC}} + b_{23}, \quad R_{ts} = b_{31}e^{b_{32}\cdot\mathrm{SoC}} + b_{33}$$
$$C_{ts} = b_{41}e^{b_{42}\cdot\mathrm{SoC}} + b_{43}, \quad R_{tl} = b_{51}e^{b_{52}\cdot\mathrm{SoC}} + b_{53}$$
$$C_{tl} = b_{61}e^{b_{62}\cdot\mathrm{SoC}} + b_{63}. \tag{1}$$

Fig. 5(a) validates the model accuracy by comparing the measured terminal voltage of the lead-acid battery bank in the HEES prototype with calculated values using this circuit model for the discharging process. As we mentioned previously, the OCV and CCV of a battery are generally not equal to each other. According to Fig. 4, the difference between two voltages is the voltage drop across the total internal resistances R_s, R_{ts}, and R_{tl} of the battery. For a discharging process, we have

$$V^{\mathrm{OC}}(t) = V^{\mathrm{CC}}(t) + V_{tl}(t) + V_{ts}(t) + I_{\mathrm{array}}(t)\cdot R_s. \tag{2}$$

Note that the battery ages as it cycles, i.e., the capacity degrades and internal resistance increases. The battery information can be updated to account for the aging effect based on the SoH estimated by the management system inside the EES array.

The rate capacity effect of batteries explains how the available charge in a battery relates to the magnitude of the discharging current [34]. Peukert's Law is an empirical relation which relates the discharging time and discharging current to the change in the battery SoC. Peukert's Law is described as $\Delta C_b = (I_{\mathrm{array}})^{\gamma}\cdot t$, where t is the discharging time, and γ is the Peukert constant for the discharging process (it typically has a value between 1.05 and 1.3 depending on the type and condition of the battery.) The process is described as follows:

$$I_{\mathrm{eq}}(t) = \left(I_{\mathrm{array}}(t)\right)^{\gamma}$$
$$\mathrm{SoC}(t') = \mathrm{SoC}(t) - \int_t^{t'} \frac{\left(I_{\mathrm{eq}}(\tau) + I_{\mathrm{sd}}(\tau)\right)}{C_b^{\mathrm{full}}}\cdot d\tau \tag{3}$$

where I_{eq} in (3) is the *equivalent discharging current* inside the kth EES array, considering the rate capacity effect. I_{eq} reflects the rate that a battery loses its charge. According to (3), I_{eq} is a convex function of I_{array}. Typically, the self-discharge current I_{sd} is very small, and thereby negligible in battery arrays. Thus, the energy drawn rate is

$$P_{\mathrm{drawn}}(t) = V^{\mathrm{OC}}_{\mathrm{array}}(t)\cdot\left(I_{\mathrm{array}}(t)\right)^{\gamma}. \tag{4}$$

2) Supercapacitor Bank: Supercapacitor banks are commonly used to deal with the peak power demand or supply. The electrical circuit model of the supercapacitor consists of a capacitance, C_{cap} and a series-connected small internal resistance R_{series}. The SoC–OCV relation of the supercapacitor is derived since the charge stored in the supercapacitor is linearly

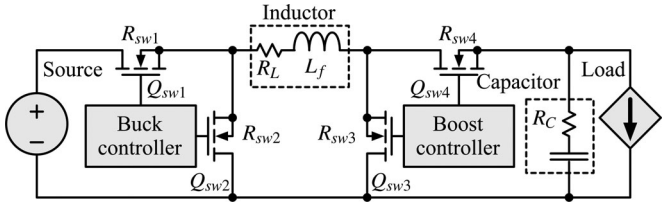

Fig. 6. Buck–boost converter circuit model.

proportional to the terminal voltage. The following relation between $V^{\mathrm{OC}}(t)$ and $V^{\mathrm{CC}}(t)$ for a discharging process is given by

$$V^{\mathrm{OC}}(t) = V^{\mathrm{CC}}(t) + I_{\mathrm{array}}(t) \cdot R_{\mathrm{series}}. \tag{5}$$

The rate capacity effect is negligible for supercapacitors such that $I_{\mathrm{eq}} \approx I_{\mathrm{array}}$. In addition, the aging effect is also negligible for supercapacitors due to its superior cycle life [4].

A primary disadvantage of supercapacitors is their high self-discharge rate, compared to batteries. A supercapacitor typically loses more than 20% of its stored energy per day due to the self-discharge [35]. The voltage decay of a supercapacitor for a short-time interval Δt is given b

$$V^{\mathrm{OC}}(t + \Delta t) = V^{\mathrm{OC}}(t) \cdot e^{-\Delta t/\tau} \tag{6}$$

where τ is the self-discharge time constant. Using Taylor Expansion, the self-discharge power is given by

$$P_{\mathrm{sd}}(t) = C_{\mathrm{cap}} \frac{\left(V^{\mathrm{OC}}_{\mathrm{array}}(t)\right)^2}{\tau}. \tag{7}$$

The energy decrease rate in the supercapacitor bank during the discharging process is given by

$$P_{\mathrm{drawn}}(t) = V^{\mathrm{OC}}_{\mathrm{array}}(t) \cdot I_{\mathrm{array}}(t) + P_{\mathrm{sd}}(t). \tag{8}$$

3) Charger and DC–DC Converter: A charger is a power converter that regulates its downstream current to a desired value. In this paper, we use a pulse width modulation (PWM) buck–boost switching converter model as the charger model, as shown in Fig. 6. The upstream voltage, upstream current, downstream voltage, and downstream current of the charger are denoted by V_{in}, I_{in}, V_{out}, and I_{out}, respectively. Depending on the relation between V_{in} and V_{out}, the charger has two operating modes: the buck mode (if $V_{\mathrm{in}} > V_{\mathrm{out}}$) and otherwise the boost mode. When the charger is turned ON, the power loss P_c^{on} of the charger consists of three components: conduction loss P_{cdct}, gate-drive loss P_{dg}, and controller loss [36]. When the charger is turned OFF, the power loss is zero because the controller is turned OFF. Therefore, we denote the charger status using a binary variable x_c such that $x_c = 1$ if the charger is turned ON and $x_c = 0$ otherwise. The conversion power loss term P_c is given by

$$P_c = P_c^{\mathrm{on}} \cdot x_c = (P_{\mathrm{cdct}} + P_{\mathrm{gd}} + P_{\mathrm{ctrl}}) \cdot x_c. \tag{9}$$

Fig. 6 shows the schematic of the charger. R_L and R_C represent the equivalent series resistances of inductor L and capacitor C, respectively. R_{swi} and Q_{swi} are the turn-on resistance and gate charge of the ith MOSFET switch. In the buck mode, the components of P_c are calculated as follows:

$$\begin{aligned} P_{\mathrm{cdct}} &= {I_{\mathrm{out}}}^2 \cdot (R_L + D \cdot R_{sw1} + (1-D) \cdot R_{sw2} + R_{sw4}) \\ &\quad + \frac{(\Delta I)^2}{12} \cdot (R_L + D \cdot R_{sw1} + (1-D) \cdot R_{sw2} + R_{sw4} + R_C) \\ P_{\mathrm{dg}} &= V_{\mathrm{in}} \cdot f_s \cdot (Q_{sw1} + Q_{sw2}), \\ P_{\mathrm{ctrl}} &= V_{\mathrm{in}} \cdot I_{\mathrm{controller}} \end{aligned} \tag{10}$$

where $D = V_{\mathrm{out}}/V_{\mathrm{in}}$ is the PWM duty ratio and $\Delta I = V_{\mathrm{out}} \cdot (1-D)/(L_f \cdot f_s)$ is the maximum current ripple; f_s is the switching frequency; $I_{\mathrm{controller}}$ is the operating current of the controller.

In the boost mode, the power loss components are given by

$$\begin{aligned} P_{\mathrm{cdct}} &= \left(\frac{I_{\mathrm{out}}}{1-D}\right)^2 \cdot (R_L + DR_{sw3} + (1-D)R_{sw4} \\ &\quad + R_{sw1} + D(1-D)R_C) + \frac{(\Delta I)^2}{12} \cdot (R_L + D \cdot R_{sw3} \\ &\quad + (1-D) \cdot R_{sw4} + R_{sw1} + (1-D) \cdot R_C) \\ P_{\mathrm{dg}} &= V_{\mathrm{out}} \cdot f_s \cdot (Q_{sw3} + Q_{sw4}) \\ P_{\mathrm{ctrl}} &= V_{\mathrm{in}} \cdot I_{\mathrm{controller}} \end{aligned} \tag{11}$$

where $D = 1 - V_{\mathrm{in}}/V_{\mathrm{out}}$ and $\Delta I = V_{\mathrm{in}} \cdot D/(L_f \cdot f_s)$ in this case.

We validate the charger model accuracy by comparing the simulated efficiency with the measured efficiency for an LTM4607 converter [37], which is a typical buck–boost converter. Fig. 5(b) shows that simulated efficiencies obtained using the converter model aforementioned match well with measured efficiencies. We use the same model for dc–dc converters which regulate the load voltages. The power loss of the jth dc–dc converter, denoted by $P_{d,j}$, is also calculated by (9)∼(11) with different sets of parameters, and corresponding upstream/downstream voltages and currents.

C. Optimization Problem Formulation

The charge replacement problem is constrained by laws of energy conservation. Let us consider a discharging process starting from T_s and ending at T_e. As illustrated in Fig. 3, the power delivered to the CTI is used to drive all load devices and corresponding dc–dc converters. For $t \in [T_s, T_e]$, we have

$$P_{\mathrm{CTI}}(t) = V_{\mathrm{CTI}}(t) \sum_{k=1}^{N} I_{\mathrm{bank},k}(t) = \sum_{j=1}^{M} (P_{\mathrm{load},j}(t) + P_{d,j}(t)) \tag{12}$$

where N and M stand for the total number of EES banks and load devices, respectively. The power provided by the kth EES array consists of two parts: the power delivered to the CTI and the power loss in the charger. Thus, we have

$$\begin{aligned} P_{\mathrm{array},k}(t) &= V^{\mathrm{CC}}_{\mathrm{array},k}(t) \cdot I_{\mathrm{array},k}(t) = V_{\mathrm{CTI}}(t) \\ &\quad \cdot I_{\mathrm{bank},k}(t) + P_{c,k}(t) \\ &= V_{\mathrm{CTI}}(t) \cdot I_{\mathrm{bank},k}(t) + P^{\mathrm{on}}_{c,k}(t) \cdot x_{c,k}(t). \end{aligned} \tag{13}$$

The initial OCVs of EES element arrays $V^{\rm OC}_{{\rm array},k}(t)|_{t=0}$, $\forall k \in S$ are known based on the initial SoCs of EES arrays, according to (1). We assume that the load profile, i.e., $P_{{\rm load},j}(t)$ and $V_{{\rm load},j}(t)$ for $t \in [T_s, T_e]$, is given or predictable.[2] The GCR optimization problem can be formulated as follows:

Given: $V^{\rm OC}_{{\rm array},k}(t)|_{t=0}, \forall k \in S$, $V_{{\rm load},j}(t)$ and $P_{{\rm load},j}(t)$ for $1 \le j \le M$ and $t \in [T_s, T_e]$.

Find: $V_{\rm CTI}(t)$, $S_{\rm on}(t)$, and $I_{{\rm bank},k}(t)$, for $\forall k \in S$ and $t \in [T_s, T_e]$.

Maximize: the GCR efficiency, defined as

$$\eta_{\rm GCR} = \frac{\int_{T_s}^{T_e} \sum_{j=1}^{M} P_{{\rm load},j}(t)dt}{\int_{T_s}^{T_e} \sum_{k=1}^{N} P_{{\rm drawn},k}(t)dt}. \quad (14)$$

Note that in (14) $P_{{\rm load},j}(t)$ denotes the power requested by the jth load device at the downstream of its power converter. Thus, the nominator in (14) is a fixed value. Maximizing $\eta_{\rm GCR}$ is equivalent to minimizing $\int_{T_s}^{T_e} \sum_{k=1}^{N} P_{{\rm drawn},k}(t)dt$.

Subject to:

1) energy conservation: (12), (13) are satisfied;
2) charge conservation: for the kth element array

$$\mathrm{SoC}_k(t) = \mathrm{SoC}_k(T_s) - \frac{1}{C^{\rm full}_{b,k}} \int_{T_s}^{t} \frac{P_{{\rm drawn},k}(\tau)}{V^{\rm OC}_{{\rm array},k}(\tau)} d\tau \quad (15)$$

3) the OCV-SoC and OCV-CCV relations for battery (2), (3) and supercapacitor (5);
4) the bank discharging current is no less than zero, and the array discharging current is no more than a maximum value

$$I_{{\rm bank},k}(t) \ge 0, I_{{\rm array},k}(t) \le I^{\max}_{{\rm array},k}, \forall t \in [0, T], \forall k \in S. \quad (16)$$

If $I_{{\rm bank},k}(t) = 0$, the charger is turned OFF, i.e., $k \notin S_{\rm on}(t)$.

V. Optimization Method

We solve the GCR optimization problem in three steps. First, we present an efficient heuristic for the *instantaneous charge replacement* (ICR) problem obtained by letting $T_e \to T_s$ in the GCR problem formulation. Second, we globally consider the complete discharging process and derive discharging power bounds for battery banks to avoid greedy results. Finally, we solve the GCR problem in a discrete time space by solving an ICR problem at the beginning of each time slot with an additional constraint of discharging power bound.

A. Instantaneous Charge Replacement

As the ICR problem implies that $T_e \to T_s$, we omit the time index t in the GCR problem formulation for simplicity in writing. We have EES array OCVs $V^{\rm OC}_{{\rm array},k}, \forall k \in S$ derived from their SoCs, and the load profile $P_{{\rm load},j}$ and $V_{{\rm load},j}$ for $1 \le j \le M$. Optimization variables are S_{on} (or $x_{c,k}, \forall k \in S$), $V_{\rm CTI}$ and $I_{{\rm bank},k}, \forall k \in S$. We let $T_e \to T_s$ in (14). The cost function for ICR is

$$P^{\rm total}_{\rm drawn} = \sum_{k=1}^{N} P_{{\rm drawn},k} = \sum_{k=1}^{N} V^{\rm OC}_{{\rm array},k} \cdot (I_{{\rm array},k})^{\gamma_k} + P_{{\rm sd},k}. \quad (17)$$

We derive the constraints from (12), (13), and (16). The ICR optimization is a mixed-integer nonlinear programming problem due to the existence of binary variables $x_{c,k}$ in (13). Thus, optimally solving the ICR problem is an NP-Complete problem.

We first consider the *optimal discharging current determination* (ODCD) problem, that is, finding the optimal $I_{{\rm bank},k}$, $\forall k \in S_{\rm on}$ to minimize $P^{\rm total}_{\rm drawn}$, under the condition that the selection set $S_{\rm on}$, CTI voltage $V_{\rm CTI}$, and $V^{\rm CC}_{{\rm array},k}$ are given. In the ODCD problem, the charger power loss $P_{c,k}$ is a quadratic function of $I_{{\rm bank},k}$ according to (9)–(11), and $x_{c,k}$ is always one for $k \in S_{\rm on}$. Thus the array discharging current $I_{{\rm array},k}$ becomes a convex function of $I_{{\rm bank},k}$ according to (13). In addition, γ_k is greater than (for battery arrays) or equal to (for supercapacitor arrays) one. Therefore, the cost function (17) becomes a convex function of $I_{{\rm bank},k}, \forall k \in S_{\rm on}$ as well, due to the rules of convexity of composite functions [38]. Moreover, the inequality constraint (16) is convex, and the equality constraint (12) is affine over the control variables of $I_{{\rm bank},k}, \forall k \in S_{\rm on}$. The constraint (13) is already integrated into the objective function. Due to the aforementioned properties of the cost function and constrains, the ODCD problem is a convex optimization problem and can be solved using standard convex optimization tools in polynomial time. We propose the following three heuristics to solve the ODCD problem in an iterative manner, to determine $S_{\rm on}$, $V_{\rm CTI}$ and $I_{{\rm bank},k}$, $\forall k \in S$ for the ICR problem.

Heuristic 1: We assume that the optimal objective function $P^{\rm total}_{\rm drawn}$ is a quasi-convex function with respect to $V_{\rm CTI}$. We first solve the ODCD problem with a fixed $V_{\rm CTI}$ value and obtain the minimal value of $P^{\rm total}_{\rm drawn}(V_{\rm CTI})$. Next, we efficiently search the feasible region of $V_{\rm CTI}$ to get the optimal $V_{\rm CTI}$ value that has the minimal $P^{\rm total}_{\rm drawn}$[3]. Simulation results validate the assumption of quasi-convexity and prove the efficiency of searching for the best-suited $V_{\rm CTI}$ value.

Heuristic 2: We initialize $S_{\rm on} = S$ and solve for proper $S_{\rm on}$ in an iterative manner. In each iteration, we only consider the banks $k \in S_{\rm on}$ in an ODCD problem, and thus $x_{c,k}$ is always one. We update $S_{\rm on}$ by excluding those banks whose discharging currents are smaller than a threshold value at the end of that iteration. We repeat this process until $S_{\rm on}$ converges.

[2] We make this assumption to simplify the presentation of key ideas and approach of our paper. Perfect knowledge of load profiles is not necessary. In practice, the proposed algorithm can take the statistics of load profiles (e.g., average value and standard deviation of the power demand and its duration) as inputs and determine discharging power bounds. At each decision epoch, the proposed algorithm is applied to determine the discharging currents from the actual power demand at that time and the corresponding discharging power bound.

[3] We perform ternary search which converges to the optimal value for unimodel function within log-time complexity. A ternary search is a divide and conquer-based algorithm that determines either that the minimum or maximum cannot be in the first third of the domain or that it cannot be in the last third of the domain. The procedure is then repeated for the remaining two third of the domain. For example, to minimize a unimodal function $f(x)$ in interval $[x_1, x_2]$, we choose two points m_1 and m_2 so that $m_1 = x_1 + (x_2 - x_1)/3$, $m_2 = x_2 - (x_2 - x_1)/3$. We update the boundary of the interval as $x_2 = m_2$ if $f(m_1) < f(m_2)$, and $x_1 = m_1$ otherwise. We repeat this process and find the minimal point when this method converges.

Heuristic 3: We start from the initial condition that $V^{\mathrm{CC}}_{\mathrm{array},k} = V^{\mathrm{OC}}_{\mathrm{array},k}$. In each iteration, we solve ODCD problem with fixed $V^{\mathrm{CC}}_{\mathrm{array},k}$ and update $V^{\mathrm{CC}}_{\mathrm{array},k}$ using (2) after the iteration. We repeat this process until all $V^{\mathrm{CC}}_{\mathrm{array},k}$ converge.

In summary, we solve ICR problem in an iterative manner based on these heuristics. We search the V_{CTI} in the outer loop and use a fixed V_{CTI} in the ODCD problem in the inner loop. We repeatedly solve ODCD problem and update S_{on} and $V^{\mathrm{CC}}_{\mathrm{array},k}$ in the inner loop until they converge. We obtain the $I^{\mathrm{opt}}_{\mathrm{bank},k}, k \in S^{\mathrm{opt}}_{\mathrm{on}}$ and the minimal value of $P^{\mathrm{total}}_{\mathrm{drawn}}(V_{\mathrm{CTI}})$ at the fixed V_{CTI}. We finally pick the V_{CTI} value that gives the minimal $P^{\mathrm{total}}_{\mathrm{drawn}}$ value over the feasible region of V_{CTI}. The complete algorithm is given in Algorithm 1. This algorithm converges because 1) ternary search always converges for a unimodal function; and 2) the number of EES banks in selection set S_{on} does not increase. We do not experience any convergence issue when performing this algorithm.

Algorithm 1: The propsoed ICR solver.

Input: $V^{OC}_{array,k}, \forall k \in S$, $P_{load,j}$ and $V_{load,j}$ for $1 \le j \le M$, CTI voltage range $[V^{min}_{CTI}, V^{max}_{CTI}]$, threshold values V_ε and I_ε

Output: Near-optimal bank discharging current set $\{I^{opt}_{bank,k}, \forall k \in S\}$, corresponding set S^{opt}_{on} and CTI voltage V^{opt}_{CTI}

repeat
- Pick $V_{CTI,1}$ and $V_{CTI,2}$ in the range of $[V^{min}_{CTI}, V^{max}_{CTI}]$
- Initialize $S_{on} \leftarrow S$, $V^{CC}_{array,k} \leftarrow V^{OC}_{array,k}, \forall k \in S_{on}$
- **for** *both* $V_{CTI,1}$ *and* $V_{CTI,2}$ **do**
  - **repeat**
    - Update near-optimal bank discharging current set: $\{I_{bank,\,k}, \forall k \in S_{on}\} \leftarrow$ *ODCD_Solver*(V_{CTI}, S_{on}, $\{V^{CC}_{array,k}, \forall k \in S_{on}\}$)
    - If $I_{bank,k} < I_\varepsilon$, remove the k-th bank from S_{on}
    - Update $V^{CC}_{array,k}, \forall k \in S_{on}$ using (2)(5)
  - **until** *both* S_{on} *and* $V^{CC}_{array,k}, \forall k \in S_{on}$ *converge*
  - $\forall k \in S$: if $k \in S_{on}$, $I^{opt}_{bank,k} \leftarrow I_{bank,k}$; else, $I^{opt}_{bank,k} \leftarrow 0$
  - Calculate P^{total}_{drawn} using (17)
- Update upper bound V^{max}_{CTI} or lower bound V^{min}_{CTI} based on P^{total}_{drawn} values obtained for $V_{CTI,1}$ and $V_{CTI,2}$

until $V^{max}_{CTI} - V^{min}_{CTI} \le V_\varepsilon$

return $\{I^{opt}_{bank,k}, \forall k \in S\}$, $S^{opt}_{on} \leftarrow S_{on}$, $V^{opt}_{CTI} \leftarrow V_{CTI}$

B. Global Charge Replacement

The GCR problem considers the optimization problem to maximize the GCR efficiency for the complete discharging process. We break the discharging process into a series of time slots and solve the GCR in a discrete time space. The time slot is short enough so that SoCs of EES banks are approximately unchanged during that time slot. Thus, we solve an ICR problem during each time slot and update SoCs of EES banks afterwards. A simple method may solve a series of ICR problems one at a time slot to tackle the GCR problem, which may fail to achieve the global optimality due to its greedy nature. In fact, the proposed ICR solver prefers to retrieve more energy from the supercapacitor banks because of their higher cycle efficiency. Thus, it is highly likely that all supercapacitor banks may be fully discharged at very early stage. The consequence is that we have to discharge the battery banks at higher rates for the rest of the discharging process, which causes more energy loss due to the rate capacity effect and in turn degrades the GCR efficiency significantly. Therefore, it is necessary to "globally consider the complete discharging process" and properly assign energy demands among different types of EES banks.

1) Estimation of Discharging Power Bounds: We start from the fact that battery banks are generally less efficient compared to supercapacitor banks in supplying higher load demands, due to their relatively large internal resistances and the rate capacity effect. Thus, we can achieve high GCR efficiency by limiting discharge currents of battery banks to relatively low levels while using the supercapacitor banks to shave the peak power demands. Inspired by this idea, we classify all EES banks into two main categories without loss of generality: supercapacitor banks and battery banks, due to their distinct characteristics.

We introduce *discharging power bound*, denoted by $P^*(t)$, and define them as time-dependent lower bounds of power provided by all battery banks. We define *effective energy* of a category as the energy delivered to load devices from all banks in that category, excluding the energy loss due to the internal resistance, rate capacity effect, and power conversion. We denote effective energy provided by the supercapacitor and battery banks by $E^{\mathrm{SB}}_{\mathrm{eff}}$ and $E^{\mathrm{BB}}_{\mathrm{eff}}$, and have

$$E^{\mathrm{BB}}_{\mathrm{eff}} \le \int_{T_s}^{T_e} \min\left\{\sum_{j=1}^{M} P_{\mathrm{load},j}(t),\ P^*(t)\right\} dt$$

$$E^{\mathrm{SB}}_{\mathrm{eff}} = \int_{T_s}^{T_e} \sum_{j=1}^{M} P_{\mathrm{load},j}(t)dt - E^{\mathrm{BB}}_{\mathrm{eff}} = E_{\mathrm{load}} - E^{\mathrm{BB}}_{\mathrm{eff}} \quad (18)$$

where E_{load} is the total energy requested by all load devices. According to (18), deriving $P^*(t)$ depends on load demand profiles and $E^{\mathrm{SB}}_{\mathrm{eff}}$. We estimate $E^{\mathrm{SB}}_{\mathrm{eff}}$ in a way that we want to fully utilize the energy stored in supercapacitor banks during the discharging process. We may typically set $E^{\mathrm{SB}}_{\mathrm{eff}}$ to be 80%–90% of total energy available in all supercapacitor banks, denoted by $E^{\mathrm{SB}}_{\mathrm{tot}}$, to leave some margin for the energy loss due to power conversion and self-discharge.

Discharging power bounds $P^*(t)$ set lower bounds for the discharging power of all battery banks, which in turns becomes upper bounds for the discharging power of all supercapacitor banks, and thereby prevents all supercapacitor banks from being completely discharged at very early stage. To present the heuristic to determine the $P^*(t)$, we first start from a proposition.

Proposition: A constant $P^*(t)$ during the discharging process $[T_s, T_e]$ yields the minimal amount of energy drawn from all battery banks, when the self-discharge of supercapacitor banks and dependence of battery OCVs on SoCs are ignored.

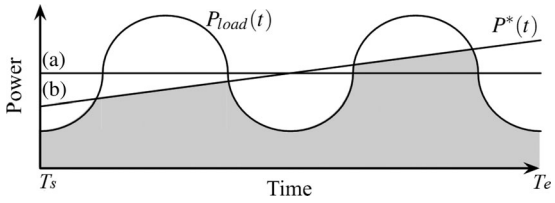

Fig. 7. Line (a) and (b) show the discharging power bounds. The shadow area and white area under $P_{\text{load}}(t)$ curve denote the $E_{\text{eff}}^{\text{BB}}$ and $E_{\text{eff}}^{\text{SB}}$, respectively.

Proof: The total energy drawn from battery banks is

$$E_{\text{drawn}}^{\text{BB}} = \int_{T_s}^{T_e} \sum_{k \in \text{BB}} V_{\text{array},k}^{\text{OC}}(t) \cdot (I_{\text{array},k}(t))^{\gamma_k} \, dt. \quad (19)$$

We let $E_{\text{eff}}^{\text{SB}}$ to be 90% of $E_{\text{tot}}^{\text{SB}}$ in (18), thus we have

$$E_{\text{eff}}^{\text{BB}} = \eta_0 \int_{T_s}^{T_e} \sum_{k \in BB} V_{\text{array},k}^{\text{OC}}(t) \cdot I_{\text{array},k}(t) dt = E_{\text{load}} - 0.9 E_{\text{tot}}^{\text{SB}} \quad (20)$$

where η_0 accounts for the conversion efficiency of power converters. Note that the RHS in (20) is a fixed value and (19) is a convex function of discharging currents. Therefore, ignoring OCV-SoC relations, a fixed $I_{\text{array},k}(t)$ during $[T_s, T_e]$ results in minimal $E_{\text{drawn}}^{\text{BB}}$. Note that if there exists $I_{\text{array},k}(t_1)$ and $I_{\text{array},k}(t_2)$ such that $I_{\text{array},k}(t_1) \neq I_{\text{array},k}(t_2)$, we can always find a better solution, which is $I'_{\text{array},k} = (I_{\text{array},k}(t_1) + I_{\text{array},k}(t_2))/2$ at time instance t_1 and t_2, such that $(I_{\text{array},k}(t_1))^{\gamma_k} + (I_{\text{array},k}(t_2))^{\gamma_k} > 2(I'_{\text{array},k})^{\gamma_k}$ for $\gamma_k > 1$. ■

Based on this proposition, we determine a constant discharging power bound $P^*(t) = P_0^*$ for $t \in [T_s, T_e]$, which is shown as Line (a) in Fig. 7. The value of P_0^* is determined by using the binary search.

We account for the self-discharge of supercapacitor banks and the dependence of battery OCVs on SoCs after we obtain $P^*(t) = P_0^*$ for $t \in [T_s, T_e]$. According to (7), the self-discharge rate is proportional to the remaining energy in a supercapacitor array. Therefore, a straight line $P^*(t) = \rho \cdot t + P^*(0)$ with positive slope ρ, shown as Line (b) in Fig. 7, reduces the total self-discharge energy loss by allowing more energy to be retrieved from supercapacitor banks at the early stage. We use the flat P_0^* line as a reference and calculate the slope curve with the same integral area.

The slope ρ determines the tradeoff between the energy loss due to rate capacity effect in battery banks and the energy loss due to self-discharge in supercapacitor banks. Greater slope ρ consumes more energy in battery banks due to the rate capacity effect. This is because that $E_{\text{drawn}}^{\text{BB}}$ is a super-linear function of $I_{\text{array},k}(t)$ for every battery bank, according to (19). On the other hand, $\rho = 0$ results in slow discharging supercapacitor banks at the early stage, which causes a high self-discharge energy loss in supercapacitor banks. Therefore, the total energy drawn from the HEES system, including the energy loss due to both the rate capacity effect and self-discharge, is an unimodal function with respect to the slope.

We perform ternary search to efficiently search in a proper interval of ρ, from zero to reasonable upper limit, to determine the appropriate slope ρ. We pick two slopes, ρ_1 and ρ_2, that correspond to one-third and two-third points of the current interval $[\rho_{\min}, \rho_{\max}]$ in each iteration. We construct the discharging power bound curves, $P_1^*(t)$ and $P_2^*(t)$, with ρ_1 and ρ_2, respectively, and let them have the same integral area with the flat P_0^* line. Then, we calculate the total energy drawn $E_{\text{drawn},1}^{\text{total}}$ and $E_{\text{drawn}n,2}^{\text{total}}$ accordingly, considering the rate capacity effect and OCV changes with respect to SoCs in battery banks, and self-discharge in supercapacitor banks. We drop the left third of the if $E_{\text{drawn},1}^{\text{total}} > E_{\text{drawn},2}^{\text{total}}$ and right third otherwise. We repeat this procedure until the optimal slope ρ_{opt} is found. A more rigorous (but also more computationally expensive) method to derive the power bound is presented in [7], in which an optimization problem is formulated and solved by using the method of Lagrange multiplier. To reduce the computation overhead, we use the method presented above to implement the control policy in the HEES prototype.

2) Solving the GCR Problem: We solve the GCR problem hierarchically. At the top level, we globally consider the complete discharging process before discharge begins and find the optimal discharging power bounds $P^*(t)$ over the discharging process. At the bottom level, we break the discharging process into a series of time slots and solve a series of ICR problems, accounting for all kinds of energy loss in detail. At the beginning of a time slot, we solve an ICR problem by using Algorithm with an additional constraint given by

$$V_{\text{CTI}}(t) \sum_{k \in \text{BB}} I_{\text{bank},k}(t) \geq \min\{P_{\text{load}}^{\text{total}}(t), \; P^*(t)\}. \quad (21)$$

Since (21) is an affine inequality constraint, the constrained ODCD problem is still solved optimally in polynomial time. Therefore, the GCR solution is obtained by solving ICR problem at each time slot and combining the solutions together. To improve GCR solutions, we may refine the estimation of discharging power bounds $P^*(t)$ according to the actual remaining energy in supercapacitor arrays over the discharging process.

We solve the convex optimization problem by using MATLAB on a host machine with specifications of Intel Duo Core 2.4 GHz and 4-G memory. The average time needed to determine the discharging currents at the beginning of each decision epoch is 2.4 s for an 8-bank HEES system. This runtime is negligible compared to the duration of each decision epoch, which is typically set to 10–15 min.

VI. Experimental Results

We perform charge replacement experiments based on the HEES prototype to validate energy efficiency benefits brought by the HEES system and the efficacy of the presented method. Specifications of HEE banks in the prototype are listed in Table II. In our experiments, we connect a tuneable ac load to the HEES prototype through a Samlex PST-100S-24A dc–ac inverter [39]. Charger boards and dc–dc converters are made by ourselves with maximum output current of 3 A and voltage rating of 6 V–36 V. We focus on the charge replacement between

TABLE II
SPECIFICATIONS OF THE EES BANKS IN THE HEES PROTOTYPE

Parameters		Supercap Bank	Li-ion Bank	Lead-acid Bank
Unit Cell	Cell	Maxwell BCAP0650	Samsung ICR18650-26F	Panasonic LC-R123R4P
	Voltage	≤2.7 V	3.7 V	12 V
	Capacity	650 F	2.6 Ah	3.4 Ah
	Energy	0.66 Wh	9.6 Wh	40.8 Wh
	Cost	$69/Wh	$3/Wh	$1/Wh
Config	Series	14	6	2
	Parallel	1	2	2
Bank	Voltage	≤37.8 V	22.2 V	24 V
	Energy	8.13 Wh	115 Wh	163 Wh

EES banks and the CTI, and treat the inverter efficiency as a constant (with a value of 85%). We assume the same constant efficiency in all experiments to make fair comparisons.

A. EES Bank Characterization

We first perform a characterization process to obtain characteristics of each component in the prototype. During the characterization process, we find the internal resistance of each EES bank, obtain conversion efficiencies of chargers at different input and output conditions, and calculate the Peukert constant for battery banks. We obtain internal resistances values around 0.15, 0.5, and 0.7 Ω for the supercapacitor bank, Li-ion battery bank, and lead-acid battery bank, respectively. We find that the internal resistance does not change much except for a rapid increase when the battery SoC approaches 0 or 1, which does not last long in practice. Therefore, we approximately treat internal resistances of EES banks as constant for the simplicity in policy implementation. We measure the conversion efficiency of the charger at different conditions using a NI-DAQ.

To calculate Peukert constants of Li-ion battery bank and lead-acid battery bank, we fully charge and then discharge them at different rates. Due to the limitation of the current rating of our charger boards (up to 3A), we do not observe significant rate capacity effect in the Li-ion battery bank. For the lead-acid battery bank, according to the datasheet [40], we charge the lead-acid bank to 26.2 V with 0.5 A current, and then completely discharge it at five different rates (0.46, 0.59, 0.95, 1.14, and 1.42 A). We log the discharging current and time before the terminal voltage reaches a stopping value, which depends on the discharging rate, e.g., 20.4 V for 0.8 A. The top panel in Fig. 8 shows that the terminal voltage of the lead-acid battery decreases with time at different discharging rates. We perform curve fittings on rated capacities, which are calculated by integrating the array discharging current over the discharging time, versus discharging rates and obtain the Peukert constant $\gamma_{\mathrm{lead-acid}} = 1.19$ by using (3). Fitting results are shown in the bottom panel in Fig. 8.

B. Optimal CTI Voltage Setting

We derive the charge replacement policy using the presented method in Section V-A. We take the terminal voltage of EES arrays, array and bank currents, and discharging power bound for each EES bank as inputs, together with the precharacterized data of charger conversion efficiency, to determine the CTI voltage,

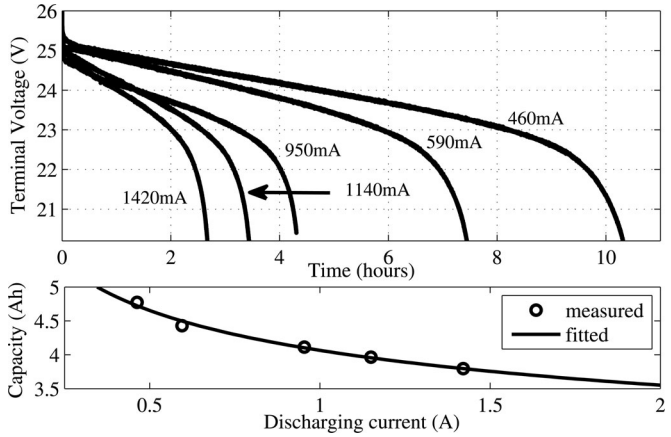

Fig. 8. Characterization of the lead-acid battery bank (top panel), and curve fitting of the rated capacities with respect to the discharging currents (bottom panel) to find the Peukert constant.

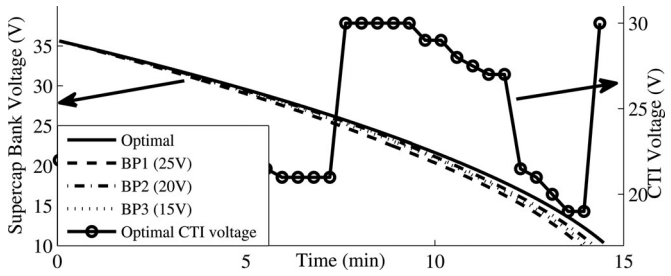

Fig. 9. Changes of the terminal voltage of the supercapacitor bank over the discharging process for the presented policy and baseline policies (left axis), and optimal CTI voltage settings in the presented policy (right axis).

as well as the operating current of each bank. To show the effect of optimal CTI voltage settings, we turn off other banks and perform discharging process by using the supercapacitor bank only. Typically, the terminal voltage of the supercapacitor bank varies in a great range thus we may observe large optimal CTI voltage change. The supercapacitor bank is charged to 36 V, then discharge for 15 min using a constant load demand profile. We perform several discharging processes using the presented policy with optimal CTI voltage settings and some baselines which use fixed CTI voltages.

Fig. 9 shows changes of terminal voltages of supercapacitor bank over the discharging process using the presented policy and baselines. One can observe that, starting from same conditions, to deliver the same amount of energy, more energy is left in the supercapacitor bank when presented policy is applied, compared to baselines policies, (i.e., the solid curve corresponding to presented policy is above the others three lines corresponding to baseline policies.) Fig. 9 shows that the optimal CTI voltage setting changes over the discharging process, depending on the terminal voltage of the supercapacitor bank. The optimal CTI voltage curve shows discontinuities because the charger is characterized discretely and charger efficiencies at some cases input–output voltage combinations are very close. Therefore, as the supercapacitor voltage changes, the optimal CTI voltage may vary greatly.

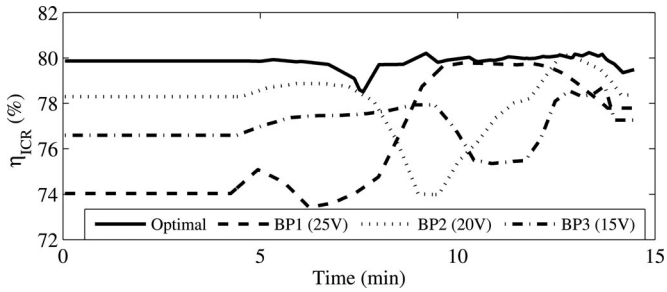

Fig. 10. Comparisons of the ICR efficiency between the presented policy and baseline policies during the discharging process.

TABLE III
COMPARISONS OF GCR EFFICIENCIES OBTAINED BY USING THE PRESENTED POLICY AND BASELINE POLICIES FOR DIFFERENT FLAT LOAD PROFILES USING SUPERCAPACITOR BANK ONLY

P_{load} (W)	Duration (min)	Initial V_{spc} (V)	Presented (%)	BP1 (%)	BP2 (%)	BP3 (%)
15	10	25	78.59	74.73	75.37	76.01
	10	36	78.09	75.83	76.45	73.99
	25	36	78.37	74.26	76.21	75.12
25	5	25	79.40	77.81	76.10	76.19
	5	36	79.67	73.73	77.18	76.34
	15	36	79.41	75.37	76.94	76.37
35	5	25	78.51	77.66	74.75	75.01
	5	36	78.38	74.95	77.09	76.54
	10	36	78.76	76.42	77.11	76.24

Fig. 10 compares *ICR efficiency* $\eta_{\rm ICR}$[4] obtained by the presented policy and baseline policies over the discharging process. The presented policy consistently outperforms baseline policies during the complete discharging process. Fig. 10 shows that no single fixed CTI voltage does the perfect job in maximizing the $\eta_{\rm ICR}$ all the time. In contrast, the presented policy achieves the optimal $\eta_{\rm ICR}$ through adaptively setting the CTI voltage. Table III lists the GCR efficiencies obtained by applying the optimal CTI voltage control policy and baseline policies for different levels of the load demand. BP1, BP2, and BP3 in the Table III stand for the baseline policy with fixed CTI voltage of 25, 20, and 15 V, respectively. Table III shows that maintaining CTI voltage at optimal value achieves up to 5.9% $\eta_{\rm GCR}$ improvement.

C. Hybrid Usage of EES Banks

To demonstrate energy benefits of the HEES system, we use supercapacitor and lead-acid battery banks as these two EES banks exhibit very different characteristics. In contrast, the Li-ion battery bank does not show distinct characteristics from the supercapacitor bank because the maximum discharging current supported by our charger boards is too low to observe the rate capacity effect in Li-ion batteries. The general idea of the presented policy is to shave peaks of the power demand, in order to reduce the energy loss due to rate capacity effect in the lead-acid battery bank. We derive discharging power bounds and assign power demands accordingly to the supercapacitor bank and the lead-acid bank, respectively, as explained in Section V-B1. Note that in Section V-B1, we present a general method of deriving power bounds with the consideration of the self-discharge of the supercapacitor bank. In our experiments, the discharging process do not last longer than 1 h, therefore, the self-discharge of the supercapacitor bank can be safely ignored.

[4]ICR efficiency $\eta_{\rm ICR}$ is defined as the ratio between the load power demand and the total power drawn from all EES banks at a time instance.

TABLE IV
COMPARISONS OF GCR EFFICIENCIES OBTAINED USING THE PRESENTED POLICY AND BASELINE POLICIES FOR FLAT LOAD PROFILES

P_{load} (W)	Duration (min)	Presented (%)	V_{cti} (V)	BP4 (%)	BP5 (%)	BP6 (%)
30	30	69.04	25	64.92	63.40	56.67
			20	64.66	67.10	55.94
			15	65.33	66.81	57.42
	20	74.00	25	69.05	64.97	56.67
			20	69.02	69.78	55.94
			15	69.28	69.11	57.42
45	25	65.01	25	63.08	62.18	55.04
			20	62.07	64.81	53.37
			15	62.48	64.15	54.26
	15	72.79	25	68.43	64.96	55.04
			20	67.87	69.23	53.37
			15	67.96	67.94	54.26

TABLE V
COMPARISONS OF GCR EFFICIENCIES OBTAINED USING THE PRESENTED POLICY AND BASELINE POLICIES FOR PULSED LOAD PROFILES

P_{load} (W)	Duration (min)	Presented (%)	V_{cti} (V)	BP4 (%)	BP5 (%)	BP6 (%)
(50, 20)	25	66.18	25	61.33	60.44	55.00
			20	61.61	62.12	55.23
			15	61.49	62.50	55.45
	12	70.27	25	64.33	63.25	55.01
			20	64.01	64.67	55.27
			15	65.32	63.84	55.48
(70, 5)	30	63.53	25	59.47	59.86	51.27
			20	59.28	59.77	50.56
			15	59.83	60.03	51.48
	15	75.21	25	67.41	64.07	51.28
			20	67.67	64.31	50.52
			15	67.86	64.43	51.43

We explore the GCR efficiency improvements by using the presented policy for various kinds of load demand profiles. A flat load profile demands same amount of power for the whole discharging process. Table IV compares the performance of the presented policy against those of baseline policies for flat load profiles with different durations and power demand levels. The pulsed load profiles are taken from real power demands generated by a military radio as reported in [41]. The profile consists of periodic alternate peaks (when transmitting signals) and off-peaks (when receiving signals) power demand levels. The duty ratios (peak time as a percent in one period) of the peak power demand are 50% for the (50 W, 20 W) case and 40% for the (70 W, 5 W) case in Table V. Randomly generated load profiles are obtained by adding random Gaussian-distributed power demands to some fixed average load demand levels. We use this kind of load profiles to mimic realistic load demand profiles which typically have fluctuations in power demand profiles.

Tables IV and V compare GCR efficiencies obtained by using the presented policy and three other baseline policies for flat and pulsed load profiles, respectively. The baseline policy BP4 discharges the supercapacitor bank first and switches to battery

TABLE VI
COMPARISONS OF THE GCR EFFICIENCIES OBTAINED USING THE PRESENTED POLICY AND BASELINE POLICIES FOR RANDOM-GENERATED LOAD PROFILES

$P_{load,avg}$ (W)	Duration (min)	Presented (%)		V_{cti} (V)	BP4 (%)	BP5 (%)	BP6 (%)
		perfect	average				
45.78	30	65.56	65.43	25	61.79	60.93	55.14
				20	61.18	63.34	54.18
				15	61.45	63.12	55.05
54.14	15	72.17	72.16	25	66.56	65.30	54.30
				20	66.60	67.75	52.77
				15	66.50	67.63	53.61

bank only if the supercapacitor bank is completely depleted. The baseline policy BP5 discharges all available EES banks with the same amount of current. The other baseline policy, BP6, uses lead-acid battery bank only. BP6 is designed to explore the energy efficiency benefit of the HEES system against the homogeneous EES system. All baseline policies keep constant CTI voltage levels (shown in the tables) over the whole discharging processes. One can observe from Tables IV and V that the presented GCR policy consistently outperforms baseline policies. The maximum GCR efficiency improvement ranges from 2.8% to 11.1% for the HEES baselines, and from 11.6% to 24.7% for homogeneous EES baseline, respectively, depending on load profiles. For short-duration load profiles, BP4 achieves better GCR efficiencies than BP5 and BP6 because it fully utilizes the energy stored in the supercapacitor bank (i.e., the supercapacitor bank has higher charge replacement efficiency due to the small internal resistance and negligible rate capacity effect.) However, for long-duration load profiles, BP5 performs better than BP4, because BP4 has to draw the energy from the lead-acid battery bank after the supercapacitor bank is depleted, which is inefficient and significantly degrades the overall GCR efficiency. In general, the GCR efficiency decreases at higher load demand because the power loss due to rate capacity effect is a superlinear function with respect to discharging currents.

We show results of the presented GCR policy for randomly generated load profiles in Table VI. The presented policy improves the GCR efficiency by up to 4.5% and 6.8% against HEES baseline policies BP4 and BP5 for two randomly generated load profiles. In addition, it improves the GCR efficiency by up to 10.3% and 19.4% against the homogeneous EES baseline BP6. We derive the GCR policy using the average power demand of the randomly generated load profile. One can observe that almost the same quality of GCR efficiency is obtained, comparing to the case that we assume the perfect knowledge of the load profile. Fig. 11 shows energy assignments between the supercapacitor bank and the lead-acid bank in the presented GCR policy, baseline policies BP4, and BP5, for the 15-min randomly generated load profile, respectively. The light gray areas denote the energy drawn from the supercapacitor bank and the dark gray areas denote that drawn from the lead-acid battery bank. According to Section V-B1, the presented GCR policy shaves peaks of the load demand and discharges the lead-acid bank at a relatively low rate over the whole discharging process. In Fig. 11(a), the discharging power bound is nearly a flat line because load demand profiles only last for a short period of time, and therefore, the self-discharge of supercapacitor banks is negligible. In contrast, the BP4 policy draws the energy from the supercapacitor bank first, thus the light gray part ends quickly. The BP5 policy equally assigns the power demand between two banks until the supercapacitor bank is depleted.

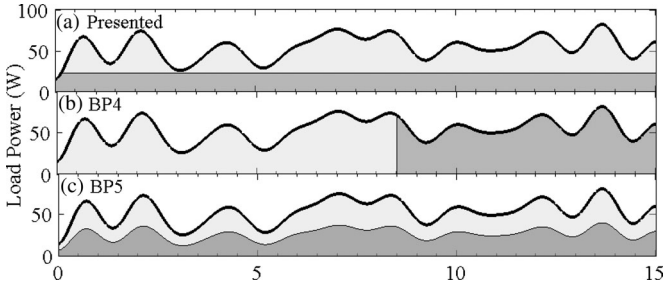

Fig. 11. Power assignments by the presented GCR policy (a), BP4 (b), BP5, and (c) for the 15-min load profiles in Table V. Light and dark gray areas denote amounts of energy drawn from the supercapacitor bank and the lead-acid battery bank, respectively.

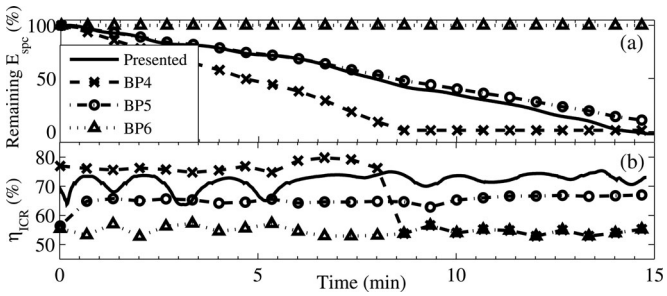

Fig. 12. Comparisons of the normalized remaining energy in the supercapacitor bank (a) and the ICR efficiencies and (b) obtained by the presented GCR policy and baseline policies, for the 15-min load profiles in Table V.

Fig. 12 shows the corresponding remaining energy in the supercapacitor bank and the ICR efficiency over for the 15-min randomly generated load profile. The energy stored in supercapacitor banks decreases from 100% to 0% for presented policy, BP4, and BP5. BP6 only uses the battery bank, and thereby the remaining energy stays close to 100%. One can observe that the BP4 drains the energy stored in the supercapacitor after 8 min. operation. The ICR efficiency is high (>80%) during that period but drops significantly thereafter. BP5 policy is less aggressive than BP4 in the sense that it simultaneously discharges both battery and supercapacitor banks. However, the energy assignment of BP5 is not optimal among these two banks. The presented policy assign power demand among EES banks more properly by globally considering the whole discharging process. It minimizes the energy loss due to the rate capacity effect in the lead-acid battery bank, through fully utilizing the energy stored in the supercapacitor bank and shaving load demand peaks over the whole discharging process.

VII. CONCLUSION

This paper introduced the GCR problem for HEES systems. We formulated the GCR problem as a mixed-integer nonlinear programming problem, and presented an efficient algorithm to

find a near-optimal solution. We first obtained a discharging power bound with a global consideration of HEES system characteristics and load demand profiles over the complete discharging process. Then, we solved the GCR problem in a discrete time manner. In particular, at beginning of each time slot, we solved an ICR problem constrained by the aforesaid power bound. We generated a near-optimal solution of the ICR problem by applying effective heuristics to simplify it to a convex optimization problem. We built an HEES prototype with the purpose of exploring the energy benefits brought by the HEES system and validating the efficacy of the presented GCR policy. The charge replacement policy was derived using the presented algorithm, and implemented in the HEES prototype. Experimental results based on the HEES prototype demonstrated significant GCR efficiency improvement against baseline policies.

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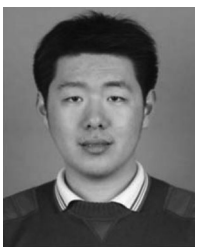

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