Control Technology for T-type Three Level Power Conversion System Under Non-ideal Grid

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Abstract— Network voltage unbalance would cause distortion of grid-connected current of power conversion system and increase its harmonic contents, and in worse conditions, devices would be disconnected to protect, which would affect power grid. To guarantee stability of system control, taking balance grid-connected current exported by power conversion system and device networking during failures as the control objectives, the essay put forward control strategies for two-stage type and T-type three-level power conversion systems in non-ideal gird conditions. By controlling AC side negative current, guaranteeing that power conversion system can steadily networked under the condition when power grid is imbalanced. To verify the control strategies, the essay had simulation and experimental verification at last to fully prove validity of the strategies in non-ideal conditions.

Key words—two-stage type power conversion system; T-type three-level; non-ideal grid; phase-locked loop

I. ABSTRACT

At present, distributed power technology is widely used in production and life, and energy storing devices are greatly concerned since they can adjust power of the whole microgrid system. As an interface device between energy storage system and grid, power conversion system (PCS) plays a decisive role to stability of the energy storage system and even the whole grid^[1].

In practical application, the phenomenon of imbalance of network voltage is serious. If control strategies for ideal conditions are used, DC bus would generate double frequency fluctuations and cause over-current protection of devices. For devices of low power, if gird goes wrong, devices can directly close down to protect; however, for energy storage devices of high power, if devices close down, it would affect grid and even cause faults and deterioration of grid^[2]. Therefore, control strategies of PCS under the condition of imbalanced grid are of great importance.

To solve device control problems in non-ideal grid, literature [3] analyzed influence of imbalanced network voltage on DC bus and put forward the control algorithms of mean value feedforward and momentary value feedforward to control current impact. Its principle is

National Natural Science Foundation of China (51777002) Beijing High Level Innovation Team Construction Plan (IDHT20180502) Scientific and Technological Innovation Engineering Plan of North China University of Technology (18XN141) introduce network voltage feedforward from the output end of electric current loop to make corresponding feedforward items also changes when there are faults of network voltage, so as to restrain falls of network voltage and reduce current impact. However, since the algorithm introduced voltage feedforward and added low pass filters within controllers, it would cause certain delays and make response of feedforward control lag behind. In regard to imbalanced network voltage, literature [4] put forward three control strategies according to different constraint conditions, namely, restraining DCbus voltage fluctuations, restraining power fluctuations compensating for reactive power, and model establishment and design of the control system are realized in dual synchronous revolting dq coordinate system and have realized favorable experimental effects. However, the above literatures were based on photovoltaic inverters or single-stage PCS, and there are seldom studies on control of two-stage PCS.

For two-stage PCS, the essay put forward the control strategies for con-ideal grid in dual revolting coordinate system which could guarantee that devices could have grid-connected operation under non-ideal grid by controlling negative sequence current, and three-phase current could have balanced output.

II. TOPOLOGICAL STRUCTURE OF PCS

PCS can be generally divided into single-stage type and two-stage type according to whether it has a DC/DC link^[5].

The essay adopted dual-stage T-type three-level PCS. Compared with single-stage PCS, dual-stage structure has a DC/DC link, which makes operating voltage range of battery wider than the topological structure of single-stage type, and its topological structure is as shown in figure 1.

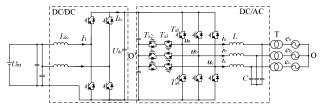


Fig.1. Topology of dual-stage PCS

In the dual-stage topology shown in figure 1, DC/DC converter adopts the dual alternating parallel structure to reduce output current ripples, and it uses single electric

current loop to control direction and size of DC side current. However, DC/AC converter adopts T-type three-level structure. Compared with traditional two-level structure, it adds an output level number and thus reduces hardware volume of AC side filters.

III. CONTROL STRATEGY IN NON-IDEAL GRID

Large power grid generally has a slight three-phase voltage unbalance which would not affect PCS, but when the whole system is connected with a three-phase unbalance load of big power, there can be serious voltage unbalance. If devices are not controlled under the voltage state, PCS is easy to close down directly and it would even affect the grid.

3.1 Phase-locked loop under the condition of grid unbalance

In the process when devices are networked, the control system needs phase signals of grid voltage, which is known as phase lock. In ideal grid, single synchronous reference coordinate system phase lock is often adopted, and its control block diagram is shown in figure 2.

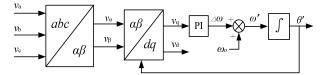


Fig.2. Single synchronous reference coordinate system phase-locked loop control

However, under the condition of grid voltage unbalance, traditional phase lock methods are not applicable and easy to cause inaccurate phase lock and thus give rise to distortion of gird-connected current. To avoid problems of grid-connected control, it is necessary to improve phase-locked loop. In non-ideal grid, positive sequence fundamental component would remain unchanged, thus the essay adopted eh phase lock method based on positive sequence fundamental component, and its control block diagram is shown in figure 3.

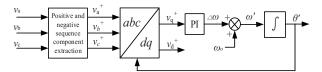


Fig. 3. Phase-locked loop based on positive sequence fundamental component

3.1.1 Separation of positive and negative sequence

To extract fundamental positive-sequence component of grid voltage, three-phase voltage should first separate positive and negative sequence^[6].

Three-phase grid voltage generally is the sum of positive sequence voltage, negative sequence voltage and zero sequence voltage. And the formula is as follows:

$$\begin{bmatrix} v_{a} \\ v_{b} \\ v_{c} \end{bmatrix} = V_{s}^{+} \begin{bmatrix} \cos(\alpha t + \varphi^{+}) \\ \cos(\alpha t + \varphi^{+} - \frac{2\pi}{3}) \\ \cos(\alpha t + \varphi^{+} + \frac{2\pi}{3}) \end{bmatrix} + V_{s}^{-} \begin{bmatrix} \cos(-\alpha t + \varphi^{-}) \\ \cos(-\alpha t + \varphi^{-} - \frac{2\pi}{3}) \\ \cos(-\alpha t + \varphi^{-} + \frac{2\pi}{3}) \end{bmatrix} + V_{s}^{0} \begin{bmatrix} \cos(\alpha t + \varphi^{0}) \\ \cos(\alpha t + \varphi^{0}) \\ \cos(\alpha t + \varphi^{0}) \end{bmatrix}$$
(1)

In formula (1), V_s stands for amplitude of positive-sequence component and negative-sequence component; φ^+ and φ^- stand for initial phase of positive sequence and negative sequence of grid voltage respectively; and ω is fundamental angle frequency of grid voltage.

The essay adopted three-phase three —wire converters without zero sequence voltage, thus it is not necessary to consider influence of zero sequence voltage component. Through Clarke conversion of formula (1), formula (1) can be:

$$\begin{bmatrix} v_{\alpha} \\ v_{\beta} \end{bmatrix} = V_{s}^{+} \begin{bmatrix} \cos(\omega t + \varphi^{+}) \\ \sin(\omega t + \varphi^{+}) \end{bmatrix} + V_{s}^{-} \begin{bmatrix} \cos(\omega t + \varphi^{-}) \\ \sin(\omega t + \varphi^{-}) \end{bmatrix}$$
(2)

And through transformation of dq coordinates, formula (2) can be:

$$\begin{bmatrix} v_{d}^{+} \\ v_{q}^{+} \end{bmatrix} = \begin{bmatrix} T_{dq}^{+} \end{bmatrix} \begin{bmatrix} v_{\alpha} \\ v_{\beta} \end{bmatrix} = V_{s}^{+} \begin{bmatrix} \cos(\alpha + \varphi^{\dagger} - \theta) \\ \sin(\alpha + \varphi^{\dagger} - \theta) \end{bmatrix} + V_{s}^{-} \begin{bmatrix} \cos(-\alpha + \varphi^{-} - \theta) \\ \sin(-\alpha + \varphi^{-} - \theta) \end{bmatrix}$$
(3)

$$\begin{bmatrix} v_{\mathbf{d}}^{-} \\ v_{\mathbf{q}}^{-} \end{bmatrix} = \begin{bmatrix} T_{\mathbf{d}\mathbf{q}}^{-} \end{bmatrix} \begin{bmatrix} v_{\alpha} \\ v_{\beta} \end{bmatrix} = V_{s}^{+} \begin{bmatrix} \cos(\alpha t + \varphi^{+} + \dot{\theta}) \\ \sin(\alpha t + \varphi^{+} + \dot{\theta}) \end{bmatrix} + V_{s}^{-} \begin{bmatrix} \cos(-\alpha t + \varphi^{-} + \dot{\theta}) \\ \sin(-\alpha t + \varphi^{-} + \dot{\theta}) \end{bmatrix}$$
(4)

 $\begin{bmatrix} T_{\mathrm{dq}}^{+} \end{bmatrix} = \begin{bmatrix} \cos \theta' & \sin \theta' \\ -\sin \theta' & \cos \theta' \end{bmatrix}$ $\begin{bmatrix} T_{\mathrm{dq}}^{-} \end{bmatrix} = \begin{bmatrix} \cos \theta' & -\sin \theta' \\ \sin \theta' & \cos \theta' \end{bmatrix}$

Based on the above conversion, grid voltage is broken up into the sum of positive sequence voltage and negative sequence voltage.

3.1.2 Decoupling of dual synchronous reference coordinate system phase-locked loop

Under the condition of non-ideal grid, since grid voltage has negative sequence component, if phase-locked loop directly collects positive sequence component of voltage as feedback quantity for phase lock, it would be disturbed by negative sequence voltage and thus cause failure of phase lock, thus the essay adopted decoupling of dual synchronous reference coordinate system to extract independent positive sequence q axis voltage component for phase lock, and its control block diagram is as shown in figure 4.

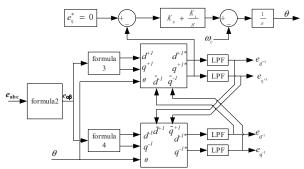


Fig.4. Decoupling of dual synchronous reference coordinate system phase-locked loop control

3.2 Control strategy in non-ideal grid

To realize the control target of three-phase gridconnected current balance, the essay improved the traditional double closed loop control strategy for voltage current and restrained negative-sequence current^[7].

Under the condition of voltage unbalance, according to the above passage, three-phase voltage can be broken up into positive sequence voltage and negative sequence voltage. According to formula (3) and (4), active and inactive power in the dq coordinate system can be obtained, and its formula is:

$$\begin{cases} P_{0} = \frac{3}{2} (e_{d}^{+} i_{d}^{+} + e_{q}^{+} i_{q}^{+} + e_{d}^{-} i_{d}^{-} + e_{q}^{-} i_{q}^{-}) \\ P_{c2} = \frac{3}{2} (e_{d}^{+} i_{d}^{-} + e_{q}^{-} i_{q}^{+} + e_{d}^{+} i_{d}^{-} + e_{q}^{-} i_{q}^{+}) \\ P_{s2} = \frac{3}{2} (e_{q}^{-} i_{d}^{+} - e_{d}^{-} i_{q}^{+} - e_{q}^{+} i_{d}^{-} + e_{d}^{+} i_{q}^{-}) \\ Q_{0} = \frac{3}{2} (e_{q}^{+} i_{d}^{+} - e_{d}^{+} i_{q}^{+} + e_{q}^{-} i_{d}^{-} - e_{d}^{-} i_{q}^{-}) \\ Q_{c2} = \frac{3}{2} (e_{q}^{+} i_{d}^{-} + e_{d}^{-} i_{q}^{+} - e_{d}^{+} i_{q}^{-} - e_{d}^{-} i_{q}^{+}) \\ Q_{s2} = \frac{3}{2} (e_{q}^{+} i_{q}^{-} - e_{d}^{-} i_{d}^{+} + e_{d}^{+} i_{d}^{-} - e_{d}^{-} i_{q}^{+}) \end{cases}$$

Then, if
$$i_{d}^{-}=0$$
, $i_{q}^{-}=0$,
$$\begin{cases}
P_{0}^{*}=1.5(e_{d}^{+}i_{d}^{+}+e_{q}^{+}i_{q}^{+}) \\
Q_{0}^{*}=1.5(e_{d}^{-}i_{d}^{+}-e_{d}^{+}i_{q}^{+})
\end{cases}$$
(6)

Since changes of DC bus is related to active power, under double loop control, orders of active power can be given by external voltage loop, and the corresponding formula is:

$$P_0^* = \frac{3}{2} \left[(K_p + \frac{K_i}{s})(U_{dc}^* - U_{dc}) \right] e_d^+$$
 (7)

In formula (7), Kp and Ki are proportion and integral coefficient of PI regulator respectively; and $U_{\rm dc}^*$ is the given DC bus voltage. Thus, through the calculating formula of power, instruction value of current is:

$$\begin{bmatrix} i_{d}^{+*} \\ i_{q}^{+*} \end{bmatrix} = \frac{2}{3} \times \frac{1}{(e_{d}^{+})^{2} + (e_{q}^{+})^{2}} \begin{bmatrix} e_{d}^{+} & e_{q}^{+} \\ e_{q}^{+} & -e_{d}^{+} \end{bmatrix} \begin{bmatrix} P_{0}^{*} \\ Q_{0}^{*} \end{bmatrix}$$
(8)

After obtaining i_d^+ and i_q^+ , input it into the control system as a given current loop, and the specific control block diagram is shown in figure 5.

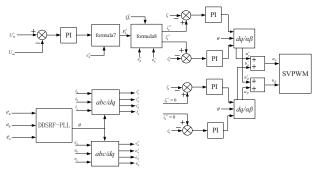


Fig. 5. The control strategy to restrain grid-connected negative-sequence current component

In figure 5, through separation of positive and negative sequence, three-phase voltage and current can be broken up into $e_{\rm q}^+$, $e_{\rm d}^-$, $e_{\rm q}^-$, $i_{\rm d}^+$, $i_{\rm q}^+$, $i_{\rm d}^-$ and $i_{\rm q}^-$. And through calculation of external voltage output, the given value of positive sequence current of the internal loop can be obtained, and the given value of negative sequence current is 0. Then, through closed-loop adjustment with PI regulators, negative sequence current can be adjusted into 0, thus restraining negative sequence current of devices and realizing three-phase balance of output current under the condition of grid voltage unbalance.

IV. SIMULATION AND EXPERIMENTAL VERIFICATION

4.1 Simulated waveforms under the condition of grid unbalance

Constructing a simulation platform in simulink, when simulation condition is 0.1s, A-phase voltage will fall to 92% of the rated value, B-phase will remain unchanged, and C-phase will rise to 108% of the rated value. 1s later, grid will get right, and simulated waveforms are as shown in figure 6.

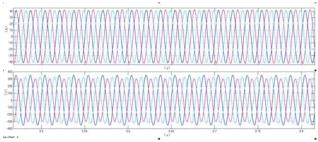


Fig. 6. Waveforms without restraining negative sequence current

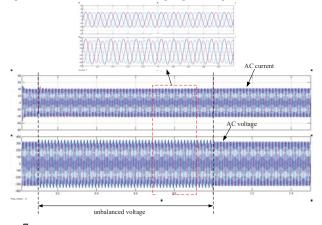


Fig. 7. Waveforms after restraining negative sequence current

In the above figure, figure 6 shows the condition of not adding unbalance control strategy and figure 7 shows the condition of adding unbalance control strategy. According to the figures, we can know that under the condition of not adding unbalance control, voltage is at the state of unbalance and AC side current is also out of balance; while after adding unbalance control, under the condition of voltage unbalance, AC current could still maintain the balance but negative sequence current is totally restrained.

4.2 Control experiment of grid voltage unbalance

Based on the above control strategy, experiment verification is carried out. The experiment condition is that DC current is 200V, DC bus is 400V, AC current voltage

output is 200V and DC side current is 20A. In the experiment, devices are first networked normally, but later at t1, a-phase voltage would be 0.92 times as big as the rated value, c-phase voltage would be 1.08 times as big as the rated value, and b-phase voltage would remain unchanged. If unbalance control strategy is not added, waveforms as shown in figure 8 can be obtained.

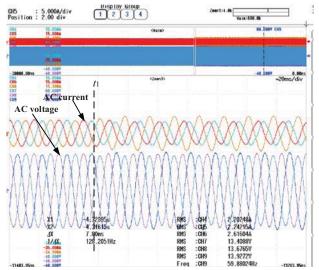


Fig. 8. Experiment waveforms without adding unbalance strategy

According to figure 8, we can see that under the condition of not adding control strategy, when grid voltage is out of balance, if current is not controlled, it is easy to cause AC side over-current of devices and thus cause failures and breakdown, and even damage the devices.

Later, after adding the control strategy in non-ideal grid, the situation of voltage unbalance maintain consistent with that of figure 8, and the waveforms shown in figure 9 can be obtained.

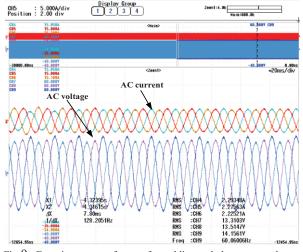


Fig.9. Experiment waveforms after adding unbalance control strategy

From figure 9, we can see that after adding unbalance control strategy, AC current three-phase of the devices is balanced and the devices can operate normally, thus proving that the unbalance control strategy is valid.

V. CONCLUSION

Based on the topological structure of dual-stage T-type three-level PCS, the essay put forward a control strategy under the condition of non-ideal grid which could control devices under unbalanced voltage by restraining negative sequence current. And at last, it proved that the strategy could make PCS do not have disconnected operation and realize balanced output of grid-connected current under the condition when three-phase grid voltage is out of balance or has failures.

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