

Hardware Design of a 13.8-kV/3-MVA PV Plus Storage Solid-State Transformer (PVS-SST)

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Abstract—Photovoltaic (PV) power generation plant with integrated battery energy storage (BES) is becoming increasingly attractive and necessary as the PV penetration increases. Traditional solutions involve two paralleled inverter systems at the same site. This increases the balance of the system cost and the control complexity. Furthermore, high-power step-up transformers are needed to connect to the distribution grid, further increasing the capital cost, land use, and installation cost. Combining PV and BES into a single inverter system without the 60-Hz step-up transformer is, therefore, very attractive as the next-generation technology for utility-scale solar. This effectively calls for the development of a PV+BES solid-state transformer (PVS-SST). This article proposes a 13.8-kV/3-MVA PVS-SST targeting a 13.8-kV grid connection on the ac side and a 1500-V PV farm on the dc side. The PVS-SST utilizes a modular SST concept with a total of 27 SiC submodules. Each submodule is based on 1700-V SiC power MOSFET devices and single-stage dual-active-bridge (DAB)-based dc/ac power conversion technology. In order to utilize the inevitable parasitic capacitances in the actual hardware, a novel turn-off loss model is proposed and experimentally verified. A comprehensive optimization strategy, including the proposed novel turn-off loss model, ZVS range, dead-time calculation, and minimum circulation current, is proposed. The medium-frequency transformer (MFT) design to achieve very high efficiency and isolation voltage is a grand challenge in the proposed PVS-SST and is discussed in detail. The power density of the SiC power submodule is 1.6 MW/m³ (26 W/inch³). The PVS-SST control architecture is discussed with a focus on voltage balancing and real and reactive power controls.

Index Terms—Battery energy storage (BES), dual active bridge (DAB), medium-frequency transformer (MFT) photovoltaic (PV) inverter, SiC MOSFET, solid-state transformer (SST).

I. INTRODUCTION

SOLAR energy is the fastest growing energy around the world due to the rapidly decreasing photovoltaic (PV) panel price [1]. Fig. 1 shows the traditional architecture of

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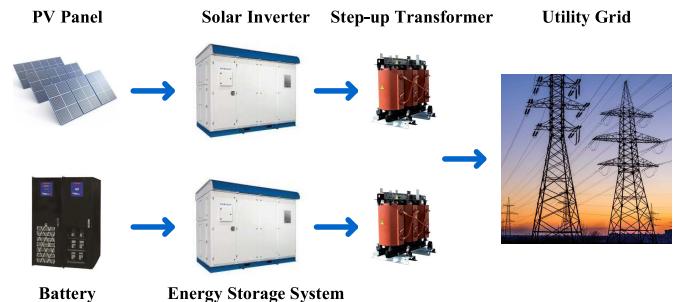


Fig. 1. Typical ac coupled utility-scale PV + energy storage system.

a utility-scale PV farm. Typically, it consists of PV panels, a central solar inverter, and a bulky line frequency transformer (LFT). The central inverter is a nonisolated dc/ac inverter and is tasked with maximum power point tracking (MPPT) and producing a high-quality ac output current. The inverter output voltage is further stepped up to the distribution grid voltage, such as 13.8 kV, through the LFT. Not only this approach is bulky and less efficient but also the additional cost associated with the installation and cabling of the LFT is also a significant part of the balance of system (BOS) cost [2], [3]. For a 3-MVA/600-V PV inverter, lower voltage cables carrying close to 3000 A are needed to connect the PV inverter with the LFT. The cost for an LFT ranges from \$40 to \$100/kVA depending on the size of the transformer. To address the PV power intermittence issue and the mismatch between solar energy production and demand, an increasingly ac coupled energy storage system is installed, as shown in Fig. 1. In this traditional ac coupled PV plus storage architecture, the overall BOS cost is increased due to the use of two inverters and two LFTs. Power conversion efficiency is also lower due to the need to process twice the power from dc to ac.

A medium-voltage solid-state transformer (SST) [4], [5] is proposed as a key technology of the future to replace the LFT and provide advanced grid supporting functionalities. Many medium-voltage SSTs have been developed and demonstrated. Table I summarizes a few reported medium-voltage SST prototypes. SiC power MOSFETs with different voltage ratings are used in many of these prototypes [6], [12]–[18]. In order to connect to the medium-voltage ac grid, most of the proposed solutions utilize a series-connected modular converters on the ac side. Some exceptions are the medium-voltage

TABLE I
PERFORMANCES' COMPARISON OF THE REPORTED SST PROTOTYPES

	Power Rating	AC Grid Voltage	Topology	Power Device	Low Voltage	Switching Frequency	Power Density	Efficiency
GE 2011 [6]	1MW	13.8kV	N.A.	10kV SiC MOSFET	465Vac	20kHz	N.A.	97%
ALSTOM 2007 [7]	1.5MW	15kV	Full bridge (two-stage)	6.5kV IGBT	1650Vdc	5kHz	7.6W/inch ³	N.A.
Bombardier 2007 [8]	3MW	15kV	SR Full bridge (two-stage)	4.5kV IGBT	2800Vdc	8kHz	28.5W/inch ³	N.A.
ABB 2014 [9]	1.2MW	15kV	SR Full bridge (two-stage)	6.5kV IGBT	3600Vdc	1.8kHz	N.A.	96%
FREEDM 2014 [10]	10kVA	3.6kV	DAB (three-stage)	6.5kV IGBT	120Vac	10.8kHz	0.5W/inch ³	92%
FREEDM 2015 [11]	100kVA	13.8kV	FEC+DAB (three-stage)	15kV SiC IGBT	480Vac	3~10kHz	N.A.	96.75%
EPRI 2016 [12]	25kW	15kV	AFe (two-stage)	1.2kV SiC MOSFET	240Vac	93kHz	N.A.	97.5%
FREEDM 2020 [13][14]	N.A.	4.16kV	FEC+DAB (two-stage)	10kV SiC MOSFET	480Vac	20kHz	N.A.	N.A.
GE & CPES 2019 [15]	50kVA	6kV	SR Full-bridge (three-stage)	1.7kV SiC MOSFET	690Vac	180kHz	N.A.	98%
FREEDM 2018 [16]	12kVA	7.2kV	SR Half-bridge (single-stage)	15kV SiC MOSFET	240Vac	37kHz	8.3W/inch ³	97.8%
ETH 2017 [17]	25kW	6.6kV	IFE (single-stage)	1.7kV SiC MOSFET	400Vdc	50kHz	24W/inch ³	97.5%
XJTU & TEBA 2019 [18]	1MW	10kV	DAB (single-stage)	1.2kV SiC MOSFET	800Vdc	20kHz	N.A.	<98%
[This paper] UT Austin 2020	3MVA	13.8kV	DAB (single-stage)	1.7kV SiC MOSFET	1500Vdc	15~60kHz	26W/inch ³	>98%

SSTs reported in [11], [13], and [14], which utilizes high blocking voltage SiC devices (10 or 15 kV) without converter series connection. Power conversion from the ac grid to the low-voltage side typically utilizes two-stage (for low-voltage dc output) or three-stage (for low-voltage ac output) topology with galvanic isolation. These solutions have a dc link bus located on the high-voltage side, which is useful to implement smart grid functions, such as reactive power support [7]–[15]. However, the major issues of these approaches are the reduced efficiency, power density, and reliability due to multiple power conversion stages and bulky dc-link capacitors. For this reason, a few reported works focus on the single-stage topology to improve the power conversion efficiency and power density [16]–[18].

Therefore, to improve the efficiency and power density, the proposed PV plus storage SST (PVS-SST) utilizes a single-stage dual-active-bridge (DAB) conversion topology with PV and battery energy storage (BES) connected at the low-voltage dc side and an advanced newly developed 1700-V SiC power MOSFET. In order to directly connect to the 13.8-kV distribution grid, the ac side utilizes a modular converter architecture in which multiple lower voltage submodules are connected in series to share the voltage and power [19], [20]. Each modular converter achieves required galvanic isolation through a medium-frequency transformer (MFT), which plays a critical role in determining the system isolation, efficiency, power density, and thermal performance [21], [22].

The circuit diagram of the proposed PVS-SST is shown in Fig. 2. The PV power is converted directly to 13.8 kV through a single dc-to-ac conversion stage. The battery can be charged directly by the dc power from the PV or from the

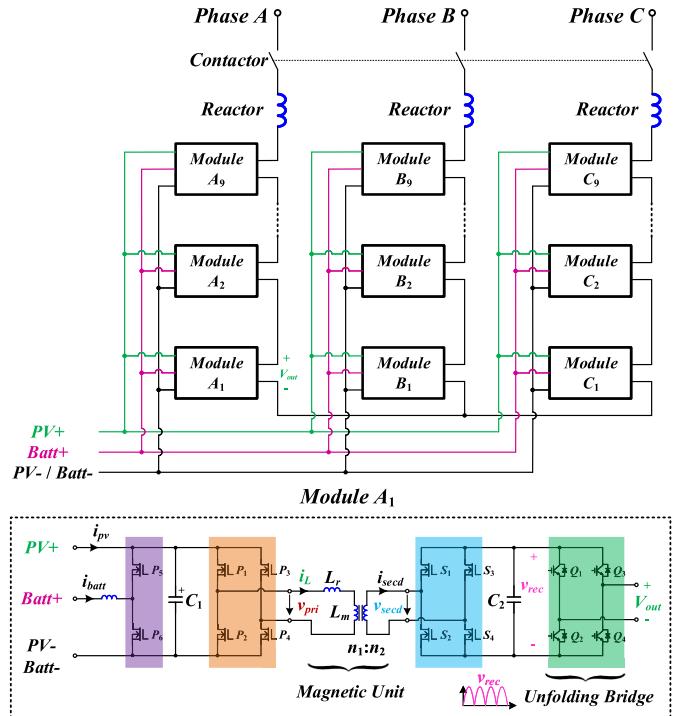


Fig. 2. Circuit diagram of the proposed 13.8-kV/3-MVA PVS-SST.

ac grid. Therefore, the PVS-SST is basically a dc-coupled PV plus storage system without a 60-Hz transformer. The galvanic isolation and voltage step-up are performed by the PVS-SST directly. The high ac output voltage is obtained by a series connection of a number of converter modules on the ac side, while the dc side is in parallel. A high-voltage BES system

TABLE II
SPECIFICATIONS OF THE PROPOSED UTILITY-SCALE PVS-SST

Symbol	Description	Value
V_s	System line to line voltage	13.8kV
P_o	Rated power capacity	3MVA
I_o	Rated output current	125A
V_{PV}	PV MPPT voltage range	900 ~ 1300V
I_{PV}	PV input current	2000 ~ 3300A
V_{Batt}	Battery voltage	504 ~ 907V
P_{Batt}	Battery energy capacity	800kWh
I_{Batt}	Maximum charging current (5C)	200A
f_s	SiC switching frequency	20 ~ 100kHz
η	Expected efficiency (PV to grid)	> 98%

is connected to the 1500-V PV bus through a boost converter. In the proposed 13.8-kV/3-MVA PVS-SST design, 27 modular converter modules (nine modules per phase and 111-kVA per module) are needed. The modular converter topology is a single-stage DAB-based dc/ac converter using 1700-V SiC MOSFET. The half-sine output voltage v_{rec} is converted to a full sine wave by a silicon IGBT unfolding bridge. Table II summarizes the key specifications of the PVS-SST targeting 1500-V PV application and 13.8-kV grid connection in the Y-configuration.

The article primarily focuses on the hardware design and optimization strategy, including high-density power stage, medium-voltage isolated MFT, and 13.8-kV modular converter [input-parallel-output-series (IPOS)] system architecture. In Section II, an evaluation of using 1700-V SiC devices for 1500-V applications together with a quantitative turn-off voltage spike prediction model based on an optimized PCB busbar design is discussed. Section III proposes a novel turn-off loss model for accurate loss estimation and presents experimental verification. Section IV focuses on the MFT design methodology and optimization. Section V discusses a comprehensive efficiency optimization strategy based on the proposed novel turn-off loss model, including the ZVS range, the dead-time calculation, and the minimum circulation current. In order to apply the proposed SiC modular converter into a 13.8-kV/3-MVA prototype, Section VI discusses the whole PVS-SST system architecture and one worst case scenario simulation result. Section VII presents the experimental verifications of the proposed PVS-SST submodule. The 13.8-kV/3-MVA prototype is under construction for further system-level experimental verification.

II. 1700-V SiC MOSFET POWER MODULE

Low switching loss SiC power MOSFET and GaN HFET are two emerging power device technologies that enable efficient power converters with compact sizes [23], [24]. For high-power applications, a number of SiC power modules are now available for MW applications [25], [26]. For the proposed PVS-SST, a newly developed 1700-V SiC MOSFET half-bridge module from Wolfspeed®, as shown in Fig. 3, is used due to its ultralow loop inductance (7 nH) and low ON-resistance (2.5 mΩ). For a 1500-V PV inverter system, the MPPT voltage is in the range of 900–1300 V. The low loop inductance, together with proper bus bar design, can ensure the device voltage overshoot less than 1450 V at the highest

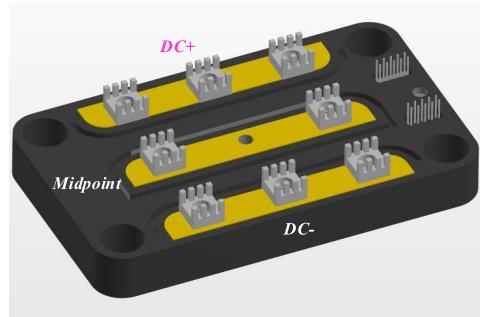
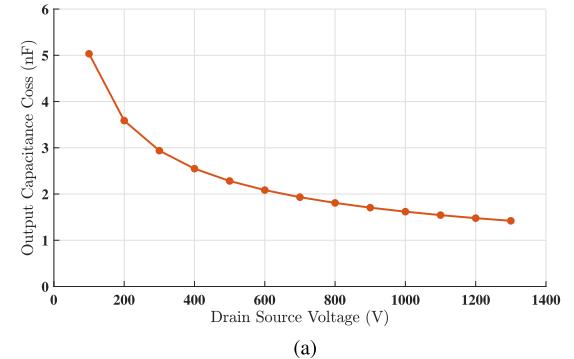
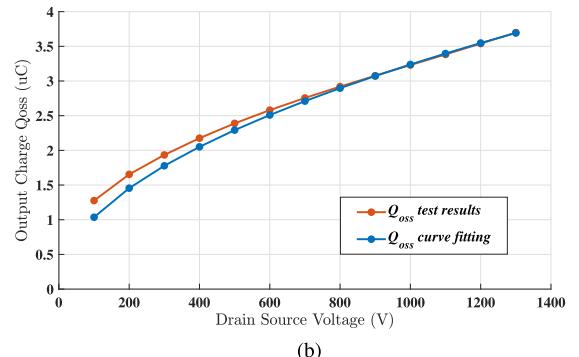


Fig. 3. 1700-V SiC power MOSFET half bridge module from Wolfspeed.



(a)



(b)

Fig. 4. Measured C_{oss}/Q_{oss} results for the 1700-V SiC MOSFET module. (a) Output capacitance C_{oss} . (b) Output capacitance Q_{oss} .

turn-off current. The power module also has a very low thermal resistance $R_{th, jc} = 0.068 \text{ }^{\circ}\text{C/W}$ and a high temperature housing allowing $T_{j,\max} = 175 \text{ }^{\circ}\text{C}$ operation. The low drain-source ON-resistance and excellent heat dissipation capability result in a device current handling of 393 A at $T_c = 125 \text{ }^{\circ}\text{C}$ and $T_j = 175 \text{ }^{\circ}\text{C}$. This ensures that the forced air cool can be used for the 111-kVA modular converter.

A. C_{oss}/Q_{oss} Extraction

The proposed DAB dc/ac converter has wide input (MPPT range) and output (half sine waves) ranges. Due to the nonlinearity of MOSFET's C_{oss}/Q_{oss} versus the drain-source voltage, the zero-voltage switching (ZVS) conditions for the primary dc side and the secondary ac side are more complicated than that of a dc-dc converter. Besides, even though the device turn-on loss is eliminated through ZVS, the accurate turn-off loss and the dead-time loss still depend on the device output capacitance. Therefore, an accurate C_{oss}/Q_{oss} model

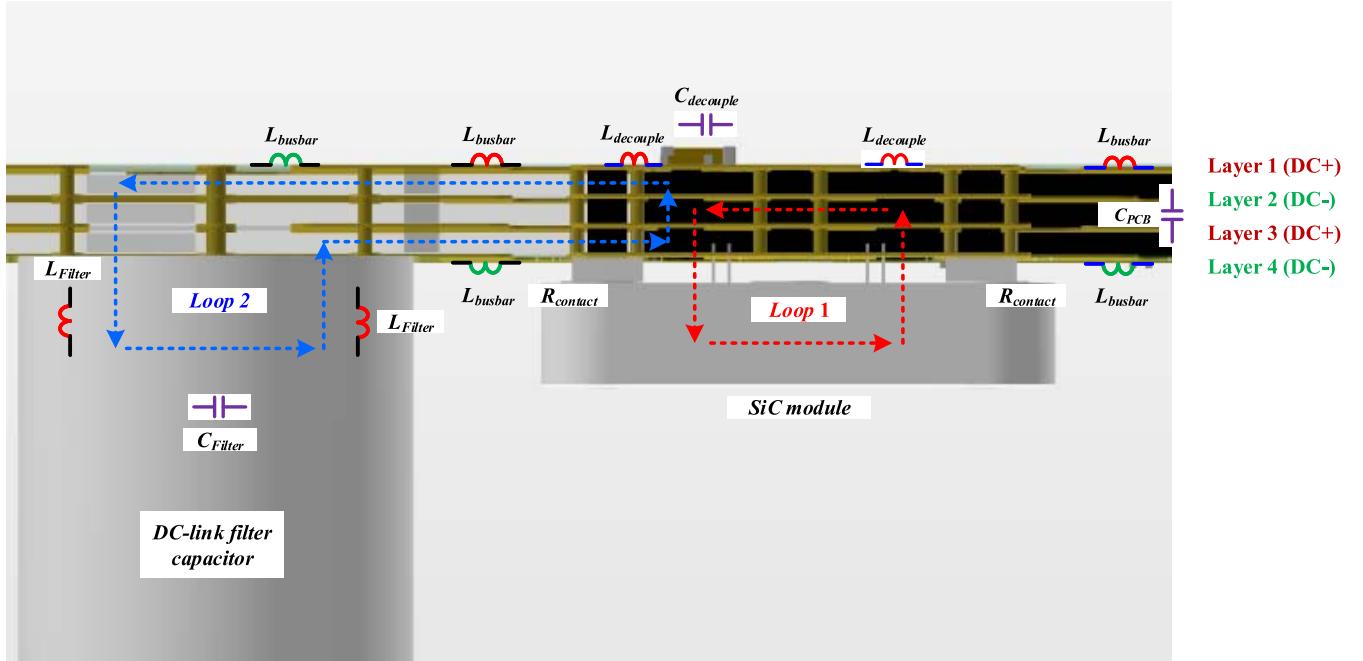


Fig. 5. Optimized PCB-based busbar layout of the SiC converter.

is needed to ensure ZVS and estimate the converter total loss. The C_{oss}/Q_{oss} model extraction results of the 1700-V SiC MOSFET using a novel test circuit [27] are shown in Fig. 4.

B. Turn-Off Voltage Overshoot Prediction

In order to evaluate the feasibility of using 1700-V SiC devices for 1500-V applications, the mechanism of how the optimized PCB-based busbar reduces the voltage overshoot is needed. For simplicity, the lossless MOSFET channel model is adopted to replicate the turn-off voltage oscillation, which could guide the practical PCB copper trace layout.

Fig. 5 shows the PCB-based busbar design. To reduce the length of the commutation loop, the middle terminal of the midpoint is eliminated (see Fig. 3), and high-frequency decoupling capacitors are placed there instead to fully utilize the effective area close to the SiC module. A sandwich structure of PCB copper trace is adopted to get a higher parasitic capacitance between dc links. Fig. 6 shows the circuit model of the PCB-based busbar. To simplify the analysis of how the PCB busbar and the decoupling capacitor $C_{decouple}$ reduce the voltage spike across the turning-off device, assuming that the voltage across the decoupling capacitors $v_{cap}(t)$ keep constant when analyzing the commutation loop 1 is appropriate since the resonant frequency of loop 1 is much higher than that of loop 2. The theoretical voltage across the outside drain and source terminal $v_{ds,out}(t)$ and across the inside die $v_{ds,in}(t)$ of the turning-off device can be calculated using (21)–(31), as shown in Appendix A. Here, $V_{OS,loop1}$ is the high-frequency component peak value of the loop 1, $V_{OS,loop2}$ is the high-frequency component peak value of the loop 2, and t_1 and $t_2 = t_1 + t_{off}$ are the time constants from Section III (the novel turn-off loss model). Part of the values in equations is extracted from the ANSYS/Q3D simulation [28].

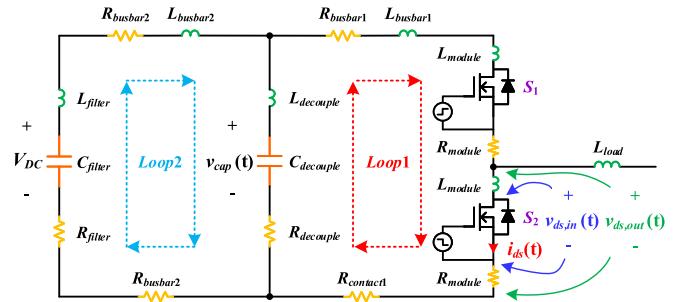


Fig. 6. Circuit model of the optimized PCB-based busbar.

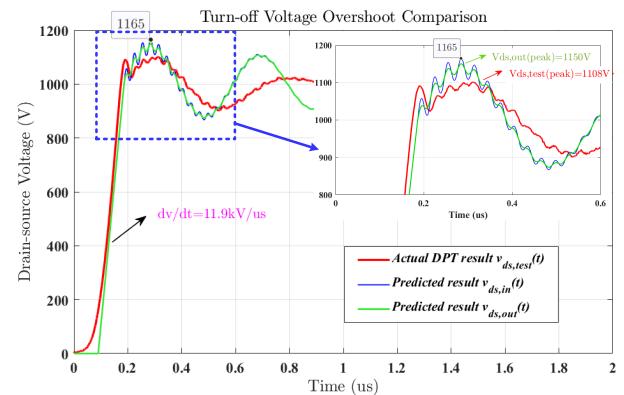


Fig. 7. 1-kV/255-A turn-off voltage overshoot comparison.

Fig. 7 shows the theoretical $v_{ds,in}(t)$ and $v_{ds,out}(t)$ calculated from (21)–(31) in Appendix A and the actual test result $v_{ds,test}(t)$ across the outside drain–source terminal under 1 kV/255 A. Due to the loop inductance inside the device, the actual voltage spike across the MOSFET dies inside the module is always higher than the measured voltage overshoot across the device outside terminals. The peak drain–source terminal voltage was observed as 1108 V from the waveform

of $v_{ds,test}(t)$ at $11.9 \text{ kV}/\mu\text{s}$. The calculated voltage spike across the drain–source terminals outside the device is 1150 V. After taking the internal L_{module} of the device into consideration, the actual voltage across the MOSFET dies is 1166 V. The voltage spike difference between the outside terminals and inside dies is around 16 V. Therefore, the prediction model and the test results suggest that around $76 \text{ V} = (200 - 108 - 16) \text{ V}$ margin can be guaranteed under 1.5-kV/250-A hard turn-off condition. The waveforms of $v_{ds,test}(t)$ enable to measure the typical value of dv/dt as $11.9 \text{ kV}/\mu\text{s}$. This value would be lower when the snubber capacitor is connected between the drain and source terminals. Compared to the traditional laminated busbar [50], the optimized PCB busbar significantly reduced the overshoot voltage across the device and enable a faster turn-off transient, which determines a lower switching loss. Therefore, the proposed voltage overshoot prediction model validates the design of using 1700-V SiC modules in 1500-V applications.

III. NOVEL TURN-OFF LOSS MODEL

One of the main drawbacks of a nonresonant DAB-based converter is the high turn-off current introduced by its trapezoidal transformer current waveform. During the turn-off transient, multiple capacitances make impacts upon the actual current flowing through the MOSFET channel, such as the turning-off MOSFET/body-diode output capacitance, the free-wheeling MOSFET/body-diode output capacitance, the parasitic capacitance of magnetic components, and external snubber capacitance across the MOSFET. In order to obtain insight into how the total equivalent capacitors influence the turn-off loss, a more accurate turn-off loss model is needed.

A. Turn-Off Transient Analysis

Fig. 8(a) shows the typical waveforms of MOSFET during turn-off. For simplicity, the drain voltage (v_{ds}) begins to increase linearly at time t_1 , but the drain current (i_{ds}) remains constant at I_{dc} . Part of the current is used to charge the output capacitance (C_{gd} and C_{ds}), and part of them flows through the channel i_{ch} . The channel current is responsible for the turn-off loss. From time t_1 to t_2 , the channel current is given by [10]

$$i_{ch}(t) = g_m \cdot (V_{GP} - V_{TH}) \quad (1)$$

where V_{GP} is the plateau voltage, V_{TH} is the gate threshold voltage, and g_m is the device transconductance. Between time t_1 and time t_2 , a drain-to-gate current i_{GP} charges the gate–drain capacitance C_{gd} , the drain voltage increases at an almost fixed rate, and the plateau voltage is given by

$$V_{GP} = R_g \left\{ C_{GD,av} \frac{dv_{ds}(t)}{dt} \right\} + V_{GS,Low} \quad (2)$$

where R_g is the gate resistance, $V_{GS,Low}$ is the gate voltage at driver input, which is either zero or a negative value during the turn-off, and $C_{GD,av}$ is an assumed constant average value of the gate–drain capacitance (Miller capacitance). Between time t_1 and time t_2 , the channel is modeled as a gate-voltage-controlled current source and the governing equation

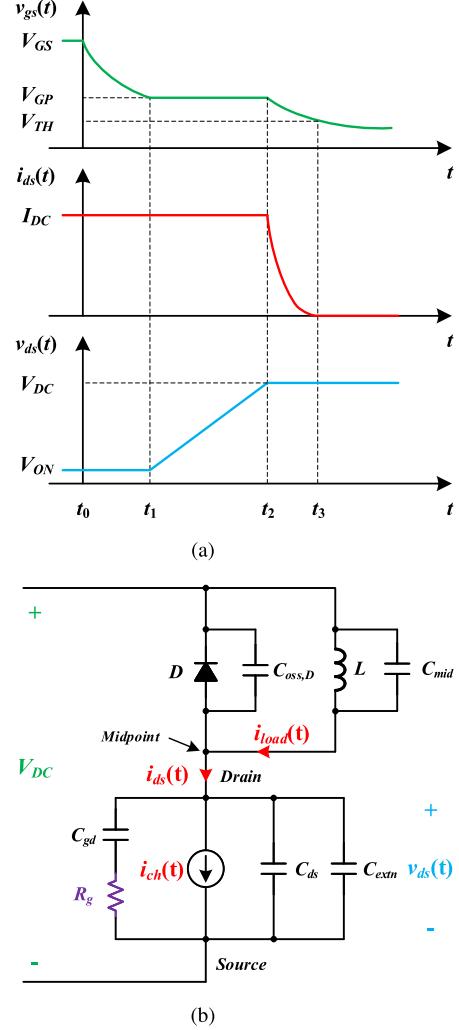


Fig. 8. Turn-off transient analysis of SiC MOSFET. (a) Typical turn-off waveforms. (b) Circuit model during turn-off.

with $v_{ds}(t)$ as the dependent variable is

$$C_{MOS} \frac{dv_{ds}(t)}{dt} + i_{ch}(t) = I_{dc} \quad (3)$$

where C_{MOS} is the total equivalent capacitance of the turning-off power MOSFET, which is given by

$$C_{MOS} = C_{oss,MOS} + C_{oss,D} + C_{mid} + C_{extn} \quad (4)$$

where $C_{oss,MOS}$ is the output capacitance of the turning-off MOSFET, which typically equals to $C_{gd} + C_{ds}$, $C_{oss,D}$ is the free-wheeling MOSFET/body-diode output capacitance, C_{mid} is the equivalent capacitance across the midpoint and dc+ of the circuit model, which typically includes the parasitic capacitance of magnetic components in a practical design, and C_{extn} is the paralleled snubber capacitance across the turning-off MOSFET. Substituting (1)–(4), the above equations can be solved as

$$v_{ds}(t) = \frac{I_{dc} + g_m V_{TH}}{C_{MOS} + g_m R_g C_{GD,av}} t. \quad (5)$$

At time t_2 , the load current begins to transfer from the MOSFET to the freewheeling diode. Between time t_2 and time t_3 , the drain–source voltage remains constant at V_{DC} , and the

TABLE III
CURVE FITTING COEFFICIENTS OF THE TURN-OFF LOSS MODEL

Symbol	Value
K_1	8.6
K_2	0.0039
K_3	-7.4
K_4	-2.618×10^5
K_5	1.765×10^{-8}

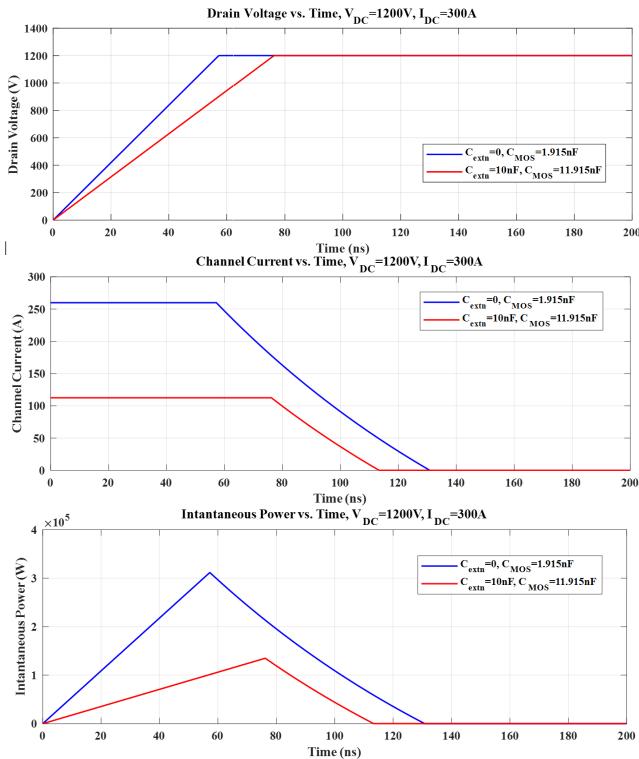


Fig. 9. Turn-off waveforms and instantaneous power loss curve.

gate current discharges the gate–source capacitance; therefore, the channel current follows the gate voltage until it reached zero at time t_3 when V_{gs} reaches V_{TH}

$$i_{ch}(t) = g_m \left[(V_{GP} - V_{GS,low}) e^{-\frac{t-t_2}{R_g C_{gs}}} - V_{TH} \right] \quad (6)$$

where C_{gs} is the gate–source capacitance. Therefore, the power loss dissipated in the MOSFET channel is

$$P_{loss}(t) = v_{ds}(t) \cdot i_{ch}(t). \quad (7)$$

Fig. 9 shows the turn-off waveforms and instantaneous power loss curves with different snubber capacitances under $V_{dc} = 1200$ V and $I_{dc} = 300$ A. The average loss during one turn-off without snubber capacitors is 19.3 mJ. Contrarily, the average loss with 10-nF snubber capacitors has decreased by 61% to 7.5 mJ. With larger C_{extn} , the turn-off loss can be reduced to close to zero at the expense of a much longer turn-off time. Due to the ZVS turn-on capability of DAB, the energy stored in the snubber capacitors during turn-off transient will be transferred to the load or source in the next switching cycle. Experimental verification under the dc/dc mode is detailed in the paper [28].

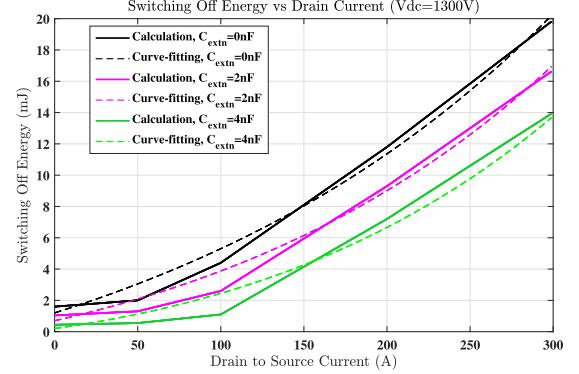


Fig. 10. Turn-off energy model versus drain–source current.

B. Curve-Fitting Turn-Off Loss Model

Using the proposed novel turn-off loss model, Fig. 10 shows the calculated turn-off energy loss E_{off} of the 1700-V SiC MOSFET versus drain current I_{ds} . A curve fitting equation is further developed to allow the use of a turn-off loss model for converter optimization. The curve fitting result is given by

$$E_{off}(V_{ds}, I_{ds}) = K_1 e^{K_2 I_{ds}} + K_3 + C_{MOS} K_4 (e^{K_5 I_{ds}} - 1) \quad (8)$$

where K_1 – K_5 are the curve fitting coefficients. For the 1700-V SiC module, Table I lists the values of K_1 – K_5 .

With larger C_{MOS} , the turn-off loss can be reduced to close to zero at the expense of much longer turn-off time due to the slow dV/dt . The minimum $(dV/dt)_{min}$ occurs when (6) equals to zero. Keep increasing C_{MOS} beyond this point is useless while making the ZVS turn-on harder and required longer dead time. $(dV/dt)_{max}$ corresponds to the case where no external C_{extn} across the drain and source terminal is used. Between $(dV/dt)_{max}$ and $(dV/dt)_{min}$, the turn-off loss is getting lower and lower with increasing C_{MOS} . However, higher C_{MOS} will result in lower turn-off loss, but higher circulation current and higher body-diode conduction losses have resulted from long dead time. Therefore, C_{MOS} optimization is needed and will be detailed in Section V in order to achieve maximum system efficiency under the full-load range.

IV. 200-kVA MFT

For the proposed PVS-SST, each modular converter needs a 111-kVA MFT. The peak power level is 222 kVA due to the dc/ac operation condition. The primary design challenges for the MFT are to balance the competing objectives including reliable electrical insulation, high efficiency, high power density, and superior thermal performance. Especially, for the proposed 13.8-kV PVS-SST, achieving the required high galvanic isolation is a grand challenge that has not been achieved by any designs in prior studies. According to IEEE Std. C57.12.01 insulation standard [30], for a 13.8-kV transformer, the basic lightning insulation test should be at least 60 kV. Within 1.2 μ s, the test voltage should be increased to 100% peak value and gradually go down to 50% of peak value for the next 50 μ s. The second insulation test is the applied voltage test. After the test voltage is increased to 34 kV, the test voltage is held for 60 s, and during this time,



Fig. 11. Prototype picture of the fabricated MFT.

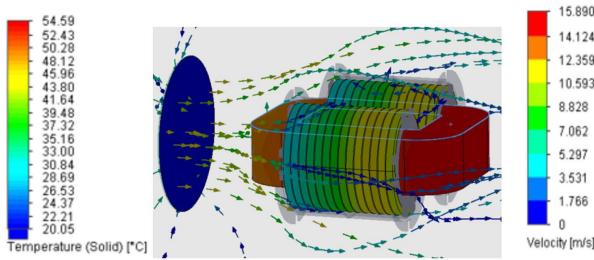


Fig. 12. Fluid thermal simulation of MFT with a 15-m/s airflow.

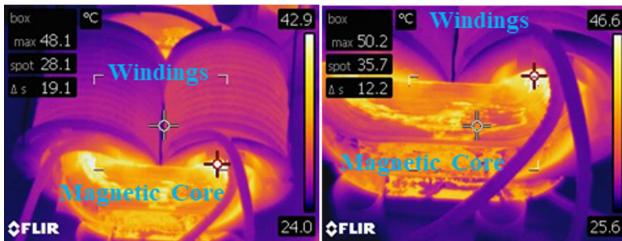


Fig. 13. Thermal test results of the MFT in the DAB dc/dc test at 200 kW.

there should be no flash over, spark over, or puncture. The third insulation test is a partial discharge test. By applying 23.5 kV for 30 s and decreasing to 18 kV for 180 s to the MFT, the maximum acceptable level of partial discharge is 50 pC. To pass the three insulation tests, the clearance and creepage distances between windings and cores need to be carefully designed. Besides, a further concern is a partial discharge at such high voltages; therefore, potting design may be necessary.

A. MFT Thermal Design

Achieving good thermal performance is the major challenge for high-power MFT [32] due to the very unfavorable mechanical structure for heat dissipation in the MFT. Heat sources are winding and core losses. For the proposed PVS-SST, the peak power of the MFT is 222 kVA due to the dc/ac operation characteristic. The first priority is to ensure that the efficiency of the design is very high, so the heat generation is minimized. To achieve superior cooling performance, a novel cooling structure is proposed which utilizes two 3-D-printed bobbins layers, as shown in Fig. 11. The 3-D-printed structure can provide airflow channels for the core and windings.

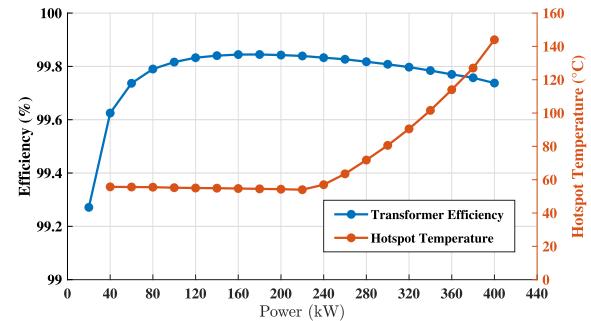


Fig. 14. MFT efficiency and hotspot temperature estimation.

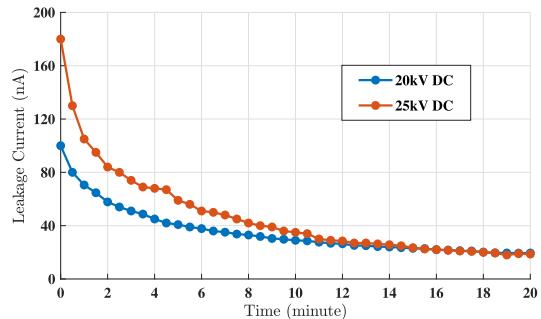


Fig. 15. DC insulation test of the developed MFT.

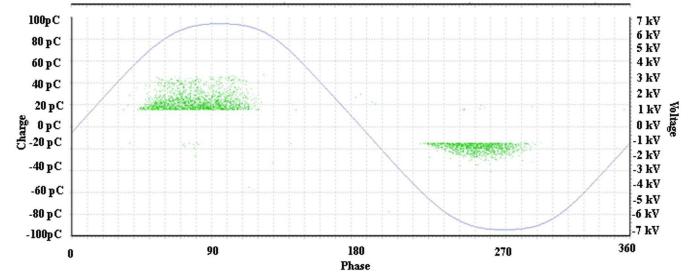


Fig. 16. PD pattern diagram at 8 kV/60 Hz (5-min test data).

To illustrate the effectiveness of the proposed cooling system, a 3-D thermal simulation is conducted with the forced air-cooling condition, as shown in Fig. 12. The MFT hotspot temperature is around 54 °C, which matches well with the 200-kW experimental results, as shown in Fig. 13. Fig. 14 shows the calculated MFT efficiency and hotspot temperature at power ratings up to 400 kW. The hotspot is at the inner windings, and it rises rapidly at higher power levels. The designed MFT can safely operate at 340 kW with a steady-state hotspot temperature lower than 100 °C.

B. Insulation Design

For the parallel-concentric winding structure shown in Fig. 11, the well-coupled layout of the primary and secondary windings creates a challenge for achieving good electrical insulation [33]. To address this issue, a new insulation structure is proposed, which utilizes two 3-D-printed bobbins layers separated by an air channel. The new design has passed 8-kV PD and 25-kV dc insulation test, as shown in Figs. 15 and 16. These results indicate that the developed MFT is capable of the 13.8-kV operation condition (grid peak

voltage is 11.2 kV due to the Y-configuration), but it has not met the IEEE standard requirements. Additional research and development are needed to meet the grand challenge targets for insulation while balancing the needs for compact size and high efficiency.

V. 111-kVA SUBMODULE EFFICIENCY OPTIMIZATION

The proposed PVS-SST is a modular SST where 27 identical power modules are connected in IPOS configuration, as shown in Fig. 2. Each power module has the same efficiency performance as the whole system. The DAB topology is selected due to its inherent ZVS and buck-boost operation capabilities. Single- or dual-phase shift can be used to achieve the required modulation [34], [35]. The ZVS conditions for DAB converter under dc/ac mode are more complicated than that under the dc/dc mode due to the half-sine voltage across the ac-link capacitors. Besides, one drawback of the DAB converter is the high turn-off loss when the current and switching frequency are high. The turn-off loss can become the dominant loss at heavy load (HL). In addition, many studies have reported that the transformer circulation current is one major concern for the DAB [36], [37].

Therefore, in order to obtain high efficiency, a comprehensive optimization strategy, including ZVS range, dead-time calculation, accurate turn-off loss estimation, and minimum circulation current, is needed.

A. Accurate MOSFET Turn-Off Loss Estimation

In a practical design, an additional snubber capacitor C_{ext} can be placed in parallel with the MOSFET to further reduce the turn-off loss. The proposed novel turn-off loss model, as shown in (8), is adopted to estimate the turn-off loss.

For the newly developed 1700-V SiC module, Table III lists the values of K_1-K_5 . The curves of $C_{\text{oss,MOS}}$ and $Q_{\text{oss,MOS}}$ versus drain-source voltage are extracted from the test in Section II. C_{mid} typically includes the parasitic capacitance of the DAB inductor and the MFT. C_{mid} is the equivalent parasitic capacitance across the switch nodes of the half-bridge that must be charged from V_{dc} to $-V_{\text{dc}}$ (secondary ac side) or V_{dc} to 0 (primary dc side). The dual-phase-shift (DPS) modulation is adopted in the optimization strategy, which means that only the dc side has zero-level voltage output. Therefore, there are totally two MOSFETs turning off at the same time for the ac side full bridge and one MOSFET turning off for the dc side.

B. Transformer Circulation Current

The simplest modulation strategy of the DAB converter is single phase shift (SPS) [38]. However, SPS will not only cause a high turn-off current and circulation current but also lose ZVS when the voltage gain is away from unity [39]. Therefore, the SPS leads to a reduction in efficiency [40]. Another modulation strategy is the triple-phase shift (TPS), which has three control degrees of freedom. However, it is complex to implement and hard to perform an efficiency optimization [41].

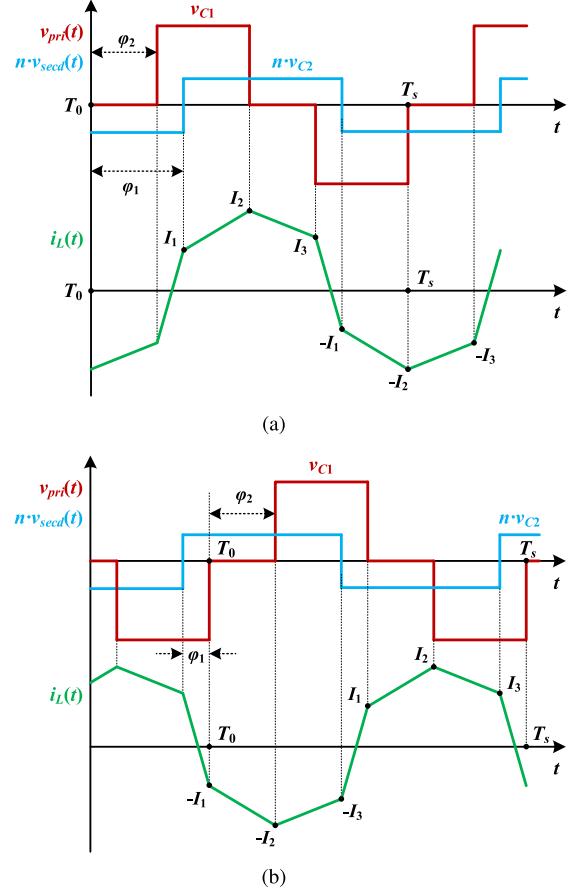


Fig. 17. Typical operating waveform of the DAB inverter with DPS. (a) $P_{\text{DAB}} > 0$, buck mode. (b) $P_{\text{DAB}} < 0$, buck mode.

The DPS modulation is proposed by Zhang and Ruan [42]. Many studies focus on minimizing the circulation current [43], [44]. However, a generalized model to evaluate optimal efficiency at any given condition for both real power and reactive power together with ZVS range, dead-time calculation, and accurate turn-off loss estimation has never been considered in detail.

The proposed PVS-SST adopts DPS modulation. Referring to Fig. 2, the single-stage DAB inverter consists of the primary and secondary side full bridges connected with the MFT. The two full bridges produce phase shifted voltages v_{pri} and v_{secd} , resulting in an inductor current i_L . The ac components of i_L and i_{secd} are rectified by the two active full bridges, leading to net dc currents i_1 and i_2 on both sides. Filter capacitors C_1 and C_2 absorb the high-frequency components of i_1 and i_2 . The rectified ac voltage $v_{\text{rec}}(t)$ is generated on the secondary side capacitor through the DAB inverter, which operates under variable switching frequency of 15–60 kHz. The rectified ac voltage $v_{\text{rec}}(t)$ is connected to the grid through an IGBT unfolding bridge, which switches at 60 Hz. The MFT transformer turns ratio $n = n_1:n_2$ is used in the analysis.

Typical waveforms of the DAB inverter with DPS modulation over one switching cycle are shown in Fig. 17. Here, ϕ_1 is the phase shift between dc and ac sides, and ϕ_2 is the phase shift between the two half-bridge legs of the dc side. $P_{\text{DAB}} > 0$ means the power flows from the dc to ac grids.

Key equations of semiconductor devices, including I_1 , I_2 , I_3 , $I_{P1,\text{rms}}$, and P_{DAB} under two different power flow directions, are listed in Appendix B. To minimize the maximum turn-off current under HL, the partial derivatives of I_2 with respect to φ_1 and φ_2 under different power flow directions are given by (9)–(12). Definitions of variables a , b , c , M , and K under different power flow directions are listed in Appendix C

$$\frac{\partial I_2}{\partial \varphi_1} = 0|_{P_{\text{DAB}}>0} \Rightarrow \varphi_{1,\text{HL}} \quad (9)$$

$$= \begin{cases} \frac{-b + \sqrt{b^2 - 4ac}}{2a} & 0 < M < 0.5 \\ \frac{-b - \sqrt{b^2 - 4ac}}{2a} & M \geq 0.5 \end{cases}$$

$$\varphi_{2,\text{HL}} = \frac{(4\varphi_1 - 1) + \sqrt{(4\varphi_1 - 1)^2 - 8(4\varphi_1^2 - 2\varphi_1 + K)}}{4} \quad (10)$$

$$\frac{\partial I_2}{\partial \varphi_1} = 0|_{P_{\text{DAB}}<0} \Rightarrow \varphi_{1,\text{HL}} = \frac{-b + \sqrt{b^2 - 4ac}}{2a} \quad (11)$$

$$\varphi_{2,\text{HL}} = \begin{cases} \frac{(4\varphi_1 + 1) + \sqrt{(4\varphi_1 + 1)^2 - 8(4\varphi_1^2 + 2\varphi_1 - K)}}{4} & 0 < M < 0.5 \\ \frac{(4\varphi_1 + 1) - \sqrt{(4\varphi_1 + 1)^2 - 8(4\varphi_1^2 + 2\varphi_1 - K)}}{4} & M \geq 0.5 \end{cases} \quad (12)$$

To guarantee ZVS for all switches under light load (LL), the energy stored in the inductor L_r is required to discharge/charge the junction capacitance [45]. Therefore, the ZVS constraints under different power flow directions are given by

$$\varphi_{1,\text{LL}}|_{P_{\text{DAB}}>0} = \frac{4L_\gamma f_s I_{\text{ZVS}} V_N + V_P^2 - V_N^2}{2V_P(V_P + V_N)} \quad (13)$$

$$\varphi_{2,\text{LL}} = \frac{(4\varphi_1 - 1) + \sqrt{(4\varphi_1 - 1)^2 - 8(4\varphi_1^2 - 2\varphi_1 + K)}}{4} \quad (14)$$

$$\varphi_{1,\text{LL}}|_{P_{\text{DAB}}<0} = \frac{4L_\gamma f_s I_{\text{ZVS}} V_N + V_P^2 - V_N^2}{2V_P(V_P + V_N)} \quad (15)$$

$$\varphi_{2,\text{LL}} = \frac{(4\varphi_1 + 1) + \sqrt{(4\varphi_1 + 1)^2 - 8(4\varphi_1^2 + 2\varphi_1 - K)}}{4} \quad (16)$$

C. ZVS Achievement and Dead-Time Calculation

To achieve ZVS for all devices in a full bridge, sufficient transformer current and dead time are required to charge/discharge the four-power MOSFETs' equivalent capacitance $C_{\text{MOS}}/Q_{\text{MOS}}$. By applying energy conservation equation to a full bridge converter before and after the ZVS transition,

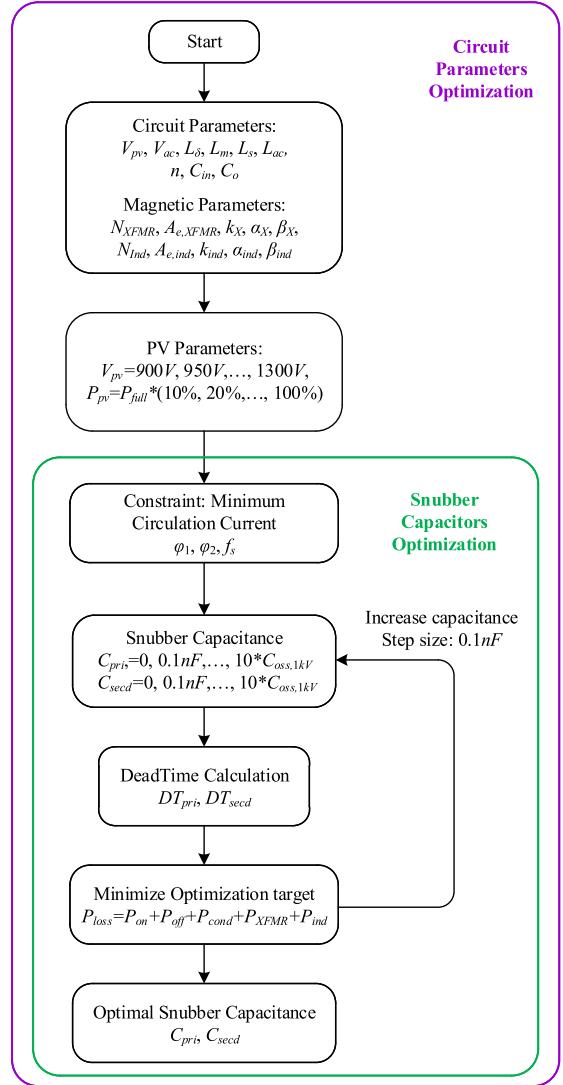


Fig. 18. Flowchart of the comprehensive optimization strategy.

the required ZVS condition from energy point of view is given by

$$\frac{1}{2} L_\gamma I_{\text{ZVS}}^2 \geq m \left[\int V_{\text{ds}} dQ_{\text{oss,MOS}} + \frac{1}{2} (C_{\text{mid}} + C_{\text{extn}}) V_{\text{ds}}^2 \right] \quad (17)$$

where $m = 2$ for the primary dc side and $m = 4$ for the secondary ac side MOSFETs. To avoid partial ZVS, a sufficient dead time is required on the primary dc side

$$\int_{t_{\text{off}}}^{t_{\text{on}}} i_L(t_{\text{off}}) dt \geq Q_{\text{equiv}} \quad (18)$$

$$Q_{\text{equiv}} = 2 [Q_{\text{oss,MOS}}(V_{\text{dc}}) + (C_{\text{mid}} + C_{\text{extn}}) V_{\text{dc}}] \quad (19)$$

where $i_L(t_{\text{off}})$ is the primary side current during the dead-time interval $DT_{\text{pri}} = t_{\text{on}} - t_{\text{off}}$, and Q_{equiv} is the equivalent output charge of the total equivalent capacitance C_{MOS} . A minimum dead time $DT_{\text{min}} = 500$ ns is used in the optimization algorithm to avoid the half bridge short circuit, and a maximum dead time $DT_{\text{max}} = 2 \mu\text{s}$ is used to allow partial ZVS turn on under LL conditions.

Similarly, the required dead time to charge/discharge the total equivalent output capacitance of secondary side is given

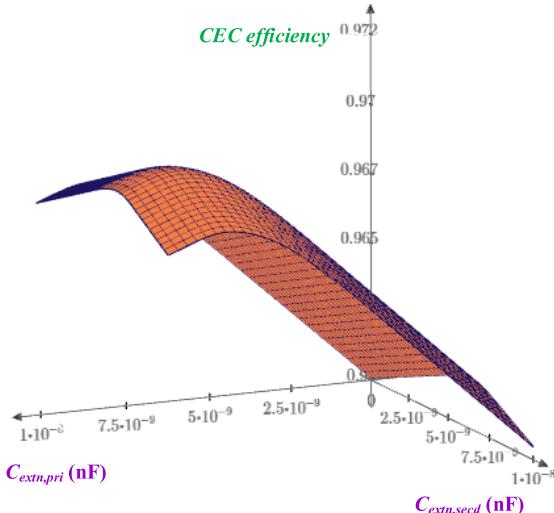


Fig. 19. C_{extn} optimization results for the single power module.

by

$$\int_{t_{\text{off}}}^{t_{\text{on}}} i_L(t_{\text{off}}) \frac{n_1}{n_2} dt \geq Q_{\text{equiv}}(v_{C_2}) \quad (20)$$

where n_1 and n_2 are the transformer winding turns of the primary and secondary sides, respectively. Since the secondary side is a rectified sine waveform, the voltage dependence of the charge must be included in the optimization. The above equations can be utilized to find the minimum required dead time to achieve ZVS while minimizing the circulation current.

D. Comprehensive Optimization Strategy

Minimizing the DAB circulation current must be satisfied while meeting the ZVS condition. The turn-off loss reduction from the external snubber capacitance C_{extn} has to be traded off with the dead-time diode conduction loss. Therefore, the external C_{extn} on both the primary and secondary sides could be one optimization target based on this algorithm. For a given set of hardware parameters and operation range, other parameters such as DAB high-frequency inductor L_r and transformer turns ratio n can be another optimization objective if necessary.

Moreover, typical PV input voltage range $V_{\text{PV}} = 900, 950, \dots, 1300$ V and load conditions $P_{\text{PV}} = P_{\text{full}} \times (10\%, 20\%, \dots, 100\%)$ are adopted in the optimization model in order to achieve the highest California Energy Commission (CEC) efficiency. The flowchart of the proposed comprehensive optimization strategy is shown in Fig. 18.

Fig. 19 shows the external total equivalent capacitance C_{extn} optimization results based on the proposed optimization model. The optimal capacitances for primary and secondary side power stages are $C_{\text{extn},\text{pri}} = 8.7$ nF and $C_{\text{extn},\text{sec}} = 4.6$ nF, respectively. The calculated maximum dc/ac efficiency under real power mode is 98.32% at 100 kW.

VI. 13.8-kV/3-MVA SYSTEM ARCHITECTURE

The mechanical structure of the proposed PVS-SST has been designed and is currently under construction, as shown

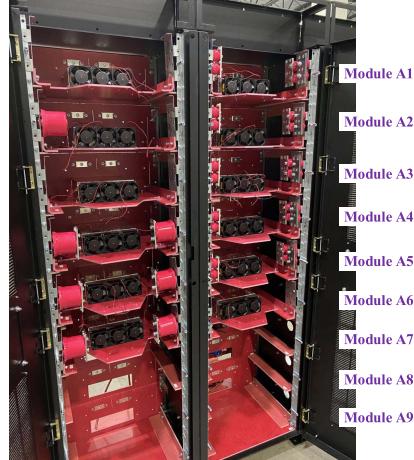


Fig. 20. 13.8-kV/3-MVA PVS-SST power cabinet. Phase A is shown.

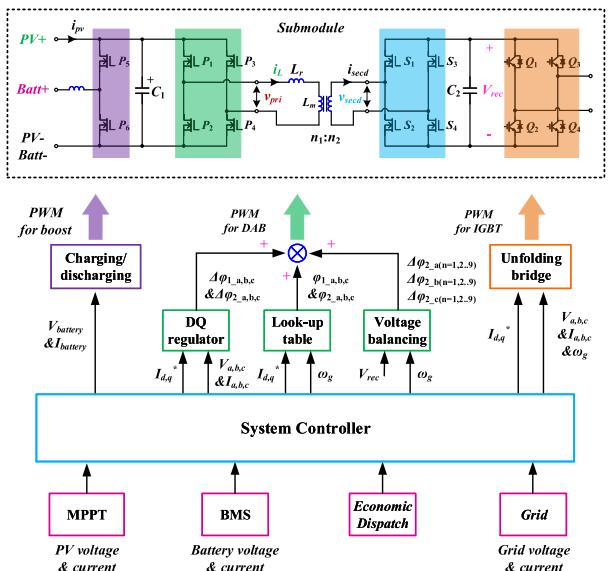


Fig. 21. 13.8-kV/3-MVA PVS-SST control architecture.

in Fig. 20. The system-level control architecture of the PVS-SST is shown in Fig. 21. On the dc side, the control objectives are MPPT for the PV port and the precise charging/discharging current control for the battery port. On the ac side, precise control of active power P and reactive power Q are required. The conventional MPPT algorithm can be used [46], which generates the PV bus voltage reference. A PI controller is used to track the PV panel terminal voltage to the reference by adjusting the active power flow $P_{\text{pv}} = P_{\text{ac}} + P_{\text{battery}}$. The battery charging reference is generated by the system controller. In addition, the PVS-SST is designed to meet the reactive power requirement specified in IEEE 1547-2018.

The control system consists of three major control targets: DPS-based DAB, unfolding bridge, and boost converter. The phase-locked loop (PLL) is used for grid voltage detection and synchronization. The system controller will calculate the desired ac side real and reactive power commands I_d^* and I_q^* based on MPPT result, system economic dispatch, and reactive power needs and will send charging/discharging command to the boost converter with additional inputs from the

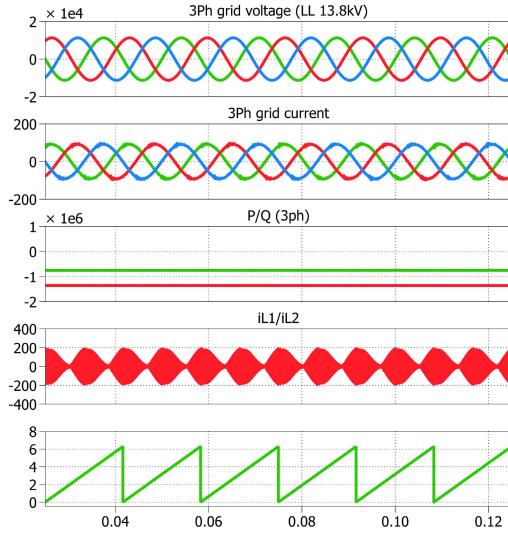


Fig. 22. Worst case operation of the PVS-SST for meeting IEEE 1547-2018. 1: grid side voltage (unit: 10 kV). 2: grid side current (A). 3: Pgrid & Qgrid (MVA). 4: transformer current (A). 5: PLL (radian). The X-axis is time in seconds.

battery management system (BMS). The lookup table-based feedforward modulator, which is synchronized with the PLL, modulates switching frequency and two-phase shifts for all the SiC switches. The DQ current regulator that is a PI-based closed-loop control only modulates two phase shifts to eliminate the steady-state error and improve the inverter output current THD. Additional individual voltage balancing regulator, which measures the secondary side capacitor voltage in each submodule, only regulates the second phase shift $\Delta\phi_{2,a,b,c(n=1,2,\dots,9)}$ in the DPS modulation. IGBT devices in the unfolding bridge will be driven according to the grid side voltage. With the above functional blocks, the PVS-SST is controlled to inject/consume the desired amount of real and reactive powers to the grid.

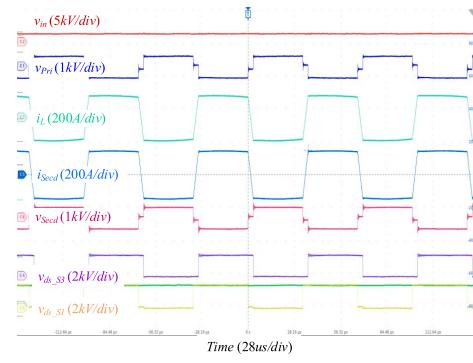
The reactive power injection capability of the proposed DAB dc/ac converter is experimentally demonstrated in Fig. 24 at the 70-kVar per module. This is the first ever demonstration of this capability for a DAB inverter at high power levels. This corresponds to a system reactive power capability of 1.9 MVar, exceeding the IEEE 1547 requirement. Typical case simulation results with 44% reactive power for the 13.8-kV/3-MVA PVS-SST according to IEEE 1547-2018 are shown in Fig. 22. The real power injected from the PVS-SST into a 13.8-kV grid is 600 kW, and the system also supports 1.35-MVar capacitive reactive power. The total RMS value of the phase current is 60 A. The maximum turn-off current flowing through the MFT is around 200 A. The grid side current waveform qualities are all within the limits of IEEE-1547.

VII. EXPERIMENTAL VERIFICATION

In order to justify the proposed hardware design and optimization strategy and verify the capability of the proposed PVS-SST submodule for supporting multiple functionalities as a whole system, necessary experiments of both the PV and battery ports are performed and tested.



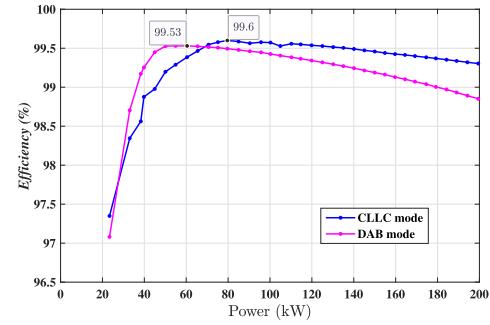
(a)



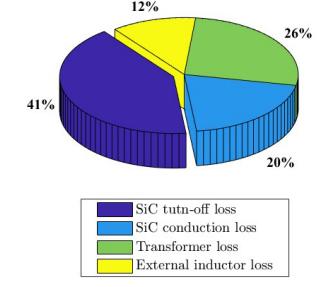
(b)



(c)



(d)

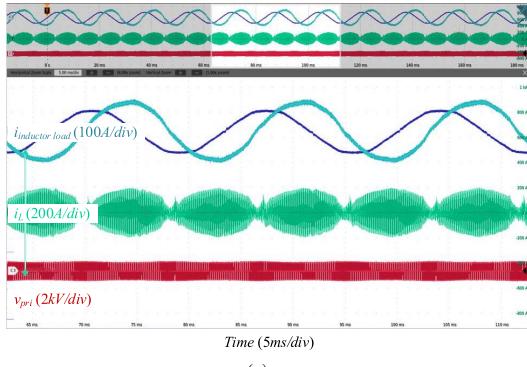


(e)

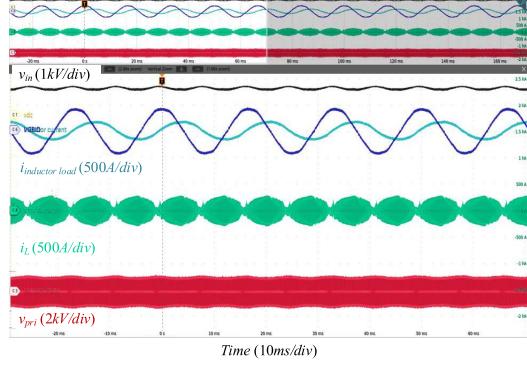
Fig. 23. SiC submodule 1.3-kV dc/dc back-to-back experimental results. (a) 111-kVA SiC power submodule. (b) Key waveforms under 200 kW. (c) PCB temperature rise under 200 kW. (d) Efficiency curves. (e) Loss breakdown under 200 kW/98.85%.

A. Submodule DC/DC Back-to-Back Test

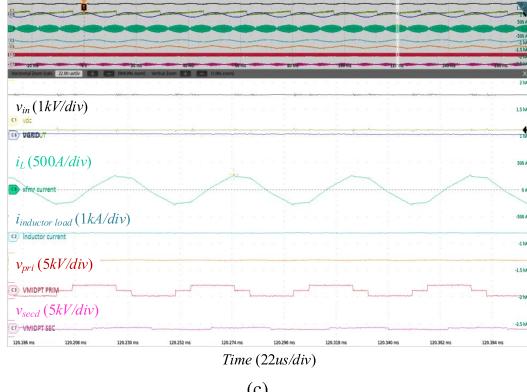
Fig. 23(a) shows the final fabricated SiC power submodule using forced air cooling. The MFT is not shown in this



(a)



(b)



(c)

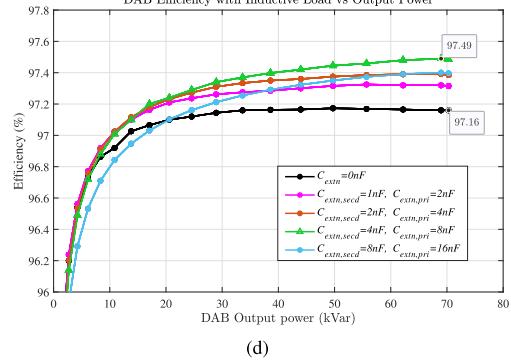
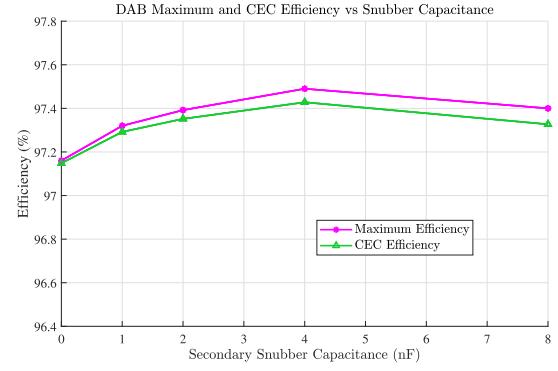
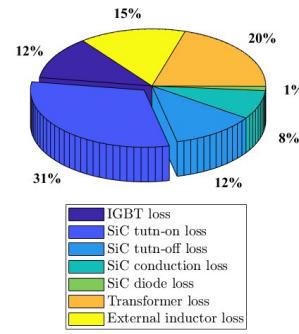


Fig. 24. SiC submodule dc/ac inductive load experimental results. (a) Key waveforms under 31 kVar. (b) Key waveforms under 70 kVar. (c) Waveforms at zero-voltage crossing under 70 kVar. (d) Efficiency curves comparison with C_{extrn} .

picture. To verify the thermal and electrical performance of the submodule, a 1.3-kV/200-kW dc/dc test is conducted using the designed MFT (discussed in Section IV). The switching



(a)



(b)

Fig. 25. SiC submodule dc/ac inductive load experimental results. (a) Maximum efficiency point versus $C_{\text{extrn},\text{secd}}$. (b) Loss breakdown under 70 kVar/97.49%.

frequency is fixed at 15 kHz. The maximum efficiency point is 99.53% at 60 kW and 98.85% at 200 kW, as shown in Fig. 23(d). The 99.53% peak efficiency is the highest DAB converter ever reported in this power range. The HIOKI power analyzer PW6001 with 1500-V voltage range and 500-A/ $\pm 0.02\%$ high-accuracy sensors CT6875 is used in the high-power test.

The blue curve is the efficiency of DAB operating in the resonant (CLLC) mode [47], which has a higher efficiency (99.6% peak), especially under HL. Some key waveforms are listed in Fig. 23(b); the maximum turn-off current of the primary side MOSFETs is around 180 A. The voltage overshoot across the drain-source terminal is less than 100 V under this condition. The temperature rise on the PCB surface is only 23 °C, as shown in Fig. 23(c). The temperature rises of transformer core, winding, and external inductors are detailed in Section IV. The 200-kW dc/dc back-to-back test is performed for totally around 2 h in order to get a steady-state thermal result.

B. Submodule DC/AC Inductive Load Test

The developed SiC submodule is also tested under the dc/ac mode with an inductive load. The pure Q -mode operation always leads to a higher transformer current (turn-off current), namely, higher loss and lower conversion efficiency, compared to the pure P -mode operation. Therefore, the pure Q -mode condition is the worst case for the DAB-based SiC submodule. The primary dc side voltage is 1000 V. DPS is used in this test.

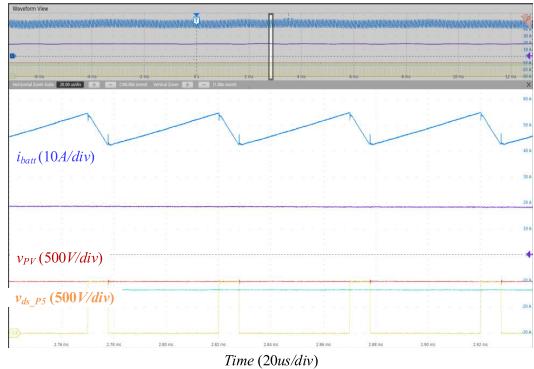


Fig. 26. SiC submodule battery port charging test.

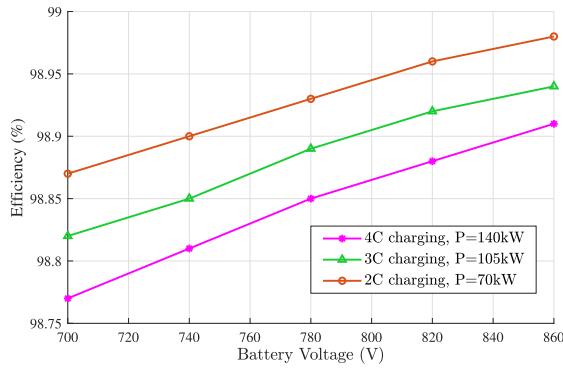


Fig. 27. Calculated efficiency curves with different charging rates.

In addition to the DPSs, the switching frequency is also varied from 15 to 40 kHz. The maximum tested efficiency is 97.49% at 70 kVar, as shown in Fig. 24(d). Some key test waveforms over few switching cycles are shown in Fig. 24(a)–(c). The maximum turn-off current of the primary side MOSFETs is around 290 A under this pure *Q*-mode, which is higher than that under pure *P*-mode (around 255 A at 111 kW). The THD of inductive load current, as shown in Fig. 24, is 4.5%. The voltage overshoot across the drain–source terminal is around 150 V under this 1-kV/70-kVar test.

Due to the ac power capacity limit in the lab, the 1-kV/70-kVar dc/ac pure *Q*-mode and the 1.3-kV/200-kW dc/dc back-to-back pure *P*-mode are carried out, respectively, which can prove the 111-kVA power capability of the proposed SiC submodule. The system-level test will be performed at one project partner’s factory, which has 4.16- and 13.8-kV ac grids.

C. C_{extn} Optimization Verification

Fig. 25(a) shows the efficiency comparison with different snubber capacitances C_{extn} ’s under the inductive mode. The maximum efficiency of the DAB inverter without external dV/dt snubber capacitors is 97.16%. The maximum efficiency is increased by 0.33%–97.49% when employing snubber capacitors $C_{\text{extn},\text{secd}} = 4 \text{ nF}$ and $C_{\text{extn},\text{pri}} = 8 \text{ nF}$ across the primary- and secondary-side MOSFETs, respectively. Between no snubber case and $C_{\text{extn},\text{secd}} = 4 \text{ nF}$ case, the system maximum efficiency and CEC efficiency increase with the snubber capacitance. The maximum efficiency decreased to 97.4% when the snubber is increased to $C_{\text{extn},\text{secd}} = 8 \text{ nF}$ and $C_{\text{extn},\text{pri}} = 16 \text{ nF}$. Keep increasing C_{extn} beyond this value

is pointless while making ZVS turn-on harder and higher loss. The optimal snubber capacitance with the highest CEC efficiency occurs around $C_{\text{extn},\text{secd}} = 4 \text{ nF}$, which verified the validity of the proposed novel turn-off loss model in Section III and the optimization strategy discussed in Section V.

D. BES Test

The 1700-V SiC MOSFET is also used to implement the SiC boost converter to interface the BES with the 1500-V PV bus. The switching frequency of the boost converter is 25 kHz. Fig. 26 shows the waveform of battery charging from the PV port. The maximum charging current flowing through the Boost inductor is 55 A. Meanwhile, all required information of the battery is obtained through a MODBUS communication protocol to the BMS. Information gathered includes SOC, real-time battery voltage (string voltage), charging or discharging current, and so on. The calculated maximum charging efficiency is 98.91% at 180-A/140-kW charging current/power, as shown in Fig. 27. This theoretical value corresponds to a 4C charge rate for a 35-kWh BES based on Toshiba’s SCiBTM battery [48].

VIII. CONCLUSION

This article primarily discusses the hardware design, analysis, optimization, and experimental verification of the proposed 13.8-kV/3-MVA PVS-SST including high-density power stage, medium-voltage isolated MFT, and 13.8-kV modular converter IPOS system architecture. Using the newly developed 1700-V SiC MOSFET module, a DAB-based 111-kVA SiC modular converter is fabricated as the building block of the PVST-SST. The evaluation of using 1700-V SiC devices for 1500-V applications together with a quantitative turn-off voltage spike prediction model based on an optimized PCB busbar design is discussed. A novel turn-off loss model for accurate loss estimation is proposed and experimentally verified. In order to improve the DAB dc/ac power conversion efficiency, a comprehensive optimization strategy based on the proposed novel turn-off loss model, including ZVS range, dead-time calculation, and the minimum circulation current, is proposed. As a grand challenge in the proposed PVS-SST, the medium-voltage isolated MFT achieves high efficiency and high power density with extreme well thermal performance at a 200-kW power rating. A 99.8% efficient MFT with a power capability of more than 340 kW is fabricated and tested. The final power density of the SiC power submodule is 26 W/inch³ or 1.6 MW/m³. PV to grid efficiency is expected to be higher than 98%, while the reactive power injection efficiency is higher than 97.5%. In order to apply the proposed 111-kVA SiC modular converter in a 13.8-kV/3-MVA prototype, the whole PVS-SST system architecture and one typical case scenario simulation results are discussed. The detailed control design will be used in the future system-level validation and test of the PVS-SST.

APPENDIX A

TURN-OFF VOLTAGE OVERSHOOT PREDICTION MODEL

The theoretical value of across the decoupling capacitor $v_{\text{cap}}(t)$, across the drain and source terminal $v_{ds,\text{out}}(t)$ and the

$$v_{\text{cap}}(t) = V_{\text{dc}} + \frac{V_{\text{OS,loop2}}}{2} \cdot \left\{ e^{\frac{t}{2} \cdot \left(-\frac{\sqrt{C_{\text{loop2}} \cdot R_{\text{loop2}}^2 - 4 \cdot L_{\text{loop2}}}}{\sqrt{C_{\text{loop2}} \cdot L_{\text{loop2}}}} - \frac{R_{\text{loop2}}}{L_{\text{loop2}}} \right)} + e^{\frac{t}{2} \cdot \left(\frac{\sqrt{C_{\text{loop2}} \cdot R_{\text{loop2}}^2 - 4 \cdot L_{\text{loop2}}}}{\sqrt{C_{\text{loop2}} \cdot L_{\text{loop2}}}} - \frac{R_{\text{loop2}}}{L_{\text{loop2}}} \right)} \right\} \quad (29)$$

$$v_{\text{ds,in}}(t) = v_{\text{cap}}(t) + \frac{V_{\text{OS,loop1}}}{2} \cdot \left\{ e^{\frac{t}{2} \cdot \left(-\frac{\sqrt{C_{\text{loop1}} \cdot R_{\text{loop1}}^2 - 4 \cdot L_{\text{loop1}}}}{\sqrt{C_{\text{loop1}} \cdot L_{\text{loop1}}}} - \frac{R_{\text{loop1}}}{L_{\text{loop1}}} \right)} + e^{\frac{t}{2} \cdot \left(\frac{\sqrt{C_{\text{loop1}} \cdot R_{\text{loop1}}^2 - 4 \cdot L_{\text{loop1}}}}{\sqrt{C_{\text{loop1}} \cdot L_{\text{loop1}}}} - \frac{R_{\text{loop1}}}{L_{\text{loop1}}} \right)} \right\} \quad (30)$$

$$v_{\text{ds,out}}(t) = v_{\text{cap}}(t) + \frac{V_{\text{OS,loop1,out}}}{2} \cdot \left\{ e^{\frac{t}{2} \cdot \left(-\frac{\sqrt{C_{\text{loop1}} \cdot R_{\text{loop1}}^2 - 4 \cdot L_{\text{loop1}}}}{\sqrt{C_{\text{loop1}} \cdot L_{\text{loop1}}}} - \frac{R_{\text{loop1}}}{L_{\text{loop1}}} \right)} + e^{\frac{t}{2} \cdot \left(\frac{\sqrt{C_{\text{loop1}} \cdot R_{\text{loop1}}^2 - 4 \cdot L_{\text{loop1}}}}{\sqrt{C_{\text{loop1}} \cdot L_{\text{loop1}}}} - \frac{R_{\text{loop1}}}{L_{\text{loop1}}} \right)} \right\} \quad (31)$$

internal dies $v_{\text{ds,in}}(t)$, can be derived according to (29)–(31), as shown at the top of the page. Part of the values, such as R , L , and C , is extracted from the ANSYS/Q3D simulation, and t_{off} is calculated from the turn-off loss model in Section III.

$$L_{\text{loop1}} = L_{\text{decouple}} + L_{\text{busbar1}} + L_{\text{module}} \approx 13 \text{ nH} \quad (21)$$

$$R_{\text{loop1}} = R_{\text{decouple}} + R_{\text{busbar1}} + R_{\text{module}} \approx 0.11 \Omega \quad (22)$$

$$L_{\text{loop2}} = L_{\text{decouple}} + L_{\text{busbar2}} + L_{\text{filter}} \approx 46 \text{ nH} \quad (23)$$

$$R_{\text{loop2}} = R_{\text{decouple}} + R_{\text{busbar2}} + R_{\text{filter}} \approx 0.06 \Omega \quad (24)$$

$$V_{\text{OS,loop1}} = L_{\text{loop1}} \cdot \frac{I_{\text{ds}}}{t_{\text{off}}} \quad (25)$$

$$V_{\text{OS,loop2}} = L_{\text{loop2}} \cdot \frac{I_{\text{ds}}}{t_{\text{off}}} \quad (26)$$

$$L_{\text{loop1,out}} = L_{\text{decouple}} + L_{\text{busbar1}} \approx 6 \text{ nH} \quad (27)$$

$$V_{\text{OS,loop1,out}} = L_{\text{loop1,out}} \cdot \frac{I_{\text{ds}}}{t_{\text{off}}}. \quad (28)$$

APPENDIX B DPS DAB MODULATION

For DAB under the DPS modulation, some key parameters of the SiC devices, including I_1 , I_2 , I_3 , $I_{P1,\text{rms}}$, and P_{DAB} under different power flow directions, are listed as follows.

1) DAB parameters' definitions for $P_{\text{DAB}} > 0$

$$I_1 = \frac{v_{c1}(4\varphi_1 - 2\varphi_2 - 1) + v_{c2}}{4L_{\gamma} f_s} \quad (32)$$

$$I_2 = \frac{v_{c1}(1 - 2\varphi_2) - v_{c2}(1 - 4\varphi_1)}{4L_{\gamma} f_s} \quad (33)$$

$$I_3 = \frac{v_{c1}(1 - 2\varphi_2) - v_{c2}(1 - 4\varphi_1 + 4\varphi_2)}{4L_{\gamma} f_s} \quad (34)$$

$$P_{\text{DAB}} = \frac{v_{c1}v_{c2}(4\varphi_1^2 - 4\varphi_1\varphi_2 + 2\varphi_2^2 - 2\varphi_1 + \varphi_2)}{-2L_{\gamma} f_s}. \quad (35)$$

2) DAB parameters' definitions for $P_{\text{DAB}} < 0$

$$I_1 = \frac{v_{c1}(1 - 2\varphi_2) - v_{c2}(1 + 4\varphi_1)}{4L_{\gamma} f_s} \quad (36)$$

$$I_2 = \frac{v_{c1}(1 - 2\varphi_2) - v_{c2}(4\varphi_1 - 4\varphi_2 + 1)}{4L_{\gamma} f_s} \quad (37)$$

$$I_3 = \frac{v_{c1}(-4\varphi_1 + 2\varphi_2 - 1) + v_{c2}}{4L_{\gamma} f_s} \quad (38)$$

$$P_{\text{DAB}} = \frac{v_{c1}v_{c2}(4\varphi_1^2 - 4\varphi_1\varphi_2 + 2\varphi_2^2 + 2\varphi_1 - \varphi_2)}{2L_{\gamma} f_s}. \quad (39)$$

APPENDIX C

COEFFICIENTS OF MINIMUM CIRCULATION CURRENT

To minimize the maximum turn-off current, some key variables, including a , b , c , M , and K under different power flow directions, are listed as follows:

$$M = \frac{V_{c2}}{V_{c1}} \quad (40)$$

$$K = \frac{2L_{\gamma} f_s P_{\text{DAB}}}{V_{c1} V_{c2}} \quad (41)$$

$$a = 16[V_{c1}^2 + (V_{c1} - 2V_{c2})^2] \quad (42)$$

$$b = 8[V_{c1}^2 + (V_{c1} - 2V_{c2})^2] \times \text{sgn}(P_{\text{DAB}}) \quad (43)$$

$$c = \begin{cases} (8K - 1)(V_{c1} - 2V_{c2})^2 + V_{c1}^2, & P_{\text{DAB}} > 0 \\ (V_{c1} - 2V_{c2})^2 - (8K + 1)V_{c1}^2, & P_{\text{DAB}} < 0. \end{cases} \quad (44)$$

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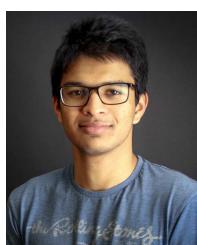
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