FPGA Remote Laboratory for Hardware E-Learning Courses

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Abstract— **This paper describes the architecture of a hardware remote laboratory based on using Field Programmable Gate Array (FPGA) development boards for hardware of digital electronic circuits design. The introduced FPGA remote laboratory is suitable for delivering digital design courses as full e-learning courses. By using the FPGA remote laboratory the students can remotely access the FPGA lab through the internet, either by using the Microsoft XP remote connection or through a webpage that has the facilities of configuring the FPGA chip online by sending the bit stream file through the internet to the lab PC which is connected through USB port to the FPGA board. The FPGA hardware remote laboratory introduced in this article is mainly consists of 20th PCs, and 20th FPGA kits. FPGA Spartan 3E Starter kits from Diligent has been used as a development board for configuring the FPGA Spartan 3E chip from Xilinx; each PC is connected to one FPGA kit and to the campus local area network. The students can remotely login to the lab machine and program the FPGA with their designs as well as testing their designs remotely. VHDL has been used as the design entry to Xilinx ISE Foundation.**

I. INTRODUCTION

Distance learning has gained in popularity not only as a way to offer instruction in locations without local expertise, but also as a cost-effective method where limited enrolment at one location would not normally warrant offering the course. In engineering technology programs, where most courses have a lab component, distance learning offers many new challenges in course delivery [1-2]. Nowadays the challenge for engineering education is about the online education: the role of laboratory is very important in engineering studies. In the past two decades great efforts have been made in this direction and many proposals of virtual and remote labs have been presented [3]. Recent advances in digital system design have had a huge impact on the learning situation for students enrolled in hardware design courses. Since the invention of the Internet, many academicians, educators, and researches have been searching for effectual virtual lab experiments, however, the very nature of real experimentation was not possible or missing [4]. Hardware Design Laboratory is one of the main concerns for e-learning courses in digital design area [5].

The use of Hardware Description Languages and Field Programmable Gate Arrays for digital design today changes the way of designing and testing the digital circuits. The students can use software tools to design and test their circuits, and then use a hardware tools "FPGA Boards" to implement their design in a real hardware implementation using FPGA chip, which is a programmable chip that can be configured with a custom digital design. Hardware design laboratory using VHDL and FPGA has been used for partial e-learning courses, where the students can do most of the work for their experiment at home using the free software tool available on the internet, that work include the simulation and implementation, then they come to the lab with a binary file that will be used for configuring the FPGA chip, and then they can test their design in a hardware level using the available FPGA development board [5].

Many techniques have been introduced for remote and virtual laboratory in different area of engineering [6-18]. In this paper we are introducing an FPGA remote laboratory for digital design that is suitable for full e-learning courses in computer engineering hardware design. The remote laboratory based on using Spartan 3E FPGA starter kits from Diligent that are connected to the lab PCs through the USB port. The PCs are connected to the Local Area Network (LAN) in the campus. The students can remotely login to the lab PCs by using Microsoft remote desktop connection or through a webpage to program the FPGA chip with their design, and then test the design remotely through the parallel port of the lab PCs. For testing the hardware circuit through the PC parallel port a Graphical User Interface (GUI) has been built using Visual Basic to forces to the design input pines that are connected to parallel port of the PC, and then read the outputs of the design by reading the data on the parallel port.

The materials included in this article are organized as follows; section II relating the VHDL design process to the ADDIE model of Instructional System Design. In section III a description of the system architecture for the FPGA remote laboratory is given, the conclusions and future work will be given in section IV.

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II. VHDL INSTRUCTIONAL SYSTEM DESIGN MODEL

In this section we are going to describe the VHDL system design with relation to the ADDIE (Analyses Design Development Implementation Evaluation) model as one of the ISD (Instructional System Design) models. Figure (1) shows the ADDIE model in which the system has to be analyzed at the beginning, then it will be designed in the second step, the third step is the development of the system, and then the implementation step, at the end the design has to be evaluated. The VHDL design process when using FPGA as the target technology goes through some steps similar to that in the ADDIE model. Where the design has to be specified and documented at the initial step. The second step is the design entry, which can be VHDL / Verilog. After checking the code or circuit, the design has to be simulated for the functionality of the design, if the function is not correct, then code or circuit has to be modified again and again until a correct function achieved, this is the third step, and it is shown in figure (2) as an example, the simulation in the figure is for 4*1 multiplexer. To build the hardware circuit, the design will be synthesized to generate the gate level circuit of the design as shown in figure (3); the top-level design in that figure is for a clock division design, in which the code is converted to logic circuit. The implementation step is for mapping the design into the FPGA chip. Then the FPGA device will be configured with the design. At the end after configuring the device, the design will be tested in a hardware level by assigning forces to the inputs and testing the corresponding outputs.

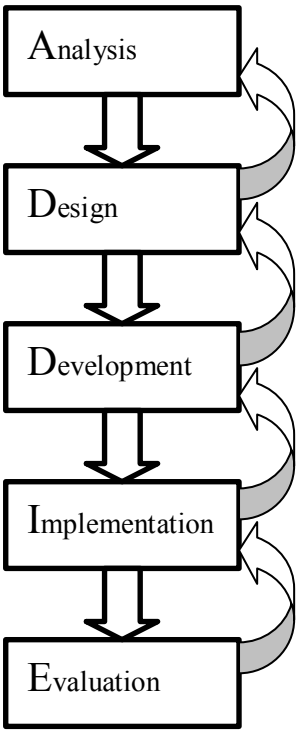

Figure (1) ISD – ADDIE Model

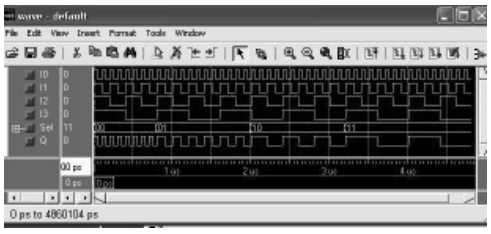

Figure (2) VHDL Design Simulation for 4*1 MUX

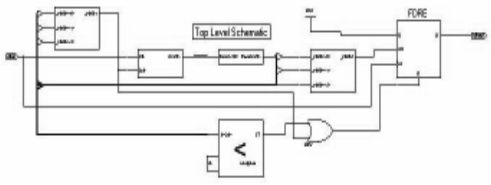

Figure (3) VHDL Top-Level Design for Clock Division

III. SYSTEM ARCHITECTURE

In this section we are going to discuss the system architecture of the remote laboratory which is shown in figure (4). The remote laboratory consists of 20 PCs; each PC is attached with one FPGA development board, with a total of 20 FPGA boards. All lab PCs are connected to the local area network of the campus. The students can use the free available webpack software from Xilinx to finish most of the design steps including the implementation and generation of the bit stream file that are required for programming the FPGA chip, then they can remotely login to the lab machine to access and run the Xilinx ISE software tools to configure the device, after that they can remotely test their design through the PC parallel port using Microsoft XP remote desktop that accesses the Lab PC from a remote machine.

Figure (5), shows the FPGA development board that is connected to the PC parallel port, with the JTAG cable is connected through the USB port of the PC instead of the parallel port JTAG cable to make the parallel port available for the design testing. Figure (5.1) shows the connection of the parallel port to a bread board, and figure (5.2) shows the parallel port pin assignments that have been used for sending and receiving data to the design for design verification. In figure (5.3) we can see the FPGA development board with the connection to the parallel port through the used bread board. A Graphical User Interface (GUI) has been designed using Visual Basic to simplify the process of applying forces to the design inputs, and then check the output. The GUI also simulate the switches and LEDs of the FPGA development board, through the GUI the student can just click the mouse to force the input, then he can see the output on his PC screen.

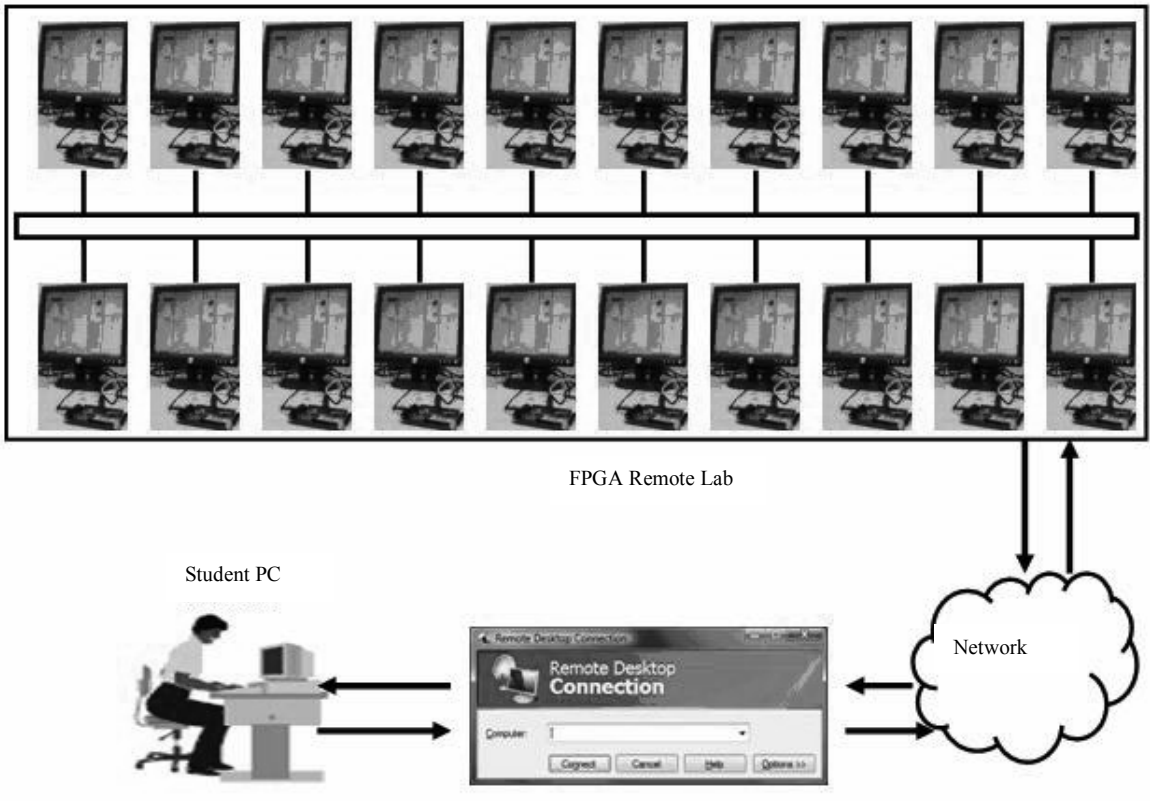

Figure (4) System Architecture

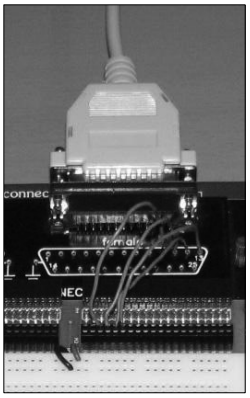

Figure (5.1) Parallel Port Connection

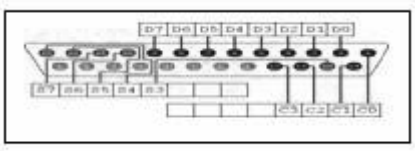

Figure (5.2) Parallel Port Pin Assignment

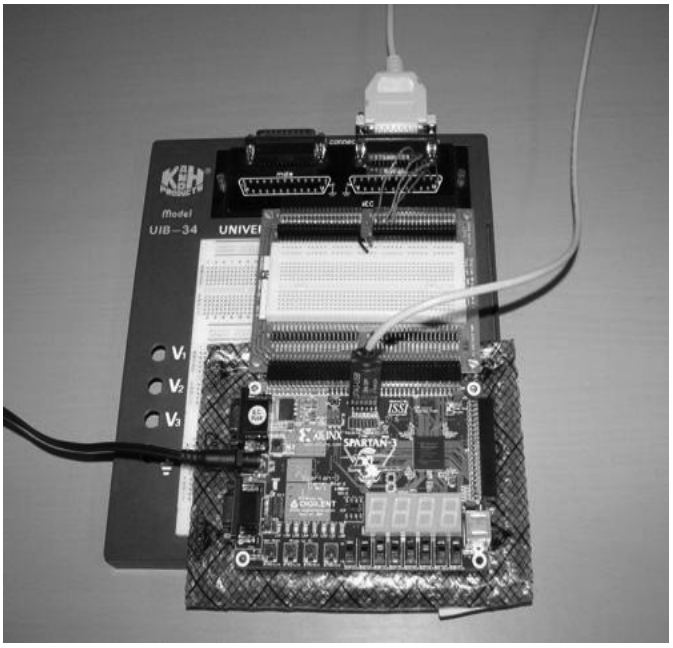

Figure (5.3) FPGA Development Board

Figure (5) FPGA Development Board Connections

IV. Conclusions And Futur Works

FPGA remote laboratory has been introduced for hardware courses in area of computer engineering to be delivered as full e-learning courses. The FPGA remote laboratory consists of 20 PCs, each PC is connected to one FPGA development board, where FPGA Spartan 3E starter kit from Digilent has been used for programming the Spartan 3E FPGA chip. VHDL has been used as the design entry for the Xilinx ISE Foundation software tools for simulation and implementation. The laboratory has been tested for remote configuration of the FPGA chip through the USB port as well as remote testing of the design through the PC parallel port. GUI has been design using Visual Basic by which the user can easily test the design remotely by applying forces to the design inputs, and then read the corresponding output. The remote access has been achieved by using Microsoft XP desktop remote connection. More developments are needed for the introduced FPGA remote laboratory. One of the developments is to use a webpage to remotely access the laboratory through the internet for programming or testing the FPGA. Another issue is to use a web camera with each FPGA development board, by which the user can monitor the FPGA board and see the output of the design on the available LEDs or 7-Segments.

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References

[1] K.D Taylor, J.W Honchell, W.E DeWitt, "Distance learning in courses with a laboratory", Frontiers in Education Conference, 26th Annual Conference, Proceedings of Volume 1, pp. 44 - 46, 6-9 Nov 1996.

[2] L. Peretto, S. Rapuano, M. Riccio, D. Bonatti, "Distance learning of electronic measurements by means of measurement set-up models", Measurement, pp. 274–283, 2008.

[3] D. Bonatti, G. Pasini, L. Peretto, E. Pivello, R. Tinarelli, "A Novel Approach for Laboratory Activities in E-Learning Courses", 2007 IEEE Instrumentation and Measurement Technology Conference, pp. 1-6, May 2007.

[4] A. Abu-El Humos, B Alhalabi, M.K. Hamzal, E. Shufro, W. Awada, "Remote labs environments (RLE): a constructivist online experimentation in science, engineering, and information technology", IECON 2005. 31st Annual Conference of IEEE, pp. 6-10, Nov 2005.

[5] W. M. El-Medany, "E-Learning for Hardware Design Laboratory Using VHDL and FPGA", Sixth International Internet Education Conference, ICT-Learn2007, Cairo, Egypt, pp. 285-289, September 2007.

[6] M. Auer, A. Pester, D. Ursutiu, C. Samoila, "Distributed virtual and remote labs in engineering", 2003 IEEE International Conference on Industrial Technology, Volume 2, pp. 1208 - 1213Issue , 10-12 Dec 2003.

[7] J. Hu, C. Meinel, "Tele-Lab ''IT-Security'' on CD: portable, reliable and safe IT security training", Computers & Security, Volume 23, pp. 282-289, 2004.

[8] J. Lucca, "An assessment of e-Learning technologies to support telecommunications laboratory learning objectives", Proceedings of the 37th Annual Hawaii International Conference on System Sciences, 2004.

[9] P. Hai Lin, M. Lin, "Design and implementation of an Internet-based virtual lab system for e-learning support", A, 2005. ICALT. Fifth IEEE International Conference on Advanced Learning Technologies, 2005.

[10] M.J. Callaghan, J. Harkin, E. McColgan, T.M. McGinnity, L.P. Maguire, "Client–server architecture for collaborative remote experimentation", Journal of Network and Computer Applications, Volume 30, pp. 1295–1308, 2007.

[11] M. Guggisberg, P. Fornaro, T. Gyalog, H. Burkhart," An interdisciplinary virtual laboratory on nanoscience", Future Generation Computer Systems volume 19, pp. 133–141, 2003.

[12] Z. Nedic, J. Machotka, A. Nafalski, "Remote laboratories versus virtual and real laboratories", FIE 2003. 33rd Annual Frontiers in Education, Volume 1, pp. T3E-1 - T3E-6, 5-8 Nov 2003.

[13] R. Hashemian, C. Pedapati, "Backboard-Based Digital Hardware Design Using FPGAs ", Proceedings of ASEE 2005 IL/IN Sectional Conference, pp. T3-4, April 1-2, 2005.

[14] R. Hashemian, J. Riddley, "A Method to Design, Construct and Test Digital Hardware all in Classroom Environment", 37th ASEE/IEEE Frontiers in Education Conference, pp. T3G 1-6, 10 – 13 October 2007.

[15] W. M. El-Medany, M. R. El-Sabry, "GSM-Based Remote Sensing and Control System Using FPGA", Proceedings of the International Conference on Computer and Communication Engineering, ICCCE'08, IEEE catalog number CFP0839D, V II, pp. 1093-1097, 2008.

[16] J. M. Jasso, G. O. Vargas, R. C Miranda, E. V. Ramos, A. Z. Garrido, G. H. Ruiz , "FPGA-based real-time remote monitoring system", Computers and Electronics in Agriculture, Volume 49, pp. 272–285, 2005.

[17] N. Fujii, "Top-down education for digital logic design course based on cellular methods", 33rd Annual Frontiers in Education (IEEE Cat. No.03CH37847C), pp. 8-14, Vol.1, 2003.

[18] S. M. Cracken, Z. Zilic and H. Y. Chan," Real Laboratories for Distance Education", Journal of Computing and Information Technology - CIT 11, pp. 67–76, 2003.