W83627DHG-P

W83627DHG-PT

NUVOTON LPC I/O

Date: July 09, 2009 Version: 1.94

TABLE OF CONTENTS –

List of Figures

List of Tables

1. GENERAL DESCRIPTION

The W83627DHG-P is a member of Nuvoton's Super I/O product line. This family features the LPC (Low Pin Count) interface. This interface is more economical than its ISA counterpart, in that it has approximately forty pins fewer, yet still provides as great performance. In addition, the improvement allows even more efficient operation of software, BIOS and device drivers.

In addition to providing an LPC interface for I/O, the W83627DHG-P monitors several critical parameters in PC hardware, including power supply voltages, fan speeds, and temperatures. In terms of temperature monitoring, the W83627DHG-P adopts the Current Mode (dual current source) approach. The W83627DHG-P also supports the Smart Fan control system, including SMART FAN™ I, SMART FAN™ III and SMART FAN™ III+, which makes the system more stable and user-friendly.

The W83627DHG-P supports four -- 360K, 720K, 1.2M, 1.44M, or 2.88M -- disk drive types and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s, 1 Mb/s, and 2 Mb/s. The disk drive adapter supports the functions of floppy disk drive controller (compatible with the industry standard 82077/ 765), data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. Such a wide range of functions integrated into one W83627DHG-P greatly reduces the number of required components to interface with floppy disk drives.

The W83627DHG-P provides two high-speed serial communication ports (UARTs), one of which provides IR functions IrDA 1.0 (SIR for 1.152K bps). Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem-control capability, and a processor interrupt system. Both UARTs support legacy speeds up to 115.2K bps as well as even higher baud rates of 230K, 460K, or 921K bps to support higher speed modems.

The W83627DHG-P supports the PC-compatible printer port (SPP), the bi-directional printer port (BPP), the enhanced parallel port (EPP) and the extended capabilities port (ECP).

The W83627DHG-P provides a bridge of the Low Pin Count interface to Serial Peripheral Interface (SPI) that supports up to 8M bits serial flash ROM. The W83627DHG-P provides flexible I/O control functions through a set of 40 general purpose I/O (GPIO) ports. These GPIO ports may serve as simple I/O ports or may be individually configured to provide alternative functions.

The W83627DHG-P supports the SST (Simple Serial Transport) interface and Intel® PECI (Platform Environment Control Interface).

The W83627DHG-P fully complies with the Microsoft© PC98, PC99 and PC2001 System Design Guides and meets the requirements of ACPI.

The configuration registers inside the W83627DHG-P support mode selection, function enable and disable, and power-down selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature in Windows 95/98/2000/XP™, making the allocation of the system resources more efficient than ever.

One special characteristic of the Super I/O product line is the separation of the power supply in normal operation from that in standby operation. Please pay attention to the layout of these two power supplies to avoid short circuits. Otherwise, the feature will not function.

In addition to W83627DHG-P, there is W83627DHG-PT. W83627DHG-PT is exactly the same as W83627DHG-P, except the IC operation temperature. W83627DHG-PT supports industrial standard, which means the IC operating temperature ranges from -40℃ to 85℃. W83627DHG-P supports commercial standard, which means the IC operating temperature ranges from 0℃ to 70℃.

2. FEATURES

General

- Comply with LPC specification 1.1 version
- Support LDRQ# (LPC DMA), SERIRQ (Serialized IRQ)
- Integrated hardware monitor functions
- Compliant with Microsoft PC98/PC99/PC2001 System Design Guide
- Support DPM (Device Power Management), ACPI (Advanced Configuration and Power Interface)
- Programmable configuration settings
- Single 24- or 48-MHz clock input
- Support selective pins of 5 V tolerance

FDC

- Variable write pre-compensation with track-selection capability
- Support vertical recording format
- DMA-enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detect all overrun and underrun conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD-write enable signal (write data signal forced to be inactive)
- Support 3.5-inch or 5.25-inch floppy disk drives
- Compatible with industry standard 82077
- 360K / 720K / 1.2M / 1.44M / 2.88M formats
- 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Support 3-mode FDD and its Windows driver

UART

- Two high-speed, 16550-compatible UARTs with 16-byte send / receive FIFOs
- Fully programmable serial-interface characteristics:
  --- 5, 6, 7 or 8-bit characters
  --- Even, odd or no parity bit generation/detection
  --- 1, 1.5 or 2 stop-bit generation
- Internal diagnostic capabilities:
  --- Loop-back controls for communications link fault isolation
  --- Break, parity, overrun, framing error simulation
- Programmable baud rate generator allows division of clock source by any value from 1 to (2^{16} - 1)
- Maximum baud rate for clock source 24 MHz is 1.5 M bps.

Parallel Port

- Compatible with IBM parallel port
- Support PS/2-compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) - Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) - Compatible with IEEE 1284 specification
- Enhanced printer port back-drive current protection
- Extension FDD mode support disk drive B; and Extension 2FDD mode support disk drives A and B through parallel port

Keyboard Controller

- 8042-based keyboard controller
- Asynchronous Access to two data registers and one status register
- Software-compatible with 8042
- Support PS/2 mouse
- Support Port 92
- Support both interrupt and polling modes
- Fast Gate A20 and Hardware Keyboard Reset
- 12MHz operating frequency

Hardware Monitor Functions

- Smart Fan control system, supporting the functions of SMART FAN™ I -- "Thermal Cruise™" and "Speed Cruise™" modes, SMART FAN™ III and SMART FAN™ III+
- Programmable threshold temperature to speed fan fully while current temperature exceeds this threshold in the Thermal Cruise™ mode
- Three thermal inputs from the different combinations of remote thermistors, and the thermal diode output
- Support Current Mode (dual current source) temperature sensing method
- Nine voltage inputs (CPUVCORE, VIN[0..3] and 3VCC, AVCC , 3VSB, VBAT)
- Five fan-speed monitoring inputs
- Four fan-speed controls
- Dual mode for fan control (PWM and DC)
- Built-in case open detection circuit
- Programmable hysteresis and setting points for all monitored items
- Over-temperature indicator output
- Issue SMI#, OVT# to activate system protection
- Nuvoton Hardware Doctor™ support
- Eight VID inputs / outputs
- Provide I^2C interface to read / write registers

Serial Peripheral Interface

- Support up to 8M bits SPI Flash Memory with clock up to 33 MHz
- Support Mode 0 and Mode 3

Infrared

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps

General Purpose I/O Ports

- 40 programmable general purpose I/O ports
- GPIO port 4 supports the optional functions of Watchdog Timer Out and Suspend LED Output
- GP30, GP31 and GP35 can distinguish whether the input pins undergo any transitions by reading the registers. All of the 3 GPIOs can assert PSOUT# or PME# to wake up the system if each of them undergoes any transition.

OnNow Functions

- Keyboard Wake-Up by programmable keys
- Mouse Wake-Up by programmable buttons
- OnNow Wake-Up from all of the ACPI sleeping states (S1-S5)

Simple Serial Transport™ Interface

- SST temperature and voltage Combination Sensor command support
- Support SST 0.9 Specification

PECI Interface

- Support PECI 1.0 and 1.1a Specifications
- Support 4 CPU addresses and 2 domains per CPU address

Package

- 128-pin QFP
- Pb-free/RoHS

3. BLOCK DIAGRAM

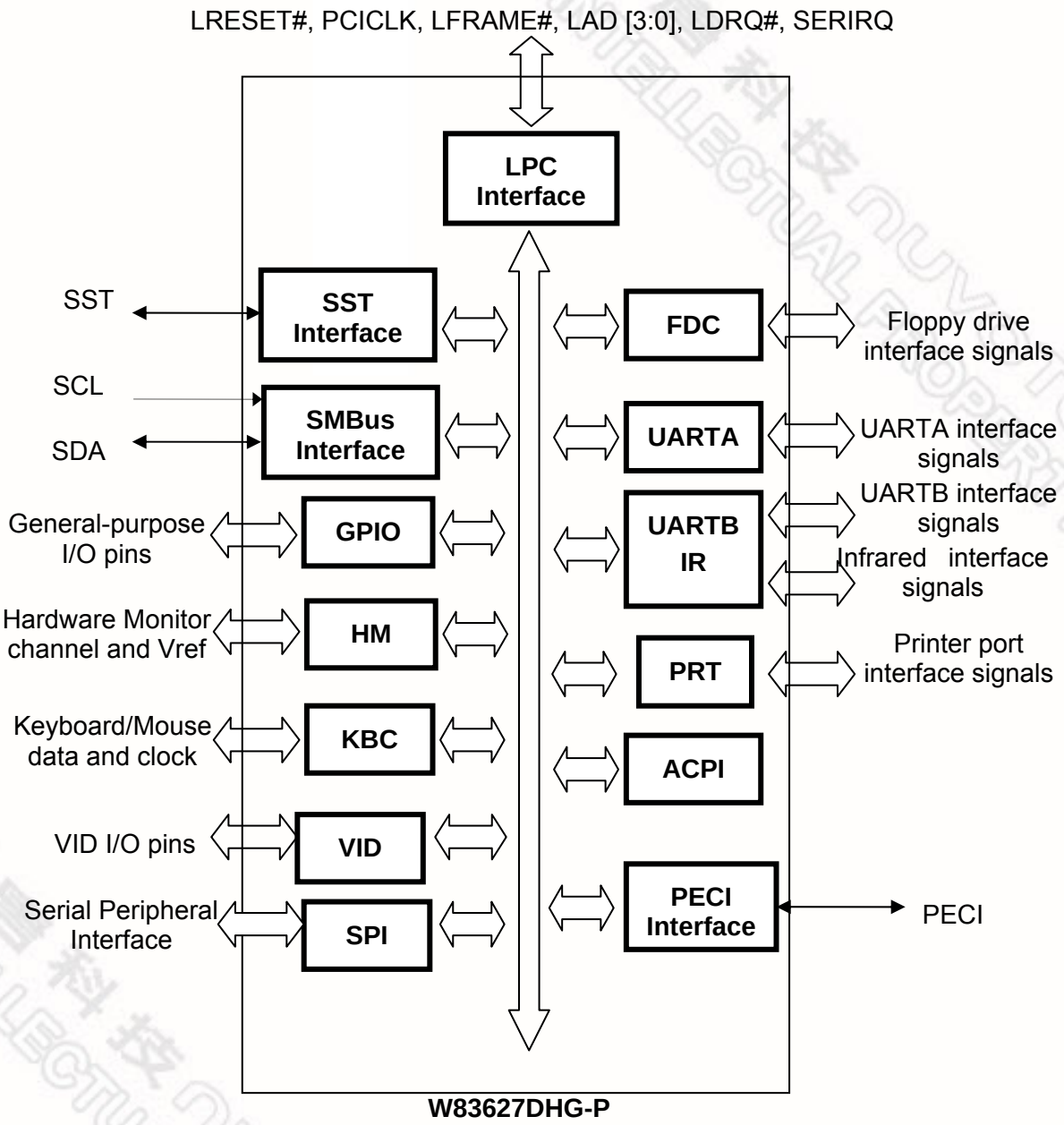


Figure 3-1 W83627DHG-P Block Diagram

4. PIN LAYOUT

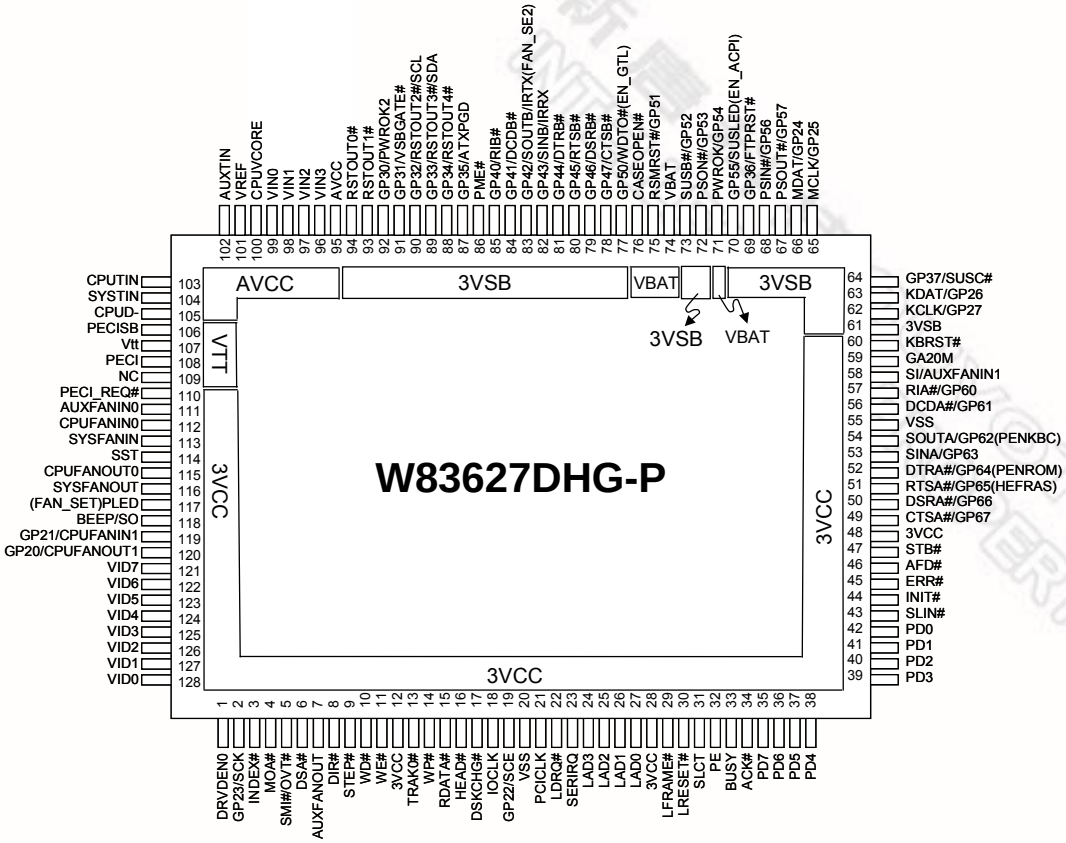


Figure 4-1 Pin Layout for W83627DHG-P

5. PIN DESCRIPTION

Note: Please refer to Section 22.3 DC CHARACTERISTICS for details.

AOUT - Analog output pin
AIN - Analog input pin
IN_{cd} - CMOS-level input pin with internal pull-down resistor
IN_{cs} - CMOS-level, Schmitt-trigger input pin
IN_{csu} - CMOS-level, Schmitt-trigger input pin with internal pull-up resistor
IN_{t} - TTL-level input pin
IN_{td} - TTL-level input pin with internal pull-down resistor
IN_{ts} - TTL-level, Schmitt-trigger input pin
IN_{tp3} - 3.3V, TTL-level input pin
IN_{tsp3} - 3.3V TTL level Schmitt-trigger input pin
IN_{tu} - TTL-level input pin with internal pull-up resistor
I/O_{8} - bi-directional pin with 8-mA source-sink capability
I/O_{8t} - TTL-level, bi-directional pin with 8-mA source-sink capability
I/O_{12} - bi-directional pin with 12-mA source-sink capability
I/O_{12t} - TTL-level, bi-directional pin with 12-mA source-sink capability
I/O_{12ts} - Schmitt-trigger, bi-directional pin with 12-mA source-sink capability
I/O_{12tp3} - 3.3V, TTL-level, bi-directional pin with 12-mA source-sink capability
I/OD_{8t} - TTL-level, bi-directional pin. Open-drain output with 8-mA sink capability
I/OD_{12} - Bi-directional pin. Open-drain output with 12-mA sink capability
I/OD_{12t} - TTL-level bi-directional pin. Open-drain output with 12-mA sink capability
I/OD_{12cs} - CMOS-level, bi-directional, Schmitt-trigger pin. Open-drain output with 12-mA sink capability
I/OD_{12ts} - TTL-level, bi-directional, Schmitt-trigger pin. Open-drain output with 12-mA sink capability
I/OD_{12tp3} - 3.3V, TTL-level, bi-directional pin. Open-drain output with 12-mA sink capability
I/OD_{16t} - TTL-level, bi-directional pin. Open-drain output with 16-mA sink capability
I/OD_{16ts} - Schmitt-trigger, bi-directional pin. Open-drain output with 16-mA sink capability
I/OD_{16cs} - CMOS-level, Schmitt-trigger, bi-directional pin. Open-drain output with 16-mA sink capability
I/OD_{24t} - TTL-level, bi-directional pin. Open-drain output with 24-mA sink capability
O_{12p3} - 3.3V output pin with 12-mA source-sink capability
O_{12tp3} - 3.3V, TTL-level output pin with 12-mA source-sink capability
O_{8} - TTL-level output pin with 8-mA source-sink capability
O_{12} - TTL-level output pin with 12-mA source-sink capability
O_{24} - TTL-level output pin with 24-mA source-sink capability
OD_{8} - Open-drain output pin with 8-mA sink capability
OD_{12} - Open-drain output pin with 12-mA sink capability
OD_{24} - Open-drain output pin with 24-mA sink capability
I_{V3} - Bi-direction pin with source capability of 6 mA and sink capability of 1 mA
I/O_{V3} - Bi-direction pin with source capability of 6 mA and sink capability of 1 mA

5.1 LPC Interface

SYMBOL	PIN	I/O	DESCRIPTION
IOCLK	18	IN_{tp3}	System clock input, either 24MHz or 48MHz. The actual frequency must be specified in the register. The default value is 48MHz.
PME#	86	OD_{12p3}	Generated PME event.
PCICLK	21	IN_{tsp3}	PCI-clock 33-MHz input.
LDRQ#	22	O_{12p3}	Encoded DMA Request signal.
SERIRQ	23	I/OD_{12tp3}	Serialized IRQ input / output.
LAD[3:0]	24-27	I/O_{12tp3}	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
LFRAME#	29	IN_{tsp3}	Indicates the start of a new cycle or the termination of a broken cycle.
LRESET#	30	IN_{tsp3}	Reset signal. It can be connected to the PCIRST# signal on the host.

5.2 FDC Interface

SYMBOL	PIN	I/O	DESCRIPTION
DRVDEN0	1	OD_{24}	Drive Density Select bit 0.
INDEX#	3	IN_{cs}	This Schmitt-trigger input from the disk drive is active-low when the head is positioned over the beginning of a track marked by an index hole. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
MOA#	4	OD_{24}	Motor A On. When set to 0, this pin activates disk drive A. This is an open-drain output.
DSA#	6	OD_{24}	Drive Select A. When set to 0, this pin activates disk drive A. This is an open-drain output.
DIR#	8	OD_{24}	Direction of the head step motor. An open-drain output. Logic 1 = outward motion Logic 0 = inward motion
STEP#	9	OD_{24}	Step output pulses. This active-low open-drain output produces a pulse to move the head to another track.
WD#	10	OD_{24}	Write data. This logic-low open-drain writes pre-compensation serial data to the selected FDD. An open-drain output.
WE#	11	OD_{24}	Write enable. An open-drain output.
TRAK0#	13	IN_{cs}	Track 0. This Schmitt-trigger input from the disk drive is active-low when the head is positioned over the outermost track. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
WP#	14	IN_{cs}	Write protected. This active-low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.

SYMBOL	PIN	I/O	DESCRIPTION
RDATA#	15	IN_{cs}	The read-data input signal from the FDD. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
HEAD#	16	OD_{24}	Head selection. This open-rain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
DSKCHG#	17	IN_{cs}	Diskette change. This signal is active-low at power-on and whenever the diskette is removed. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.

5.3 Multi-Mode Parallel Port

SYMBOL	PIN	I/O	DESCRIPTION
SLCT	31	IN_{ts}	PRINTER MODE: An active-high input on this pin indicates that the printer is selected. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
WE2#		OD_{12}	EXTENSION FDD MODE: This pin is for Extension FDD B; its function is the same as the WE# pin of FDC. EXTENSION 2FDD MODE: This pin is for Extension FDD A and B; its function is the same as the WE# pin of FDC.
PE	32	IN_{ts}	PRINTER MODE: An active-high input on this pin indicates that the printer has detected the end of the paper. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
WD2#		OD_{12}	EXTENSION FDD MODE: This pin is for Extension FDD B; its function is the same as the WD# pin of FDC. EXTENSION 2FDD MODE This pin is for Extension FDD A and B; its function is the same as the WD# pin of FDC
BUSY	33	IN_{ts}	PRINTER MODE: An active-high input indicates that the printer is not ready to receive data. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
MOB2#		OD_{12}	EXTENSION FDD MODE: This pin is for Extension FDD B; its function is the same as the MOB# pin of FDC. EXTENSION 2FDD MODE: This pin is for Extension FDD A and B; its function is the same as the MOB# pin of FDC.

SYMBOL	PIN	I/O	DESCRIPTION
ACK#	34	IN_{ts}	PRINTER MODE: ACK# An active-low input on this pin indicates that the printer has received data and is ready to accept more data. See the descriptions of the parallel port for the definition of this pin in ECP and EPP modes.
DSB2#		OD_{12}	EXTENSION FDD MODE: This pin is for Extension FDD B; its function is the same as the DSB# pin of FDC. EXTENSION 2FDD MODE: This pin is for Extension FDD A and B; its function is the same as the DSB# pin of FDC.
ERR#	45	IN_{ts}	PRINTER MODE: ERR# An active-low input on this pin indicates that the printer has encountered an error condition. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
HEAD2#		OD_{12}	EXTENSION FDD MODE: This pin is for Extension FDD B; its function is the same as the HEAD# pin of FDC. EXTENSION 2FDD MODE: This pin is for Extension FDD A and B; its function is the same as the HEAD# pin of FDC.
SLIN#	43	OD_{12}	PRINTER MODE: SLIN# Output line for detection of printer selection. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
STEP2#		OD_{12}	EXTENSION FDD MODE: This pin is for Extension FDD B; its function is the same as the STEP# pin of FDC. EXTENSION 2FDD MODE: This pin is for Extension FDD A and B; its function is the same as the STEP# pin of FDC.
INIT#	44	OD_{12}	PRINTER MODE: INIT# Output line for the printer initialization. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
DIR2#		OD_{12}	EXTENSION FDD MODE: This pin is for Extension FDD B; its function is the same as the DIR# pin of FDC. EXTENSION 2FDD MODE: This pin is for Extension FDD A and B; its function is the same as the DIR# pin of FDC.

SYMBOL	PIN	I/O	DESCRIPTION
AFD# DRVDEN02	46	OD_{12} OD_{12}	PRINTER MODE: AFD# An active-low output from this pin causes the printer to auto feed a line after a line is printed. See the description of the parallel port for the definitions of this pin in ECP and EPP modes. EXTENSION FDD MODE: This pin is for Extension FDD B; its function is the same as the DRVDEN0# pin of FDC. EXTENSION 2FDD MODE: This pin is for Extension FDD A and B; its function is the same as the DRVDEN0# pin of FDC.
STB#	47	OD_{12}	PRINTER MODE: STB# An active-low output is used to latch the parallel data into the printer. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
PD0 INDEX2#	42	I/O_{12ts} IN_{ts}	PRINTER MODE: PD0 Parallel port data bus bit 0. See the description of the parallel port for the definitions of this pin in ECP and EPP modes. EXTENSION FDD MODE: This pin is for Extension FDD B; its function is the same as the INDEX# pin of FDC. EXTENSION 2FDD MODE: This pin is for Extension FDD A and B; its function is the same as the INDEX# pin of FDC.
PD1 TRAK02#	41	I/O_{12ts} IN_{ts}	PRINTER MODE: PD1 Parallel port data bus bit 1. See the description of the parallel port for the definitions of this pin in ECP and EPP modes. EXTENSION FDD MODE: This pin is for Extension FDD B; its function is the same as the TRAK0# pin of FDC. EXTENSION 2FDD MODE: This pin is for Extension FDD A and B; its function is the same as the TRAK0# pin of FDC.
PD2 WP2#	40	I/O_{12ts} IN_{ts}	PRINTER MODE: PD2 Parallel port data bus bit 2. See the description of the parallel port for the definitions of this pin in ECP and EPP modes. EXTENSION FDD MODE: This pin is for Extension FDD B; its function is the same as the WP# pin of FDC. EXTENSION 2FDD MODE: This pin is for Extension FDD A and B; its function is the same as the WP# pin of FDC.

SYMBOL	PIN	I/O	DESCRIPTION
PD3 RDATA2#	39	I/O_{12ts} IN_{ts}	PRINTER MODE: PD3 Parallel port data bus bit 3. See the description of the parallel port for the definitions of this pin in ECP and EPP modes. EXTENSION FDD MODE: This pin is for Extension FDD B; its function is the same as the RDATA# pin of FDC. EXTENSION 2FDD MODE: This pin is for Extension FDD A and B; its function is the same as the RDATA# pin of FDC.
PD4 DSKCHG2#	38	I/O_{12ts} IN_{ts}	PRINTER MODE: PD4 Parallel port data bus bit 4. See the description of the parallel port for the definition of this pin in ECP and EPP modes. EXTENSION FDD MODE: This pin is for Extension FDD B; its function is the same as the DSKCHG# pin of FDC. EXTENSION 2FDD MODE: This pin is for Extension FDD A and B; its function is the same as the DSKCHG# pin of FDC.
PD5	37	I/O_{12ts}	PRINTER MODE: PD5 Parallel port data bus bit 5. See the description of the parallel port for the definitions of this pin in ECP and EPP modes. EXTENSION FDD MODE: This pin is a tri-state output. EXTENSION 2FDD MODE:MOA2# This pin is a tri-state output.
PD6 MOA2#	36	I/O_{12ts} OD_{12}	PRINTER MODE: PD6 Parallel port data bus bit 6. See the description of the parallel port for the definitions of this pin in ECP and EPP modes. EXTENSION FDD MODE: This pin is a tri-state output. EXTENSION 2FDD MODE: This pin is for Extension FDD A; its function is the same as the MOA# pin of FDC
PD7 DSA2#	35	I/O_{12ts} OD_{12}	PRINTER MODE: PD7 Parallel port data bus bit 7. See the description of the parallel port for the definitions of this pin in ECP and EPP modes. EXTENSION FDD MODE: This pin is a tri-state output. EXTENSION 2FDD MODE: This pin is for Extension FDD A; its function is the same as the DSA# pin of FDC.

5.4 Serial Port & Infrared Port Interface

SYMBOL	PIN	I/O	DESCRIPTION

SYMBOL	PIN	I/O	DESCRIPTION
RIA#	57	IN_t	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
GP60		I/OD_{12t}	General-purpose I/O port 6 bit 0.
DCDA#	56	INt	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
GP61		I/OD_{12t}	General-purpose I/O port 6 bit 1.
SOUTA	54	O_8	UART A Serial Output. This pin is used to transmit serial data out to the communication link.
PENKBC		IN_t	During power on reset, this pin is pulled down internally and is defined as PENKBC, and the power-on values are shown at CR24 bit 2. The PCB layout should reserve space for a 1-kΩ resistor to pull down this pin to ensure the disabling of KBC, and a 1-kΩ resistor is recommended to pull the pin up If wish to enable KBC.
GP62		I/O_8	General-purpose I/O port 6 bit 2.
SINA	53	IN_t	Serial Input. This pin is used to receive serial data through the communication link.
GP63		I/OD_{12t}	General-purpose I/O port 6 bit 3.
DTRA#	52	O_8	UART A Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
PENROM		IN_t	During power-on reset, this pin is pulled down internally and is defined as PENROM disabled, and the power-on values are shown at CR24 bit 1 (ENROM). The PCB layout should reserve space for a 1-kΩ resistor to pull down this pin to ensure the disabling of SPI interface, and a 1-kΩ resistor is recommended to pull the pin up if wish to enable ROM.
GP64		I/O_8	General-purpose I/O port 6 bit 4.
RTSA#	51	O_8	UART A Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
HEFRAS		IN_t	During power-on reset, this pin is pulled down internally and is defined as HEFRAS, which provides the power-on value for CR26 bit 6 (HEFRAS). The PCB layout should reserve space for a 1-kΩ resistor to pull down this pin so as to ensure the selection of I/O port's configuration address to 2EH, and a 1-kΩ resistor is recommended to pull it up if 4EH is selected as I/O port's configuration address.
GP65		I/O_8	General-purpose I/O port 6 bit 5.
DSRA#	50	IN_t	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
GP66		I/OD_{12t}	General-purpose I/O port 6 bit 6.
CTSA#	49	IN_t	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.

SYMBOL	PIN	I/O	DESCRIPTION
GP67		I/OD_{12t}	General-purpose I/O port 6 bit 7.
RIB#	85	IN_t	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
GP40*		I/OD_{12t}	General-purpose I/O port 4 bit 0.
DCDB#	84	IN_t	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
GP41***		I/OD_{12t}	General-purpose I/O port 4 bit 1.
FAN_SET2	83	IN_t	Determines the initial FAN speed. Power-on configuration for 2 fan speeds, 50% or 100%. When VCC is on, this pin needs a pulled-up or a pulled-down resistor to decide whether the fan speed is 50% or 100%. Only CPUFANOUT1 is supported.
SOUTB		O_{12}	UART B Serial Output. This pin is used to transmit serial data out to the communication link.
IRTX			IR Transmitter output.
GP42*		I/O_{12t}	General-purpose I/O port 4 bit 2. Note: This pin changes to input state during internal PWROK from low to high, then goes back to the previous setting state. (Please see the AP Note 1 of W83627DHG-P)
SINB	82	IN_t	Serial Input. This pin is used to receive serial data through the communication link.
IRRX			IR Receiver input.
GP43***		I/OD_{12t}	General-purpose I/O port 4 bit 3.
DTRB#	81	O_{12}	UART B Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
GP44*		I/OD_{12t}	General-purpose I/O port 4 bit 4.
RTSB#	80	O_{12}	UART B Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
GP45***		I/OD_{12t}	General-purpose I/O port 4 bit 5.
DSRB#	79	IN_t	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
GP46*		I/OD_{12t}	General-purpose I/O port 4 bit 6.
CTSB#	78	IN_t	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
GP47***		I/OD_{12t}	General-purpose I/O port 4 bit 7.

Note: Regarding the * sign, please see 5.12.7 GPIO-4 with WDTO# / SUSLED Multi-function for detailed information.

5.5 KBC Interface

SYMBOL	PIN	I/O	DESCRIPTION
GA20M	59	O_{12}	Gate A20 output. This pin is high after system reset. (KBC P21)

SYMBOL	PIN	I/O	DESCRIPTION
KBRST#	60	O_{12}	Keyboard reset. This pin is high after system reset. (KBC P20)
KCLK	62	I/OD_{16ts}	Keyboard Clock.
GP27		I/OD_{16t}	General-purpose I/O port 2 bit 7.
KDAT	63	I/OD_{16ts}	Keyboard Data.
GP26		I/OD_{16t}	General-purpose I/O port 2 bit 6.
MCLK	65	I/OD_{16ts}	PS2 Mouse Clock.
GP25		I/OD_{16t}	General-purpose I/O port 2 bit 5.
MDAT	66	I/OD_{16ts}	PS2 Mouse Data.
GP24		I/OD_{16t}	General-purpose I/O port 2 bit 4.

5.6 Serial Peripheral Interface

The SPI employs a master-slave model and typically has three signal lines: serial data input line (SI), serial data output line (SO), and serial clock line (SCK). Different slaves are addressed on the bus by chip select signals from the master. The data bits are first shifted in/out the most significant bit (MSB). The data are often shifted simultaneously out from the output pin and into the input pin. Among the parameters, only the communication lines and the clock edge are defined by the SPI. The others differ from device to device.

SPI Operation

To initiate the data transfer between the W83627DHG-P and a slave device, SCE# must go low. This synchronizes the slave device with the W83627DHG-P. Data can now be transferred between the W83627DHG-P and the slave device in one of two modes: the data is sampled either on the rising or the falling edge of the clock.

In a slave device, a logic low is received on the SCE# line and the clock input is at the SCK pin, which synchronizes the slave with the W83627DHG-P. Data is then received serially at the SI pin. During a write cycle, data is shifted out to the SO pin on clocks from the W83627DHG-P.

SYMBOL	PIN	I/O	DESCRIPTION
SCE#	19	O_{12}	Serial flash ROM interface chip selection.
GP22		I/OD_{12t}	General-purpose I/O port 2 bit 2.
SCK	2	O_{12}	Clock output for serial flash.
GP23		I/OD_{12t}	General-purpose I/O port 2 bit 3.
SO	118	O_{8}	Transfer commands, addresses or data to serial flash. This pin is connected to SI of serial flash.
BEEP		OD_{8}	Beep function for hardware monitor. This pin is low after system reset.
SI	58	IN_{ts}	Receive data from serial flash. This pin is connected to SO of serial flash.
AUXFANIN1		I/O_{12ts}	0 to +3 V amplitude fan tachometer input.

5.7 Hardware Monitor Interface

SYMBOL	PIN	I/O	DESCRIPTION
BEEP	118	OD_8	Beep function for hardware monitor. This pin is low after system reset.
SO		O_8	Transfer commands, address or data to serial flash. This pin is connected to SI of serial flash.
CASEOPEN#	76	IN_t	CASE OPEN detection. An active-low input from an external device when the case is open. This signal can be latched if pin VBAT is connected to the battery, even if the W83627DHG-P is turned off. Pulling up a 2-MΩ resistor to VBAT is recommended if not in use.
VIN3	96	AIN	Analog Inputs for voltage measurement (Range: 0 to 2.048 V)
VIN2	97	AIN	Analog Inputs for voltage measurement (Range: 0 to 2.048 V)
VIN1	98	AIN	Analog Inputs for voltage measurement (Range: 0 to 2.048 V)
VIN0	99	AIN	Analog Inputs for voltage measurement (Range: 0 to 2.048 V)
CPUVCORE	100	AIN	Analog Inputs for voltage measurement (Range: 0 to 2.048 V)
VREF	101	AOUT	Reference Voltage (2.048 V).
AUXTIN	102	AIN	The input of temperature sensor 3. It is used for temperature sensing.
CPUTIN	103	AIN	The input of temperature sensor 2. It is used for CPU temperature sensing.
SYSTIN	104	AIN	The input of temperature sensor 1. It is used for system temperature sensing.
OVT#	5	OD_{12}	The output of over temperature Shutdown. This pin indicates the temperature is over the temperature limit. (Default after LRESET#)
SMI#		OD_{12}	System Management Interrupt channel output.
VID7 VID6 VID5 VID4 VID3 VID2 VID1 VID0	121 122 123 124 125 126 127 128	I/O_{12}	VID input detection, also with output control.
AUXFANIN1	58	I/O_{12ts}	0 to +3 V amplitude fan tachometer input.
SI		IN_{ts}	Receive data from serial flash. This pin is connected to SO of serial flash..

SYMBOL	PIN	I/O	DESCRIPTION
AUXFANIN0	111	I/O_{12ts}	0 to +3 V amplitude fan tachometer input.
CPUFANIN0	112		
SYSFANIN	113		
CPUFANIN1	119	I/O_{12ts}	0 to +3 V amplitude fan tachometer input. (Default)
GP21		I/OD_{12t}	General-purpose I/O port 2 bit 1.
AUXFANOUT	7	AOUT/ OD_{12}/ O_{12}	DC/PWM fan output control. CPUFANOUT0 and AUXFANOUT are default PWM mode, CPUFANOUT1 and SYSFANOUT are default DC mode.
CPUFANOUT0	115		
SYSFANOUT	116		
CPUFANOUT1	120	AOUT/ O_{12}/ OD_{12}	DC/PWM fan output control. (Default) CPUFANOUT0 and AUXFANOUT are default PWM mode, CPUFANOUT1 and SYSFANOUT are default DC mode.
GP20		I/OD_{12t}	General-purpose I/O port 2 bit 0.
FAN_SET	117	IN_{td}	Determines the initial FAN speed. Power on configuration for 2 fan speeds, 50% or 100%. During power-on reset, this pin is pulled down internally and the fan speed is 50%. Only CPUFANOUT0 is supported.
PLED		O_{12}	Power LED output. Drive high 3.3 V after strapping.

5.8 PECI Interface

SYMBOL	PIN	I/O	DESCRIPTION
PECI_REQ#	110	OD_{12}	INTEL® CPU PECI interface.
PECI	108	I/O_{V3}	INTEL® CPU PECI interface. Connect to CPU.
Vtt	107	Power	INTEL® CPU Vtt Power. This pin is connected to GND if the PECI function is not in use.
PECISB	106	I/O_{V3}	INTEL® CPU PECI interface. Connect to ICH8.

5.9 SST Interface

SYMBOL	PIN	I/O	DESCRIPTION
SST	114	I/O_{V4}	Simple Serial Transport (SST) Interface.

5.10 Advanced Configuration and Power Interface

The Advanced Configuration and Power Interface (ACPI) is an interface that allows OS-directed Power Management (OSPM). The ACPI replaces the APM (Advanced Power Management), MPS (Multiprocessor Specification), and PnP BIOS Specification. In addition to power management, the ACPI supports the functions of thermal management, state management, and speed control, as well as the global system states and different device power states. Two of the primary states that the W83627DHG-P supports are the S0 (working) and S3 (suspend to RAM) states. S0 is a full-power state, in which the computer is actively used. S3 is a sleeping state, in which the processor is powered down, but the memory, where the last procedural state is stored, is still active. By employing the ACPI, the system conserves more energy through transiting unused devices into lower power states, including placing the entire system in a low-power state when possible.

SYMBOL	PIN	I/O	DESCRIPTION
PSIN#	68	IN_{tu}	Panel Switch Input. This pin is active-low with an internal pulled-up resistor.
GP56		I/OD_{12t}	General-purpose I/O port 5 bit 6.
PSOUT#	67	OD_{12}	Panel Switch Output. This signal is used to wake-up the system from S3/S5 state.
GP57		I/OD_{12t}	General-purpose I/O port 5 bit 7.
RSMRST#	75	OD_{12}	Resume reset signal output.
GP51		I/OD_{12t}	General-purpose I/O port 5 bit 1.
SUSB#	73	IN_t	System S3 state input.
GP52		I/OD_{12t}	General-purpose I/O port 5 bit 2.
PSON#	72	OD_{12}	Power supply on-off output.
GP53		I/OD_{12t}	General-purpose I/O port 5 bit 3.
PWROK	71	OD_{12}	This pin generates the PWROK signal while 3VCC comes in.
GP54		I/OD_{12t}	General-purpose I/O port 5 bit 4.
RSTOUT0#	94	OD_{12}	PCI Reset Buffer 0.
RSTOUT1#	93	O_{12}	PCI Reset Buffer 1.
RSTOUT2#	90	O_{12}	PCI Reset Buffer 2. (Default)
GP32		I/OD_{12t}	General-purpose I/O port 3 bit 2.
SCL		IN_{ts}	Serial Bus clock.
RSTOUT3#	89	O_{12}	PCI Reset Buffer 3. (Default)
GP33		I/OD_{12t}	General-purpose I/O port 3 bit 3.
SDA		I/OD_{12ts}	Serial bus bi-directional Data.
RSTOUT4#	88	O_{12}	PCI Reset Buffer 4. (Default)
GP34		I/OD_{12t}	General-purpose I/O port 3 bit 4.

5.11 SMBus Interface

SYMBOL	PIN	I/O	DESCRIPTION
RSTOUT2#	90	O_{12}	PCI Reset Buffer 2. (Default)
GP32		I/OD_{12t}	General-purpose I/O port 3 bit 2.
SCL		IN_{ts}	Serial Bus clock.
RSTOUT3#	89	O_{12}	PCI Reset Buffer 3. (Default)
GP33		I/OD_{12t}	General-purpose I/O port 3 bit 3.
SDA		I/OD_{12ts}	Serial bus bi-directional Data.

5.12 General Purpose I/O Port

5.12.1 GPIO Power Source

SYMBOL	POWER SOURCE
GPIO port 2 (Bit0-3)	3VCC
GPIO port 2 (Bit4-7)	3VSB
GPIO port 3	3VSB
GPIO port 4	3VSB
GPIO port 5	3VSB
GPIO port 6	3VCC

5.12.2 GPIO-2 Interface

SYMBOL	PIN	I/O	DESCRIPTION
GP20	120	I/OD_{12t}	General-purpose I/O port 2 bit 0.
CPUFANOUT1		AOUT/ $OD_{12/}$ O_{12}	DC/PWM fan output control. (Default) CPUFANOUT0 and AUXFANOUT are default PWM mode, CPUFANOUT1 and SYSFANOUT are default DC mode.
GP21	119	I/OD_{12t}	General-purpose I/O port 2 bit 1.
CPUFANIN1		I/O_{12ts}	0 to +3 V amplitude fan tachometer input. (Default)
GP22	19	I/OD_{12t}	General-purpose I/O port 2 bit 2.
SCE#		O_{12}	Serial flash ROM interface chip selection.
GP23	2	I/OD_{12t}	General-purpose I/O port 2 bit 3.
SCK		O_{12}	Clock output for serial flash.
GP24	66	I/OD_{16t}	General-purpose I/O port 2 bit 4.
MDAT		I/OD_{16ts}	PS2 Mouse Data.
GP25	65	I/OD_{16t}	General-purpose I/O port 2 bit 5.
MCLK		I/OD_{16ts}	PS2 Mouse Clock.

SYMBOL	PIN	I/O	DESCRIPTION
GP26	63	I/OD_{16t}	General-purpose I/O port 2 bit 6.
KDAT		I/OD_{16ts}	Keyboard Data.
GP27	62	I/OD_{16t}	General-purpose I/O port 2 bit 7.
KCLK		I/OD_{16ts}	Keyboard Clock.

5.12.3 GPIO-3 Interface

SYMBOL	PIN	I/O	DESCRIPTION
GP30	92	I/OD_{12t}	General-purpose I/O port 3 bit 0.
PWROK2		OD_{12}	This pin generates the PWROK2 signal while 3VCC comes in.
GP31	91	I/OD_{12t}	General-purpose I/O port 3 bit 1.
VSBGATE#		O_{12}	Switch 3VSB power to memory when in S3 state. The default is disabled while the particular ACPI functions are enabled. The control bit is at Logical Device A, CR [E4h] bit 4.
GP32	90	I/OD_{12t}	General-purpose I/O port 3 bit 2.
RSTOUT2#		O_{12}	PCI Reset Buffer 2. (Default)
SCL		IN_{ts}	Serial Bus clock.
GP33	89	I/OD_{12t}	General-purpose I/O port 3 bit 3.
RSTOUT3#		O_{12}	PCI Reset Buffer 3. (Default)
SDA		I/OD_{12ts}	Serial bus bi-directional Data.
GP34	88	I/OD_{12t}	General-purpose I/O port 3 bit 4.
RSTOUT4#		O_{12}	PCI Reset Buffer 4. (Default)
GP35	87	I/OD_{12t}	General-purpose I/O port 3 bit 5.
ATXPGD		IN_t	ATX power good input signal. It is connected to the PWROK signal from the power supply for PWROK/PWROK2 generation. The default is enabled.
GP36	69	I/OD_{12t}	General-purpose I/O port 3 bit 6.
FTPRST#		IN_t	Connect to the reset button. This pin has internal de-bounce circuit whose de-bounce time is at least 32 mS.
GP37	64	I/OD_{12t}	General-purpose I/O port 3 bit 7.
SUSC#		IN_t	SLP_S5# input.

5.12.4 GPIO-4 Interface

See 5.4 Serial Port & Infrared Port Interface

5.12.5 GPIO-5 Interface

SYMBOL	PIN	I/O	DESCRIPTION
GP50	77	I/O_{12t}	General-purpose I/O port 5 bit 0. (Default after strapping)
EN_GTL		IN_{cu}	During VSB power reset (RSMRST#), this pin is pulled high internally and is defined as VID transition voltage level (GTL or TTL), and the value is shown at CR2C bit 3. The PCB layout should reserve space for a 1-kΩ resistor to pull down this pin if TTL is the selected VID level.
WDTO#		O_{12}	Watchdog Timer output signal.
GP51	75	I/OD_{12t}	General-purpose I/O port 5 bit 1.
RSMRST#		OD_{12}	Resume reset signal output.
GP52	73	I/OD_{12t}	General-purpose I/O port 5 bit 2.
SUSB#		IN_t	System S3 state input.
GP53	72	I/OD_{12t}	General-purpose I/O port 5 bit 3.
PSON#		OD_{12}	Power supply on-off output.
GP54	71	I/OD_{12t}	General-purpose I/O port 5 bit 4.
PWROK		OD_{12}	This pin generates the PWROK signal while 3VCC comes in.
GP55	70	I/O_{12t}	General-purpose I/O port 5 bit 5. (Default)
EN_ACPI		IN_{cd}	During VSB power reset (RSMRST#), this pin is pulled down internally and is defined as EN_ACPI (enabling particular ACPI functions), which provides the value for CR2C bit 4 (EN_ACPI). The PCB layout should reserve space for a 1-kΩ resistor to pull down this pin to ensure successful disabling of particular ACPI functions, and a 1-kΩ resistor is recommended to pull the pin up if wish to enable particular ACPI functions.
SUSLED		O_{12}	Suspended LED output.
GP56	68	I/OD_{12t}	General-purpose I/O port 5 bit 6.
PSIN#		IN_{tu}	Panel Switch Input. This pin is active-low with an internal pulled-up resistor.
GP57	67	I/OD_{12t}	General-purpose I/O port 5 bit 7.
PSOUT#		OD_{12}	Panel Switch Output. This signal is used to wake-up the system from S3/S5 state.

5.12.6 GPIO-6 Interface

See 5.4 Serial Port & Infrared Port Interface

5.12.7 GPIO-4 with WDTO# / SUSLED Multi-function

SYMBOL	PIN	I/O	DESCRIPTION
GPxx*	---	I/OD_{12t}	This GPxx* can serve as GPIO or the Watchdog Timer output signals.
WDTO#		OD_{12}	
GPxx***	---	I/OD_{12t}	This GPxx*** can serve as GPIO or Suspend-LED output signals.
SUSLED		OD_{12}	

5.13 Particular ACPI Function pins

SYMBOL	PIN	I/O	DESCRIPTION
SUSC#	64	IN_t	SLP_S5# input.
GP37		I/OD_{12t}	General-purpose I/O port 3 bit 7
EN_ACPI	70	IN_{cd}	During VSB power reset (RSMRST#), this pin is pulled down internally and is defined as EN_ACPI (enabling particular ACPI functions), which provides the value for CR2C bit 4 (EN_ACPI). The PCB layout should reserve space for a 1-kΩ resistor to pull down this pin to ensure successful disabling of particular ACPI functions, and a 1-kΩ resistor is recommended to pull the pin up if wish to enable particular ACPI functions.
GP55		I/O_{12t}	General-purpose I/O port 5 bit 5.
SUSLED		O_{12}	Suspended LED output.
VSBGATE#	91	O_{12}	Switch 3VSB power to memory when in S3 state. The default is disabled while the particular ACPI functions are enabled. The control bit is at Logical Device A, CR [E4h] bit 4.
GP31		I/OD_{12t}	General-purpose I/O port 3 bit 1.
PWROK2	92	OD_{12}	This pin generates the PWROK2 signal while 3VCC comes in.
GP30		I/OD_{12t}	General-purpose I/O port 3 bit 0.
ATXPGD	87	IN_t	ATX power good input signal. It is connected to the PWROK signal from the power supply for PWROK/PWROK2 generation. The default is enabled.
GP35		I/OD_{12}	General-purpose I/O port 3 bit 5.
FTPRST#	69	IN_t	Connect to the reset button. This pin has internal de-bounce circuit whose de-bounce time is at least 32 mS.
GP36		I/OD_{12}	General-purpose I/O port 3 bit 6.

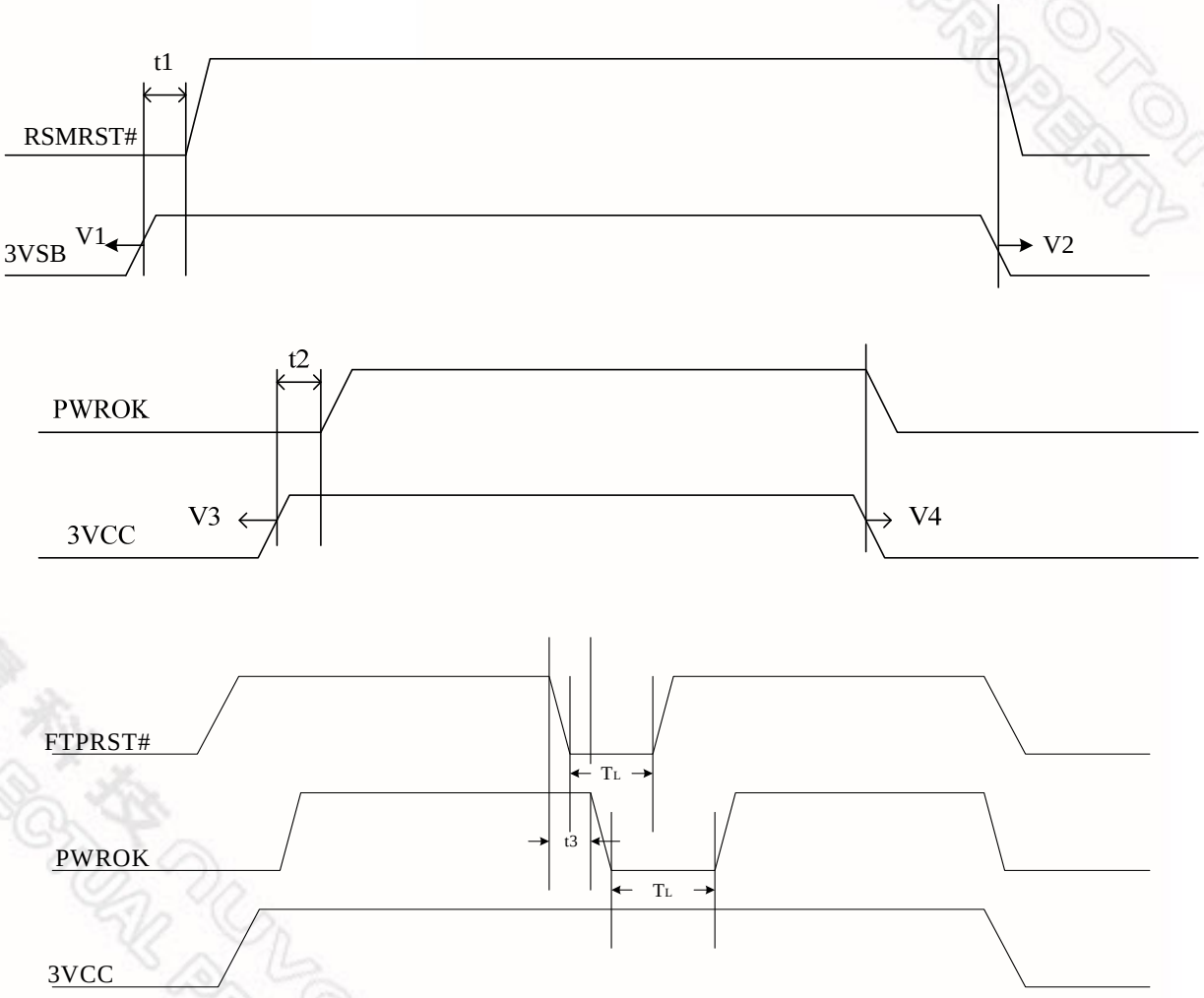
5.14 POWER PINS

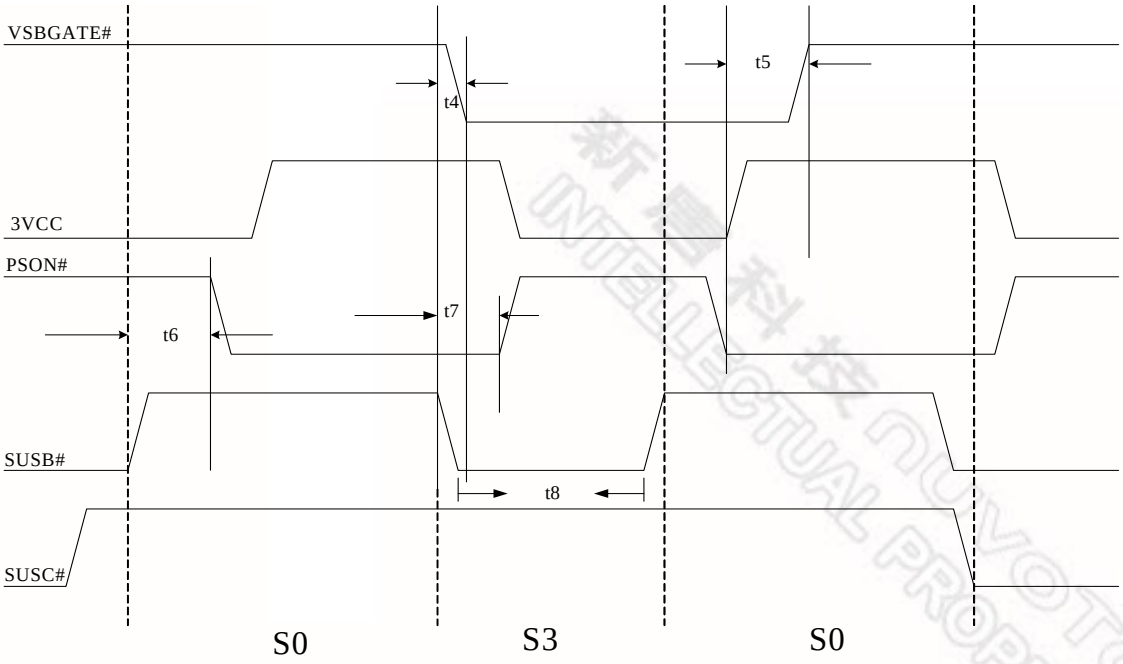
SYMBOL	PIN	DESCRIPTION
3VSB	61	+3.3 V stand-by power supply for the digital circuits.

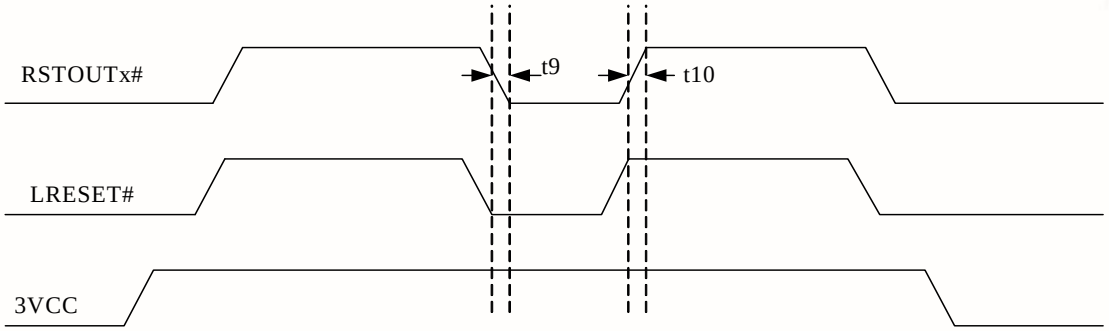
SYMBOL	PIN	DESCRIPTION
VBAT	74	+3 V on-board battery for the digital circuits.
3VCC	12,28,48	+3.3 V power supply for driving 3 V on host interface.
AVCC	95	Analog +3.3 V power input. Internally supply power to all analog circuits.
CPUD-(AGND)	105	Analog ground. The ground reference for all analog input. Internally connected to all analog circuits.
VSS	20,55	Ground.
Vtt	107	INTEL® CPU Vtt power.

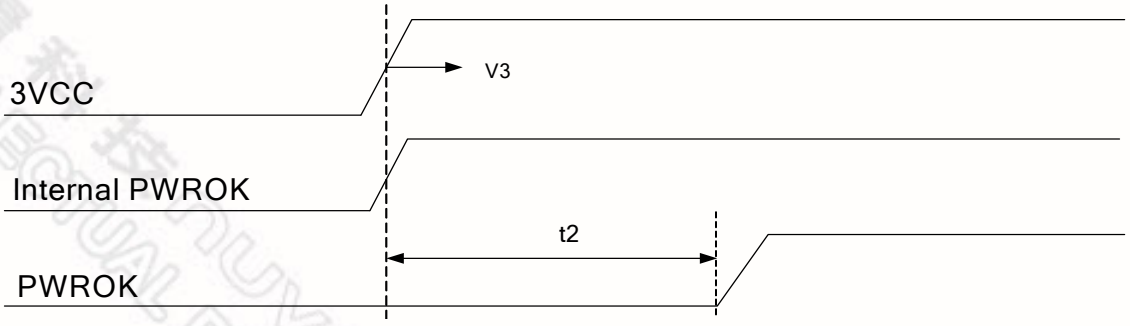
6. ACPI GLUE LOGIC

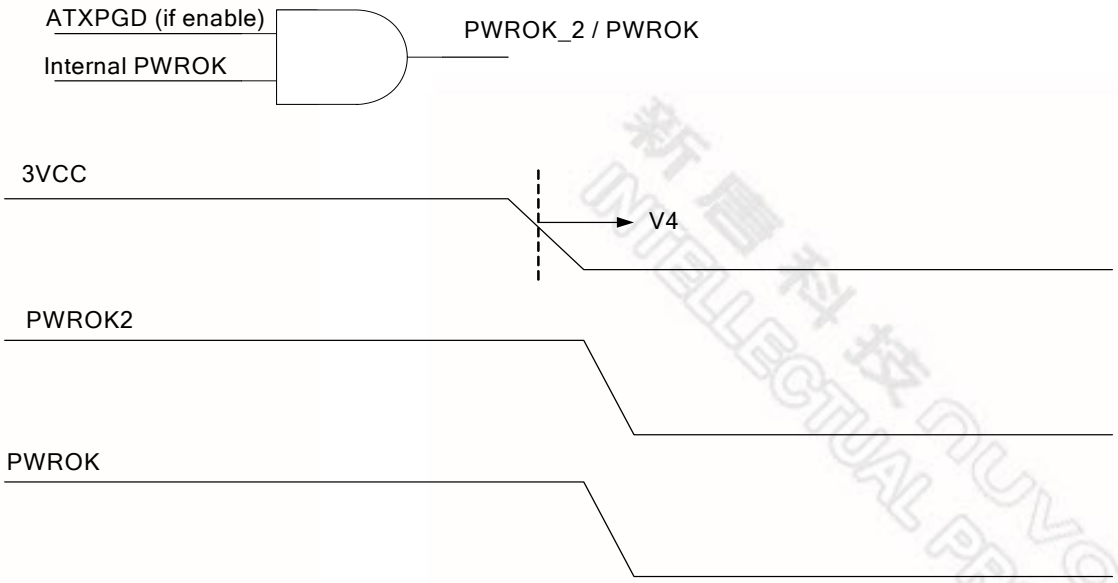
SYMBOL	PIN	DESCRIPTION
SUSC#	64	SLP_S5# input.
FTPRST#	69	Connect to the reset button. This pin has internal de-bounce circuit whose de-bounce time is at least 32 mS.
VSBGATE#	91	Switch 3VSB power to memory when in S3 state.
PWROK	71	This pin generates the PWRGD signals while 3VCC is present.
ATXPGD	87	ATX power good input signal. It is connected to the PWROK signal from the power supply for PWROK/PWRGD generation. The default is enabled.




VSBGATE#
t4
t5
3VCC
PSON#
t6
t7
SUSB#
t8
SUSC#
S0
S3
S0


RSTOUTx#
t9
t10
LRESET#
3VCC


3VCC
V3
Internal PWROK
t2
PWROK



TIMING	PARAMETER	MIN	MAX	UNIT
t1	Valid 3VSB to RSMRST# inactive	100	200	mS
t2	Valid 3VCC to PWROK/PWRGD active	300	500	mS
t3	FTPRST# active to PWROK/PWRGD active	28	39	mS
t4	SUSB# active to VSBGATE# active	0	80	nS
t5	PSON# active to VSBGATE# inactive	90	142	mS
t6	SUSB# inactive to PSON# active	0	80	nS
t7	SUSB# active to PSON# inactive	28	39	mS
t8	SUSB# minimal Low Time	40	-	mS
t9	LRESET# active to RSTOUTx# active	0	80	nS
t10	LRESET# inactive to RSTOUTx# inactive	0	80	nS

DC	PARAMETER	MIN	TYPICAL	MAX	UNIT
V1	3VSB Valid Voltage	-	-	3.0	Volt
V2	3VSB Ineffective Voltage	2.4	-	-	Volt
V3	3VCC Valid Voltage	-	-	3.0	Volt
V4	3VCC Ineffective Voltage	2.4	-	-	Volt

Note： 1. The values above are the worst-case results of R&D simulation.
2. The length of T_L level is based on the length of the low level of FTPRST#

7. CONFIGURATION REGISTER ACCESS PROTOCOL

The W83627DHG-P uses Super I/O protocol to access configuration registers to set up different types of configurations. The W83627DHG-P has totally twelve Logical Devices (from Logical Device 0 to Logical Device C with the exception of Logical Device 4 for backward compatibility) corresponding to twelve individual functions: FDC (Logical Device 0), Parallel Port (Logical Device 1), UARTA (Logical Device 2), UARTB (Logical Device 3), Keyboard Controller (Logical Device 5), SPI (Serial Peripheral Interface, Logical Device 6), GPIO6 (Logical Device 7), WDTO# & PLED (Logical Device 8), GPIO2, 3, 4, 5 (Logical Device 9), ACPI (Logical Device A), Hardware Monitor (Logical Device B), and PECI & SST (Logical Device C). Each Logical Device has its own configuration registers (above CR30). The host can access those registers by writing an appropriate Logical Device Number into the Logical Device select register at CR7. Please note that GPIO1 is not defined in the W83627DHG-P.

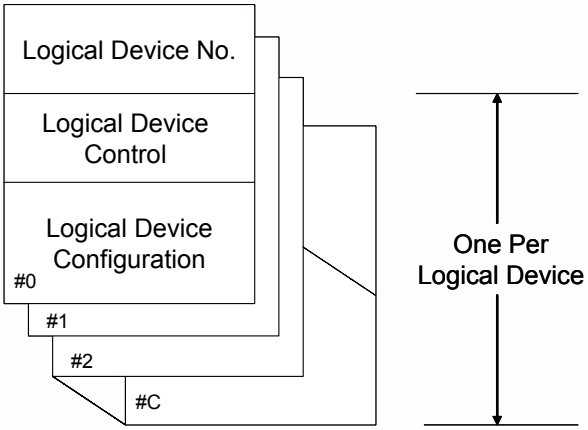


Figure 7-1 Structure of the Configuration Register

LOGICAL DEVICE NUMBER	FUNCTION	I/O BASE ADDRESS
0	FDC	100h ~ FF8h
1	Parallel Port	100h ~ FF8h
2	UART A	100h ~ FF8h
3	UART B	100h ~ FF8h
4	Reserved	
5	Keyboard Controller	100h ~ FFFh
6	Serial Peripheral Interface	100h ~ FF8h
7	GPIO 6	100h ~ FFFh
8	WDTO# & PLED	Reserved
9	GPIO 2, 3, 4, 5	Reserved
A	ACPI	Reserved

LOGICAL DEVICE NUMBER	FUNCTION	I/O BASE ADDRESS
B	Hardware Monitor	100h ~ FFEh
C	PECI & SST	Reserved

Figure 7-2 Devices of I/O Base Address

7.1 Configuration Sequence

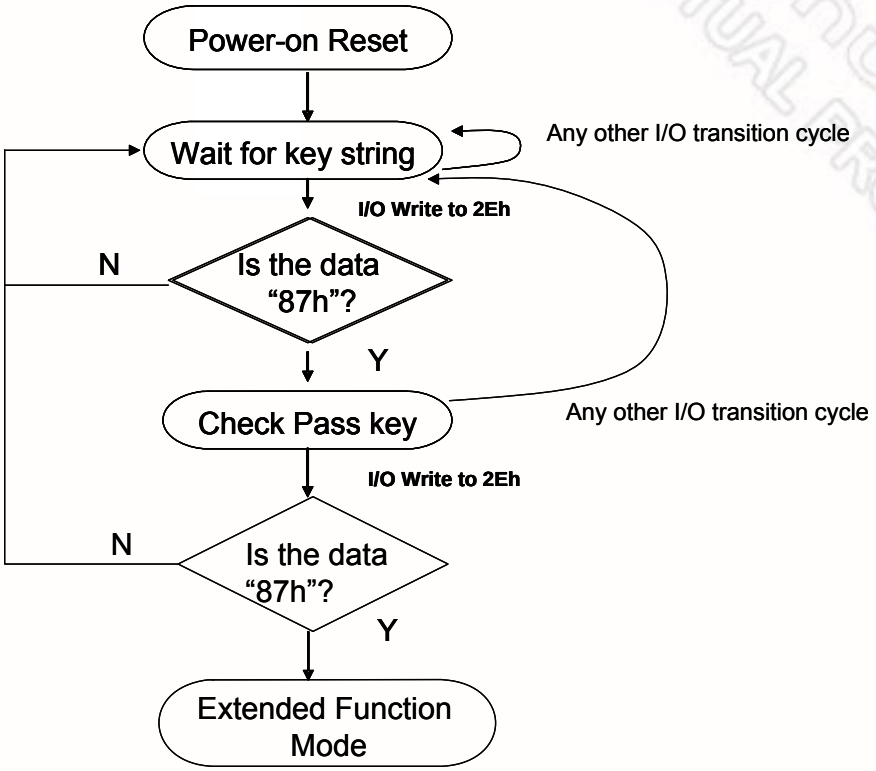


Figure 7-3 Configuration Register

To program the W83627DHG-P configuration registers, the following configuration procedures must be followed in sequence:

(1). Enter the Extended Function Mode.

(2). Configure the configuration registers.

(3). Exit the Extended Function Mode.

7.1.1 Enter the Extended Function Mode

To place the chip into the Extended Function Mode, two successive writes of 0x87 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh).

7.1.2 Configure the Configuration Registers

The chip selects the Logical Device and activates the desired Logical Devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). The EFIR is located at the same address as the EFER, and the EFDR is located at address (EFIR+1).

First, write the Logical Device Number (i.e. 0x07) to the EFIR and then write the number of the desired Logical Device to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required.

Secondly, write the address of the desired configuration register within the Logical Device to the EFIR and then write (or read) the desired configuration register through the EFDR.

7.1.3 Exit the Extended Function Mode

To exit the Extended Function Mode, writing 0xAA to the EFER is required. Once the chip exits the Extended Function Mode, it is in the normal running mode and is ready to enter the configuration mode.

7.1.4 Software Programming Example

The following example is written in Intel 8086 assembly language. It assumes that the EFER is located at 2Eh, so the EFIR is located at 2Eh and the EFDR is located at 2Fh. If the HEFRAS (CR26 bit 6) is set, 2Eh can be directly replaced by 4Eh and 2Fh replaced by 4Fh.

```
;-----------------------------------------------------
; Enter the Extended Function Mode
;-----------------------------------------------------
MOV    DX, 2EH
MOV    AL, 87H
OUT    DX, AL
OUT    DX, AL
;-------------------------------------------------------------------------------
; Configure Logical Device 1, Configuration Register CRF0
;-------------------------------------------------------------------------------
MOV    DX, 2EH
MOV    AL, 07H
OUT    DX, AL          ; point to Logical Device Number Reg.
MOV    DX, 2FH
MOV    AL, 01H
OUT    DX, AL          ; select Logical Device 1
;
MOV    DX, 2EH
```

```
MOV     AL, F0H
OUT     DX, AL          ; select CRF0
MOV     DX, 2FH
MOV     AL, 3CH
OUT     DX, AL          ; update CRF0 with value 3CH
;-------------------------------------------------------------------------
; Exit the Extended Function Mode
;-------------------------------------------------------------------------
MOV     DX, 2EH
MOV     AL, AAH
OUT     DX, AL
```

Figure 7-4 Chip (Global) Control Registers

INDEX	R/W	DEFAULT VALUE	DESCRIPTION
02h	Write Only		Software Reset
07h	R/W	00h	Logical Device
20h	Read Only	B0h	Chip ID, MSB
21h	Read Only	7xh	Chip ID, LSB
22h	R/W	FFh	Device Power Down
23h	R/W	00h	Immediate Power Down
24h	R/W	0100_0ss0b	Global Option
25h	R/W	00h	Interface Tri-state Enable
26h	R/W	0s000000b	Global Option
27h	Reserved		
28h	R/W	50h	Global Option
29h	R/W	00h	Multi-function Pin Selection
2Ah	R/W	00h	SPI Configuration
2Bh	Reserved		
2Ch	R/W	E2h	Multi-function Pin Selection
2Dh	R/W	21h	Multi-function Pin Selection
2Eh	R/W	00h	Reserved
2Fh	R/W	00h	Reserved

S: Strapping; x: chip version.

8. HARDWARE MONITOR

8.1 General Description

The W83627DHG-P monitors several critical parameters in PC hardware, including power supply voltages, fan speeds, and temperatures, all of which are very important for a high-end computer system to work stably and properly.

The W83627DHG-P can simultaneously monitor all of the following inputs:

- Nine analog voltage inputs (four intrinsic monitor VBAT, 3VSB, 3VCC and AVCC power; five externally monitored power)
- Five fan tachometer inputs
- Three remote temperatures, by thermistor or from the CPU thermal-diode output (voltage or Current Mode)
- One case-open detection signal.

These inputs are converted to digital values using a built-in, eight-bit analog-to-digital converter (ADC).

In response to these inputs, the W83627DHG-P can generate the following outputs:

- Four PWM (pulse width modulation) or DC fan outputs for the fan speed control
- Beep tone output for warnings
- SMI#
- OVT# signals for system protection events

The W83627DHG-P provides hardware access to all monitored parameters through the LPC or I^2C interface and software access through application software, such as Nuvoton's Hardware Doctor™, or BIOS. In addition, the W83627DHG-P can generate pop-up warnings or beep tones when a parameter goes outside of a user-specified range.

The rest of this section introduces the various features of the W83627DHG-P hardware-monitor capability. These features are divided into the following sections:

- Access Interfaces
- Analog Inputs
- Fan Speed Measurement and Control
- Smart Fan Control
- SMI# interrupt mode
- OVT# interrupt mode
- Registers and Value RAM

8.2 Access Interfaces

The W83627DHG-P provides two interfaces, LPC and I^2C, for the microprocessor to read or write the internal registers of the hardware monitor.

8.2.1 LPC Interface

This interface uses the LPC bus to access the index and data ports. These two ports are located at the 16-bit port specified in CR60 and CR61, plus 5h and 6h, respectively. If the 16-bit port value is 290h, so the default index and data port addresses are 295h and 296h, respectively. The structure of the internal registers is shown in the following figure.

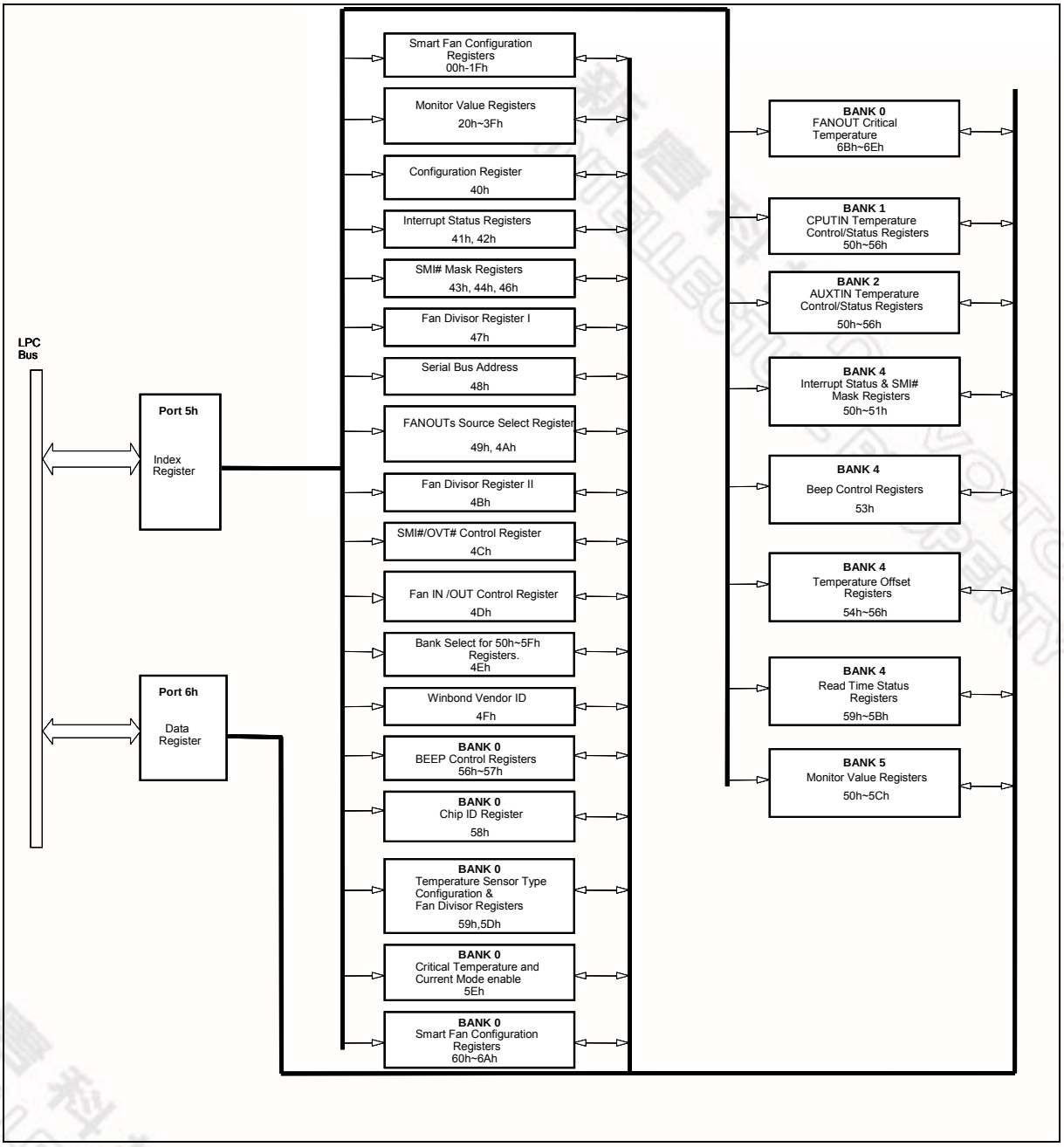


Figure 8-1 LPC Bus' Reads from / Writes to Internal Registers

8.2.2 I²C interface

This interface uses the I²C Serial Bus to access the internal registers. The W83627DHG-P has a programmable serial-bus address that is controlled by index 48h.

The two timing diagrams below illustrate how to use the I²C interface to write to an internal register and how to read the value in an internal register, respectively.

(a) Serial bus write to internal address register followed by the data byte

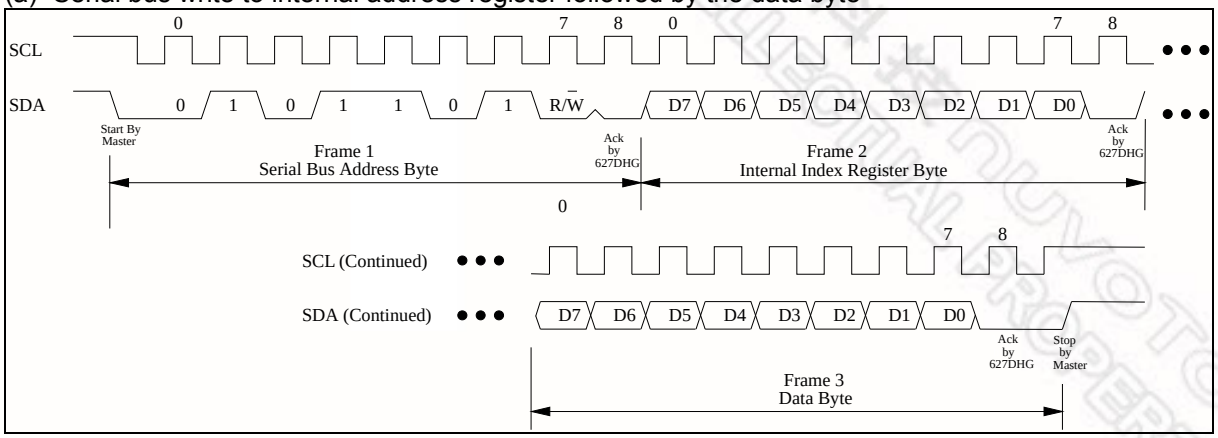


Figure 8-2 Serial Bus Write to Internal Address Register Followed by the Data Byte

(b) Serial bus read from a register

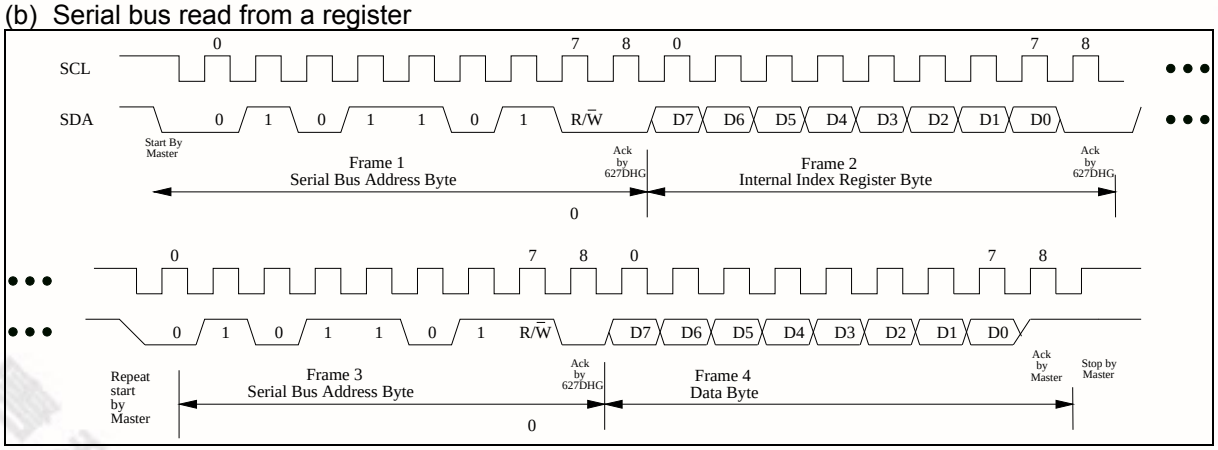


Figure 8-3 Serial Bus Read from Internal Address Register

8.3 Analog Inputs

The maximum input voltage on analog pins is 2.048 V because the 8-bit ADC has an 8-mV LSB. Usually, the voltage ports of CPU Vcore (pin 100), battery (pin 74), 3VSB (pin 61), 3VCC (pin 12), and AVCC (pin 95) can be directly connected to their respective analog pins, as illustrated in the figure below.

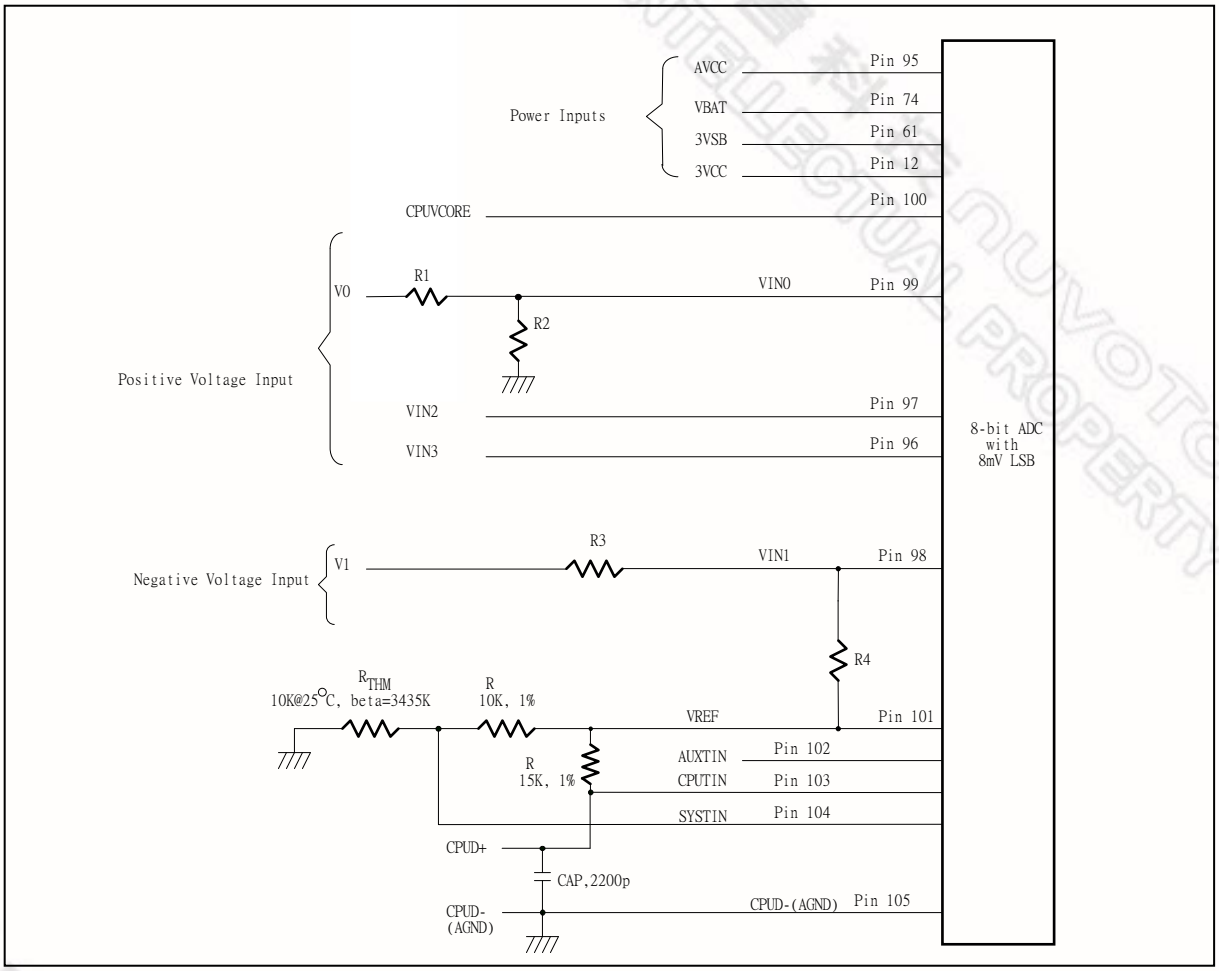


Figure 8-4 Analog Inputs and Application Circuit of the W83627DHG-P

As illustrated in the figure above, other connections may require some external circuits. The rest of this section provides more information about voltages outside the range of the 8-bit ADC, CPU Vcore voltage detection, and temperature sensing

8.3.1 Voltages Over 2.048 V or Less Than 0 V

Input voltages greater than 2.048 V should be reduced by external resistors to keep the input voltages in the proper range. For example, input voltage V_0 (+12 V) should be reduced before it is connected to VIN0 according to the following equation:

$$VIN0 = V_0 \times \frac{R_2}{R_1 + R_2}$$

R1 and R2 can be set to 56 KΩ and 10 KΩ, respectively, to reduce V_0 from +12 V to less than 2.048 V.

The W83627DHG-P uses the same approach. Pins 12 and 95 provide two functions. One, these pins are connected to VCC at +3.3 V to supply internal (digital / analog) power to the W83627DHG-P. Two, these pins monitor VCC. The W83627DHG-P has two internal, 34-KΩ serial resistors that reduce the ADC-input voltage to 1.65 V.

$$V_{in} = VCC \times \frac{34K\Omega}{34K\Omega + 34K\Omega} \cong 1.65V$$, where VCC is set to 3.3V

Pin 61 is implemented likewise to monitor its +3.3 V stand-by power supply.

Negative voltages are handled similarly, though the equation looks a little more complicated. For example, negative voltage V1 (-12V) can be reduced according to the following equation:

$$VIN1 = (V_1 - 2.048) \times \frac{R_4}{R_3 + R_4} + 2.048, where V_1 = -12$$

R3 and R4 can be set to 232 KΩ and 10 KΩ, respectively, to reduce negative input voltage V_1 from –12 V to less than 2.048 V.

Both of these solutions are illustrated in the figure above.

8.3.2 Voltage Detection

The data format for voltage detection is an eight-bit value, and each unit represents an interval of 8 mV.

Detected Voltage = Reading * 0.008 V

If the source voltage was reduced, the detected voltage value may have to be scaled up accordingly.

8.3.3 Temperature Sensing

The data format for sensor SYSTIN is 8-bit, two's-complement, and the data format for sensors CPUTIN and AUXTIN is 9-bit, two's-complement. This is illustrated in the table below.

Table 8-1 Temperature Data Format

TEMPERATURE	8-BIT DIGITAL OUTPUT		9-BIT DIGITAL OUTPUT	
	8-BIT BINARY	8-BIT HEX	9-BIT BINARY	9-BIT HEX
+125°C	0111,1101	7Dh	0,1111,1010	0FAh
+25°C	0001,1001	19h	0,0011,0010	032h
+1°C	0000,0001	01h	0,0000,0010	002h
+0.5°C	-	-	0,0000,0001	001h
+0°C	0000,0000	00h	0,0000,0000	000h
-0.5°C	-	-	1,1111,1111	1FFh
-1°C	1111,1111	FFh	1,1111,1110	1FFh
-25°C	1110,0111	E7h	1,1100,1110	1CEh
-55°C	1100,1001	C9h	1,1001,0010	192h

Eight-bit temperature data is read from Index [27h]. For nine-bit temperature data, the 8 MSB are read from Bank1 / Bank2 Index [50h], and the LSB is read from Bank1 / Bank2 Index [51h], bit 7.
There are two sources of temperature data: external thermistors or thermal diodes.

8.3.3.1. Monitor Temperature From Thermistor

External thermistors should have a β value of 3435K and a resistance of 10 KΩ at 25°C. As illustrated in the schematic below, the thermistor is connected in series with a 10-KΩ resistor and then connects to VREF (pin 101).

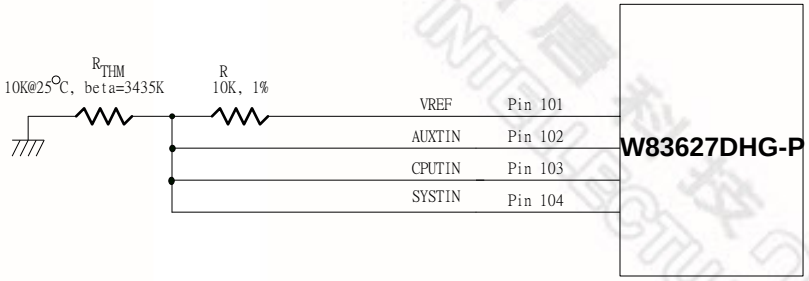


Figure 8-5 Monitoring Temperature from Thermistor

8.3.3.2. Monitor Temperature from Thermal Diode (Voltage Mode)

The thermal diode D- pin is connected to CPUD- (pin 105), and the D+ pin is connected to the temperature sensor pin in the W83627DHG-P. A 15-KΩ resistor is connected to VREF to supply the bias current for the diode, and the 2200-pF, bypass capacitor is added to filter high-frequency noise.

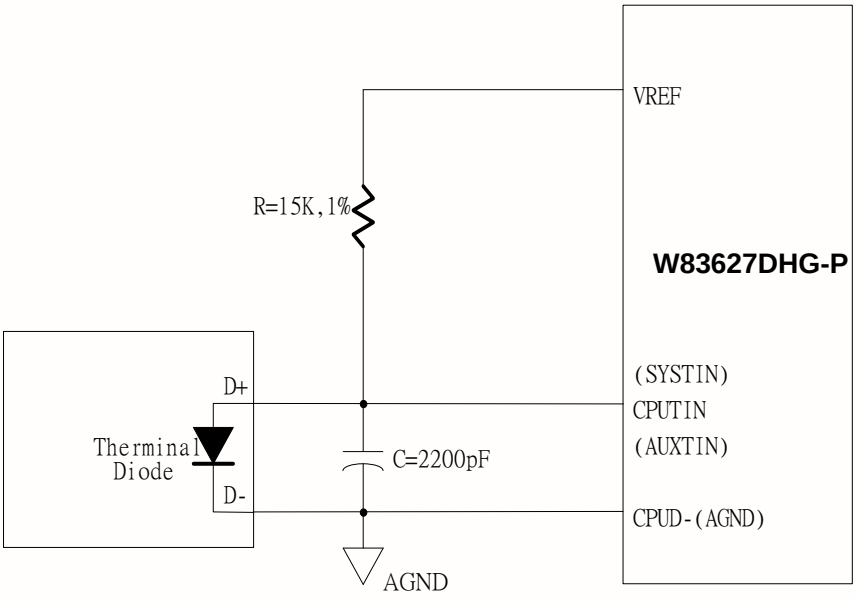


Figure 8-6 Monitoring Temperature from Thermal Diode (Voltage Mode)

8.3.3.3. Monitor Temperature from Thermal Diode (Current Mode)

The W83627DHG-P can also sense the diode temperature through Current Mode and the circuit is shown in the following figure.

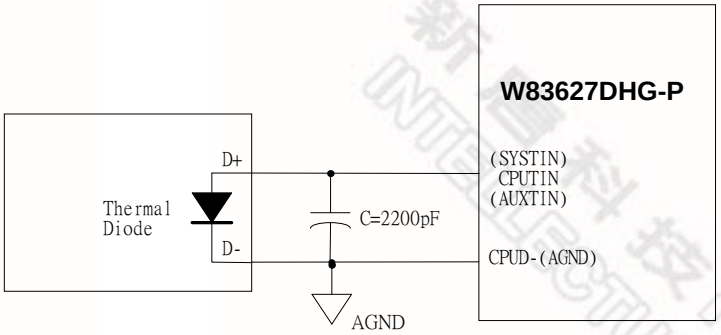


Figure 8-7 Monitoring Temperature from Thermal Diode (Current Mode)

The pin of processor D- is connected to CPUD- (pin 105) and the pin D+ is connected to temperature sensor pin in the W83627DHG-P. A bypass capacitor C=2200pF should be added to filter the high frequency noise.

8.4 SST Command Summary

The W83627DHG-P is equipped with a built-in voltage and temperature sensor which uses the Simple Serial Transport (SST) interface. The sensor provides a means for an analog signal to travel over a digital bus enabling remote voltage and temperature sensing in areas previously not monitored in the PC.

SST is a self-clocked, one-wire bus for data transfer. The bus requires no additional control lines. In addition, SST also includes variable data transfer rate established with every message. Therefore, it is comparatively flexible. The W83627DHG-P has a programmable SST address defined at Logical Device C CR [F1h]. The default address is 0x48h which is within the range of 0x48h-0x4ah defined in the SST specification.

8.4.1 Command Summary

The W83627DHG-P supports SST commands as shown in the following table:

Table 8-2 SST Command Summary

COMMAND	DESCRIPTION
GetIntTemp()	Returns the 2-byte temperature data values for pin SYSTIN (Pin 104)
GetExtTemp()	Returns the 2-byte temperature data values for pin CPUTIN (Pin 103)
GetAllTemps()	Returns the 4-byte temperature data values for both SYSTIN and CPUTIN
GetVolt12V()	Returns the 2-byte voltage data values for pin VIN0 (Pin 99). This pin should be connected to +12V power through scaling resistors Refer to 8.4.2.2 Voltage Data Format.
GetVolt5V()	Returns the 2-byte voltage data values for pin VIN1 (Pin 98). This pin should be connected to +5V power through scaling resistors Refer to

COMMAND	DESCRIPTION
	8.4.2.2 Voltage Data Format.
GetVolt3p3V()	Returns the 2-byte voltage data values for pin 3VCC (Pin 12, 28, 48).This pin should be connected to +3.3V power directly Refer to 8.4.2.2 Voltage Data Format.
GetVolt2p5V()	Returns the 2-byte voltage data values for pin VIN2 (Pin 97). This pin should be connected to +2.5V power through scaling resistors. Refer to 8.4.2.2 Voltage Data Format.
GetVoltVccp()	Returns the 2-byte voltage data values of CPUVCORE (Pin 100). This pin should be connected to CPU power supply directly. The CPU power supply voltage must not be higher than **2.048** volt
GetAllVoltages()	Returns a 10-byte voltage data value containing all the above listed five (5) voltages

8.4.2 Combination Sensor Data Format

8.4.2.1. Temperature Data Format

The W83627DHG-P temperature data format of both CPUTIN and SYSTIN is 16-bit two's-complement binary value. It represents multiple of 1/64°C in the temperature reading.

Table 1 shows some typical temperature values in 16-bit two's complement format.

Table 8-3 Typical Temperature Values

TEMPERATURE	16-BIT DIGITAL OUTPUT (TWO'S COMPLEMENT)	
	16-BIT BINARY	16-BIT HEX
+80°C	0001 0100 0000 0000	1400h
+79.5°C	0001 0011 1110 0000	13E0h
+1°C	0000 0000 0100 0000	0010h
+0°C	0000 0000 0000 0000	0000h
-1°C	1111 1111 1100 0000	FFC0h
-5°C	1111 1110 1100 0000	FEC0h

8.4.2.2. Voltage Data Format

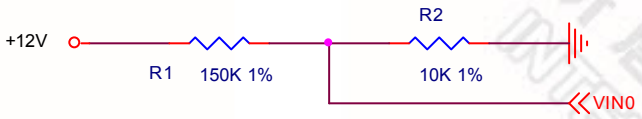
The W83627DHG-P can return five (5) voltage values through the SST interface. The voltage data format is 16-bit two's-complement binary. The relation between the 2-byte data and the monitored voltage is listed below:

1) CPUVCORE (pin 100) = Decimal[2-byte data by GetVoltVccp()] / 1024 volts

2) 3VCC (pin 12) = Decimal[2-byte data by GetVolt3p3V()] / 1024 volts

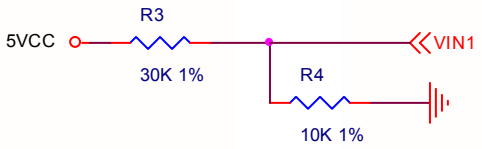
3) "+12V" = Decimal[2-byte data by GetVolt12V()] / 1024 / ((R1+R2) / R2) volts

VIN0 (pin 99) is connected as shown below:.



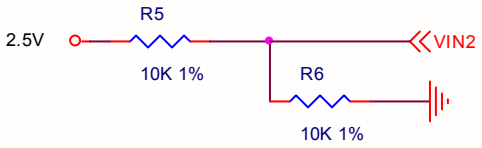
4) "+5VCC" = Decimal[2-byte data by GetVolt5V()] / 1024 / ((R3+R4) / R4) volts

VIN1 (pin 98) is connected as shown below:



5) "+2.5V" = Decimal[2-byte data by GetVolt2p5V()] / 1024 / ((R5+R6) / R6) volts

VIN2 (pin 97) is connected as shown below:



8.5 PECI

PECI (Platform Environment Control Interface) is a new digital interface to read the CPU temperature of Intel® CPUs. With a bandwidth ranging from 2 Kbps to 2 Mbps, PECI uses a single wire for self-clocking and data transfer. By interfacing to the Digital Thermal Sensor (DTS) in the Intel® CPU, PECI reports a negative temperature (in counts) relative to the processor's temperature at which the thermal control circuit (TCC) is activated. At the TCC Activation temperature, the Intel CPU will operate at reduced performance to prevent the device from thermal damage.

PECI is one of the temperature sensing methods that the W83627DHG-P supports. The W83627DHG-P contains a PECI master and reads the CPU PECI temperature. The CPU is a PECI client.

The PECI temperature values returning from the CPU are in "counts" which are approximately linear in relation to changes in temperature in degrees centigrade. However, this linearity is approximate and cannot be guaranteed over the entire range of PECI temperatures. For further information, refer to the PECI specification. All references to "temperature" in this section are in "counts" instead of "°C".

Figure 8-8 shows a typical fan speed (PWM duty cycle) and PECI temperature relationship.

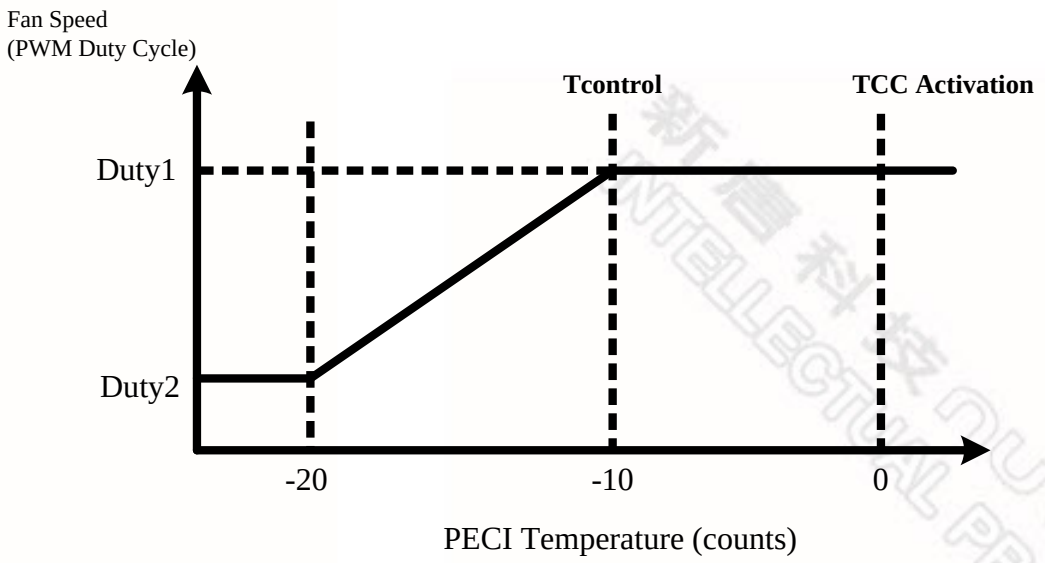


Figure 8-8 PECI Temperature

In this illustration, when PECI temperature is -20, the PWM duty cycle for fan control is at Duty2. When CPU is getting hotter and the PECI temperature is -10, the PWM duty cycle is at Duty1.

At TControl PECI temperature, the recommendation from Intel is to operate the CPU fan at full speed. Therefore Duty1 is 100% if this recommendation is followed. The value of TControl can be obtained by reading the related Machine Specific Register (MSR) in the Intel CPU. The TControl MSR address is usually in the BIOS Writer's guide for the CPU family in question. Refer to the relevant CPU documentation from Intel for more information. In this example, TControl is -10.

When the PECI temperature is below -20, the duty cycle is fixed at Duty2 to maintain a minimum (and constant) RPM for the CPU fan.

W83627DHG-P's fan control circuit can only accept positive real-time temperature inputs and limits setting (in Smart Fan ™ mode). The device provides offset registers to 'shift' the negative PECI readings to positive values otherwise the fan control circuit will not function properly. The offset registers are the TBase registers located at Logical Device C, CR [E1h] ~ CR [E4h]. These registers should be programmed with (positive) values so that the resultant value (Tbase + PECI) is always positive. The unit of the TBase register contents is "count" to match that of PECI values. The resultant value (TBase + PECI) should not be interpreted as the "temperature" (whether in count or °C) of the PECI client (CPU).

Figure 8-9 shows the temperature/fan speed relationship after Tbase offsets are applied (based on Figure 8-8). This view is from the perspective of the W83627DHG-P fan control circuit.

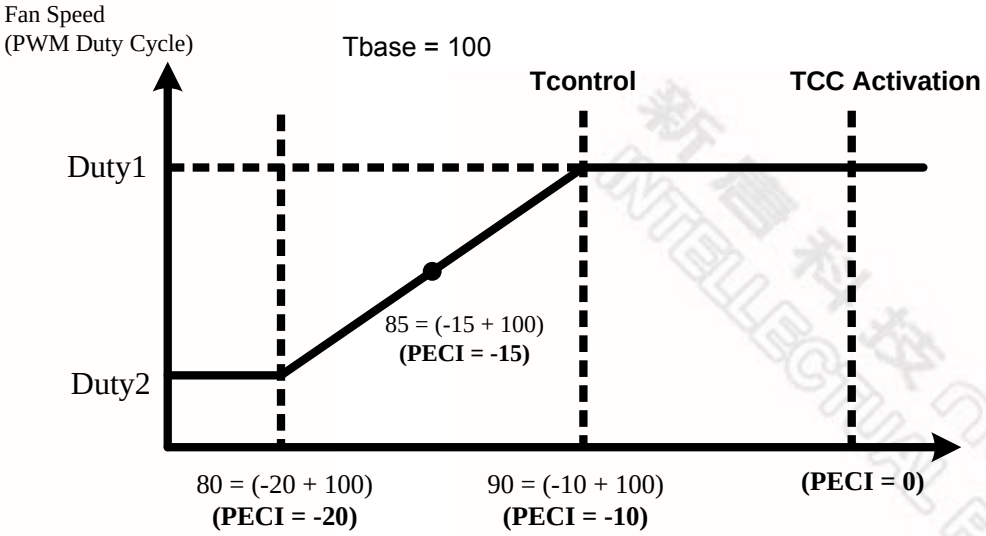


Figure 8-9 Temperature and Fan Speed Relation after Tbase Offsets

Assuming TBase is set to 100 and the PECI temperature is -15 , the real-time temperature value to the fan control circuit will be 85 (-15 + 100). The value of 55 (hex) will appear in the relevant real-time temperature register.

While using Smart Fan control function of W83627DHG-P, BIOS/software must include Tbase in determining the thresholds (limits). In this example, assuming TControl is -10 and Tbase is set to 100 [(1)], the threshold temperature value corresponding to the "100% fan duty cycle" event is 90 (-10+100). The value of 5A (hex) should be written to the relevant threshold register.

[(1)] *TControl is typically -10 to -20 for PECI-enabled CPUs. Base on that, a value of 85 ~100 for Tbase could be set for proper operation of the fan control circuit. This recommendation is applicable for most designs. In general, the concept presented in this section could be used to determine the optimum value of TControl to match the specific application.*

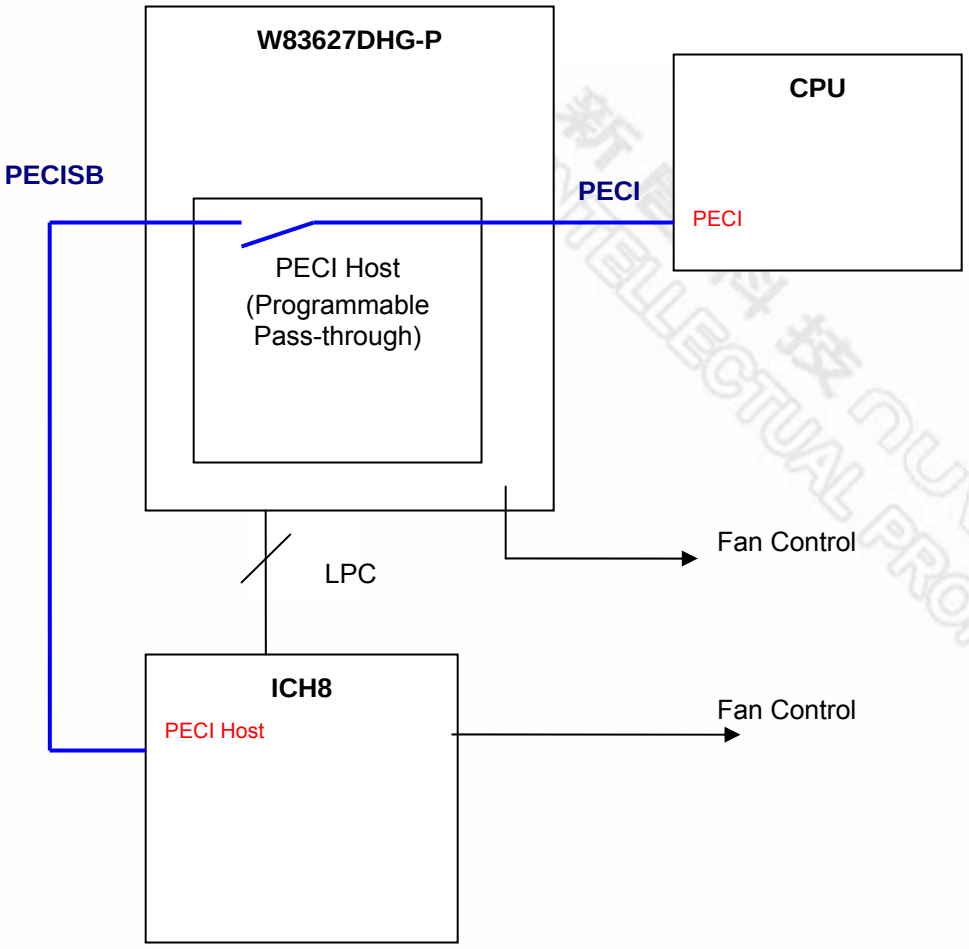


Figure 8-10 Block Diagram for PECI 1.0

The W83627DHG-P provides a PECISB pin that can be connected to a PECI host (e.g. chipset), so the W83627DHG-P becomes a bridge between that PECI host and the PECI client (e.g. CPU with PECI function). The bridge can pass the CPU PECI signals by programming Configure Register at Logical Device C, CR [E5h] Bit 0. An illustration is provided below (ICH8 is the alternative PECI host).

8.6 Fan Speed Measurement and Control

This section is divided into two parts, one to measure the speed and one to control the speed.

8.6.1 Fan Speed Measurement

The W83627DHG-P can measure fan speed for fans equipped with tachometer outputs. The tachometer signals should be set to TTL-level, and the maximum input voltage cannot exceed +3.3 V. If the tachometer signal exceeds +3.3 V, an external trimming circuit should be added to reduce the voltage accordingly.

The fan speed counter is read from Bank0 Index 28h, 29h, 2Ah, and 3Fh and Bank5 Index 53h. The fan speed can then be evaluated by the following equation:

$$RPM = \frac{1.35 \times 10^6}{Count \times Divisor}$$

The default divisor is 2 and is specified at Bank0 Index 47h, bits 7 ~ 4; Index 4Bh, bits 7 ~ 6; Index 4Ch, bit 7; Index 59h, bit 7 and bits 3 ~ 2; and Index 5Dh, bits 5 ~ 7. There are three bits for each divisor, and the corresponding divisor is listed in the table below.

Table 8-4 Fan Divisor Definition

BIT 2	BIT 1	BIT 0	FAN DIVISOR	BIT 2	BIT 1	BIT 0	FAN DIVISOR
0	0	0	***1***	1	0	0	***16***
0	0	1	***2***	1	0	1	***32***
0	1	0	***4***	1	1	0	***64***
0	1	1	***8***	1	1	1	***128***

The following table provides some examples of the relationship between divisor, RPM, and count.

Table 8-5 Divisor, RPM, and Count Relation

DIVISOR	NOMINAL RPM	TIME PER REVOLUTION	COUNTS	70% RPM	TIME FOR 70%
1	8800	6.82 ms	*153*	6160	9.84 ms
2 (default)	4400	13.64 ms	*153*	3080	19.48 ms
4	2200	27.27 ms	*153*	1540	38.96 ms
8	1100	54.54 ms	*153*	770	77.92 ms
16	550	109.08 ms	*153*	385	155.84 ms
32	275	218.16 ms	*153*	192	311.68 ms
64	137	436.32 ms	*153*	96	623.36 ms
128	68	872.64 ms	*153*	48	1246.72 ms

8.6.2 Fan Speed Control

The W83627DHG-P has four output pins for fan control, each of which offers PWM duty cycle and DC voltage to control the fan speed. The output type (PWM or DC) of each pin is configured by Bank0 Index 04h, bits 1 ~ 0; Index 12h, bit 0; and Index 62h, bit 6.

For PWM, the duty cycle is programmed by eight-bit registers at Bank0 Index 01h, Index 03h, Index 11h and Index 61h. The duty cycle can be calculated using the following equation:

$$\text{Dutycycle}(\%) = \frac{\text{Programmed 8 - bit Register Value}}{255} \times 100\%$$

The default duty cycle is FFh, or 100%. The PWM clock frequency is programmed at Bank0 Index 00h, Index 02h, Index 10h and Index 60h.

For DC, the W83627DHG-P has a six bit digital-to-analog converter (DAC) that produces 0 to 3.3 Volts DC. The analog output is programmed at Bank0 Index 01h, Index 03h, Index 11h and Index 61h. The analog output can be calculated using the following equation:

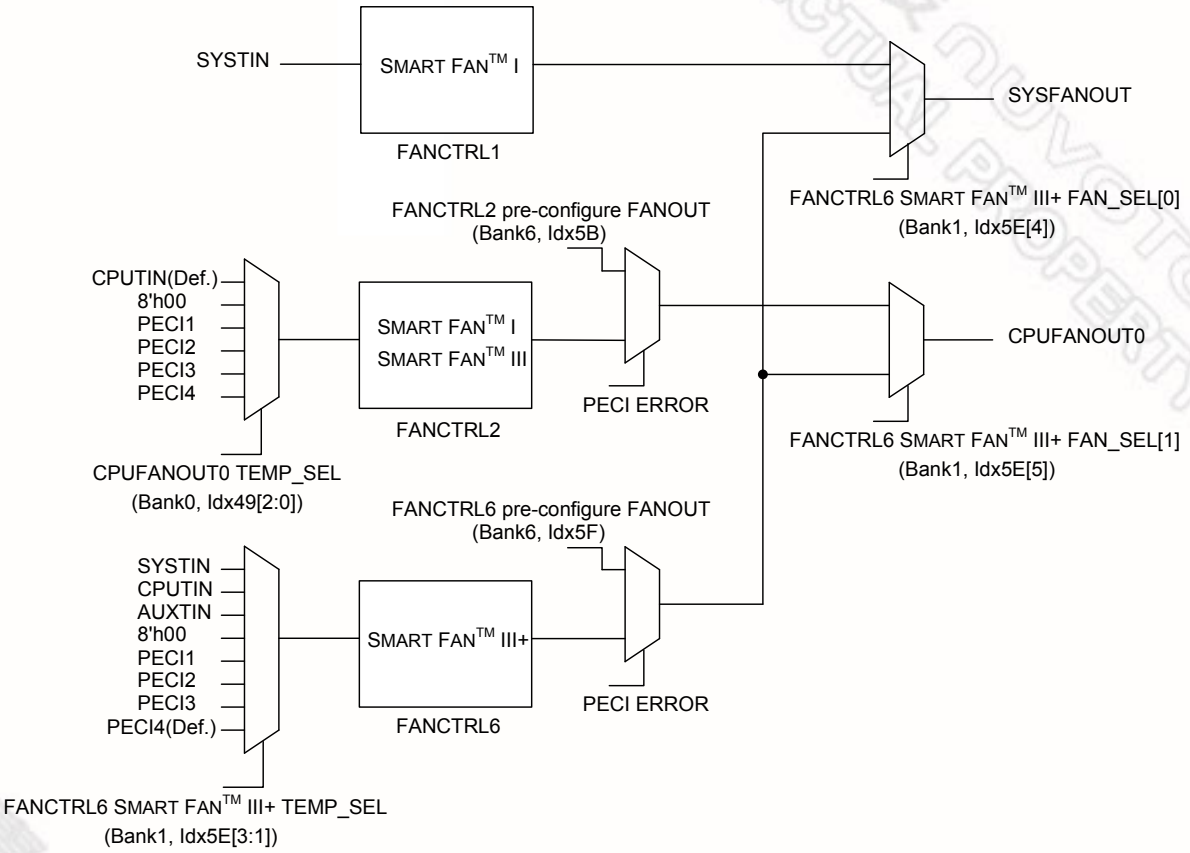
$$\text{OUTPUT Voltage (V)} = AVCC \times \frac{\text{Programmed 6 - bit Register Value}}{64}$$

The default value is 111111YY, or nearly 3.3 V, and Y is a reserved bit.

8.6.3 SMART FAN™ Control

The W83627DHG-P supports two SMART FAN™ I features — Thermal Cruise™ mode and Fan Speed Cruise™ mode, SMART FAN™ III features, and SMART FAN™ III+ features. Each of these is discussed in the following sections.

Each fan output and corresponding temperature sensor is illustrated in the figure below.



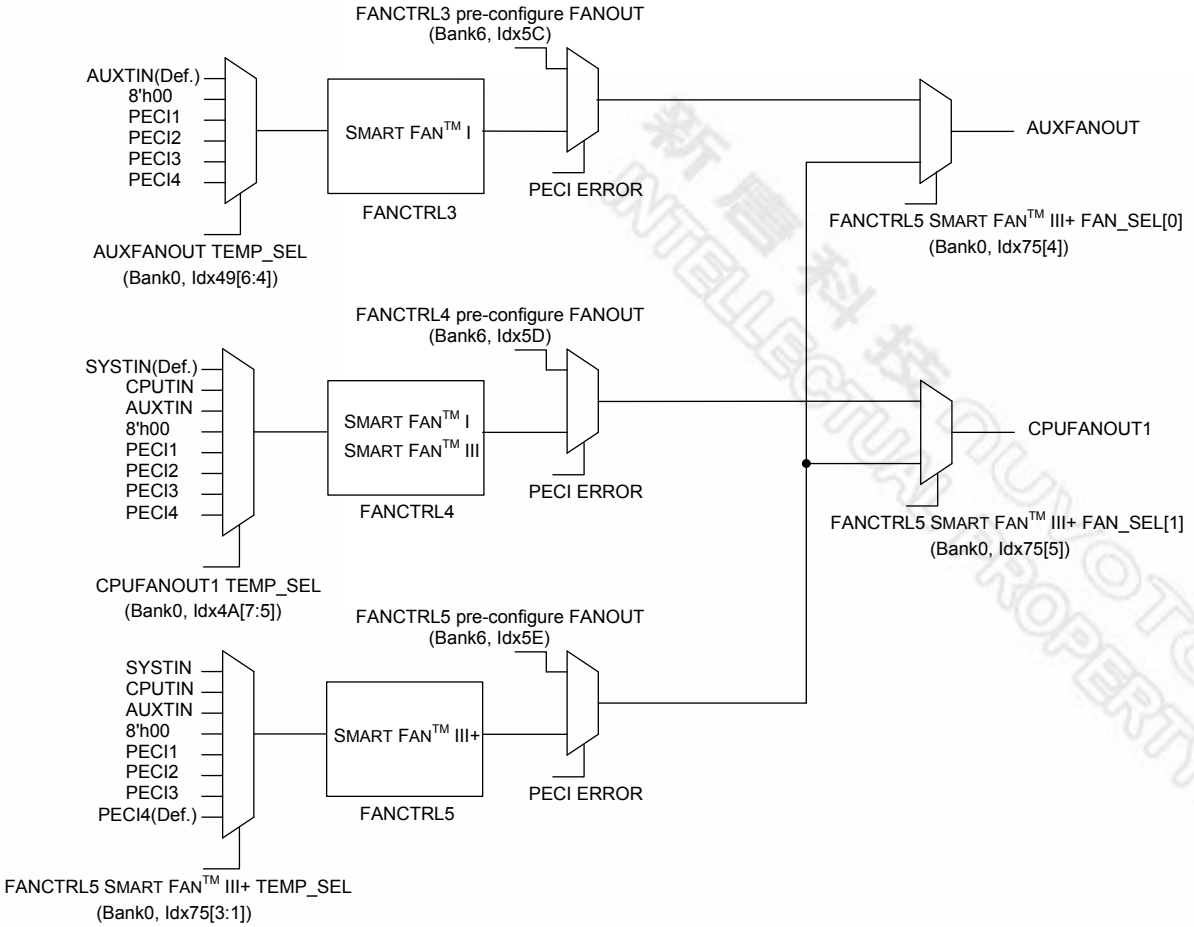


Figure 8-11 FANOUT and Corresponding Temperature Sensors in SMART FAN™ I, III, and III+

8.6.3.1. Thermal Cruise™ Mode

Four pairs of temperature sensors and fan outputs in Thermal Cruise™ mode:

- SYSTIN and SYSFANOUT
- CPUFANOUT0 and the temperature sensor selected by Bank0 Index 49h, bits 2 ~ 0
- AUXFANOUT and the temperature sensor selected by Bank0 Index 49h, bits 6 ~ 4
- CPUFANOUT1 and the temperature sensor selected by Bank0 Index 4Ah, bits 7 ~ 5

Thermal Cruise™ mode controls the fan speed to keep the temperature in a specified range. First, this range is defined in BIOS by a temperature and the interval (e.g., 55 °C ± 3 °C). As long as the current temperature remains below the low end of this range (i.e., 52 °C), the fan is off. Once the temperature exceeds the low end, the fan turns on at a speed defined in BIOS (e.g., 20% output). Thermal Cruise™ mode then controls the fan output according to the current temperature. Three conditions may occur:

(1) If the temperature still exceeds the high end, fan output increases slowly. If the fan is operating at full speed but the temperature still exceeds the high end, a warning message is issued to protect the system.

(2) If the temperature falls below the high end (i.e., 58 °C) but remains above the low end (e.g., 52 °C), fan output remains the same.

(3) If the temperature falls below the low end (e.g., 52 °C), fan output decreases slowly to zero or to a specified “stop value”. This stop value is enabled by Bank0 Index 12h, bits 3 ~ 5, and the value itself is specified in Bank0 Index 08h, Index 09h, Index 15h, and Index 64h. The fan remains at the stop value for the period of time defined in Bank0 Index 0Ch, Index 0Dh, Index 17h, and Index 66h.

In general, Thermal Cruise™ mode means

- if the current temperature is higher than the high end, increase the fan speed;
- if the current temperature is lower than the low end, decrease the fan speed;
- otherwise, keep the fan speed the same.

The following figures illustrate two examples of Thermal Cruise™ mode.

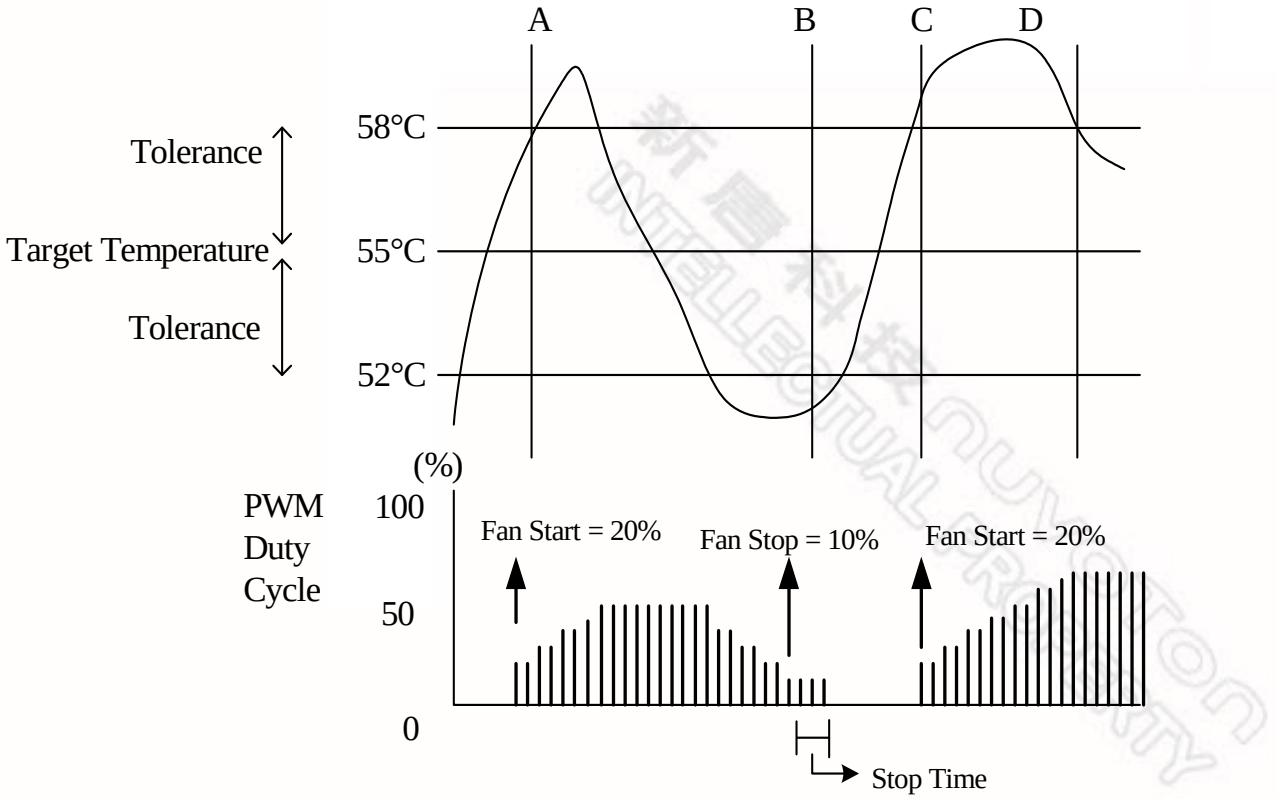


Figure 8-12 Mechanism of Thermal Curise™ Mode (PWM Duty Cycle)

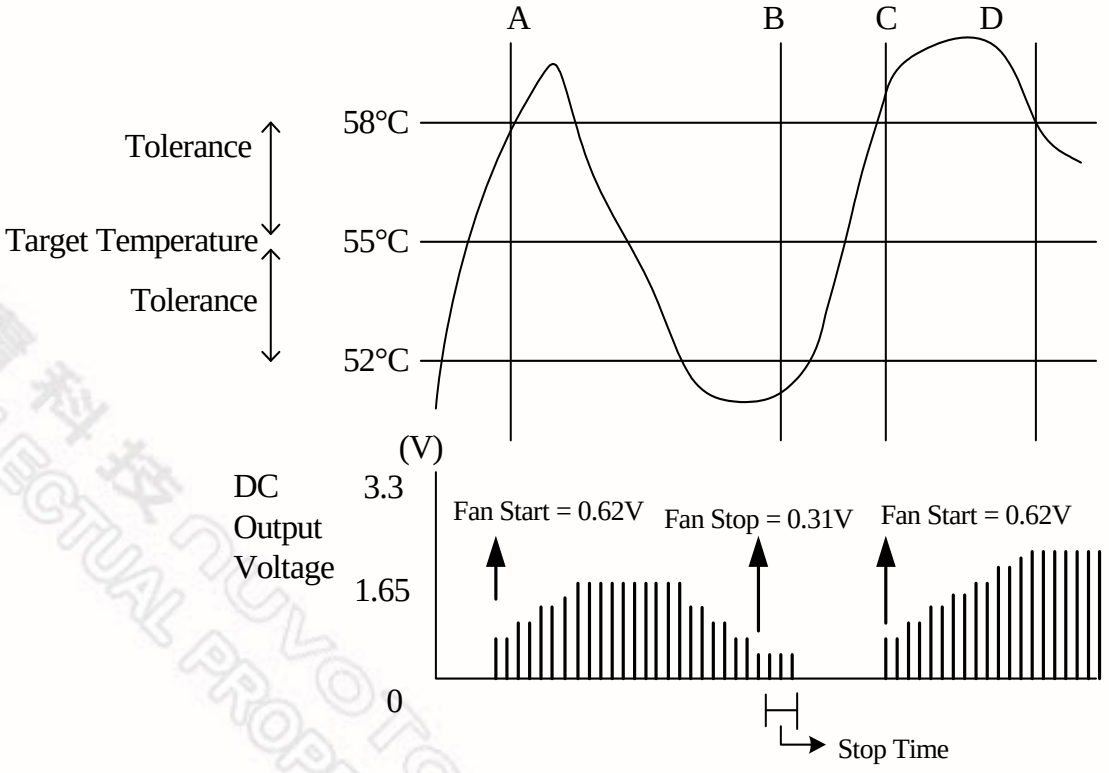


Figure 8-13 Mechanism of Thermal Curise™ Mode (DC Output Value)

8.6.3.2. Fan Speed Cruise™ Mode

Four pairs of fan input sensors and fan outputs in Fan Speed Cruise™ mode.

- SYSFANIN and SYSFANOUT
- CPUFANIN0 and the temperature sensor selected by Bank0 Index 49h, bits 2 ~ 0
- AUXFANOUT and the temperature sensor selected by Bank0 Index 49h, bits 6 ~ 4
- CPUFANOUT1 and the temperature sensor selected by Bank0 Index 4Ah, bits 7 ~ 5

Fan Speed Cruise™ mode keeps the fan speed in a specified range. First, this range is defined in BIOS by a fan speed count (the amount of time between clock input signals, not the number of clock input signals in a period of time) and an interval (e.g., 160 ± 10). As long as the fan speed count is in the specified range, fan output remains the same. If the fan speed count is higher than the high end (e.g., 170), fan output increases to make the count lower. If the fan speed count is lower than the low end (e.g., 150), fan output decreases to make the count higher. One example is illustrated in this figure.

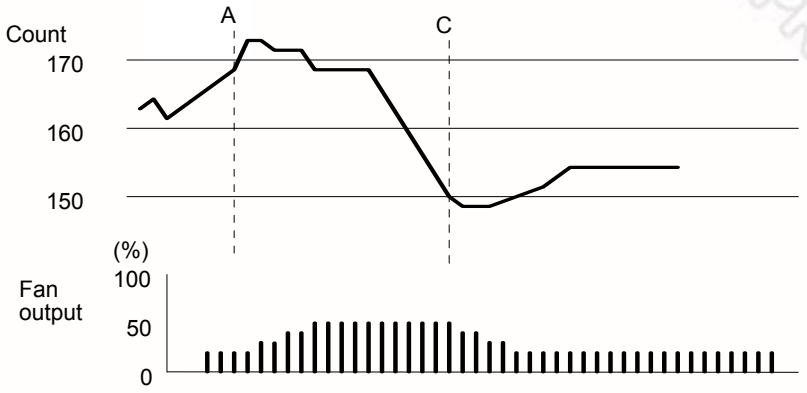


Figure 8-14 Mechanism of Fan Speed Cruise™ Mode

The following tables show current temperatures, fan output values and the relative control registers at Thermal Cruise™ and Fan Speed Cruise™ mode.

Table 8-6 Display Registers - at SMART FAN™ I Mode

DESCRIPTION	REGISTER ADDRESS	REGISTER NAME	ATTRIBUTE	BIT DATA
Current CPU Temperature	Bank1 Index 50h ,51h	CPUTIN Temperature Sensor	Read only	8 MSB, 1°C bit 7, 0.5 °C
Current SYS Temperature	Bank 0 Index 27h	SYSTIN Temperature Sensor	Read only	8 MSB, 1°C
Current AUX Temperature	Bank2 Index 50h,51h	AUXTIN Temperature Sensor	Read only	8 MSB, 1°C bit 7, 0.5 °C
Current CPUFANOUT0 Output Value	Bank0 Index 03h	CPUFANOUT0 Output Value Select	80h / FFh by strapping	bits 7~0 CPUFANOUT0 Value
Current SYSFANOUT	Bank0 Index 01h	SYSFANOUT Output Value Select	FFh	bits 7~0 SYSFANOUT Value

DESCRIPTION	REGISTER ADDRESS	REGISTER NAME	ATTRIBUTE	BIT DATA
Output Value				
Current AUXFANOUT Output Value	Bank0 Index 11h	AUXFANOUT Output Value Select	FFh	bits 7~0 AUXFANOUT Value
Current CPUFANOUT1 Output Value	Bank0 Index 61h	CPUFANOUT1 Output Value Select	80h / FFh by strapping	bits 7~0 CPUFANOUT1 Value

Table 8-7 Relative Registers - at Thermal Cruise™ Mode

THERMAL-CRUISE™ MODE	TARGET TEMPERATURE	TOLERANCE	START-UP VALUE	STOP VALUE	KEEP MIN. FAN OUTPUT VALUE	STOP TIME	STEP-DOWN TIME	STEP-UP TIME
SYSFANOUT	Bank0, 05h	Bank0, 07h Bit0-3	Bank0, 0Ah	Bank0, 08h	Bank0, 12h, Bit5	Bank0, 0Ch	Bank0, 0Eh	Bank0, 0Fh
CPUFANOUT0	Bank0, 06h	Bank0, 07h, Bit4-7	Bank0, 0Bh	Bank0, 09h	Bank0, 12h, Bit4	Bank0, 0Dh		
AUXFANOUT	Bank0, 13h	Bank0, 14h, Bit0-3	Bank0, 16h	Bank0, 15h	Bank0, 12h, Bit3	Bank0, 17h		
CPUFANOUT1	Bank0, 63h	Bank0, 62h, Bit0-3	Bank0, 65h	Bank0, 64h	Bank0, 12h, Bit6	Bank0, 66h		

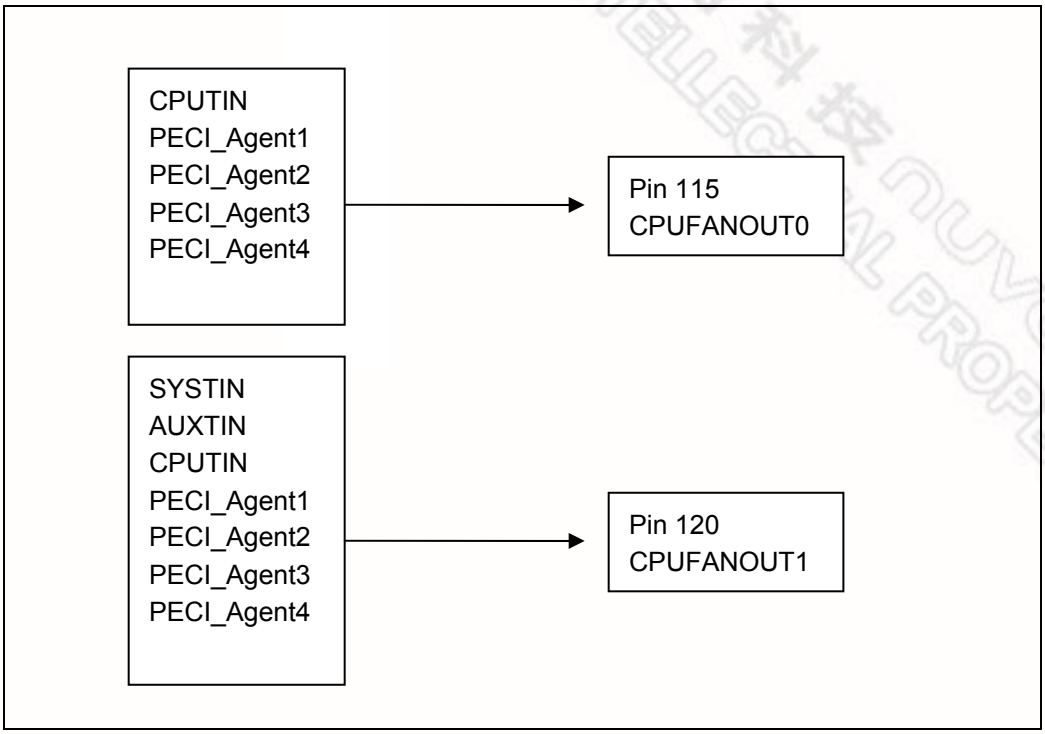
Table 8-8 Relative Registers-at Fan Speed Cruise™ Mode

SPEED CRUISE™ MODE	TARGET-SPEED COUNT	TOLERANCE	KEEP MIN. FAN OUTPUT VALUE	STEP-DOWN TIME	STEP-UP TIME
SYSFANOUT	Bank0, Index 05h	Bank0, Index 07h, bits 0-3	Bank0, Index 12h, Bit5	Bank0, Index 0Eh	Bank0, Index 0Fh
CPUFANOUT0	Bank0, Index 06h	Bank0, Index 07h, bits 4-7	Bank0, Index 12h, Bit4		
AUXFANOUT	Bank0, Index 13h	Bank0, Index 14h, bits 0-3	Bank0, Index 12h, Bit3		
CPUFANOUT1	Bank0, Index 63h	Bank0, Index 62h, bits 0-3	Bank0, Index 12h, Bit6		

8.6.3.3. SMART FAN™ III

SMART FAN™ III controls the fan speed so that the temperature meets the target temperature set in BIOS or application software. There are only two pairs of fan outputs and temperature sensors in SMART FAN™ III mode.

- CPUFANOUT0 and the temperature sensor selected by Bank0 Index 49h, bits 2 ~ 0
- CPUFANOUT1 and the temperature sensor selected by Bank0 Index 4Ah, bits 7 ~ 5



The algorithm is as follows:

(1) The target temperature, temperature tolerance, maximum and minimum fan outputs and step are set.

(2) The following figure shows the initial conditions. If the current temperature is within (Target Temperature ± Temperature Tolerance), the fan speed remains constant.

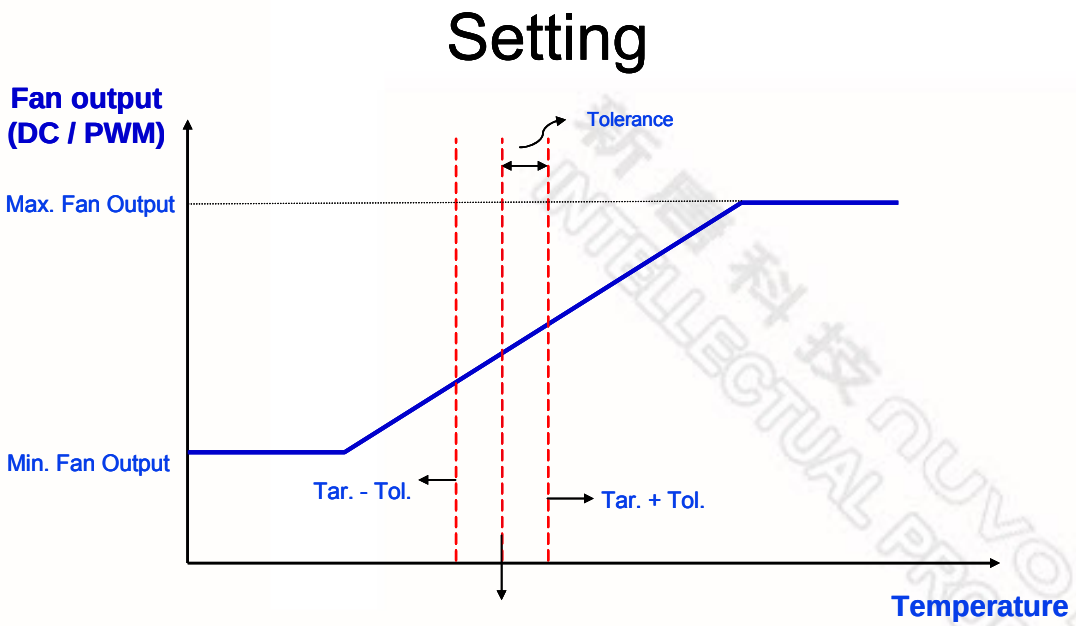


Figure 8-15 Setting of SMART FAN™ III

(3) If the current temperature is higher than (Target Temperature + Temperature Tolerance), fan speed rises one step. The step is the value in the CPUFANOUT Output Value Select Register, Bank0 Index 03h or Index 61h. In addition, the target temperature shifts to (Target Temperature + Temperature Tolerance), creating a new target temperature, named Target Temperature 1 in this figure.

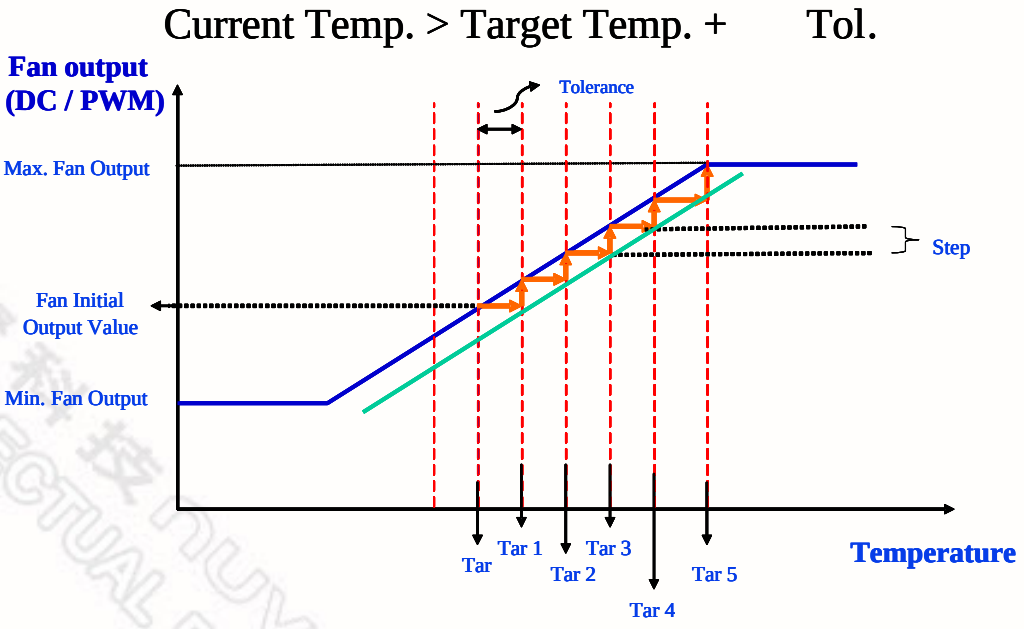


Figure 8-16 SMART FAN™ III Mechanism (Current Temp. > Target Temp. + Tol.)

If the current temperature rises higher than (Target Temperature 1 + Temperature Tolerance), the fan speed will rise one step, and the target temperature will shift to (Target Temperature 1 +

Temperature Tolerance), or Target Temperature 2. This process repeats whenever the current temperature is higher than (Target Temperature X ± Temperature Tolerance) or until the fan speed reaches its maximum speed.

(4) If the current temperature falls below (Target Temperature — Temperature Tolerance), the fan speed falls one step. The step is the value in the CPUFANOUT Output Value Select Register, Bank0 Index 03h or Index 61h. In addition, the target temperature shifts to (Target Temperature — Temperature Tolerance), creating a new target temperature named Target Temperature 1.This is illustrated in the figure below.

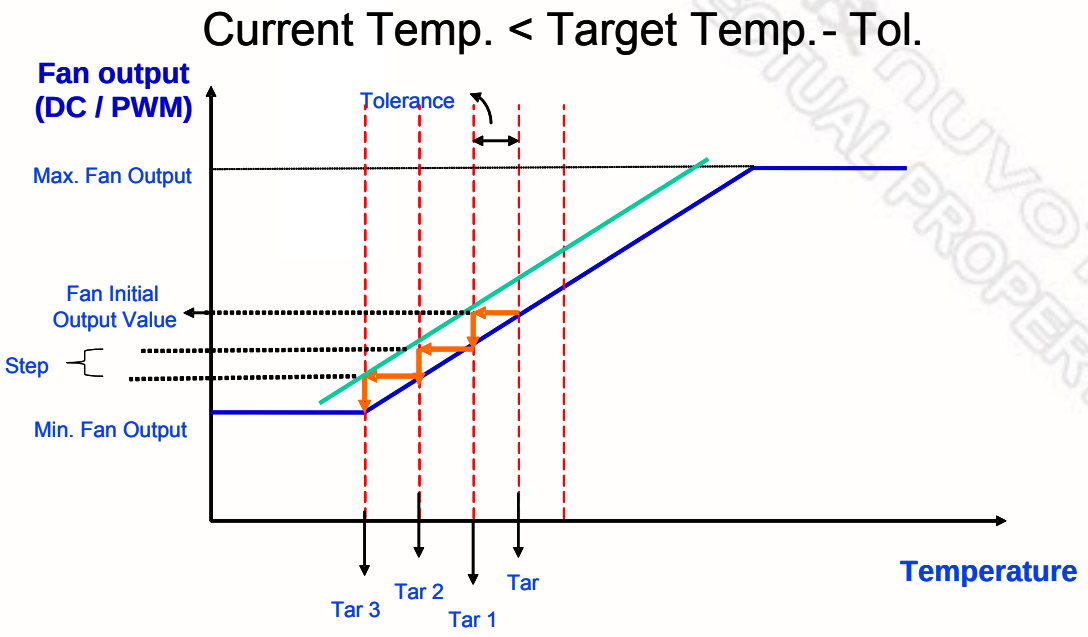


Figure 8-17 SMART FAN™ III Mechanism (Current Temp. < Target Temp. - Tol.)

If the current temperature falls lower than (Target Temperature 1 — Temperature Tolerance), the fan speed is reduced one step again, and the target temperature shifts to (Target Temperature 1 — Temperature Tolerance), or Target Temperature 2. This process repeats whenever the current temperature is lower than (Target Temperature X — Temperature Tolerance) or until the fan speed reaches its minimum speed.

(5) If the current temperature is always lower than (Target Temperature X — Temperature Tolerance), the fan speed decreases slowly to zero or to a specified stop value. The stop value is enabled by register Bank0 Index 12h, bit 4 and bit 6, and the stop value is specified in Bank0 Index 09h and Index 64h. The fan remains at the stop value for the period of time defined in Bank0 Index 0Dh and Index 66h.

The following tables show current temperatures, fan output values and the relative control registers at SMART FAN™ III mode.

Table 8-9 Display Register - in SMART FAN™ III Mode

DESCRIPTION	REGISTER ADDRESS	REGISTER NAME	ATTRIBUTE	BIT DATA
Current CPU Temperature	Bank1 Index 50h ,51h	CPUTIN Temperature Sensor	Read only	8 MSB, 1°C bit 7, 0.5 °C
Current SYS Temperature	Bank 0 Index 27h	SYSTIN Temperature Sensor	Read only	8 MSB, 1°C
Current AUX Temperature	Bank2 Index 50h,51h	AUXTIN Temperature Sensor	Read only	8 MSB, 1°C bit 7, 0.5 °C
Current CPUFANOUT0 Output Value	Bank0 Index 03h	CPUFANOUT0 Output Value Select	80h / FFh by strapping	bits 7~0 CPUFANOUT0 Value
Current CPUFANOUT1 Output Value	Bank0 Index 61h	CPUFANOUT1 Output Value Select	80h / FFh by strapping	bits 7~0 CPUFANOUT1 Value

Table 8-10 Relative Register - in SMART FAN™ III Control Mode

SMART FAN™ III MODE	TARGET TEMPERATURE	TOLERANCE	STOP VALUE (MIN. FAN OUTPUT)	MAX. FAN OUTPUT	STOP TIME
CPUFANOUT0	Bank0, Index 06h	Bank0, Index 07h, bits 4-7	Bank0, Index 09h	Bank0, Index 67h	Bank0, Index 0Dh
CPUFANOUT1	Bank0, Index 63h	Bank0, Index 62h, bits 0-3	Bank0, Index 64h	Bank0, Index 69h	Bank0, Index 66h
SMART FAN™ III MODE	**OUTPUT STEP**	**STEP DOWN TIME**	**STEP UP TIME**	**KEEP MIN. FAN OUTPUT VALUE**	**INITIAL VALUE**
CPUFANOUT0	Bank0, Index 68h	Bank0, Index 0Eh	Bank0, Index 0Fh	Bank0, Index 12h, bit 4	Bank0, Index 03h
CPUFANOUT1	Bank0, Index 6Ah			Bank0, Index 12h, bit 6	Bank0, Index 03h

8.6.3.4. SMART FAN™ III+

SMART FAN™ III+ offers 2 slopes to control the fan speed. There are four fan outputs and temperature sensors in SMART FAN™ III+ mode.

- The temperature sensor is selected by Bank0 Index 75h, bits 3~1 & Bank1 Index 5Eh, bits 3~1.
- The fan output (SYSFANOUT, CPUFANOUT0, AUXFANOUT & CPUFANOUT1) is selected by Bank0 Index 75, bits 5~4 & Bank1 Index 5Eh, bit 5~4.

The 2 slopes can be obtained by setting PWM1~PWM3 and Temperature1~Temperature3 through the registers. When the temperature changes, FAN Output will calculate the DC/PWM output based on the current slope. For example, in the following figure, T1~T3 are the temperature set and DC/PWM1 ~ DC/PWM3 are the fan output set. Assume Tx and Ty are the current temperature and DC/PWMx and DC/PWMy are the fan outputs, then

The slope:

$$X = \frac{(DC/PWM2)-(DC/PWM1)}{(T2-T1)}$$

$$Y = \frac{(DC/PWM3)-(DC/PWM2)}{(T3-T2)}$$

Fan Output:

$$DC/PWMx = (DC/PWM1)+(Tx-T1)\cdot X$$

$$DC/PWMy = (DC/PWM2)+(Ty-T2)\cdot Y$$

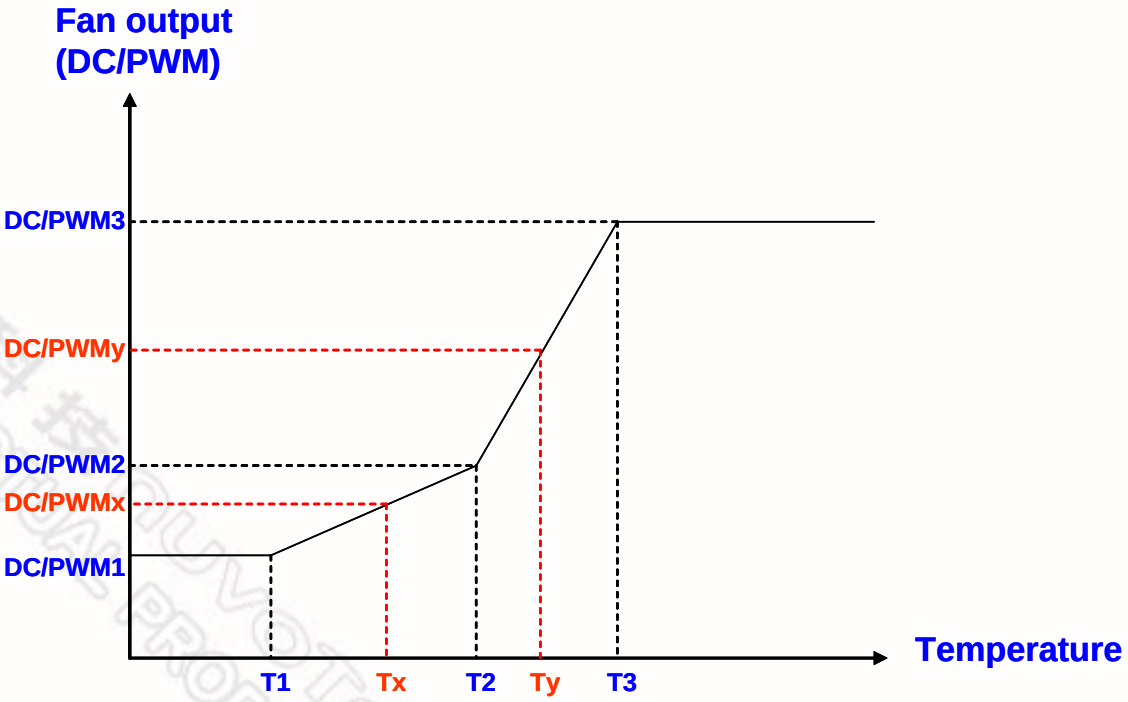


Figure 8-18 SMART FAN™ III+ Mechanism

Table 8-11 Display Registers - in SMART FAN™ III+ Mode

DESCRIPTION	REGISTER ADDRESS	REGISTER NAME	ATTRIBUTE
FANCTRL5 SMART FAN™ III + Temperature 1	Bank0 Index 6Fh	FANCTRL5 SMART FAN™ III + Temperature 1	Read / Write
FANCTRL5 SMART FAN™ III + Temperature 2	Bank0 Index 70h	FANCTRL5 SMART FAN™ III + Temperature 2	Read / Write
FANCTRL5 SMART FAN™ III + Temperature 3	Bank0 Index 71h	FANCTRL5 SMART FAN™ III + Temperature 3	Read / Write
FANCTRL5 SMART FAN™ III + DC/PWM 1	Bank0 Index 72h	FANCTRL5 SMART FAN™ III + DC/PWM 1	Read / Write
FANCTRL5 SMART FAN™ III + DC/PWM 2	Bank0 Index 73h	FANCTRL5 SMART FAN™ III + DC/PWM 2	Read / Write
FANCTRL5 SMART FAN™ III + DC/PWM 3	Bank0 Index 74h	FANCTRL5 SMART FAN™ III + DC/PWM 3	Read / Write
FANCTRL5 SMART FAN™ III + input source & output FAN select	Bank0 Index 75h, bit5-1	FANCTRL5 SMART FAN™ III + input source & output FAN select	Read / Write
FANCTRL6 SMART FAN™ III + Temperature 1	Bank1 Index 58h	FANCTRL6 SMART FAN™ III + Temperature 1	Read / Write
FANCTRL6 SMART FAN™ III + Temperature 2	Bank1 Index 59h	FANCTRL6 SMART FAN™ III + Temperature 2	Read / Write
FANCTRL6 SMART FAN™ III + Temperature 3	Bank1 Index 5Ah	FANCTRL6 SMART FAN™ III + Temperature 3	Read / Write
FANCTRL6 SMART FAN™ III + DC/PWM 1	Bank1 Index 5Bh	FANCTRL6 SMART FAN™ III + DC/PWM 1	Read / Write
FANCTRL6 SMART FAN™ III + DC/PWM 2	Bank1 Index 5Ch	FANCTRL6 SMART FAN™ III + DC/PWM 2	Read / Write
FANCTRL6 SMART FAN™ III + DC/PWM 3	Bank1 Index 5Dh	FANCTRL6 SMART FAN™ III + DC/PWM 3	Read / Write
FANCTRL6 SMART FAN™ III + input source & output FAN select	Bank1 Index 5Eh, bit5-1	FANCTRL6 SMART FAN™ III + input source & output FAN select	Read / Write

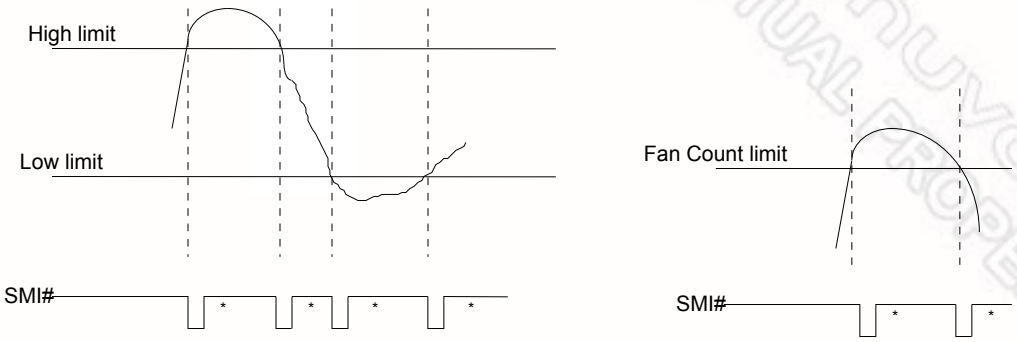
8.7 Interrupt Detection

8.7.1 SMI# Interrupt Mode

The SMI#/OVT# pin (pin 5) is a multi-function pin. It can be in SMI# mode or in OVT# mode by setting Configuration Register CR [29h], bit 6 to one or zero, respectively. In SMI# mode, it can monitor voltages, fan counts, or temperatures.

8.7.1.1. Voltage SMI# Mode

The SMI# pin can create an interrupt if a voltage exceeds a specified high limit or falls below a specified low limit. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This mode is illustrated in the following figure.



*Interrupt Reset when Interrupt Status Registers are read

Figure 8-19 SMI Mode of Voltage and Fan Inputs

8.7.1.2. Fan SMI# Mode

The SMI# pin can create an interrupt if a fan count crosses a specified fan limit (rises above it or falls below it). This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This mode is illustrated in the figure above.

8.7.1.3. Temperature SMI# Mode

The SMI# pin can create interrupts that depend on the temperatures measured by SYSTIN, CPUTIN, and AUXTIN. These interrupts are divided into two parts, one for SYSTIN and the other for CPUTIN / AUXTIN.

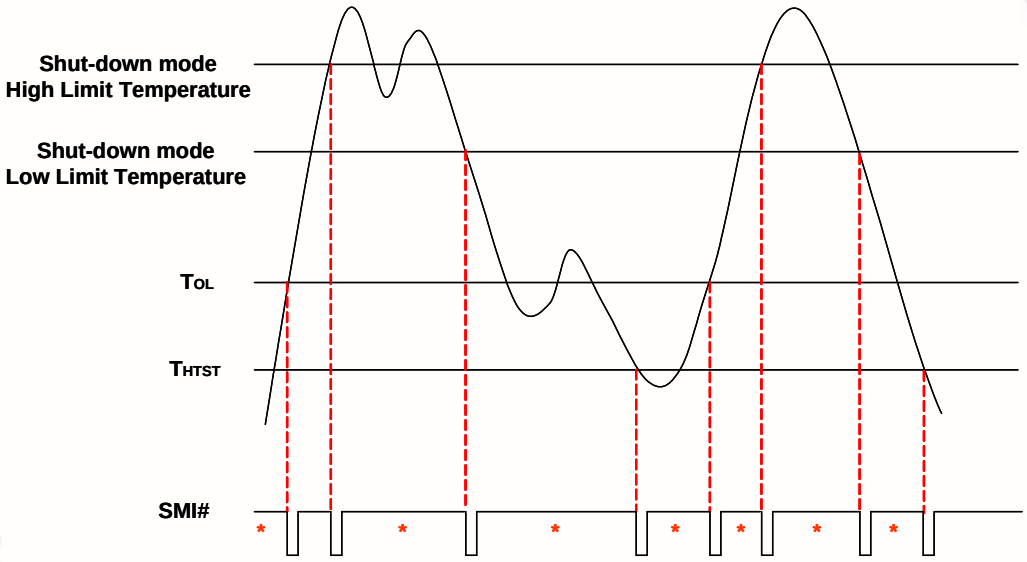
8.7.1.3.1. Temperature Sensor 1 (SYSTIN) SMI# Interrupt

The SMI# pin has four interrupt modes with SYSTIN.

(1) Shut-down Interrupt Mode

This mode is enabled by setting T_{HYST} (Temperature Hysteresis) lower than T_{OL} and setting Bank0 Index 40h, bit 4 to 1.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_{OL} or Shut-down mode high limit temperature, and when the current temperature falls below T_{HYST} or Shut-down mode low limit temperature. Once the temperature rises above T_{OL}, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_{OL}, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts, except the first time current temperature rises above Shut-down mode high limit temperature. This is illustrated in the following figure.



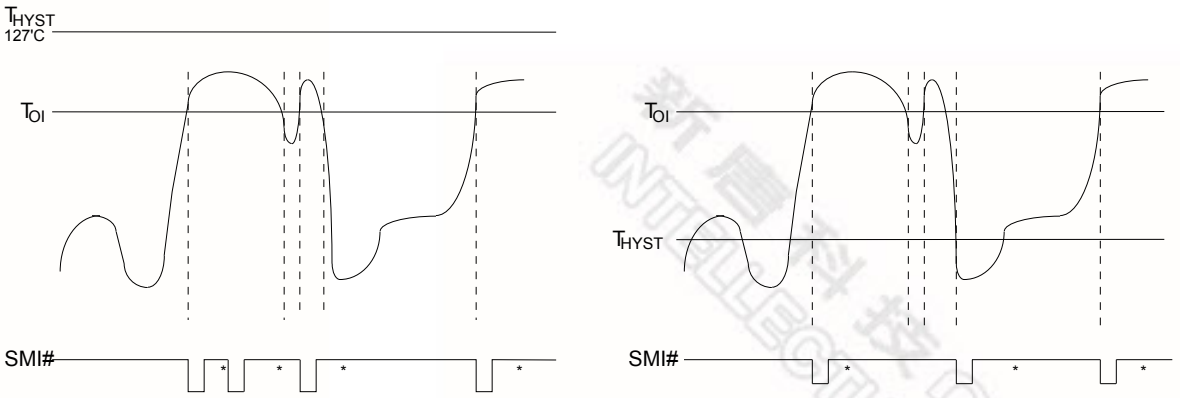
*** Interrupt Reset when Interrupt Status Registers are read**

Shut-down Interrupt Mode

(2) Comparator Interrupt Mode

This mode is enabled by setting T_{HYST} (Temperature Hysteresis) to 127°C.

In this mode, the SMI# pin can create an interrupt as long as the current temperature exceeds T_O (Over Temperature). This interrupt can be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. If the interrupt is reset, the SMI# pin continues to create interrupts until the temperature goes below T_O. This is illustrated in the figure below.



*Interrupt Reset when Interrupt Status Registers are read

Comparator Interrupt Mode **Two-Time Interrupt Mode**

Figure 8-20 SMI Mode of SYSTIN I

(3) Two-Time Interrupt Mode

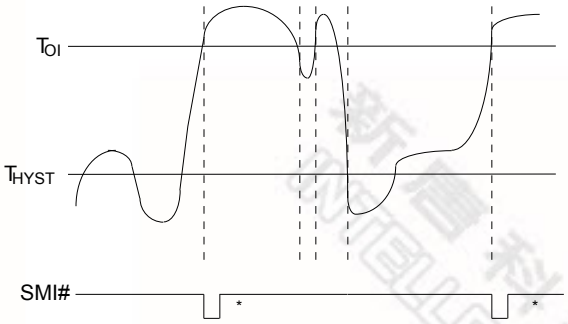
This mode is enabled by setting T_{HYST} (Temperature Hysteresis) lower than T_O and setting Bank0 Index 4Ch, bit 5 to zero.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O or when the current temperature falls below T_{HYST}. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure above.

(4) One-Time Interrupt Mode

This mode is enabled by setting T_{HYST} (Temperature Hysteresis) lower than T_O and setting Bank0 Index 4Ch, bit 5 to one.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the following figure.



*Interrupt Reset when Interrupt Status Registers are read

One-Time Interrupt Mode

Figure 8-21 SMI Mode of SYSTIN II

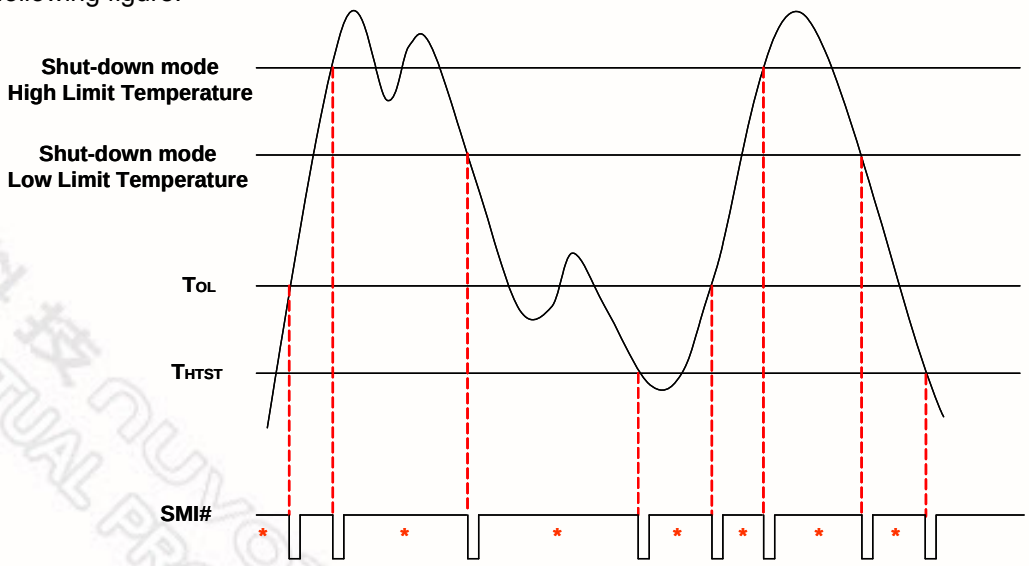
8.7.1.3.2. Temperature Sensor 2 (CPUTIN) And Sensor 3 (AUXTIN) SMI# Interrupt

The SMI# pin has three interrupt modes with CPUTIN / AUXTIN.

(1) Shut-down Interrupt Mode

This mode is enabled by setting Bank0 Index 4Ch, bit 6 to zero and Bank0 Index 40h, bit 6-5 to one.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_{OL} or Shut-down mode high limit temperature, and when the current temperature falls below T_{HYST} or Shut-down mode low limit temperature. Once the temperature rises above T_{OL}, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_{OL}, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts, except the first time current temperature rises above Shut-down mode high limit temperature. This is illustrated in the following figure.



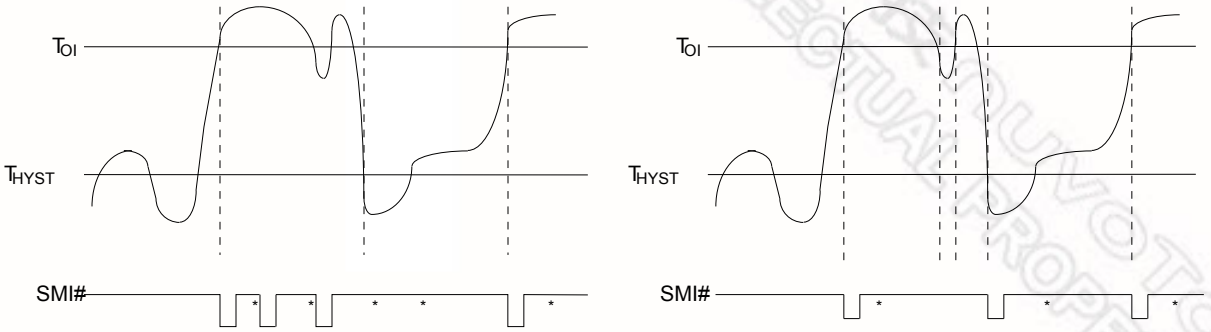
*** Interrupt Reset when Interrupt Status Registers are read**

Shut-down Interrupt Mode

(2) Comparator Interrupt Mode

This mode is enabled by setting Bank0 Index 4Ch, bit 6, to one.

In this mode, the SMI# pin can create an interrupt when the current temperature exceeds T_O (Over Temperature) and continues to create interrupts until the temperature falls below T_{HYST}. This interrupt can be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure below.



*Interrupt Reset when Interrupt Status Registers are read

Comparator Interrupt Mode **Two-Time Interrupt Mode**

Figure 8-22 SMI Mode of CPUTIN

(3) Two-Times Interrupt Mode

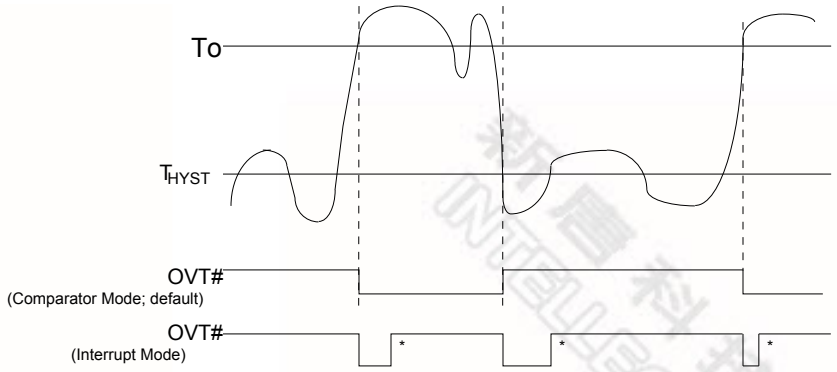
This mode is enabled by setting Bank0 Index 4Ch, bit 6, to zero.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O or when the current temperature falls below T_{HYST}. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure above.

8.7.2 OVT# Interrupt Mode

The SMI#/OVT# pin is a multi-function pin. It can be in SMI# mode or in OVT# mode by setting Configuration Register CR [29h], bit 6 to one or zero, respectively. In OVT# mode, it can monitor temperatures, and it is enabled or disabled for SYSTIN, CPUTIN, and AUXTIN by Bank0 Index 18h, bit 6; Bank0 Index 4Ch, bit 3; and Bank0 Index 4Ch, bit4.

The OVT# pin has two interrupt modes, comparator and interrupt. The modes are illustrated in this figure.



*Interrupt Reset when Temperature sensor registers are read

Figure 8-23 OVT# Modes of Temperature Inputs

If Bank0 Index 18h, bit 4, Bank1 Index 52h, bit 1, and Bank2 Index 52h, bit1 are set to zero, the OVT# pin is in comparator mode. In comparator mode, the OVT# pin can create an interrupt once the current temperature exceeds T_O and continues to create interrupts until the temperature falls below T_{HYST}. The OVT# pin is asserted once the temperature has exceeded T_O and has not yet fallen below T_{HYST}.

If Bank0 Index 18h, bit 4, Bank1 Index 52h, bit1, and Bank2 Index 52h, bit 1 are set to one, the OVT# pin is in interrupt mode. In interrupt mode, the OVT# pin can create an interrupt once the current temperature rises above T_O or when the temperature falls below T_{HYST}. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers. The OVT# pin is asserted when an interrupt is generated and remains asserted until the interrupt is reset.

8.7.3 Caseopen Detection

The purpose of Caseopen function is used to detect whether the computer case is opened. This feature must be able to function even when there is no 3VSB power. Consequently, the power source for the circuit is from either Pin 74 (VBAT) or Pin 61 (3VSB). 3VSB is the default power source. If there is no 3VSB power, the power source is VBAT. This is designed to save power consumption of the battery.

When the case is closed, the signal of Pin 76 must be pulled high by an externally pulled-up 2MΩ resistor that is connected to Pin 74. Once the case is opened, the signal will be changed from high to low. Meanwhile, the detection circuit inside the IC latches the signal. As a result, the interrupt status and the real-time status can be read at the registers next time when the computer is booted. The status will not be cleared unless Bank 0, Index 46h, bit 7, or CR [E6h] bit 5 at Logical Device A is set to "1" first and then to "0".

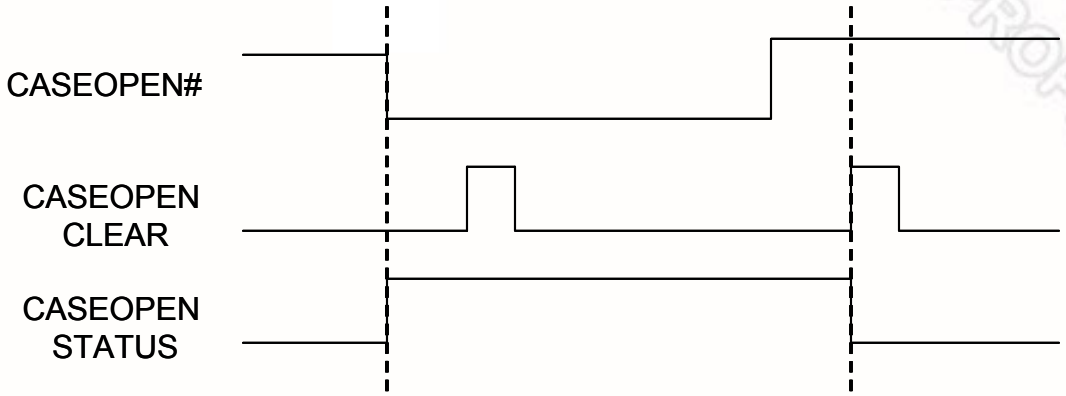


Figure 8-24 Caseopen Mechanism

8.7.4 BEEP Alarm Function

The W83627DHG-P provides an alarm output function at the BEEP/SO pin. The BEEP/SO pin is a multi-function pin and can be configured as BEEP output, if Configuration Register CR [24h], bit 1 is set to zero.

The BEEP outputs a warning tone when one of the monitored parameters in the following events is out of the preset range.

- Any voltage input of the nine pins (CPUVCORE, VIN[0..3], 3VCC, AVCC , 3VSB and VBAT) is out of the allowed range;
- Any temperature input of the three pins (SYSTIN, CPUTIN and AUXTIN) exceeds the limit;
- Any fan input of the five pins (SYSFANIN, CPUFANIN0, AUXFANIN0, CPUFANIN1 and AUXFANIN1) exceeds the limit;
- CASEOPEN# input pin is sampled low;
- User-defined bit (Bank 4, Index 53h, bit 5) is written to 1.

Whether the BEEP alarm function is enabled or disabled is determined by the control bit at Hardware Monitor Device, Bank 0, Index 57h, bit 7. Also, each event has their individual enable bit at Hardware Monitor Device, Bank 0, Index 56h bit [7:0], Index 57h bit [6:0] and Bank 4, Index 53h, bit [1:0].

BEEP/SO is an open-drain output pin and its default state is low. When the BEEP alarm function is activated, this pin repeatedly outputs 600 Hz square wave for 0.5 second and 1.2 KHz square wave for 0.5 second in turn until the enable bit or the abnormal event is cleared.

9. HARDWARE MONITOR REGISTER SET

The base address of the Address Port and Data Port is specified in registers CR [60h] and CR [61h] of Device B, the hardware monitor device. CR [60h] is the high byte, and CR [61h] is the low byte. The Address Port and Data Port are located at the base address, plus 5h and 6h, respectively. For example, if CR [60h] is 02h and CR [61h] is 90h, the Address Port is at 0x295h, and the Data Port is at 0x296h.

9.1 Address Port (Port x5h)

Attribute: Bit 6:0 Read/write , Bit 7: Reserved

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	A6	A5	A4	A3	A2	A1	A0
DEFAULT	0	00h (Address Pointer)						

BIT	DESCRIPTION
7	**Reserved.**
6-0	**Read/Write.**

9.2 Data Port (Port x6h)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Data							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Data to be read from or to be written to Value RAM and Register.

9.3 SYSFANOUT PWM Output Frequency Configuration Register - Index 00h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL1	PWM_SCALE1						
DEFAULT	0	0	0	0	0	1	0	0

The register is meaningful only when SYSFANOUT is programmed for PWM output (i.e., Bank0 Index 04h, bit 0 is 0).

BIT	DESCRIPTION
7	**SYSFANOUT PWM Input Clock Source Select.** This bit selects the clock source for PWM output frequency. 0: The clock source is 24 MHz. 1: The clock source is 180 KHz.
6-0	**SYSFANOUT PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. $\text{PWM output frequency} = \frac{\text{Input Clock}}{\text{Pre\_Scale Divider}} * \frac{1}{256}$ The maximum value of the divider is 127 (7Fh), and it should not be set to 0.

9.4 SYSFANOUT Output Value Select Register - Index 01h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT VALUE							
DEFAULT	1	1	1	1	1	1	1	1

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output (Bank 0, Index 04h, bit 0 is 0)	DESCRIPTION	The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
	DEFAULT	1	1	1	1	1	1	1	1
DC Voltage Output (Bank 0, Index 04h, bit 0 is 1)	DESCRIPTION	SYSFANOUT voltage control. The output voltage is calculated according to this equation: **OUTPUT Voltage =** $AVCC * \frac{FANOUT}{64}$						Reserved	
	DEFAULT	1	1	1	1	1	1		

9.5 CPUFANOUT0 PWM Output Frequency Configuration Register - Index 02h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL2	PWM_SCALE2						
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7	**CPUFANOUT0 PWM Input Clock Source Select.** This bit selects the clock source for PWM output. 0: The clock source is 24 MHz. 1: The clock source is 180 KHz.
6-0	**CPUFANOUT0 PWM Pre-Scale divider.** The clock source for PWM output is divided by the seven-bit value to calculate the actual PWM output frequency. **PWM output frequency =** $\frac{\text{Input Clock}}{\text{Pre\_Scale Divider}} * \frac{1}{256}$ The maximum value of the divider is 127 (7Fh), and it should not be set to 0.

The register is meaningful only when CPUFANOUT0 is programmed for PWM output.

9.6 CPUFANOUT0 Output Value Select Register - Index 03h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT0 VALUE							
DEFAULT	Strap by FAN_SET (Pin 117)							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output (Bank 0, Index 04h, bit 1 is 0)	DESCRIPTION	**CPUFANOUT0 PWM Duty Cycle.** The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
	DEFAULT	Strap by FAN_SET (Pin 117)							
DC Voltage Output (Bank 0, Index 04h, bit 1 is 1)	DESCRIPTION	**CPUFANOUT0 Voltage Control.** The output voltage is calculated according to this equation: **OUTPUT Voltage =** $AVCC * \frac{FANOUT}{64}$						Reserved	
	DEFAULT	Strap by FAN_SET (Pin 117)							

9.7 FAN Configuration Register I - Index 04h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		CPUFANOUT0_MODE		SYSFANOUT_MODE		CPUFANOUT0_SEL	SYSFANOUT_SEL
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-6	**Reserved.**
5-4	**CPUFANOUT0 Mode Control.** **Bits** **5 4** 0 0: CPUFANOUT0 is in Manual Mode. (Default) 0 1: CPUFANOUT0 is in Thermal Cruise™ Mode. 1 0: CPUFANOUT0 is in Fan Speed Cruise™ Mode. 1 1: CPUFANOUT0 is in SMART FAN™ III Mode.
3-2	**SYSFANOUT Mode Control.** **Bits** **3 2** 0 0: SYSFANOUT is in Manual Mode. (Default) 0 1: SYSFANOUT is in Thermal Cruise™ Mode. 1 0: SYSFANOUT is in Fan Speed Cruise™ Mode. 1 1: Reserved.
1	**CPUFANOUT0 Output Mode Selection.** 0: CPUFANOUT0 pin produces a PWM output duty cycle. (Default) 1: CPUFANOUT0 pin produces DC output.
0	**SYSFANOUT Output Mode Selection.** 0: SYSFANOUT pin produces a PWM duty cycle output. 1: SYSFANOUT pin produces DC output. (Default)

9.8 SYSTIN Target Temperature Register/ SYSFANIN Target Speed Register - Index 05h (Bank 0)

Attribute: Read/Write
Size: 8 bits

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	Reserved	SYSTIN Target Temperature						
	DEFAULT	0	0	0	0	0	0	0	0
Fan Speed Cruise™	DESCRIPTION	SYSFANIN Target Speed							
	DEFAULT	0	0	0	0	0	0	0	0

9.9 CPUTIN Target Temperature Register/ CPUFANIN0 Target Speed Register - Index 06h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUTIN Target Temperature / CPUFANIN0 Target Speed							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™ or SMART FAN™ III	DESCRIPTION	Reserved	CPUTIN Target Temperature						
	DEFAULT	0	0	0	0	0	0	0	0
Fan Speed Cruise™	DESCRIPTION	CPUFANIN0 Target Speed							
	DEFAULT	0	0	0	0	0	0	0	0

9.10 Tolerance of Target Temperature or Target Speed Register - Index 07h (Bank 0)

Attribute: Read/Write
Size: 8 bits

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™ or SMART FAN™ III	DESCRIPTION	Tolerance of CPUTIN Target Temperature				Tolerance of SYSTIN Target Temperature			
	DEFAULT	0	0	0	0	0	0	0	0
Fan Speed Cruise™	DESCRIPTION	Tolerance of CPUFANIN0 Target Speed				Tolerance of SYSFANIN Target Speed			
	DEFAULT	0	0	0	0	0	0	0	0

9.11 SYSFANOUT Stop Value Register - Index 08h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT STOP VALUE							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise™ mode, the SYSFANOUT value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.12 CPUFANOUT0 Stop Value Register - Index 09h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT0 STOP VALUE							
DEFAULT	0	0	0	0	0	0	0	1

InThermal Cruise™ mode or SMART FAN™ III mode, the CPUFANOUT0 value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.13 SYSFANOUT Start-up Value Register - Index 0Ah (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT START-UP VALUE							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise™ mode, SYSFANOUT value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan.

9.14 CPUFANOUT0 Start-up Value Register - Index 0Bh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT0 START-UP VALUE							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise™ mode, CPUFANOUT0 value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan.

9.15 SYSFANOUT Stop Time Register - Index 0Ch (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT STOP TIME							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise™ mode, if the stop value is enabled, this register determines the amount of time it takes the SYSFANOUT value to fall from the stop value to zero.
(1)For PWM output:
The units are intervals of 0.1 seconds. The default time is 6 seconds.
(2)For DC output:
The units are intervals of 0.4 seconds. The default time is 24 seconds.

9.16 CPUFANOUT0 Stop Time Register - Index 0Dh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT0 STOP TIME							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise™ mode or SMART FAN™ III mode, this register determines the amount of time it takes the CPUFANOUT0 value to fall from the stop value to zero.
(1)For PWM output:
The units are intervals of 0.1 seconds. The default time is 6 seconds.
(2)For DC output:
The units are intervals of 0.4 seconds. The default time is 24 seconds.

9.17 Fan Output Step Down Time Register - Index 0Eh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANOUT VALUE STEP DOWN TIME							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time it takes FANOUT to decrease its value by one step.
(1)For PWM output:
The units are intervals of 0.1 seconds. The default time is 1 seconds.
(2)For DC output:
The units are intervals of 0.4 seconds. The default time is 4 seconds.

9.18 Fan Output Step Up Time Register - Index 0Fh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANOUT VALUE STEP UP TIME							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time it takes FANOUT to increase its value by one step.

(1)For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

(2)For DC output:

The units are intervals of 0.4 second. The default time is 4 seconds.

9.19 AUXFANOUT PWM Output Frequency Configuration Register - Index 10h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL3	PWM_SCALE3						
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7	**AUXFANOUT PWM Input Clock Source Select.** This bit selects the clock source of PWM output frequency. 0: The clock source is 24 MHz. 1: The clock source is 180 KHz.
6-0	**AUXFANOUT PWM Pre-Scale Divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. **PWM output frequency =** $\frac{\text{Input Clock}}{\text{Pre\_Scale Divider}} * \frac{1}{256}$ The maximum value of the divider is 127 (7Fh), and it should be set to 0.

The register is only meaningful when AUXFANOUT is programmed for PWM output(i.e., Bank0 Index 12h, bit 0 is 0).

9.20 AUXFANOUT Output Value Select Register - Index 11h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Value							
DEFAULT	1	1	1	1	1	1	1	1

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output (Bank 0, Index 12h, bit 0 is 0)	DESCRIPTION	AUXFANOUT PWM Duty Cycle. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
	DEFAULT	1	1	1	1	1	1	1	1
DC Output (Bank 0, Index 12h, bit 0 is 1)	DESCRIPTION	AUXFANOUT Voltage Control. The output voltage is calculated according to this equation: **OUTPUT Voltage =** $AVCC * \frac{FANOUT}{64}$						Reserved	
	DEFAULT	1	1	1	1	1	1		

9.21 FAN Configuration Register II - Index 12h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	CPUFANOUT1 _MIN_VALUE	SYSFANOUT _MIN_VALUE	CPUFANOUT0 _MIN_VALUE	AUXFANOUT _MIN_VALUE	AUXFANOUT _MODE		AUXFANOUT _SEL
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**RESERVED.**
6	**CPUFANOUT1_MINT_VALUE.** 0: CPUFANOUT1 value decreases to zero when the temperature goes below the target range. 1: CPUFANOUT1 value decreases to the value specified in Index 64h when the temperature goes below the target range.
5	**SYSFANOUT_MIN_VALUE.** 0: SYSFANOUT value decreases to zero when the temperature goes below the target range.

BIT	DESCRIPTION
	1: SYSFANOUT value decreases to the value specified in Index 08h when the temperature goes below the target range.
4	**CPUFANOUT0_MIN_VALUE.** 0: CPUFANOUT0 value decreases to zero when the temperature goes below the target range. 1: CPUFANOUT0 value decreases to the value specified in Index 09h when the temperature goes below the target range.
3	**AUXFANOUT_MIN_VALUE.** 0: AUXFANOUT value decreases to zero when the temperature goes below the target range. 1: AUXFANOUT value decreases to the value specified in Index 17h when the temperature goes below the target range.
2-1	**AUXFANOUT_MODE.** **Bits** **2 1** 0 0: AUXFANOUT is in Manual Mode. (Default) 0 1: AUXFANOUT is in Thermal Cruise™ Mode. 1 0: AUXFANOUT is in Fan Speed Cruise™ Mode. 1 1: Reserved and no function.
0	**AUXFANOUT_SEL.** 0: AUXFANOUT pin produces a PWM output duty cycle. (Default) 1: AUXFANOUT pin produces DC output.

9.22 AUXTIN Target Temperature Register/ AUXFANIN0 Target Speed Register - Index 13h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXTIN Target Temperature / AUXFANIN0 Target Speed							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	Reserved	AUXTIN Target Temperature						
	DEFAULT	0	0	0	0	0	0	0	0
Fan Speed Cruise™	DESCRIPTION	AUXFANIN0 Target Speed							
	DEFAULT	0	0	0	0	0	0	0	0

9.23 Tolerance of Target Temperature or Target Speed Register - Index 14h (Bank 0)

Attribute: Read/Write
Size: 8 bits

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	Reserved				Tolerance of AUXTIN Target Temperature			
	DEFAULT	0	0	0	0	0	0	0	0
Fan Speed Cruise™	DESCRIPTION	Reserved				Tolerance of AUXFANIN0 Target Speed			
	DEFAULT	0	0	0	0	0	0	0	0

9.24 AUXFANOUT Stop Value Register - Index 15h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT STOP VALUE							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise™ mode, the AUXFANOUT value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.25 AUXFANOUT Start-up Value Register - Index 16h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT START-UP VALUE							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise™ mode, the AUXFANOUT value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan.

9.26 AUXFANOUT Stop Time Register - Index 17h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT STOP TIME							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise™ mode, if the stop value is enabled, this register determines the amount of time it takes the AUXFANOUT value to fall from the stop value to zero.

(1) For PWM output,
The units are intervals of 0.1 second. The default time is 6 seconds.
(2) For DC output,
The units are intervals of 0.4 second. The default time is 24 seconds.

9.27 OVT# Configuration Register - Index 18h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	DIS_OVT1	RESERVED	OVT1_MODE	RESERVED			
DEFAULT	0	1	0	0	0	0	1	1

BIT	DESCRIPTION
7	**RESERVED.**
6	**DIS_OVT1.** 0: Enable SYSTIN OVT# output. 1: Disable temperature sensor SYSTIN over-temperature (OVT#) output. (Default)
5	**RESERVED.**
4	**OVT1_MODE.** 0: Compare Mode. (Default) 1: Interrupt Mode.
3-0	**RESERVED.**

9.28 Reserved Registers - Index 19h ~ 1Fh (Bank 0)

9.29 Value RAM — Index 20h ~ 3Fh (Bank 0)

ADDRESS A6-A0	DESCRIPTION
20h	CPUVCORE reading
21h	VIN0 reading
22h	AVCC reading
23h	3VCC reading
24h	VIN1 reading
25h	VIN2 reading
26h	VIN3 reading
27h	SYSTIN temperature sensor reading
28h	SYSFANIN reading Note: This location stores the number of counts of the internal clock per revolution.
29h	CPUFANIN0 reading Note: This location stores the number of counts of the internal clock per revolution.
2Ah	AUXFANIN0 reading Note: This location stores the number of counts of the internal clock per revolution.
2Bh	CPUVCORE High Limit
2Ch	CPUVCORE Low Limit
2Dh	VIN0 High Limit
2Eh	VIN0 Low Limit
2Fh	AVCC High Limit
30h	AVCC Low Limit
31h	3VCC High Limit
32h	3VCC Low Limit
33h	VIN1 High Limit
34h	VIN1 Low Limit
35h	VIN2 High Limit
36h	VIN2 Low Limit
37h	VIN3 High Limit
38h	VIN3 Low Limit
39h	SYSTIN temperature sensor High Limit
3Ah	SYSTIN temperature sensor Hysteresis Limit
3Bh	SYSFANIN Fan Count Limit **Note:** It is the number of counts of the internal clock for the Limit of the fan speed.

ADDRESS A6-A0	DESCRIPTION
3Ch	CPUFANIN0 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Limit of the fan speed.
3Dh	AUXFANIN0 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Limit of the fan speed.
3Eh	CPUFANIN1 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Limit of the fan speed.
3Fh	CPUFANIN1 reading Note: This location stores the number of counts of the internal clock per revolution.

9.30 Configuration Register - Index 40h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	INITIALIZATION	EN_WS2	EN_WS1	EN_WS	INT_CLEAR	RESERVED	SMI#ENABLE	START
DEFAULT	0	0	0	0	0	0	1	1

BIT	DESCRIPTION
7	**Initialization.** A one restores the power-on default values to some registers. This bit clears itself since the power-on default of this bit is zero.
6	**EN_WS2.** 1: SMI# output type of temperature AUXTIN is Shut-down Interrupt Mode. 0: SMI# output type is in Shut-down Interrupt Mode. (Default)
5	**EN_WS1.** 1: SMI# output type of temperature CPUTIN is Shut-down Interrupt Mode. 0: SMI# output type is in Shut-down Interrupt Mode. (Default)
4	**EN_WS.** 1: SMI# output type of temperature SYSTIN is Shut-down Interrupt Mode. 0: SMI# output type is in Shut-down Interrupt Mode. (Default)
3	**INT_Clear.** A one disables the SMI# output without affecting the contents of Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing of this bit.
2	**Reserved.**
1	**SMI#Enable.** A one enables the SMI# Interrupt output.
0	**Start.** A one enables startup of monitoring operations. A zero puts the part in standby mode. **Note:** Unlike the "INT_Clear" bit, the outputs of interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred.

9.31 Interrupt Status Register 1 - Index 41h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN0	SYSFANIN	CPUTIN	SYSTIN	3VCC	AVCC	VIN0	CPUVCORE
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**CPUFANIN0.** A one indicates the fan count limit of CPUFANIN0 has been exceeded.
6	**SYSFANIN.** A one indicates the fan count limit of SYSFANIN has been exceeded.
5	**CPUTIN.** A one indicates the high limit of CPUTIN temperature has been exceeded.
4	**SYSTIN.** A one indicates the high limit of SYSTIN temperature has been exceeded.
3	**3VCC.** A one indicates the high or low limit of 3VCC has been exceeded.
2	**AVCC.** A one indicates the high or low limit of AVCC has been exceeded.
1	**VIN0.** A one indicates the high or low limit of VIN0 has been exceeded.
0	**CPUVCORE.** A one indicates the high or low limit of CPUVCORE has been exceeded.

9.32 Interrupt Status Register 2 - Index 42h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TAR2	TAR1	AUXTIN	CASEOPEN	AUXFANIN0	VIN2	VIN3	VIN1
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**TAR2.** A one indicates that the CPUTIN temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise™ mode.
6	**TAR1.** A one indicates that the SYSTIN temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise™ mode.
5	**AUXTIN.** A one indicates the high limit of AUXTIN temperature has been exceeded.
4	**CASEOPEN.** A one indicates the case has been opened.
3	**AUXFANIN0.** A one indicates the fan count limit of AUXFANIN0 has been exceeded.
2	**VIN2.** A one indicates the high or low limit of VIN2 has been exceeded.
1	**VIN3.** A one indicates the high or low limit of VIN3 has been exceeded.
0	**VIN1.** A one indicates the high or low limit of VIn1 has been exceeded.

9.33 SMI# Mask Register 1 - Index 43h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN0	SYSFANIN	CPUTIN	SYSTIN	3VCC	AVCC	VIN0	CPUVCORE
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION	
7	CPUFANIN0	A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 1 – Index 41h (Bank0))
6	SYSFANIN	
5	CPUTIN	
4	SYSTIN	
3	3VCC	
2	AVCC	
1	VIN0	
0	CPUVCORE	

9.34 SMI# Mask Register 2 - Index 44h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TAR2	TAR1	AUXTIN	CASEOPEN	AUXFANIN0	VIN2	VIN3	VIN1
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION	
7	TAR2	A one disables the corresponding interrupt status bit for the interrupt. (See Interrupt Status Register 2 – Index 42h (Bank0))
6	TAR1	
5	AUXTIN	
4	CASEOPEN	
3	AUXFANIN0	
2	VIN2	
1	VIN3	
0	VIN1	

9.35 Interrupt Status Register 4 - Index 45h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved.					Shut_AUX	Shut_CPU	Shut_SYS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	**Reserved.**
2	**Shut_AUX.** A one indicates the SMI# Shut-down mode high limit of AUXTIN temperature has been exceeded.
1	**Shut_CPU.** A one indicates the SMI# Shut-down mode high limit of CPUTIN temperature has been exceeded.
0	**Shut_SYS.** A one indicates the SMI# Shut-down mode high limit of SYSTIN temperature has been exceeded.

9.36 SMI# Mask Register 3 - Index 46h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CASEOPEN CLEAR	RESERVED	Shut_AUX	Shut_CPU	Shut_SYS	AUXFANIN1	CPUFANIN1	RESERVED
DEFAULT	0	0	1	1	1	1	1	1

BIT	DESCRIPTION	
7	**CASEOPEN Clear Control.** Write 1 to this bit will clear CASEOPEN status. This bit will not be self cleared. Please write 0 after the event is cleared. The function is the same as LDA, CR [E6h], bit 5.	
6	**Reserved.**	
5	**Shut_AUX**	A one disables the corresponding interrupt status bit for the $\overline{SMI}$ interrupt. (See Interrupt Status Register 4 – Index 45h (Bank 0)).
4	**Shut_CPU**	
3	**Shut_SYS**	
2	**AUXFANIN1.**	A one disables the corresponding interrupt status bit for the $\overline{SMI}$ interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4)).
1	**CPUFANIN1.**	
0	**Reserved.**	

9.37 Fan Divisor Register I - Index 47h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN0 DIV_B1	CPUFANIN0 DIV_B0	SYSFANIN DIV_B1	SYSFANIN DIV_B0	FANOPV4	FANINC4	FANOPV5	FANINC5
DEFAULT	0	1	0	1	0	1	0	1

BIT	DESCRIPTION	
7	**CPUFANIN0 DIV_B1.**	CPUFANIN0 Divisor, bits 1-0. (See VBAT Monitor Control Register – Index 5Dh (Bank 0))
6	**CPUFANIN0 DIV_B0.**	
5	**SYSFANIN DIV_B1.**	SYSFANIN Divisor, bits 1-0. (See VBAT Monitor Control Register – Index 5Dh (Bank0))
4	**SYSFANIN DIV_B0.**	
3	**FANOPV4. CPUFANIN1 output value**, only if bit 2 is set to zero. Otherwise, this bit has no meaning. 1: Pin 119 (CPUFANIN1) generates a logic-high signal. 0: Pin 119 generates a logic-low signal. (Default)	
2	**FANINC4. CPUFANIN1 Input Control.** 1: Pin 119 (CPUFANIN1) acts as a FAN tachometer input. (Default) 0: Pin 119 acts as a FAN control signal, and the output value is set by register bit 3.	
1	**FANOPV5. AUXFANIN1 output value**, only if bit 0 is set to zero. Otherwise, this bit has no meaning. 1: Pin 58 (AUXFANIN1) generates a logic-high signal. 0: Pin 58 generates a logic-low signal. (Default)	
0	**FANINC5. AUXFANIN1 Input Control.** 1: Pin 58 (AUXFANIN1) acts as a FAN tachometer input. (Default) 0: Pin 58 acts as a FAN control signal, and the output value is set by bit 1.	

9.38 Serial Bus Address Register - Index 48h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	SERIAL BUS ADDR.						
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7	**RESERVED.** (Read only)
6-0	**SERIAL BUS ADDR.** Serial Bus address <7:1>.

9.39 CPUFANOUT0/AUXFANOUT Monitor Temperature Source Select Register - Index 49h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	AUXFANOUT TEMP_SEL[2]	AUXFANOUT TEMP_SEL[1]	AUXFANOUT TEMP_SEL[0]	RESERVED	CPUFANOUT0 TEMP_SEL[2]	CPUFANOUT0 TEMP_SEL[1]	CPUFANOUT TEMP_SEL[0]
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7	**RESERVED.**	
6	**AUXFANOUT TEMP_SEL[2].**	**AUXFANOUT Temperature Source Select.** **Bits** **6 5 4** 0 0 0: Select AUXTIN as AUXFANOUT monitor source (Default). Please be noted that the temperature source / reading in the Bank 2, Index 50 and 51, AUXTIN Temperature Sensor is AUXTIN when this is selected. 0 0 1: Reserved. 0 1 0: Select PECI Agent 1 as AUXFANOUT monitor source. Please be noted that the temperature source / reading in the Bank 2, Index 50 and 51, AUXTIN Temperature Sensor is PECI Agent 1 when this is selected. 0 1 1: Select PECI Agent 2 as AUXFANOUT monitor source. Please be noted that the temperature source / reading in the Bank 2, Index 50 and 51, AUXTIN Temperature Sensor is PECI Agent 2 when this is selected. 1 0 0: Select PECI Agent 3 as AUXFANOUT monitor source. Please be noted that the temperature source / reading in the Bank 2, Index 50 and 51, AUXTIN Temperature Sensor is PECI Agent 3 when this is selected. 1 0 1: Select PECI Agent 4 as AUXFANOUT monitor source. Please be noted that the temperature source / reading in the Bank 2, Index 50 and 51, AUXTIN Temperature Sensor is PECI Agent 4 when this is selected.
5	**AUXFANOUT TEMP_SEL[1].**	
4	**AUXFANOUT TEMP_SEL[0].**	
3	**RESERVED.**	
2	**CPUFANOUT0 TEMP_SEL[2].**	**CPUFANOUT0 Temperature Source Select**. **Bits** **2 1 0** 0 0 0: Select CPUTIN as CPUFANOUT0 monitor

BIT	DESCRIPTION	
1	**CPUFANOUT0 TEMP_SEL[1].**	source (Default). Please be noted that the temperature source / reading in the Bank 1, Index 50 and 51, CPUTIN Temperature Sensor is CPUTIN when this is selected. 0 0 1: Reserved. 0 1 0: Select PECI Agent 1 as CPUFANOUT0 monitor source. Please be noted that the temperature source / reading in the Bank 1, Index 50 and 51, CPUTIN Temperature Sensor is PECI Agent 1 when this is selected. 0 1 1: Select PECI Agent 2 as CPUFANOUT0 monitor source. Please be noted that the temperature source / reading in the Bank 1, Index 50 and 51, CPUTIN Temperature Sensor is PECI Agent 2 when this is selected. 1 0 0: Select PECI Agent 3 as CPUFANOUT0 monitor source. Please be noted that the temperature source / reading in the Bank 1, Index 50 and 51, CPUTIN Temperature Sensor is PECI Agent 3 when this is selected. 1 0 1: Select PECI Agent 4 as CPUFANOUT0 monitor source. Please be noted that the temperature source / reading in the Bank 1, Index 50 and 51, CPUTIN Temperature Sensor is PECI Agent 4 when this is selected.
0	**CPUFANOUT0 TEMP_SEL[0].**	

9.40 CPUFANOUT1 Monitor Temperature Source Select Register - Index 4Ah (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT1 TEMP_SEL[2]	CPUFANOUT1 TEMP_SEL[1]	CPUFANOUT1 TEMP[0]	RESERVED				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7	**CPUFANOUT1 TEMP_SEL[2].**	**CPUFANOUT1 Temperature Source Select Bits** **7 6 5** 0 0 0: Select SYSTIN as CPUFANOUT1 monitor source. (Default)

BIT	DESCRIPTION	
6	**CPUFANOUT1 TEMP_SEL[1].**	0 0 1: Select CPUTIN as CPUFANOUT1 monitor source. 0 1 0: Select AUXTIN as CPUFANOUT1 monitor source. 0 1 1: Reserved. 1 0 0: Select PECI Agent 1 as CPUFANOUT1 monitor source. 1 0 1: Select PECI Agent 2 as CPUFANOUT1 monitor source. 1 1 0: Select PECI Agent 3 as CPUFANOUT1 monitor source. 1 1 1: Select PECI Agent 4 as CPUFANOUT1 monitor source.
5	**CPUFANOUT1 TEMP_SEL[0].**	
4-0	**RESERVED.**	

9.41 Fan Divisor Register II - Index 4Bh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN0 DIV_B1	AUXFANIN0 DIV_B0	ADCOVSEL		RESERVED			
DEFAULT	0	1	0	0	0	1	0	0

BIT	DESCRIPTION
7	**AUXFANIN0 DIV_B1.**
6	**AUXFANIN0 DIV_B0.**
5-4	**ADCOVSEL. A/D Converter Clock Input select.** **Bits** **5 4** 0 0: ADC clock select 22.5 KHz. (Default) 0 1: ADC clock select 5.6 KHz. (22.5K/4) 1 0: ADC clock select 1.4 KHz. (22.5/16) 1 1: ADC clock select 0.35 KHz. (22.5/64)
3-2	**RESERVED.** These two bits should be set to 01h, the default value.
1-0	**RESERVED.**

9.42 SMI#/OVT# Control Register - Index 4Ch (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN1 DIV_B2	T2T3_INT MODE	EN_T1 _ONE	DIS_ OVT3	DIS_ OVT2	OVTPOL	RESERVED	
DEFAULT	0	0	0	1	0	0	0	0

BIT	DESCRIPTION
7	**CPUFANIN1 DIV_B2. CPUFANIN1 Divisor bit 2.**
6	**T2T3_INT MODE.** 1: SMI# output type of Temperature CPUTIN / AUXTIN is in Comparator Interrupt mode. 0: SMI# output type is in Two-Times Interrupt mode. (Default)
5	**EN_T1_ONE.** 1: SMI# output type of temperature SYSTIN is One-Time Interrupt mode. 0: SMI# output type is Two-Times Interrupt mode. (Default)
4	**DIS_OVT3.** 1: Disable temperature sensor AUXTIN over-temperature (OVT) output. (Default) 0: Enable AUXTIN OVT output through pin OVT#.
3	**DIS_OVT2.** 1: Disable temperature sensor CPUTIN over-temperature (OVT) output. 0: Enable CPUTIN OVT output through pin OVT#. (Default)
2	**OVTPOL. Over-temperature polarity.** 1: OVT# active high. 0: OVT# active low. (Default)
1-0	**RESERVED.**

9.43 FAN IN/OUT Control Register - Index 4Dh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		FANOPV3	FANINC3	FANOPV2	FANINC2	FANOPV1	FANINC1
DEFAULT	1	0	0	1	0	1	0	1

BIT	DESCRIPTION
7-6	**RESERVED.**
5	**FANOPV3. AUXFANIN0 output value**, only if bit 4 is set to zero. 1: Pin 111 (AUXFANIN0) generates a logic-high signal. 0: Pin 111 generates a logic-low signal. (Default)
4	**FANINC3. AUXFANIN0 Input Control.**

BIT	DESCRIPTION
	1: Pin 111 (AUXFANIN0) acts as a FAN tachometer input. (Default) 0: Pin 111 acts as a FAN control signal, and the output value is set by bit 5.
3	**FANOPV2. CPUFANIN0 output value**, only if bit 2 is set to zero. 1: Pin 112 (CPUFANIN0) generates a logic-high signal. 0: Pin 112 generates a logic-low signal. (Default)
2	**FANINC2. CPUFANIN0 Input Control.** 1: Pin 112 (CPUFANIN0) acts as a FAN tachometer input. (Default) 0: Pin 112 acts as a FAN control signal, and the output value is set by bit 3.
1	**FANOPV1. SYSFANIN output value**, only if bit 0 is set to zero. 1: Pin 113 (SYSFANIN) generates a logic-high signal. 0: Pin 113 generates a logic-low signal. (Default)
0	**FANINC1. SYSFANIN Input Control.** 1: Pin 113 (SYSFANIN) acts as a FAN tachometer input. (Default) 0: Pin 113 acts as a FAN control signal, and the output value is set by bit 1.

9.44 Register 50h ~ 5Fh Bank Select Register - Index 4Eh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	HBACS	RESERVED	EN_AUXFANIN1_BP	EN_CPUFANIN1_BP	RESERVED	BANKSEL2	BANKSEL1	BANKSEL0
DEFAULT	1	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7	**HBACS. High Byte Access.** 1: Access Index 4Fh high-byte register. (Default) 0: Access Index 4Fh low-byte register.	
6	**RESERVED.**	
5	**EN_AUXFANIN1_BP. BEEP output control for AUXFANIN1** if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)	
4	**EN_CPUFANIN1_BP. BEEP output control for CPUFANIN1** if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)	
3	**RESERVED.** This bit should be set to 0.	
2	**BANKSEL2.**	Bank Select for Index Ports 0x50h ~ 0x5Fh. The three-bit binary value corresponds to the bank number. For example, “010” selects Bank 2.
1	**BANKSEL1.**	
0	**BANKSEL0.**	

9.45 Nuvoton Vendor ID Register - Index 4Fh (Bank 0)

Attribute: Read Only
Size: 16 bits

BIT	15	14	13	12	11	10	9	8
NAME	VIDH							
DEFAULT	0	1	0	1	1	1	0	0

BIT	7	6	5	4	3	2	1	0
NAME	VIDL							
DEFAULT	1	0	1	0	0	0	1	1

BIT	DESCRIPTION
15-8	Vendor ID High-Byte, if Index 4Eh, bit 7 is 1. Default 5Ch.
7-0	Vendor ID Low-Byte, if Index 4Eh, bit 7 is 0. Default A3h.

9.46 Reserved Register - Index 50h ~ 55h (Bank 0)

9.47 BEEP Control Register 1 - Index 56h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	EN_ CPUFANIN0 _BP	EN_ SYSFANIN _BP	EN_ CPUTIN _BP	EN_ SYSTIN _BP	EN_ 3VCC _BP	EN_ AVCC _BP	EN_ VIN0 _BP	EN_ CPUVCORE _BP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**EN_CPUFANIN0_BP. BEEP output control for CPUFANIN0** if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
6	**EN_SYSFANIN_BP. BEEP output control for SYSFANIN** if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
5	**EN_CPUTIN_BP. BEEP output control fro temperature CPUTIN** if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
4	**EN_SYSTIN_BP. BEEP output control for temperature SYSTIN** if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
3	**EN_3VCC_BP. BEEP output control for 3VCC** if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
2	**EN_AVCC_BP. BEEP output control for AVCC** if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
1	**EN_VIN0_BP. BEEP output control for VIN0** if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
0	**EN_CPUVCORE_BP. BEEP output control for CPUVCORE** if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)

9.48 BEEP Control Register 2 - Index 57h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	EN_GBP	EN_ VIN4_BP	EN_ AUXTIN _BP	EN_ CASEOPEN _BP	EN_ AUXFANIN0 _BP	EN_VIN3 _BP	EN_VIN2 _BP	EN_VIN1 _BP
DEFAULT	1	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**EN_GBP. Global BEEP control.** 1: Enable global BEEP output. (Default) 0: Disable all BEEP output.
6	**EN_VIN4_BP. BEEP output control for VIN4** if the monitored value exceeds the limit value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
5	**EN_AUXTIN_BP. BEEP output control for temperature AUXTIN** if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
4	**EN_CASEOPEN_BP. BEEP output control for CASEOPEN** if the case has been opened. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
3	**EN_AUXFANIN0_BP. BEEP output control for AUXFANIN0** if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
2	**EN_VIN3_BP. BEEP output control for VIN3** if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
1	**EN_VIN2_BP. BEEP output control for VIN2** if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
0	**EN_VIN1_BP. BEEP output control for VIN1** if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)

9.49 Chip ID - Index 58h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CHIPID							
DEFAULT	1	1	0	0	0	0	0	1

BIT	DESCRIPTION
7-0	CHIPID. Nuvoton Chip ID number. Default C1h.

9.50 Fan Divisor Selection Register - Index 59h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN1 DIV_B2	RESERVED			AUXFANIN1 DIV_B1	AUXFANIN1 DIV_B0	CPUFANIN1 DIV_B1	CPUFANIN1 DIV_B0
DEFAULT	0	1	1	1	0	0	0	0

BIT	DESCRIPTION	
7	**AUXFANIN1 DIV_B2. AUXFANIN1 Divisor, bit 2.** (See VBAT Monitor Control Register – Index 5Dh (Bank 0))	
6~4		
3	**AUXFANIN1 DIV_B1.**	AUXFANIN1 Divisor, bits 1-0. (See VBAT Monitor Control Register – Index 5Dh (Bank 0))
2	**AUXFANIN1 DIV_B0.**	
1	**CPUFANIN1 DIV_B1**	CPUFANIN1 Divisor, bits 1-0. (See VBAT Monitor Control Register – Index 5Dh (Bank 0))
0	**CPUFANIN1 DIV_B0**	

9.51 Reserved Register - Index 5Ah ~ 5Ch (Bank 0)

9.52 VBAT Monitor Control Register - Index 5Dh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	AUXFANIN0 DIV_B2	CPUFANIN0 DIV_B2	SYSFANIN DIV_B2	RESERVED	DIODES3	DIODES2	DIODES1	EN_ VBAT _MNT
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7	**AUXFANIN0 DIV_B2. AUXFANIN0 Divisor, bit 2.**
6	**CPUFANIN0 DIV_B2. CPUFANIN0 Divisor, bit 2.**
5	**SYSFANIN DIV_B2. SYSFANIN Divisor, bit 2.**
4	**RESERVED.**
3	**DIODES3. Sensor Type Selection for AUXTIN.** 1: Diode sensor. 0: Thermistor sensor.
2	**DIODES2. Sensor Type Selection for CPUTIN.** 1: Diode sensor. 0: Thermistor sensor.
1	**DIODES1. Sensor Type Selection for SYSTIN.** 1: Diode Sensor. 0: Thermistor sensor.
0	**EN_VBAT_MNT.** 1: Enable battery voltage monitor. When this bit changes from zero to one, it takes one monitor cycle time to update the VBAT reading value register. 0: disable battery voltage monitor.

Fan divisor table:

BIT 2	BIT 1	BIT 0	FAN DIVISOR	BIT 2	BIT 1	BIT 0	FAN DIVISOR
0	0	0	**1**	1	0	0	**16**
0	0	1	**2**	1	0	1	**32**
0	1	0	**4**	1	1	0	**64**
0	1	1	**8**	1	1	1	**128**

9.53 Critical Temperature and Current Mode Enable Register - Index 5Eh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	EN_ CPUFANOUT1 CRITICAL TEMP	EN_ AUXFANOUT CRITICAL TEMP	EN_ CPUFANOUT CRITICAL TEMP	EN_ SYSFANOUT CRITICAL TEMP	EN_ AUXTIN CURRENT MODE	EN_ CPUTIN CURRENT MODE	EN_ SYSTIN CURRENT MODE	RESERVED
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7	**EN_CPUFANOUT1 CRITICAL TEMP.** 1: Enable CPUFANOUT1 critical temperature protection. 0: Disable CPUFANOUT1 critical temperature protection. (Default)
6	**EN_AUXFANOUT CRITICAL TEMP.** 1: Enable AUXFANOUT critical temperature protection. 0: Disable AUXFANOUT critical temperature protection. (Default)
5	**EN_CPUFANOUT CRITICAL TEMP.** 1: Enable CPUFANOUT0 critical temperature protection. 0: Disable CPUFANOUT0 critical temperature protection. (Default)
4	**EN_SYSFANOUT CRITICAL TEMP.** 1: Enable SYSFANOUT critical temperature protection. 0: Disable SYSFANOUT critical temperature protection. (Default)
3	**EN_AUXTIN CURRENT MODE.** (To enable the current mode, please also set Bank0, Index 5Dh, Bit 3 to '1') 1: Temperature sensing of AUXTIN by Current Mode. 0: Temperature sensing of AUXTIN depends on the setting of Index 5Dh. (Default)
2	**EN_CPUTIN CURRENT MODE.** (To enable the current mode, please also set Bank0, Index 5Dh, Bit 2 to '1') 1: Temperature sensing of CPUTIN by Current Mode. (Default) 0: Temperature sensing of CPUTIN depends on the setting of Index 5Dh.
1	**EN_SYSTIN CURRENT MODE.** (To enable the current mode, please also set Bank0, Index 5Dh, Bit 1 to '1') 1: Temperature sensing of SYSTIN by Current Mode. 0: Temperature sensing of SYSTIN depends on the setting of Index 5Dh. (Default)
0	**RESERVED.**

9.54 Reserved Register - Index 5Fh (Bank 0)

9.55 CPUFANOUT1 PWM Output Frequency Configuration Register - Index 60h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL4	PWM_SCALE4						
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7	**PWM_CLK_SEL4. CPUFANOUT1 PWM Input Clock Source Select.** This bit selects the clock source for PWM output. 0: The clock source is 24 MHz. 1: The clock source is 180 KHz.
6-0	**PWM_SCALE4. CPUFANOUT1 PWM Pre-Scale Divider.** The clock source of PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. PWM output frequency = $\frac{\text{Input Clock}}{\text{Pre\_Scale Divider}} * \frac{1}{256}$ The maximum value of the divider is 127 (7Fh), and it should not be set to 0.

The register is only meaningful when CPUFANOUT1 is programmed for PWM output.

9.56 CPUFANOUT1 Output Value Select Register - Index 61h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT1 Value							
DEFAULT	Strap by FAN_SET2 (Pin 83)							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output (Bank 0, Index 62h, bit 6 is 0)	DESCRIPTION	CPUFANOUT1 PWM Duty Cycle. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and creates a duty cycle of 0%.							
	DEFAULT	Strap by FAN_SET2 (Pin 83)							
DC Output (Bank 0, Index 62h, bit 6 is 1)	DESCRIPTION	CPUFANOUT1 Voltage Control. The output voltage is calculated according to this equation: **OUTPUT Voltage =** $AVCC * \frac{FANOUT}{64}$						Reserved	
	DEFAULT	Strap by FAN_SET2 (Pin 83)							

9.57 FAN Configuration Register III - Index 62h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	CPUFANOUT1 _SEL	CPUFANOUT1_MODE		TARGET TEMPERATURE TOLERANCE / CPUFANIN1 TARGET SPEED TOLERANCE			
DEFAULT	0	1	0	0	0	0	0	0

BIT	DESCRIPTION	
7	**RESERVED.**	
6	**CPUFANOUT1_SEL. CPUFANOUT1 Output Mode Selection.** 0: CPUFANOUT1 pin produces a PWM output duty cycle. 1: CPUFANOUT1 pin produces DC output. (Default)	
5-4	**CPUFANOUT1_MODE. CPUFANOUT1 Mode Control.** **Bits** **5 4** 0 0: CPUFANOUT1 is in Manual Mode. (Default) 0 1: CPUFANOUT1 is in Thermal Cruise™ Mode. 1 0: CPUFANOUT1 is in Fan Speed Cruise™ Mode. 1 1: CPUFANOUT1 is in SMART FAN™ III Mode.	
3-0	In Thermal Cruise™ mode or SMART FAN™ III Mode: **Tolerance of select temperature source Target Temperature.**	In Fan Speed Cruise™ mode: **Tolerance of CPUFANIN1 Target Speed.**

9.58 Target Temperature Register/CPUFANIN1 Target Speed Register - Index 63h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Target Temperature / Target Speed							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™ or SMART FAN™ III mode	DESCRIPTION	Reserved	Target Temperature of select temperature source.						
	DEFAULT	0	0	0	0	0	0	0	0
Fan Speed Cruise™	DESCRIPTION	CPUFANIN1 Target Speed							
	DEFAULT	0	0	0	0	0	0	0	0

9.59 CPUFANOUT1 Stop Value Register - Index 64h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT1 STOP VALUE							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise™ mode, the CPUFANOUT1 value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.60 CPUFANOUT1 Start-up Value Register - Index 65h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT1 START-UP VALUE							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise™ mode, CPUFANOUT1 value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan.

9.61 CPUFANOUT1 Stop Time Register - Index 66h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT1 STOP TIME							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise™ mode or SMART FAN™ III mode, if the stop value is enabled, this register determines the amount of time it takes the CPUFANOUT1 value to fall from the stop value to zero.

(1)For PWM output:

The units are intervals of 0.1 second. The default time is 6 seconds.

(2)For DC output:

The units are intervals of 0.4 second. The default time is 24 seconds.

9.62 CPUFANOUT0 Maximum Output Value Register - Index 67h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT0 MAX. VALUE							
DEFAULT	1	1	1	1	1	1	1	1

In SMART FAN™ III mode, the CPUFANOUT0 value increases to this value. This value cannot be zero, and it cannot be lower than the CPUFANOUT0 Stop value.

9.63 CPUFANOUT0 Output Step Value Register - Index 68h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT0 STEP							
DEFAULT	0	0	0	0	0	0	0	1

In SMART FAN™ III mode, the CPUFANOUT0 value decreases or increases by this eight-bit value, when needed.

9.64 CPUFANOUT1 Maximum Output Value Register - Index 69h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT1 MAX. VALUE							
DEFAULT	1	1	1	1	1	1	1	1

In SMART FAN™ III mode, the CPUFANOUT1 value increases to this value. This value cannot be zero, and it cannot be lower than the CPUFANOUT1 Stop value.

9.65 CPUFANOUT1 Output Step Value Register - Index 6Ah (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT1 STEP							
DEFAULT	0	0	0	0	0	0	0	1

In SMART FAN™ III mode, the CPUFANOUT1 value decreases or increases by this eight-bit value, when needed.

9.66 SYSFANOUT Critical Temperature register - Index 6Bh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT THRESHOLD TEMPERATURE							
DEFAULT	1	1	1	1	1	1	1	1

In Thermal Cruise™ mode, when the function of SYSFANOUT temperature sensing is enabled, and the monitored temperature exceeds the threshold temperature, the SYSFANOUT will work at full speed.

9.67 CPUFANOUT0 Critical Temperature Register - Index 6Ch (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT0 CRITICAL TEMPERATURE							
DEFAULT	1	1	1	1	1	1	1	1

In Thermal Cruise™ mode, when the function of CPUFANOUT0 temperature sensing is enabled, and the monitored temperature exceeds the threshold temperature, the CPUFANOUT0 will work at full speed.

9.68 AUXFANOUT Critical Temperature Register - Index 6Dh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT CRITICAL TEMPERATURE							
DEFAULT	1	1	1	1	1	1	1	1

In Thermal Cruise™ mode, when the function of AUXFANOUT temperature sensing is enabled, and the monitored temperature exceeds the threshold temperature, the AUXFANOUT will work at full speed.

9.69 CPUFANOUT1 Critical Temperature Register - Index 6Eh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT1 CRITICAL TEMPERATURE							
DEFAULT	1	1	1	1	1	1	1	1

In Thermal Cruise™ mode, when the function of CPUFANOUT1 temperature sensing is enabled, and the monitored temperature exceeds the threshold temperature, the CPUFANOUT1 will work at full speed.

9.70 FANCTRL5 SMART FAN™ III+ Temperature 1 Register (T1) – Index 6Fh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMART FAN IV III+ Temperature 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	SMART FAN™ III+ Temperature 1 Register (T1).

9.71 FANCTRL5 SMART FAN™ III+ Temperature 2 Register (T2) – Index 70h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMART FAN ™ III+ Temperature 2							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	SMART FAN™ III+ Temperature 2 Register (T2).

9.72 FANCTRL5 SMART FAN™ III+ Temperature 3 Register (T3) – Index 71h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMART FAN ™ III+-1 Temperature 3							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	SMART FAN™ III+-1 Temperature 3 Register (T3).

9.73 FANCTRL5 SMART FAN™ III+ DC/PWM 1 Register - Index 72h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMART FAN ™ III+ DC/PWM 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	SMART FAN™ III+ DC/PWM 1 Register.

9.74 FANCTRL5 SMART FAN™ III+ DC/PWM 2 Register - Index 73h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMART FAN ™ III+ DC/PWM 2							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	SMART FAN™ III+ DC/PWM 2 Register.

9.75 FANCTRL5 SMART FAN™ III+ DC/PWM 3 Register - Index 74h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMART FAN™ III+ DC/PWM 3							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SMART FAN™ III+ DC/PWM 3 Register.**

9.76 SMART FAN™ III+-1 input source & output FAN select Register - Index 75h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	SMART FAN™ III+-1 FAN_SEL		SMART FAN™ III+-1 TEMP_SEL			Reserved
DEFAULT	0	0	0	0	1	1	1	0

BIT	DESCRIPTION
7-6	**Reserved.**
5-4	**SMART FAN™ III+-1 FAN_SEL.** **Bits** **5 4** 0 0: SMART FAN™ I → AUXFANOUT SMART FAN™ I or III → CPUFANOUT1 0 1: SMART FAN™ III+ → AUXFANOUT SMART FAN™ I or III → CPUFANOUT1 1 0: SMART FAN™ I → AUXFANOUT SMART FAN™ III+ → CPUFANOUT1 1 1: SMART FAN™ III+ → AUXFANOUT SMART FAN™ III+ → CPUFANOUT1
3-1	**SMART FAN™ III+-1 TEMP_SEL .** **Bits** **3 2 1** 0 0 0: SYS Temperature 0 0 1: CPU Temperature 0 1 0: AUX Temperature 0 1 1: PECI1 1 0 0: PECI2 1 0 1: PECI3 1 1 0: PECI4

BIT	DESCRIPTION
	1 1 1: Reserved (Default)
0	**Reserved.**

9.77 SYSTIN SMI# Shut-down mode High Limit Temperature Register - Index 76h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSTIN SMI# Shut-down mode High Limit Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SYSTIN SMI# Shut-down mode High Limit Temperature.**

9.78 SYSTIN SMI# Shut-down mode Low Limit Temperature Register - Index 77h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSTIN SMI# Shut-down mode Low Limit Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SYSTIN SMI# Shut-down mode Low Limit Temperature.**

9.79 CPUTIN SMI# Shut-down mode High Limit Temperature Register - Index 78h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUTIN SMI# Shut-down mode High Limit Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUTIN SMI# Shut-down mode High Limit Temperature.**

9.80 CPUTIN SMI# Shut-down mode Low Limit Temperature Register - Index 79h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUTIN SMI# Shut-down mode Low Limit Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUTIN SMI# Shut-down mode Low Limit Temperature.**

9.81 AUXTIN SMI# Shut-down mode High Limit Temperature Register - Index 7Ah (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXTIN SMI# Shut-down mode High Limit Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXTIN SMI# Shut-down mode High Limit Temperature.**

9.82 AUXTIN SMI# Shut-down mode Low Limit Temperature Register - Index 7Bh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXTIN SMI# Shut-down mode Low Limit Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXTIN SMI# Shut-down mode Low Limit Temperature.**

9.83 Temperature selection Register - Index 7Ch (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved			MNTEMP2_SEL	MNTEMP1_SEL	Tread_SEL		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**Reserved.**
4	**MNTEMP2_SEL.** 0: CPUTIN Temperature (Default) 1: PECI1
3	**MNTEMP1_SEL.** 0: SYSTIN Temperature (Default) 1: PECI1
2-0	**Tread_SEL. (see Temperature Register – Index 7Dh (Bank 0))** **Bits** **2 1 0** 0 0 0: SYSTIN Temperature (Default) 0 0 1: CPUTIN Temperature 0 1 0: AUXTIN Temperature 0 1 1: Reserved 1 0 0: PECI1 1 0 1: PECI2 1 1 0: PECI3 1 1 1: PECI4

9.84 Temperature Register - Index 7Dh (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Temperature Register							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**Temperature Register. (see Temperature selection Register – Index 7C (Bank 0))**

9.85 CPUTIN Temperature Sensor Temperature (High Byte) Register - Index 50h (Bank 1)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<8:1>							
DEFAULT								

BIT	DESCRIPTION
7-0	**TEMP<8:1>. Temperature <8:1> of the CPUTIN sensor.** The nine-bit value is in units of 0.5°C.

Note: The temperature source / reading is affected by the register value at Bank0, Index 49, bit [2:0]. Please refer to Chapter 9.39 for detail information.

9.86 CPUTIN Temperature Sensor Temperature (Low Byte) Register - Index 51h (Bank 1)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<0>	RESERVED						
DEFAULT								

BIT	DESCRIPTION
7	**TEMP<0>. Temperature <0> of the CPUTIN sensor.** The nine-bit value is in units of 0.5°C.
6-0	**RESERVED.**

Note: The temperature source / reading is affected by the register value at Bank0, Index 49, bit [2:0]. Please refer to Chapter 9.39 for detail information.

9.87 CPUTIN Temperature Sensor Configuration Register - Index 52h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FAULT		RESERVED	OVTMOD	STOP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**RESERVED.** These bits should be set to zero.
4-3	**FAULT.** Number of faults to detect before setting OVT# output. This avoids false strapping due to noise.
2	**RESERVED.** This bit should be set to zero.
1	**OVTMOD. OVT# Mode Select.**

BIT	DESCRIPTION
	0: Compare mode. (Default) 1: Interrupt mode.
0	**STOP.** 0: Monitor CPUTIN. 1: Stop monitoring CPUTIN.

9.88 CPUTIN Temperature Sensor Hysteresis (High Byte) Register - Index 53h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	**THYST<8:1>. Hysteresis temperature bits 8-1.** The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.89 CPUTIN Temperature Sensor Hysteresis (Low Byte) Register - Index 54h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST<0>	RESERVED						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**THYST<0>. Hysteresis temperature bit 0.** The nine-bit value is in units of 0.5°C.
6-0	**RESERVED.**

9.90 CPUTIN Temperature Sensor Over-temperature (High Byte) Register - Index 55h (Bank1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	**TOVF<8:1>. Over-temperature bits 8-1.** The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.91 CPUTIN Temperature Sensor Over-temperature (Low Byte) Register - Index 56h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<0>	RESERVED						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**TOVF<0>. Over-temperature bit 0.** The nine-bit value is in units of 0.5°C.
6-0	**RESERVED.**

9.92 FANCTRL6 SMART FAN™ III+ Temperature 1 Register (T1) – Index 58h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMART FAN ™ III+ Temperature 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SMART FAN™ III+ Temperature 1 Register (T1).**

9.93 FANCTRL6 SMART FAN™ III+ Temperature 2 Register (T2) – Index 59h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMART FAN™ III+ Temperature 2							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SMART FAN™ III+ Temperature 2 Register (T2).**

9.94 FANCTRL6 SMART FAN™ III+ Temperature 3 Register (T3) – Index 5Ah (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMART FAN™ III+ Temperature 3							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SMART FAN™ III+ Temperature 3 Register (T3).**

9.95 FANCTRL6 SMART FAN™ III+ DC/PWM 1 Register - Index 5Bh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMART FAN IV III+ DC/PWM 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SMART FAN™ III+ DC/PWM 1 Register.**

9.96 FANCTRL6 SMART FAN™ III+ DC/PWM 2 Register - Index 5Ch (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMART FAN ™ III+ DC/PWM 2							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SMART FAN™ III+ DC/PWM 2 Register.**

9.97 FANCTRL6 SMART FAN™ III+ DC/PWM 3 Register - Index 5Dh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMART FAN ™ III+ DC/PWM 3							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SMART FAN™ III+ DC/PWM 3 Register.**

9.98 FANCTRL6 SMART FAN™ III+ input source & output FAN select Register - Index 5Eh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	SMART FAN™ III+ FAN_SEL		SMART FAN™ III+ TEMP_SEL			Reserved
DEFAULT	0	0	0	0	1	1	1	0

BIT	DESCRIPTION
7-6	**Reserved.**
5-4	**SMART FAN™ III+ FAN_SEL.** **Bits** **5 4** 0 0: SMART FAN™ I → SYSFANOUT SMART FAN™ I or III → CPUFANOUT0 0 1: SMART FAN™ III+ → SYSFANOUT SMART FAN™ I or III → CPUFANOUT0

BIT	DESCRIPTION
	1 0: SMART FAN™ I → SYSFANOUT SMART FAN™ III+ → CPUFANOUT0 1 1: SMART FAN™ III+ → SYSFANOUT SMART FAN™ III+ → CPUFANOUT0
3-1	**SMART FAN™ III+ TEMP_SEL.** **Bits** **3 2 1** 0 0 0: SYS Temperature 0 0 1: CPU Temperature 0 1 0: AUX Temperature 0 1 1: Reserved 1 0 0: PECI1 1 0 1: PECI2 1 1 0: PECI3 1 1 1: PECI4 (Default)
0	**Reserved.**

9.99 AUXTIN Temperature Sensor Temperature (High Byte) Register - Index 50h (Bank 2)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<8:1>							
DEFAULT								

BIT	DESCRIPTION
7-0	**TEMP<8:1>. Temperature <8:1> of the AUXTIN sensor.** The nine-bit value is in units of 0.5°C.

Note: The temperature source / reading is affected by the register value at Bank0, Index 49, bit [6:4]. Please refer to Chapter 9.39 for detail information.

9.100 AUXTIN Temperature Sensor Temperature (Low Byte) Register - Index 51h (Bank 2)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<0>	RESERVED						
DEFAULT								

BIT	DESCRIPTION
7	**TEMP<0>. Temperature <0> of the AUXTIN sensor.** The nine-bit value is in units of

BIT	DESCRIPTION
	0.5°C.
6-0	**RESERVED.**

Note: The temperature source / reading is affected by the register value at Bank0, Index 49, bit [6:4]. Please refer to Chapter 9.39 for detail information.

9.101 AUXTIN Temperature Sensor Configuration Register - Index 52h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FAULT		RESERVED	OVTMOD	STOP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**RESERVED.** These bits should be set to zero.
4-3	**FAULT.** Number of faults to detect before setting OVT# output. This avoids false strapping due to noise.
2	**RESERVED.**
1	**OVTMOD. OVT# mode select.** 0: Compare Mode. (Default) 1: Interrupt Mode.
0	**STOP.** 0: Monitor AUXTIN. 1: Stop monitoring AUXTIN.

9.102 AUXTIN Temperature Sensor Hysteresis (High Byte) Register - Index 53h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	**THYST<8:1>. Hysteresis temperature, bits 8-1.** The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.103 AUXTIN Temperature Sensor Hysteresis (Low Byte) Register - Index 54h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST<0>	RESERVED						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**THYST<0>. Hysteresis temperature, bit 0.** The nine-bit value is in units of 0.5°C.
6-0	RESERVED.

9.104 AUXTIN Temperature Sensor Over-temperature (High Byte) Register - Index 55h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	**TOVF<8:1>. Over-temperature, bits 8-1.** The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.105 AUXTIN Temperature Sensor Over-temperature (Low Byte) Register - Index 56h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<0>	RESERVED						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**TOVF<0>. Over-temperature, bit 0.** The nine-bit value is in units of 0.5°C.
6-0	**RESERVED.**

9.106 Interrupt Status Register 3 - Index 50h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		AUXFANIN1	CPUFANIN1	RESERVED	TAR3	VBAT	3VSB
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	**RESERVED.**
5	**AUXFANIN1.** A one indicates the fan count limit of AUXFANIN1 has been exceeded.
4	**CPUFANIN1.** A one indicates the fan count limit of CPUFANIN1 has been exceeded.
3	**RESERVED.**
2	**TAR3.** A one indicates that the AUXTIN temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise™ mode.
1	**VBAT.** A one indicates the high or low limit of VBAT has been exceeded.
0	**3VSB.** A one indicates the high or low limit of 3VSB has been exceeded.

9.107 SMI# Mask Register 4 - Index 51h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			TAR3	RESERVED		VBAT	3VSB
DEFAULT	0	0	0	1	0	0	1	1

BIT	DESCRIPTION	
7-5	**RESERVED.**	
4	**TAR3.** A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4)).	
3-2	**RESERVED.**	
1	**VBAT.**	A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4)).
0	**3VSB.**	

9.108 Reserved Register - Index 52h (Bank 4)

9.109 BEEP Control Register 3 - Index 53h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		EN_ USER_BP	RESERVED			EN_ VBAT_BP	EN_ 3VSB_BP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	**RESERVED.**
5	**EN_USER_BP. User-defined BEEP output function.** 0: BEEP is activated. (Default) 1: BEEP is not activated.
4-2	**RESERVED.**
1	**EN_VBAT_BP. BEEP output control for VBAT** if the monitored value exceeds the threshold value. 0: Disable BEEP output. (Default) 1: Enable BEEP output.
0	**EN_3VSB_BP. BEEP output control for 3VSB** if the monitored value exceeds the threshold value. 0: Disable BEEP output. (Default) 1: Enable BEEP output.

9.110 SYSTIN Temperature Sensor Offset Register - Index 54h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**OFFSET<7:0> SYSTIN Temperature Offset Value.** The value in this register is added to the monitored value so that the read value will be the sum of the monitored value and this offset value.

9.111 CPUTIN Temperature Sensor Offset Register - Index 55h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**OFFSET<7:0>. CPUTIN Temperature Offset Value.** The value in this register will be added to the monitored value so that the read value is the sum of the monitored value and this offset value.

9.112 AUXTIN Temperature Sensor Offset Register - Index 56h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**OFFSET<7:0>. AUTIN Temperature Offset Value.** The value in this register is added to the monitored value so that the reading value is the sum of the monitored value and this offset value.

9.113 Reserved Register - Index 57h-58h (Bank 4)

9.114 Real Time Hardware Status Register I - Index 59h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN0 _STS	SYSFANIN _STS	CPUTIN _STS	SYSTIN _STS	3VCC _STS	AVCC _STS	VIN0 _STS	CPUVCORE _STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**CPUFANIN0_STS. CPUFANIN0 Status.** 1: The fan speed count is over the threshold value.

BIT	DESCRIPTION
	0: The fan speed count is in the allowed range.
6	**SYSFANIN_STS. SYSFANIN Status.** 1: The fan speed count is over the threshold value. 0: The fan speed count is in the allowed range.
5	**CPUTIN_STS. CPUTIN Temperature Sensor Status.** 1: The temperature exceeds the over-temperature value. 0: The temperature is under the hysteresis value.
4	**SYSTIN_STS. SYSTIN Temperature Sensor Status.** 1: The temperature exceeds the over-temperature value. 0: The temperature is under the hysteresis value.
3	**3VCC_STS. 3VCC Voltage Status.** 1: The 3VCC voltage is over or under the allowed range. 0: The 3VCC voltage is in the allowed range.
2	**AVCC_STS. AVCC Voltage Status.** 1: The AVCC voltage is over or under the allowed range. 0: The 3VCC voltage is in the allowed range.
1	**VIN0_STS. VIN0 Voltage Status.** 1: The VIN0 voltage is over or under the allowed range. 0: The VIN0 voltage is in the allowed range.
0	**CPUVCORE_STS. CPUVCORE Voltage Status.** 1: The CPUVCORE voltage is over or under the allowed range. 0: The CPUVCORE voltage is in the allowed range.

9.115 Real Time Hardware Status Register II - Index 5Ah (Bank 4)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TAR2 _STS	TAR1 _STS	AUXTIN _STS	CASEOPEN _STS	AUXFANIN0 _STS	CPUFANIN1 _STS	TAR4 _STS	VIN1 _STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**TAR2_STS. Smart Fan of CPUFANIN0 Warning Status.** 1: The selected temperature has been over the target temperature for three minutes at full fan speed in the Thermal Cruise™ mode. 0: The selected temperature has not reached the warning range.
6	**TAR1_STS. Smart Fan of SYSFANIN Warning Status.** 1: The SYSTIN temperature has been over the target temperature for three minutes at full fan speed in the Thermal Cruise™ mode. 0: The SYSTIN temperature has not reached the warning range.
5	**AUXTIN_STS. AUXTIN Temperature Sensor Status.** 1: The temperature exceeds the over-temperature value. 0: The temperature is under the hysteresis value.

BIT	DESCRIPTION
4	**CASEOPEN_STS. CASEOPEN Status.** 1: CASEOPEN is detected and latched. 0: CASEOPEN is not latched.
3	**AUXFANIN0_STS. AUXFANIN0 Status.** 1: The fan speed count is over the threshold value. 0: The fan speed count is in the allowed range.
2	**CPUFANIN1_STS. CPUFANIN1 Status.** 1: The fan speed count is over the threshold value. 0: The fan speed count is in the allowed range.
1	**TAR4_STS. Smart Fan of CPUFANIN1 Warning Status.** 1: The selected temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise™ mode. 0: The selected temperature has not reached the warning range.
0	**VIN1_STS. VIN1 Voltage Status.** 1: The VIN1 voltage is over or under the allowed range. 0: The VIN1 voltage is in the allowed range.

9.116 Real Time Hardware Status Register III - Index 5Bh (Bank 4)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN1 _STS	RESERVED	VIN2 _STS	VIN3 _STS	RESERVED	TAR3 _STS	VBAT _STS	VSB _STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**AUXFANIN1_STS. AIXFANIN1 Status.** 1: The fan speed count is over the threshold value. 0: The fan speed count is in the allowed range.
6	**RESERVED.**
5	**VIN2_STS. VIN2 Voltage Status.** 1: The VIN2 voltage is over or under the allowed range. 0: The VIN2 voltage is in the allowed range.
4	**VIN3_STS. VIN3 Voltage Status.** 1: The VIN3 voltage is over or under the allowed range. 0: The VIN3 voltage is in the allowed range.
3	**RESERVED.**
2	**TAR3_STS. Smart Fan of AUXFANIN Warning Status.** 1: The selected temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise™ mode. 0: The selected temperature has not reached the warning range.
1	**VBAT_STS. VBAT Voltage Status.**

BIT	DESCRIPTION
	1: The VBAT voltage is over or under the allowed range. 0: The VBAT voltage is in the allowed range.
0	**VSB_STS. 3VSB Voltage Status.** 1: The 3VSB voltage is over or under the allowed range. 0: The 3VSB voltage is in the allowed range.

9.117 Reserved Register - Index 5Ch ~ 5Fh (Bank 4)

9.118 Value RAM 2 — Index 50h-59h (Bank 5)

ADDRESS A6-A0	DESCRIPTION
50h	3VSB reading
51h	VBAT reading. The reading is meaningless unless EN_VBAT_MN (Bank0 Index 5Dh, bit0) is set.
52h	Reserved
53h	AUXFANIN1 reading Note: This location stores the number of counts of the internal clock per revolution.
54h	3VSB High Limit
55h	3VSB Low Limit
56h	VBAT High Limit
57h	VBAT Low Limit
58h	Reserved
59h	Reserved
5Ah	Reserved
5Bh	Reserved
5Ch	AUXFANIN1 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.

9.119 SYSFANIN SPEED HIGH-BYTE VALUE (RPM) - Index 50h (Bank 6)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANIN SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION

BIT	DESCRIPTION
7-0	**SYSFANIN SPEED HIGH-BYTE VALUE.**

9.120 SYSFANIN SPEED LOW-BYTE VALUE (RPM) - Index 51h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANIN SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SYSFANIN SPEED LOW-BYTE VALUE.**

9.121 CPUFANIN0 SPEED HIGH-BYTE VALUE (RPM) - Index 52h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN0 SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUFANIN0 SPEED HIGH-BYTE VALUE.**

9.122 CPUFANIN0 SPEED LOW-BYTE VALUE (RPM) - Index 53h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN0 SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUFANIN0 SPEED LOW-BYTE VALUE.**

9.123 AUXFANIN0 SPEED HIGH-BYTE VALUE (RPM) - Index 54h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN0 SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIN0 SPEED HIGH-BYTE VALUE.**

9.124 AUXFANIN0 SPEED LOW-BYTE VALUE (RPM) - Index 55h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN0 SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIN0 SPEED LOW-BYTE VALUE.**

9.125 CPUFANIN1 SPEED HIGH-BYTE VALUE (RPM) - Index 56h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN1 SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUFANIN1 SPEED HIGH-BYTE VALUE.**

9.126 CPUFANIN1 SPEED LOW-BYTE VALUE (RPM) - Index 57h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN1 SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUFANIN1 SPEED LOW-BYTE VALUE.**

9.127 AUXFANIN1 SPEED HIGH-BYTE VALUE (RPM) - Index 58h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN1 SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIN1 SPEED HIGH-BYTE VALUE.**

9.128 AUXFANIN1 SPEED LOW-BYTE VALUE (RPM) - Index 59h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN1 SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIN1 SPEED LOW-BYTE VALUE.**

9.129 FANOUT Configure register of PECI Error - Index 5Ah (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved.					PECI Error Condition		
DEFAULT	0	0	0	0	1	1	0	1

BIT	DESCRIPTION
7-3	**Reserved.**
2-0	**PECI Error Condition** **Bits** **2 1 0** 0 0 0 : FANOUT keeps at its current value 1 1 1 : FANOUT will be set to the pre-configured value when PECI error.

9.130 FANCTRL2 pre-configured fan output value for PECI error - Index 5Bh (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCTRL2 pre-configured fan output value							
DEFAULT	1	1	1	1	1	1	1	1

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	FANCTRL2 PWM Duty Cycle. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
	DEFAULT	1	1	1	1	1	1	1	1
DC Output	DESCRIPTION	FANCTRL2 Voltage Control. The output voltage is calculated according to this equation: **OUTPUT Voltage =** $AVCC * \frac{FANOUT}{64}$						Reserved	
	DEFAULT	1	1	1	1	1	1		

9.131 FANCTRL3 pre-configured fan output value for PECI error - Index 5Ch (Bank 6)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCTRL3 pre-configured fan output value							
DEFAULT	1	1	1	1	1	1	1	1

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	FANCTRL3 PWM Duty Cycle. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
	DEFAULT	1	1	1	1	1	1	1	1
DC Output	DESCRIPTION	FANCTRL3 Voltage Control. The output voltage is calculated according to this equation: **OUTPUT Voltage =** $AVCC * \frac{FANOUT}{64}$						Reserved	
	DEFAULT	1	1	1	1	1	1		

9.132 FANCTRL4 pre-configured fan output value for PECI error - Index 5Dh (Bank 6)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCTRL4 pre-configured fan output value							
DEFAULT	1	1	1	1	1	1	1	1

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	FANCTRL4 PWM Duty Cycle. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
	DEFAULT	1	1	1	1	1	1	1	1
DC Output	DESCRIPTION	FANCTRL4 Voltage Control. The output voltage is calculated according to this equation: **OUTPUT Voltage =** $AVCC * \frac{FANOUT}{64}$						Reserved	
	DEFAULT	1	1	1	1	1	1		

9.133 FANCTRL5 pre-configured fan output value for PECI error - Index 5Eh (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCTRL5 pre-configured fan output value							
DEFAULT	1	1	1	1	1	1	1	1

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	FANCTRL5 PWM Duty Cycle. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
	DEFAULT	1	1	1	1	1	1	1	1
DC Output	DESCRIPTION	FANCTRL5 Voltage Control. The output voltage is calculated according to this equation: **OUTPUT Voltage =** $AVCC * \frac{FANOUT}{64}$						Reserved	
	DEFAULT	1	1	1	1	1	1		

9.134 FANCTRL6 pre-configured fan output value for PECI error - Index 5Fh (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCTRL6 pre-configured fan output value							
DEFAULT	1	1	1	1	1	1	1	1

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	FANCTRL6 PWM Duty Cycle. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
	DEFAULT	1	1	1	1	1	1	1	1
DC Output	DESCRIPTION	FANCTRL6 Voltage Control. The output voltage is calculated according to this equation: **OUTPUT Voltage =** $AVCC * \frac{FANOUT}{64}$						Reserved	
	DEFAULT	1	1	1	1	1	1		

10. SERIAL PERIPHERAL INTERFACE

The W83627DHG-P provides a bridge of the Low Pin Count (LPC) Interface to Serial Peripheral Interface (SPI). The signals in the SPI are transmitted through Pin 2 (SCK), Pin 19 (SCE#), Pin 58 (SI), and Pin 118 (SO). In the Super I/O (W83627DHG-P), these 4 pins are multi-functional. The SPI functions are activated through strapping. Pin 52 determines whether to enable or disable the SPI functions. In the Super I/O (W83627DHG-P), the SPI functions are activated when Pin 52 is pulled-up to the power source. The function status can be seen/read at CR [24h], bit 1.

The SPI is primarily used to store the BIOS ROM. When booting the computer, the memory read instructions or timing sequences are transmitted from the CPU, the South Bridge, the LPC bus to the Super I/O (W83627DHG-P). After receiving the instruction, the Super I/O (W83627DHG-P) generates and transmits the correct instructions and memory addresses to the SPI which responds with the corresponding data of the addresses. The data are placed to the LPC bus by the Super I/O (W83627DHG-P) and returned to the South Bridge. All of the data are read in this manner. By setting the registers shown at Table 10.3, the Super I/O (W83627DHG-P) supports all the instructions given, such as erase, read, program, to SPI flash. For more details, please see Table 10-2 SPI Address Map.

To make it more user-friendly, regularly used SPI instructions/functions can be generated via the LPC I/O read/write commands. That is, the flash devices with SPI can be programmed, erased, or read on the motherboard.

10.1 Using the SPI Interface via the LPC

- The allowed range is 8 bytes above the base address. The base address is configured at Configuration Register CR62h and CR63h in Logical Device 6. For example, if 03h is written to Configuration Register CR62h, and F8h to Configuration Register CR63h, 03F8h ~ 03FFh is the allowed range.

Table 10-1 Base Address Setting

LOGICAL DEVICE	CONFIGURATION REGISTER	BIT	FUNCTION
6	62	7:0	High byte of Base Address
	63	7:0	Low byte of Base Address

- Functions and Definitions

The functions and definitions of the 8 bytes are shown in the following table.

Table 10-2 SPI Address Map

Address	Bit	Function	Description
Base+0	7:0	CMD	Commands or instructions of each SPI device
	7:4	MODE	Mode execution. Please see Table 10-3 MODE for the details of each mode.

Address	Bit	Function	Description
Base+1	3:0	ADD2	Address [19:16]
Base+2	7:0	ADD1	Address [15:8]
Base+3	7:0	ADD0	Address [7:0]
Base+4	7:0	DATA0	Data byte 0
Base+5	7:0	DATA1	Data byte 1
Base+6	7:0	DATA2	Data byte 2
Base+7	7:0	DATA3	Data byte 3

- Usages

Write SPI instructions to Base+0. Set up the addresses and the data in Base+2 ~ Base+7. Implement the instruction by setting the instruction mode in Base+1.

- Accessing SPI Devices

Take erasing the SPI for example, first write the "Chip Erase" instruction to Base+0 and 1Xh[§1] to Base+1 (Bit3~Bit0 of Base +1 is the parameter of address [19:16].). The instruction modes are listed in the table below. For Mode 1, only a one-byte instruction is generated. For Mode 2, in addition to a one-byte instruction, a one-byte parameter, which is set up in Base+4 in advance, is also generated.

[§1] The "X" of 1X stands for the parameters of the address [19:16] (A19~A16, the most significant byte (MSB) of the address).

Table 10-3 MODE

MODE	DEFINITION	FUNCTION	COMMAND EXAMPLE
1	CMD	Command only	Chip Enable, Write Enable, Write Disable
2	CMD_Da(1)	Command with 1byte data write	Write Status Register
3	CMD_Da(2)	Command with 2bytes data read	Read ID (Atmel®)
4	CMD_Add(3)	Command with 3 bytes address	Block Erase, Sector Erase
5	CMD_Ad(3)_Da(1)_W	Command with 3bytes address and 1byte data read	Byte Program (1 byte)
6	CMD_Ad(3)_Da(4)_W	Command with 3bytes address and 4bytes data write	Page Program (4 bytes)
7	CMD_Ad(4)_Da(4)_R	Command with 3bytes and a dummy byte address and 4byte data read	FAST READ (4 bytes)
8	CMD_Ad(3)_Da(1)_R	Command with 3bytes address and 1byte data read	READ, Read Status Read ID (ST/SST®)
9	CMD_Ad(3)_Da(2)_R	Command with 3bytes address and	Read ID (Nuvoton ®)

MODE	DEFINITION	FUNCTION	COMMAND EXAMPLE
		2bytes data read	
a	CMD_Ad(3)_Da(3)_R	Command with 3bytes address and 3bytes data read	Read ID (PMC®)
b	CMD_Ad(3)_Da(4)_R	Command with 3bytes address and 4 bytes data read	

- Reading Data From SPI Devices

  First, write the "Read" instruction to Base+0. Then write the addresses to Base+2 ~ Base+3. Last, write 8X to Base+1.

- Programming SPI Devices

  First, write the "Byte Program" instruction to Base+0. Then write the addresses into Base+2 ~ Base+3 and parameters to Base+4. Last, write 5X to Base+1. For correct programming, make sure the state of the device is ready and write enabled.

* For more details, please see the Programming Guide of the W83627DHG-P.

11. FLOPPY DISK CONTROLLER

11.1 FDC Functional Description

The floppy disk controller (FDC) of the W83627DHG-P integrates all of the logic required for floppy disk control. The FDC implements a FIFO which provides better system performance in multi-master systems, and the digital data separator supports data rates up to 2 M bits/sec.

The FDC includes the following blocks: Precompensation, Data Rate Selection, Digital Data Separator, FIFO, and FDC Core. The rest of this section discusses these blocks through the following topics: FIFO, Data Separator, Write Precompensation, Perpendicular Recording mode, FDC core, FDC commands, and FDC registers.

11.1.1 FIFO (Data)

The FIFO is 16 bytes in size and has programmable threshold values. All command parameter information and disk data transfers go through the FIFO. Data transfers are governed by the RQM (Request for Master) and DIO (Data Input/Output) bits in the Main Status Register.

The FIFO is defaulted to disabled mode after any form of reset, which maintains PC/AT hardware compatibility. The default values can be changed through the configure command. The advantage of the FIFO is that it lets the system have a larger DMA latency without causing disk errors. The following tables give several examples of the delays with the FIFO. The data are based upon the following formula:

DELAY = THRESHOLD # x (1 / DATA RATE) * 8 - 1.5 μs

Table 11-1 The Delays of the FIFO

FIFO THRESHOLD	MAXIMUM DELAY UNTIL SERVICING AT 500K BPS
	Data Rate
1 Byte	1 x 16 μs - 1.5 μs = 14.5 μs
2 Byte	2 x 16 μs - 1.5 μs = 30.5 μs
8 Byte	8 x 16 μs - 1.5 μs = 6.5 μs
15 Byte	15 x 16 μs - 1.5 μs = 238.5 μs
FIFO THRESHOLD	**MAXIMUM DELAY UNTIL SERVICING AT 1M BPS**
	Data Rate
1 Byte	1 x 8 μs - 1.5 μs = 6.5 μs
2 Byte	2 x 8 μs - 1.5 μs = 14.5 μs
8 Byte	8 x 8 μs - 1.5 μs = 62.5 μs
15 Byte	15 x 8 μs - 1.5 μs = 118.5 μs

At the start of a command, the FIFO is always disabled, and command parameters must be sent based upon the RQM and DIO bit settings in the Main Status Register. When the FDC enters the command execution phase, it clears the FIFO off any data to ensure that invalid data are not transferred.

An overrun or underrun terminates the current command and data transfer. Disk writes complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

DMA transfers are enabled by the specify command and are initiated by the FDC when the LDRQ pin is activated during a data transfer command.

11.1.2 Data Separator

The function of the data separator is to lock onto incoming serial read data. When a lock is achieved, the serial front-end logic in the chip is provided with a clock that is synchronized with the read data. The synchronized clock, called the Data Window, is used to internally sample the serial data portion of the bit cell, and the alternate state samples the clock portion. Serial-to-parallel conversion logic separates the read data into clock and data bytes.

The Digital Data Separator (DDS) has three parts: control logic, error adjustment, and speed tracking. The control logic generates RDD and RWD for every pulse input, and any data pulse input is synchronized and then adjusted immediately by error adjustment. A digital integrator keeps track of the speed changes in the input data stream.

11.1.3 Write Precompensation

The write precompensation logic minimizes bit shifts in the RDDATA stream from the disk drive. Shifting of bits is a known phenomenon in magnetic media and depends on the disk media and the floppy drive.

The FDC monitors the bit stream that is being sent to the drive. The data patterns that require precompensation are well known, so, depending on the pattern, the bit is shifted either early or late, relative to the surrounding bits.

11.1.4 Perpendicular Recording Mode

The FDC is also capable of interfacing directly to perpendicular recording floppy drives. Perpendicular recording differs from the traditional longitudinal method in that the magnetic bits are oriented vertically. This scheme packs more data bits into the same area.

FDCs with perpendicular recording drives can read standard 3.5" floppy disks and can read and write perpendicular media. Some manufacturers offer drives that can read and write standard and perpendicular media in a perpendicular media drive.

A single command puts the FDC into perpendicular mode. All other commands operate as they normally do. Perpendicular mode requires a 1 Mbps data rate for the FDC, and, at this data rate, the FIFO manages the host interface bottleneck due to the high speed of data transfer to and from the disk.

11.1.5 FDC Core

The W83627DHG-P FDC is capable of performing twenty commands. Each command is initiated by a multi-byte transfer from the microprocessor, and the result may be a multi-byte transfer back to the microprocessor. Each command consists of three phases: command, execution, and result.

Command

The microprocessor issues all required information to the controller to perform a specific operation.

Execution

The controller performs the specified operation.

Result

After the operation is completed, status information and other housekeeping information are provided to the microprocessor.

The next section introduces each of the commands.

11.1.6 FDC Commands

Command Symbol Descriptions:

C:	Cylinder Number 0 - 256
D:	Data Pattern
DIR:	Step Direction DIR = 0: step out DIR = 1: step in
DS0:	Disk Drive Select 0
DS1:	Disk Drive Select 1
DTL:	Data Length
EC:	Enable Count
EFIFO:	Enable FIFO
EIS:	Enable Implied Seek
EOT:	End of Track
FIFOTHR:	FIFO Threshold
GAP:	Gap Length Selection
GPL:	Gap Length
H:	Head Number
HDS:	Head Number Select
HLT:	Head Load Time
HUT:	Head Unload Time
LOCK:	Lock EFIFO, FIFOTHR, and PTRTRK bits to prevent being affected by software reset
MFM:	MFM or FM Mode
MT:	Multitrack
N:	The number of data bytes written in a sector
NCN:	New Cylinder Number
ND:	Non-DMA Mode
OW:	Overwritten
PCN:	Present Cylinder Number

POLL: Polling Disable
PRETRK: Precompensation Start Track Number
R: Record
RCN: Relative Cylinder Number
R/W: Read/Write
SC: Sectors per Cylinder
SK: Skip deleted data address mark
SRT: Step Rate Time
ST0: Status Register 0
ST1: Status Register 1
ST2: Status Register 2
ST3: Status Register 3
WG: Write gate alters timing of WE

(1) Read Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	0	1	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(2) Read Deleted Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	1	1	0	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(3) Read A Track

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	0	0	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system; FDD reads contents of all cylinders from index hole to EOT
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(4) Read ID

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	0	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the cylinder is stored in the Data Register
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Disk status after the command has been completed
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(5) Verify

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	1	0	1	1	0	Command codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
		---------- DTL/SC ----------								
Execution										No data transfer takes place
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(6) Version

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	0	0	Command code
Result	R	1	0	0	1	0	0	0	0	Enhanced controller

(7) Write Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	0	1	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to Command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and the system
Result	R	---------- ST0 ----------								Status information after Command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after Command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(8) Write Deleted Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	1	0	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and the system
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(9) Format A Track

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	1	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- N ----------								Bytes per Sector
	W	---------- SC ----------								Sectors per Cylinder
	W	---------- GPL ----------								Gap 3
	W	---------- D ----------								Filler Byte
Execution for Each Sector: (Repeat)	W	---------- C ----------								Input Sector Parameters
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- Undefined ----------								
	R	---------- Undefined ----------								
	R	---------- Undefined ----------								
	R	---------- Undefined ----------								

(10) Recalibrate

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	1	1	Command codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0 Interrupt

(11) Sense Interrupt Status

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	0	0	0	Command code
Result	R	---------- ST0 ----------								Status information at the end of each seek operation
	R	---------- PCN ----------								

(12) Specify

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	0	1	1	Command codes
	W	| ---------SRT ---------- | --------- HUT ---------- |								
	W	|---------- HLT ----------| ND								

(13) Seek

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- NCN ----------								
Execution	R									Head positioned over proper cylinder on the diskette

(14) Configure

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	1	Configure information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFIFO	POLL	------ FIFOTHR ----				
	W		----------PRETRK ----------							
Execution										Internal registers written

(15) Relative Seek

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	1	DIR	0	0	1	1	1	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- RCN ----------								

(16) Dumpreg

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	0	Registers placed in FIFO
Result	R	---------- PCN-Drive 0----------								
	R	---------- PCN-Drive 1 ----------								
	R	---------- PCN-Drive 2----------								
	R	---------- PCN-Drive 3 ----------								
	R	--------SRT ----------	--------- HUT --------							
	R	---------- HLT ----------	ND							
	R	---------- SC/EOT ----------								
	R	LOCK	0	D3	D2	D1	D0	GAP	WG	
	R	0	EIS	EFIFO	POLL	------ FIFOTHR --------				
	R	----------PRETRK ----------								

(17) Perpendicular Mode

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	0	Command Code
	W	OW	0	D3	D2	D1	D0	GAP	WG	

(18) Lock

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	LOCK	0	0	1	0	1	0	0	Command Code
Result	R	0	0	0	LOCK	0	0	0	0	

(19) Sense Drive Status

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	0	0	Command Code
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	---------- ST3 ----------								Status information about the disk drive

(20) Invalid

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	---------- Invalid Codes ----------								Invalid codes (no operation-FDC goes to standby state)
Result	R	---------- ST0 ----------								ST0 = 80h

11.2 Register Descriptions

There are several status, data, and control registers in the W83627DHG-P. These registers are defined below, and the rest of this section provides more details about each one of them.

Table 11-2 FDC Registers

ADDRESS OFFSET	REGISTER	
	READ	WRITE
base address + 0	SA REGISTER	
base address + 1	SB REGISTER	
base address + 2		DO REGISTER
base address + 3	TD REGISTER	TD REGISTER
base address + 4	MS REGISTER	DR REGISTER
base address + 5	DT (FIFO) REGISTER	DT (FIFO) REGISTER
base address + 7	DI REGISTER	CC REGISTER

11.2.1 Status Register A (SA Register) (Read base address + 0)

Along with the SB register, the SA register is used to monitor several disk-interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	INIT PEDNDING	RESERVED	STEP	TRAK0#	HEAD	INDEX#	WP#	DIR
DEFAULT	0	0	NA	1	NA	1	1	NA

BIT	DESCRIPTION
7	**INIT PENDING.** This bit indicates the value of the floppy disk interrupt output.
6	**RESERVED.**
5	**STEP.** This bit indicates the complement of the STEP# output.
4	**TRAK0#.** This bit indicates the value of the TRAK0# input.
3	**HEAD.** This bit indicates the complement of the HEAD# output. 0: Side 0. 1: Side 1.
2	**INDEX#.** This bit indicates the value of INDEX# output.
1	**WP#.** 0: The disk is write-protected. 1: The disk is not write-protected.
0	**DIR.** This bit indicates the direction of head movement. 0: Outward direction. 1: Inward direction.

In PS/2 Model 30 mode, the bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	INIT PENDING	DRQ	STEP F/F	TRAK0#	HEAD#	INDEX	WP	DIR#
DEFAULT	0	0	NA	0	NA	0	0	NA

BIT	DESCRIPTION
7	**INIT PENDING.** This bit indicates the value of the floppy disk interrupt output.
6	**DRQ.** This bit indicates the value of the DRQ output pin.
5	**STEP F/F.** This bit indicates the complement of the latched STEP# output.
4	**TRAK0.** This bit indicates the complement of the TRAK0# input.
3	**HEAD#.** This bit indicates the value of the HEAD# value. 0: Side 1. 1: Side 0.
2	**INDEX.** This bit indicates the complement of the INDEX output.
1	**WP.** 0: The disk is not write-protected. 1: The disk is write-protected.
0	**DIR#.** This bit indicates the direction of head movement. 0: Inward direction. 1: Outward direction.

11.2.2 Status Register B (SB Register) (Read base address + 1)

Along with the SA register, the SB register is used to monitor several disk interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME			DRIVE SEL0	WDATA TOGGLE	RDATA TOGGLE	WE	RESERVED	MOT EN A
DEFAULT	1	1	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	**RESERVED.**
5	**DRIVE SEL0.** This bit indicates the status of the DO REGISTER, bit 0 (drive-select bit 0).
4	**WDATA TOGGLE.** This bit changes state on every rising edge of the WD# output pin.
3	**RDATA TOGGLE.** This bit changes state on every rising edge of the RDATA# output pin.
2	**WE.** This bit indicates the complement of the WE# output pin.
1	**RESERVED.**
0	**MOT EN A.** This bit indicates the complement of the MOA# output pin.

In PS/2 Model 30 mode, the bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		DSA#	WD F/F	RDATA F/F	WE F/F	RESERVED	
DEFAULT	0	1	1	0	0	0	1	1

BIT	DESCRIPTION
7-6	**RESERVED.**
5	**DSA#.** This bit indicates the status of the DSA# output pin.
4	**WD F/F.** This bit indicates the complement of the WD# output pin, which is latched on every rising edge of the WD# output pin.
3	**RDATA F/F.** This bit indicates the complement of the latched RDATA# output pin.
2	**WE F/F.** This bit indicates the complement of the latched WE# output pin.
1-0	**RESERVED.**

11.2.3 Digital Output Register (DO Register) (Write base address + 2)

The Digital Output Register is a write-only register that controls drive motors, drive selection, DRQ/IRQ enable, and FDC reset. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			MOTOR ENABLE A	DMA & INT ENABLE	FDC RESET	DRIVE SELECT	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**RESERVED.**
4	**MOTOR ENABLE A.** Motor A on when active high.
3	**DMA & INT ENABLE.** An active high signal enables DRQ/IRQ.
2	**FDC RESET.** Floppy Disk Controller Reset. An active low signal resets the FDC.
1-0	**DRIVE SELECT.** **Bits** **1 0** 0 0: Select Drive A. 0 1: Reserved. 1 0: Reserved. 1 1: Reserved.

11.2.4 Tape Drive Register (TD Register) (Read base address + 3)

This register is used to assign a particular drive number to the tape drive support mode of the data separator. This register also holds the media ID, drive type, and floppy boot drive information for the floppy disk drive.

In normal floppy mode, this register only has bits 0 and 1, and the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED						TAPE SEL 1	TAPE SEL 0
DEFAULT	NA	NA	NA	NA	NA	NA	0	0

BIT	DESCRIPTION
7-2	**RESERVED.**
1	**TAPE SEL 1.**
0	**TAPE SEL 0.**

If the three-mode FDD function is enabled (EN3MODE = 1 in LD0 CRF0, Bit 0), the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	MEDIA ID1	MEDIA ID0	DRIVE TYPE ID1	DRIVE TYPE ID0	FLOPPY BOOT DRIVE 1	FLOPPY BOOT DRIVE 0	TAPE SEL1	TAPE SEL0
DEFAULT	0	0	1	1	0	0	0	0

BIT	DESCRIPTION	
7	**MEDIA ID1.**	These two bits are read-only. These two bits reflect the value of LD0, CR [F1h], bits 5 and 4.
6	**MEDIA ID0.**	
5	**DRIVE TYPE ID1.**	These two bits reflect two of the bits in LD0, CR [F2h]. Which two bits are reflected depends on the last drive selection in the DO register.
4	**DRIVE TYPE ID0.**	
3	**FLOPPY BOOT DRIVE 1.**	These two bits reflect the value of LD0, CR [F1h], bits 7 and 8.
2	**FLOPPY BOOT DRIVE 0.**	
1	**TAPE SEL 1.**	These two bits assign a logical drive number to the tape drive. Drive 0 is not available as a tape drive and is reserved for the floppy disk boot drive.
0	**TAPE SEL 0.**	

TAPE SEL 1	TAPE SEL 0	DRIVE SELECTED
0	0	None
0	1	1

TAPE SEL 1	TAPE SEL 0	DRIVE SELECTED
1	0	2
1	1	3

11.2.5 Main Status Register (MS Register) (Read base address + 4)

The Main Status Register is used to control the flow of data between the microprocessor and the controller. The bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RQM	DIO	NON-DMA MODE	CB	RESERVED			FDD 0 BUSY
DEFAULT	0	NA	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7	**RQM. Request for Master.** A high on this bit indicates Data Register is ready to send or receive data to or from the processor.
6	**DIO. Data Input/Output.** If DIO= HIGH, the transfer is from Data Register to the processor. If DIO=LOW, the transfer is from the processor to Data Register.
5	**NON-DMA MODE.** The FDC is in the non-DMA mode. This bit is set only during the execution phase in the non-DMA mode. Transition to LOW state indicates execution phase has ended.
4	**CB. FDC Busy.** A read or write command is in the process when CB = HIGH.
3-1	**RESERVED.**
0	**FDD0 BUSY.** (D0B = 1). FDD number 0 is in the SEEK mode.

11.2.6 Data Rate Register (DR Register) (Write base address + 4)

The Data Rate Register is used to set the transfer rate and write precompensation. However, in PC-AT and PS/2 Model 30 and PS/2 modes, the data rate is controlled by the CC register, not by the DR register. As a result, the real data rate is determined by the most recent write to either the DR or CC register. The bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	S/W RESET	POWER DOWN	RESERVED	PRECOMP 2	PRECOMP 1	PRECOMP 0	DRATE 1	DRATE 0
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION	
7	**S/W RESET.** This bit is the software reset bit.	
6	**POWER DOWN.** 0: The FDC is in the normal mode. 1: The FDC is in the power-down mode.	
5	**RESERVED.**	
4	**PRECOMP 2.**	These three bits select the value of write

BIT	DESCRIPTION	
3	**PRECOMP 1.**	precompensation. The following tables show the precompensation values for every combination of these bits.
2	**PRECOMP 0.**	
1	**DRATE 1.**	These two bits select the data rate of the FDC and reduced write-current control. Bits 1 0 0 0: 500 KB/S (MFM), 250 KB/S (FM), RWC# = 1 0 1: 300 KB/S (MFM), 150 KB/S (FM), RWC# = 0 1 0: 250 KB/S (MFM), 125 KB/S (FM), RWC# = 0 1 1: 1 MB/S (MFM), Illegal (FM), RWC# = 1 The 2 MB/S data rate for the tape drive is only supported by setting DRATE1 and DRATE0 to 01, as well as setting DRT1 and DRT0 (CR [F4h] and CR [F5h] for logical device 0) to 10. Please see the functional description of CR [F4h] or CR [F5h] and the data rate table for individual data-rate settings.
0	**DRATE 0.**	

PRECOMP	PRECOMPENSATION DELAY	
2 1 0	250K - 1 Mbps	2 Mbps Tape drive
0 0 0	Default Delays	Default Delays
0 0 1	41.67 ns	20.8 ns
0 1 0	83.34 ns	41.17 ns
0 1 1	125.00 ns	62.5ns
1 0 0	166.67 ns	83.3 ns
1 0 1	208.33 ns	104.2 ns
1 1 0	250.00 ns	125.00 ns
1 1 1	0.00 ns (disabled)	0.00 ns (disabled)

DATA RATE	DEFAULT PRECOMPENSATION DELAYS
250 KB/S	125 ns
300 KB/S	125 ns
500 KB/S	125 ns
1 MB/S	41.67ns
2 MB/S	20.8 ns

11.2.7 FIFO Register (R/W base address + 5)

The FIFO register consists of four status registers in a stack, and only one register is presented to the data bus at a time. The FIFO register stores data, commands, and parameters, and it provides disk-drive status information. In addition, data bytes pass through the data register to program or obtain results after a command. In the W83627DHG-P, this register is disabled after reset. The FIFO can enable it and change its values through the configure command.

Status Register 0 (ST0)

BIT	7	6	5	4	3	2	1	0
NAME	IC		SE	EC	NR	HD	US1 DRIVE SELECT	US0 DRIVE SELECT

BIT	DESCRIPTION	
7-6	**IC. Interrupt Code.** **Bits** **7 6** 0 0: Normal termination of command. 0 1: Abnormal termination of command. 1 0: Invalid command issue. 1 1: Abnormal termination because the ready signal from FDD changes state during command execution.	
5	**SE. Seek Mode.** 1: Seek end. 0: Seek error.	
4	**EC. Equipment Check.** 1: When a fault signal is received form the FDD or the track. 0: The signal fails to occur after 77 step pulses.	
3	**NR. Not Ready.** 0: Drive is not ready. 1: Drive is ready.	
2	**HD. Head Address.** 0: Head selected. 1: Head selected.	
1	**US1 DRIVE SELECT.**	Drive Select. **Bits** **1 0** 0 0: Drive A selected. 0 1: Reserved. 1 0: Reserved. 1 1: Reserved.
0	**US0 DRIVE SELECT.**	

Status Register 1 (ST1)

BIT	7	6	5	4	3	2	1	0
NAME	EN	RESERVED	DE	OR	RESERVED	ND	NW	MAM

BIT	DESCRIPTION
7	**EN. End of track.** 1 when the FDC tries to access a sector beyond the final sector of a cylinder
6	**RESERVED.** This bit is always 0.
5	**DE. Data Error.** 1 when the FDC detects a CRC error in either the ID field or the data filed.
4	**OR. Over Run.** 1 if the FDC is not served by the host system within a certain time interval during data transfer.
3	**RESERVED.** This bit is always 0.
2	**ND (No Data).** 1 if the specified sector cannot be found during execution of a read, write or verify data.
1	**NW. Not Writable.** 1 if a write protect signal is detected from the diskette drive during execution of write data.
0	**MAM. Missing Address Mark.** 1 when the FDC cannot detect the data address mark or the data address mark has been deleted.

Status Register 2 (ST2)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	CM	DD	WC	SH	SN	BC	MD

BIT	DESCRIPTION
7	**RESERVED.** This bit is always 0.
6	**CM. Control Mark.** 1: During execution of the read data or scan command. 0: No error.
5	**DD. Data Error in the Data Field.** 1: If the FDC detects a CRC error in the data field. 0: No error.
4	**WC. Wrong Cylinder.** 1 indicates wrong cylinder.
3	**SH. Scan Equal Hit.** 1: During execution of the Scan command, if the equal condition is satisfied. 0: No error.
2	**SN. Scan Not Satisfied.** 1: During execution of the Scan command. 0: No error.
1	**BC. Bad Cylinder.** 1: Bad Cylinder.

BIT	DESCRIPTION
	0: No error.
0	**MD. Missing Address Mark in Data Field.** 1: If the FDC cannot find a data address mark (or the address mark has been deleted) when reading data from the media. 0: No error.

Status Register 3 (ST3)

BIT	7	6	5	4	3	2	1	0
NAME	FT	WP	RY	T0	TS	HD	US1	US0

BIT	DESCRIPTION
7	**FT.** Fault.
6	**WP.** Write Protected.
5	**RY.** Ready.
4	**T0.** Track 0.
3	**TS.** Two-Side.
2	**HD.** Head Address.
1	**US1.** Unit Select 1.
0	**US0.** Unit Select 0.

11.2.8 Digital Input Register (DI Register) (Read base address + 7)

The Digital Input Register is an 8-bit, read-only register used for diagnostic purposes. In PC/XT or PC/AT mode, only bit 7 is checked by the BIOS. When the register is read, bit 7 shows the complement of DSKCHG#, while the other bits remain in tri-state. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	DSKCHG	RESERVED						
DEFAULT	0	NA	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7	**DSKCHG.**
6-0	**RESERVED.** Reserved for the hard disk controller. During a read of this register, these bits are in tri-state.

In PS/2 mode, the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	DSKCHG	RESERVED				DRATE1	DRATE0	HIGH DENS#
DEFAULT	0	1	1	1	1	1	0	1

BIT	DESCRIPTION	
7	**DSKCHG.** This bit indicates the complement of the DSKCHG# input.	
6-3	**RESERVED.** These bits are always logic 1 during a read.	
2	**DRATE1.**	These two bits select the data rate of the FDC. See DR register bits 1 and 0 (Data Rate Register (DR Register) (Write base address + 4)) for how the settings correspond to individual data rates.
1	**DRATE0.**	
0	**HIGH DENS#.** 0: 500 KB/S or 1 MB/S data rate (high-density FDD). 1: 250 KB/S or 300 KB/S data rate.	

In PS/2 Model 30 mode, the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	DSKCHG#	RESERVED			DMAEN	NOPREC	DRATE1	DRATE0
DEFAULT	1	0	0	0	0	0	1	0

BIT	DESCRIPTION	
7	**DSKCHG#.** This bit indicates the status of the DSKCHG# input.	
6-4	**RESERVED.** These bits are always a logic 0 during a read.	
3	**DMAEN.** This bit indicates the value of DO register, bit 3.	
2	**NOPREC.** This bit indicates the value of the NOPREC bit in the CC REGISTER.	
1	**DRATE1.**	These two bits select the data rate of the FDC. See DR register bits 1 and 0 (Data Rate Register (DR Register) (Write base address + 4)) for how the settings correspond to individual data rates.
0	**DRATE0.**	

11.2.9 Configuration Control Register (CC Register) (Write base address + 7)

This register is used to control the data rate. In PC/AT and PS/2 mode, the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED						DRATE1	DRATE0
DEFAULT	NA	NA	NA	NA	NA	NA	1	0

BIT	DESCRIPTION	
7-2	**RESERVED.** These bits should be set to 0.	
1	**DRATE1.**	These two bits select data rate of the FDC. See DR register bits 1 and 0 (Data Rate Register (DR Register) (Write base address + 4)) for how the settings correspond to individual data rates.
0	**DRATE0.**	

In the PS/2 Model 30 mode, the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED					NOPREC	DRATE1	DRATE0
DEFAULT	NA	NA	NA	NA	NA	0	1	0

BIT	DESCRIPTION	
7-3	**RESERVED.** These bits should be set to 0.	
2	**NOPREC.** This bit disables the precompensation function. It can be set by the software.	
1	**DRATE1.**	These two bits select the data rate of the FDC. See DR register bits 1 and 0 (Data Rate Register (DR Register) (Write base address + 4)) for how the settings correspond to individual data rates.
0	**DRATE0.**	

12. UART PORT

12.1 Universal Asynchronous Receiver/Transmitter (UART A, UART B)

The UARTs are used to convert parallel data into serial format for transmission and to convert serial data into parallel format during reception. The serial data format is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one-and-a-half (five-bit format only) or two stop bits. The UARTs are capable of handling divisors of 1 to 65535 and producing a 16x clock for driving the internal transmitter logic. Provisions are also included to use this 16x clock to drive the receiver logic. The UARTs also support the MIDI data rate. Furthermore, the UARTs also include a complete modem control capability and 16-byte FIFOs for reception and transmission to reduce the number of interrupts presented to the CPU.

12.2 Register Description

12.2.1 UART Control Register (UCR) (Read/Write)

The UART Control Register defines and controls the protocol for asynchronous data communication, including data length, stop bit, parity, and baud rate selection.

BIT	7	6	5	4	3	2	1	0
NAME	BDLAB	SSE	PBFE	EPE	PBE	MSBE	DLS1	DLS0
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**BDLAB. Baudrate Divisor Latch Access Bit.** When this bit is set to logical 1, designers can access the divisor (in 16-bit binary format) from the divisor latches of the baud-rate generator during a read or write operation. When this bit is set to logical 0, the Receiver Buffer Register, the Transmitter Buffer Register, and the Interrupt Control Register can be accessed.
6	**SSE. Set Silence Enable.** A logical 1 forces the Serial Output (SOUT) to a silent state (a logical 0). Only IRTX is affected by this bit; the transmitter is not affected.
5	**PBFE. Parity Bit Fixed Enable.** When PBE and PBFE of UCR are both set to logical 1, (1) If EPE is logical 1, the parity bit is fixed at logical 0 when transmitting and checking. (2) If EPE is logical 0, the parity bit is fixed at logical 1 when transmitting and checking.
4	**EPE. Even Parity Enable.** When PBE is set to logical 1, this bit counts the number of logical 1's in the data word bits and determines the parity bit. When this bit is set to logical 1, the parity bit is set to logical 1 if an even number of logical 1's are sent or checked. When the bit is set to logical 0, the parity bit is logical 1 if an odd number of logic 1's are sent or checked.
3	**PBE. Parity Bit Enable.** When this bit is set to logical 1, the transmitter inserts a stop bit between the last data bit and the stop bit of the SOUT, and the receiver checks the parity bit in the same position.
2	**MSBE. Multiple Stop Bits Enable.** This bit defines the number of stop bits in each serial character that is transmitted or received. (1) If MSBE is set to logical 0, one stop bit is sent and checked. (2) If MSBE is set to logical 1 and the data length is 5 bits, one-and-a-half stop bits are sent and checked. (3) If MSBE is set to logical 1 and the data length is 6, 7 or 8 bits, two stop bits are sent

BIT	DESCRIPTION	
	and checked.	
1	**DLS1. Data Length Select Bit 1.**	These two bits define the number of data bits that are sent or checked in each serial character.
0	**DLS0. Data Length Select Bit 0.**	

DLS1	DLS0	DATA LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

The following table identifies the remaining UART registers. Each one is described separately in the following sections.

Table 12-1 Register Summary for UART

Register Address Base			Bit Number 0	1	2	3	4	5	6	7
+ 0 BDLAB = 0	Receiver Buffer Register (Read Only)	RBR	RX Data Bit 0	RX Data Bit 1	RX Data Bit 2	RX Data Bit 3	RX Data Bit 4	RX Data Bit 5	RX Data Bit 6	RX Data Bit 7
+ 0 BDLAB = 0	Transmitter Buffer Register (Write Only)	TBR	TX Data Bit 0	TX Data Bit 1	TX Data Bit 2	TX Data Bit 3	TX Data Bit 4	TX Data Bit 5	TX Data Bit 6	TX Data Bit 7
+ 1 BDLAB = 0	Interrupt Control Register	ICR	RBR Data Ready Interrupt Enable (ERDRI)	TBR Empty Interrupt Enable (ETBREI)	USR Interrupt Enable (EUSRI)	HSR Interrupt Enable (EHSRI)	0	0	0	0
+ 2	Interrupt Status Register (Read Only)	ISR	"0" if Interrupt Pending	Interrupt Status Bit (0)	Interrupt Status Bit (1)	Interrupt Status Bit (2)**	0	0	FIFOs Enabled **	FIFOs Enabled **
+ 2	UART FIFO Control Register (Write Only)	UFR	FIFO Enable	RCVR FIFO Reset	XMIT FIFO Reset	DMA Mode Select	Reserved	Reversed	RX Interrupt Active Level (LSB)	RX Interrupt Active Level (MSB)
+ 3	UART Control Register	UCR	Data Length Select Bit 0 (DLS0)	Data Length Select Bit 1 (DLS1)	Multiple Stop Bits Enable (MSBE)	Parity Bit Enable (PBE)	Even Parity Enable (EPE)	Parity Bit Fixed Enable PBFE)	Set Silence Enable (SSE)	Baudrate Divisor Latch Access Bit (BDLAB)
+ 4	Handshake Control Register	HCR	Data Terminal Ready (DTR)	Request to Send (RTS)	Loopback RI Input	IRQ Enable	Internal Loopback Enable	0	0	0
+ 5	UART Status Register	USR	RBR Data Ready (RDR)	Overrun Error (OER)	Parity Bit Error (PBER)	No Stop Bit Error (NSER)	Silent Byte Detected (SBD)	TBR Empty (TBRE)	TSR Empty (TSRE)	RX FIFO Error Indication (RFEI) **
+ 6	Handshake Status Register	HSR	CTS Toggling (TCTS)	DSR Toggling (TDSR)	RI Falling Edge (FERI)	DCD Toggling (TDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
+ 7	User Defined Register	UDR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 0 BDLAB = 1	Baudrate Divisor Latch Low	BLL	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 1 BDLAB = 1	Baudrate Divisor Latch High	BHL	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

*: Bit 0 is the least significant bit. The least significant bit is the first bit serially transmitted or received.
**: These bits are always 0 in 16450 Mode.

12.2.2 UART Status Register (USR) (Read/Write)

This 8-bit register provides information about the status of data transfer during communication.

BIT	7	6	5	4	3	2	1	0
NAME	RFEI	TSRE	TBRE	SBD	NSER	PBER	OER	RDR
DEFAULT	0	1	1	0	0	0	0	0

BIT	DESCRIPTION
7	**RFEI. RX FIFO Error Indication.** In 16450 mode, this bit is always set to logical 0. In 16550 mode, this bit is set to logical 1 when there is at least one parity-bit error and no stop-bit error or silent-byte detected in the FIFO. In 16550 mode, this bit is cleared to logical 0 by reading from the USR if there are no remaining errors left in the FIFO.
6	**TSRE. Transmitter Shift Register Empty.** In 16450 mode, this bit is set to logical 1 when TBR and TSR are both empty. In 16550 mode, it is set to logical 1 when the transmit FIFO and TSR are both empty. Otherwise, this bit is set to logical 0.
5	**TBRE. Transmitter Buffer Register Empty.** In 16450 mode, when a data character is transferred from TBR to TSR, this bit is set to logical 1. If ETREI or ICR is high, an interrupt is generated to notify the CPU to write the next data. In 16550 mode, this bit is set to logical 1 when the transmit FIFO is empty. It is set to logical 0 when the CPU writes data into TBR or the FIFO.
4	**SBD. Silent Byte Detected.** This bit is set to logical 1 to indicate that received data are kept in silent state for the time it takes to receive a full word, which includes the start bit, data bits, parity bit, and stop bits. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
3	**NSER. No Stop Bit Error.** This bit is set to logical 1 to indicate that the received data have no stop bit. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
2	**PBER. Parity Bit Error.** This bit is set to logical 1 to indicate that the received data has the wrong parity bit. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
1	**OER. Overrun Error.** This bit is set to logical 1 to indicate that the received data have been overwritten by the next received data before they are read by the CPU. In 16550 mode, it indicates the same condition, instead of FIFO full. When the CPU reads USR, it sets this bit to logical 0.
0	**RDR. RBR Data Ready.** This bit is set to logical 1 to indicate that the received data are ready to be read by the CPU in the RBR or FIFO. When no data are left in the RBR or FIFO, the bit is set to logical 0.

12.2.3 Handshake Control Register (HCR) (Read/Write)

This register controls pins used with handshaking peripherals such as modems and also controls the diagnostic mode of the UART.

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			INTERNAL LOOPBACK ENABLE	IRQ ENABLE	LOOPBACK RI INPUT	RTS	DTR
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**RESERVED.**
4	**INTERNAL LOOPBACK ENABLE.** When this bit is set to logical 1, the UART enters diagnostic mode, as follows: (1) SOUT is forced to logical 1, and SIN is isolated from the communication link. (2) The modem output pins are set to their inactive state. (3) The modem input pins are isolated from the communication link and connect internally as DTR(bit 0 of HCR) →DSR#, RTS (bit 1 of HCR) →CTS#, Loopback RI input (bit 2 of HCR) → RI# and IRQ enable (bit 3 of HCR) →DCD#. Aside from the above connections, the UART operates normally. This method allows the CPU to test the UART in a convenient way.
3	**IRQ ENABLE.** The UART interrupt output is enabled by setting this bit to logical 1. In diagnostic mode, this bit is internally connected to the modem control input DCD#.
2	**LOOPBACK RI INPUT.** This bit is only used in the diagnostic mode. In diagnostic mode, this bit is internally connected to the modem control input RI#.
1	**RTS. Request to Send.** This bit controls the RTS# output. The value of this bit is inverted and output to RTS#.
0	**DTR. Data Terminal Ready.** This bit controls the DTR# output. The value of this bit is inverted and output to DTR#.

12.2.4 Handshake Status Register (HSR) (Read/Write)

This register reflects the current state of the four input pins used with handshake peripherals such as modems and records changes on these pins.

BIT	7	6	5	4	3	2	1	0
NAME	DCD	RI	DSR	CTS	TDCD	FERI	TDSR	TCTS
DEFAULT	NA	NA	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7	**DCD. Data Carrier Detect.** This bit is the opposite of the DCD# input. This bit is equivalent to bit 3 of HCR in the loopback mode.
6	**RI. Ring Indicator.** This bit is the opposite of the RI# input. This bit is equivalent to bit 2 of HCR in the loopback mode.
5	**DSR. Data Set Ready.** This bit is the opposite of the DSR# input. This bit is equivalent to bit 0 of HCR in the loopback mode.
4	**CTS. Clear to Send.** This bit is the opposite of the CTS# input. This bit is equivalent to bit 1 of HCR in the loopback mode.
3	**TDCD. DCD# Toggling.** This bit indicates that the DCD# pin has changed state after HSR was read by the CPU.
2	**FERI. RI Falling Edge.** This bit indicates that the RI# pin has changed from low to high after HSR was read by the CPU.
1	**TDSR. DSR# Toggling.** This bit indicates that the DSR# pin has changed state after HSR was read by the CPU.
0	**TCTS. CTS# Toggling.** This bit indicates that the CTS# pin has changed state after HSR was read by the CPU.

12.2.5 UART FIFO Control Register (UFR) (Write only)

This register is used to control the FIFO functions of the UART.

BIT	7	6	5	4	3	2	1	0
NAME	RX IAL (MSB)	RXIAL (LSB)	RESREVED		DMA MODE SELECT	TRANSMITTER FIFO RESET	RECEIVER FIFO RESET	FIFO ENABLE
DEFAULT	0	0	NA	NA	0	0	0	0

BIT	DESCRIPTION	
7	**RX IAL (MSB). RX INTERRUPT ACTIVE LEVEL.**	These two bits are used to set the active level of the receiver FIFO interrupt. The active level is the number of bytes that must be in the receiver FIFO to generate an interrupt.
6	**RX IAL (LSB). RX INTERRUPT ACTIVE LEVEL.**	
5-4	**RESERVED.**	
3	**DMA MODE SELECT.** When this bit is set to logical 1, the DMA mode changes from mode 0 to mode 1 if UFR bit 0 = 1.	
2	**TRANSMITTER FIFO RESET.** Setting this bit to logical 1 resets the TX FIFO counter logic to its initial state. This bit is automatically cleared afterwards.	
1	**RECEIVER FIFO RESET.** Setting this bit to logical 1 resets the RX FIFO counter logic to its initial state. This bit is automatically cleared afterwards.	
0	**FIFO ENABLE.** This bit enables 16550 mode. This bit should be set to logical 1 before the other UFR bits are programmed.	

BIT 7	BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

12.2.6 Interrupt Status Register (ISR) (Read only)

This register reflects the UART interrupt status.

BIT	7	6	5	4	3	2	1	0
NAME	FIFOS ENABLED		RESERVED		INTERRUPT STATUS BIT2	INTERRUPT STATUS BIT1	INTERRUPT STATUS BIT0	0 IF INTERRUPT PENDING
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-6	**FIFOS ENABLED.** These two bits are set to logical 1 when UFR, bit 0 = 1.
5-4	**RESERVED.** These two bits are always logical 0.

BIT	DESCRIPTION	
3	**INTERRUPT STATUS BIT2.** In 16450 mode, this bit is logical 0. In 16550 mode, bit 3 and 2 are set to logical 1 when a time-out interrupts is pending. See the table below.	
2	**INTERRUPT STATUS BIT1.**	These two bits identify the priority level of the pending interrupt, as shown in the table below.
1	**INTERRUPT STATUS BIT0.**	
0	**0 IF INTERRUPT PENDING.** This bit is logical 1 if there is no interrupt pending. If one of the interrupt sources has occurred, this bit is set to logical 0.	

ISR				INTERRUPT SET AND FUNCTION			
Bit 3	Bit 2	Bit 1	Bit 0	Interrupt priority	Interrupt Type	Interrupt Source	Clear Interrupt
0	0	0	1	-	-	No Interrupt pending	-
0	1	1	0	First	UART Receive Status	1. OER = 1 2. PBER =1 3. NSER = 1 4. SBD = 1	Read USR
0	1	0	0	Second	RBR Data Ready	1. RBR data ready 2. FIFO interrupt active level reached	1. Read RBR 2. Read RBR until FIFO data under active level
1	1	0	0	Second	FIFO Data Timeout	Data present in RX FIFO for 4 characters period of time since last access of RX FIFO.	Read RBR
0	0	1	0	Third	TBR Empty	TBR empty	1. Write data into TBR 2. Read ISR (if priority is third)
0	0	0	0	Fourth	Handshake status	1. TCTS = 1 2. TDSR = 1 3. FERI = 1 4. TDCD = 1	Read HSR

** Bit 3 of ISR is enabled when bit 0 of UFR is logical 1.

12.2.7 Interrupt Control Register (ICR) (Read/Write)

This 8-bit register enables and disables the five types of controller interrupts separately. A selected interrupt can be enabled by setting the appropriate bit to logical 1. The interrupt system can be totally disabled by setting bits 0 through 3 to logical 0.

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				EHSRI	EUSRI	ETBREI	ERDRI
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	**RESERVED.** These four bits are always logical 0.
3	**EHSRI.** Set this bit to logical 1 to enable the handshake status register interrupt.
2	**EUSRI.** Set this bit to logical 1 to enable the UART status register interrupt.
1	**ETBREI.** Set this bit to logical 1 to enable the TBR empty interrupt.
0	**ERDRI.** Set this bit to logical 1 to enable the RBR data ready interrupt.

12.2.8 Programmable Baud Generator (BLL/BHL) (Read/Write)

Two 8-bit registers, BLL and BHL, compose a programmable baud generator that uses 24 MHz to generate a 1.8461 MHz frequency and divide it by a divisor from 1 to (2^{16} –1). The output frequency of the baud generator is the baud rate multiplied by 16, and this is the base frequency for the transmitter and receiver. The table below illustrates the use of the baud generator with a frequency of 1.8461 MHz. In high-speed UART mode (CR0C, bits 7 and 6), the programmable baud generator directly uses 24 MHz and the same divisor as the normal speed divisor. As a result, in high-speed mode, the data transmission rate can be as high as 1.5M bps.

BAUD RATE FROM DIFFERENT PRE-DIVIDER			
PRE-DIV: 13 1.8461M HZ	**PRE-DIV: 1.0 24M HZ**	**DECIMAL DIVISOR USED TO GENERATE 16X CLOCK**	**ERROR PERCENTAGE**
50	650	2304	**
75	975	1536	**
110	1430	1047	0.18%
134.5	1478.5	857	0.099%
150	1950	768	**
300	3900	384	**
600	7800	192	**
1200	15600	96	**
1800	23400	64	**
2000	26000	58	0.53%
2400	31200	48	**
3600	46800	32	**
4800	62400	24	**
7200	93600	16	**
9600	124800	12	**
19200	249600	6	**
38400	499200	3	**
57600	748800	2	**
115200	1497600	1	**

** Unless specified, the error percentage for all of the baud rates is 0.16%.

Note: Pre-Divisor is determined by CRF0 of UART A and B.

12.2.9 User-defined Register (UDR) (Read/Write)

This is a temporary register that can be accessed and defined by the user.

13. PARALLEL PORT

13.1 Printer Interface Logic

The W83627DHG-P parallel port can be attached to devices that accept eight bits of parallel data at standard TTL level. The W83627DHG-P supports the IBM XT/AT compatible parallel port (SPP), the bi-directional parallel port (BPP), the Enhanced Parallel Port (EPP), and the Extended Capabilities Parallel Port (ECP) on the parallel port.

The following tables show the pin definitions for different modes of the parallel port.

Table 13-1 Pin Descriptions for SPP, EPP, and ECP Modes

HOST CONNECTOR	PIN NUMBER OF W83627DHG-P	PIN ATTRIBUTE	SPP	EPP	ECP
1	36	O	nSTB	nWrite	nSTB, HostClk[2]
2-9	31-26, 24-23	I/O	PD<0:7>	PD<0:7>	PD<0:7>
10	22	I	nACK	Intr	nACK, PeriphClk[2]
11	21	I	BUSY	nWait	BUSY, PeriphAck[2]
12	19	I	PE	PE	PEerror, nAckReverse[2]
13	18	I	SLCT	Select	SLCT, Xflag[2]
14	35	O	nAFD	nDStrb	nAFD, HostAck[2]
15	34	I	nERR	nError	nFault[1], nPeriphRequest[2]
16	33	O	nINIT	nInit	nINIT[1], nReverseRqst[2]
17	32	O	nSLIN	nAStrb	nSLIN[1], ECPMode[2]

Notes:

n<name > : Active Low

1. Compatible Mode
2. High Speed Mode
3. For more information, please refer to the IEEE 1284 standard.

HOST CONNECTOR	PIN NUMBER OF W83627DHG-P	PIN ATTRIBUTE	SPP
1	36	O	nSTB
2	31	I/O	PD0
3	30	I/O	PD1
4	29	I/O	PD2
5	28	I/O	PD3
6	27	I/O	PD4
7	26	I/O	PD5
8	24	I/O	PD6
9	23	I/O	PD7
10	22	I	nACK
11	21	I	BUSY
12	19	I	PE
13	18	I	SLCT
14	35	O	nAFD
15	34	I	nERR
16	33	O	nINIT

HOST CONNECTOR	PIN NUMBER OF W83627DHG-P	PIN ATTRIBUTE	SPP
17	32	O	nSLIN

13.2 Enhanced Parallel Port (EPP)

The following table lists the registers used in the EPP mode and identifies the bit map of the parallel port and EPP registers. Some of the registers are used in other modes as well.

Table 13-2 EPP Register Addresses

A2	A1	A0	REGISTER	NOTE
0	0	0	Data pot (R/W)	1
0	0	1	Printer status buffer (Read)	1
0	1	0	Printer control latch (Write)	1
0	1	0	Printer control swapper (Read)	1
0	1	1	EPP address port (R/W)	2
1	0	0	EPP data port 0 (R/W)	2
1	0	1	EPP data port 1 (R/W)	2
1	1	0	EPP data port 2 (R/W)	2
1	1	1	EPP data port 2 (R/W)	2

Notes:

1. These registers are available in all modes.
2. These registers are available only in EPP mode.

Table 13-3 Address and Bit Map for SPP and EPP Modes

REGISTER	7	6	5	4	3	2	1	0
Data Port (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Status Buffer (Read)	BUSY#	ACK#	PE	SLCT	ERROR#	1	1	TMOUT
Control Swapper (Read)	1	1	1	IRQEN	SLIN	INIT#	AUTOFD#	STROBE#
Control Latch (Write)	1	1	DIR	IRQ	SLIN	INIT#	AUTOFD#	STROBE#
EPP Address Port (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 0 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 1 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 2 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 3 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Each register (or pair of registers, in some cases) is discussed below.

13.2.1 Data Port (Data Swapper)

The CPU reads the contents of the printer's data latch by reading the data port.

13.2.2 Printer Status Buffer

The CPU reads the printer status by reading the printer status buffer. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	BUSY#	ACK#	PE	SLCT	ERROR#	RESERVED		TMOUT
DEFAULT	NA	NA	NA	NA	NA	1	1	0

BIT	DESCRIPTION
7	**BUSY#.** This signal is active during data entry, when the printer is off-line during printing, when the printer head is changing position, or in an error state. When this signal is active, the printer is busy and cannot accept data.
6	**ACK#.** This bit represents the current state of the printer's ACK# signal. A logical 0 means the printer has received a character and is ready to accept another. Normally, this signal is active for approximately before 5 μs BUSY# stops.
5	**PE.** A logical 1 means the printer has detected the end of paper.
4	**SLCT.** A logical 1 means the printer is selected.
3	**ERROR#.** A logical 0 means the printer has encountered an error condition.
2-1	**RESERVED.** These bits are always read as logical 1.
0	**TMOUT.** This bit is only valid in the EPP mode. A logical 1 indicates that a 10 μs time-out has occurred on the EPP bus. A logical 0 means that no time-out error has occurred. Writing a logical 1 to this bit clears the time-out status bit; writing a logical 0 has no effect.

13.2.3 Printer Control Latch and Printer Control Swapper

The CPU reads the contents of the printer control latch by reading the printer control swapper. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		DIR	IRQ ENABLE	SLCT IN	INIT#	AUTO FD	STROBE
DEFAULT	1	1	NA	0	NA	NA	NA	NA

BIT	DESCRIPTION
7-6	**RESERVED.** These two bits are always read as logical 1. They can be written.
5	**DIR. Direction Control Bit.** When this bit is logical 1, the parallel port is in the input mode (read). When it is logical 0, the parallel port is in the output mode (write). This bit can be read and written. In the SPP mode, this bit is invalid and fixed at zero.
4	**IRQ ENABLE.** A logical 1 allows an interrupt to occur when ACK# changes from low to high.
3	**SLCT IN.** A logical 1 selects the printer.
2	**INIT#.** A logical 0 starts the printer (50 microsecond pulse, minimum).
1	**AUTO FD.** A logical 1 causes the printer to line-feed after a line is printed.
0	**STROBE.** A logical 1 generates an active-high pulse for a minimum of 0.5 μs to clock data into the printer. Valid data must be present for a minimum of 0.5 μs before and after the strobe pulse.

13.2.4 EPP Address Port

The address port is available only in EPP mode. Bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

The contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of IOW# causes an EPP address write cycle to be performed, and the trailing edge of IOW# latches the data for the duration of the EPP write cycle.

PD0-PD7 ports are read during a read operation. The leading edge of IOR# causes an EPP address read cycle to be performed and the data to be output to the host CPU.

13.2.5 EPP Data Port 0-3

These four registers are available only in EPP mode. The bit definitions for each data port are the same and as follows:

BIT	7	6	5	4	3	2	1	0
NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

When any EPP data port is accessed, the contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of IOW# causes an EPP data write cycle to be performed, and the trailing edge of IOW# latches the data for the duration of the EPP write cycle.

During a read operation, ports PD0-PD7 are read, and the leading edge of IOR# causes an EPP read cycle to be performed and the data to be output to the host CPU.

13.2.6 EPP Pin Descriptions

EPP NAME	TYPE	EPP DESCRIPTION
NWrite	O	Denotes read or write operation for address or data.
PD<0:7>	I/O	Bi-directional EPP address and data bus.
Intr	I	Used by peripheral devices to interrupt the host.
NWait	I	Inactivated to acknowledge that data transfer is complete. Activated to indicate that the device is ready for the next transfer.
PE	I	Paper end; same as SPP mode.
Select	I	Printer-select status; same as SPP mode.
NDStrb	O	This signal is active low. It denotes a data read or write operation.
Nerror	I	Error; same as SPP mode.
Ninits	O	This signal is active low. When it is active, the EPP device is reset to its initial operating mode.
NAStrb	O	This signal is active low. It denotes an address read or write operation.

13.2.7 EPP Operation

When EPP mode is selected, the PDx bus is in standard or bi-directional mode when no EPP read, write, or address cycle is being executed. In this situation, all output signals are set by the SPP Control Port and the direction is controlled by DIR of the Control Port.

A watchdog timer is required to prevent system lockup. The timer indicates that more than 10 µs have elapsed from the start of the EPP cycle to the time WAIT# is deasserted. The current EPP cycle is aborted when a time-out occurs. The time-out condition is indicated in status bit 0.

The EPP operates on a two-phase cycle. First, the host selects the register within the device for subsequent operations. Second, the host performs a series of read and/or write byte operations to the selected register. Four operations are supported on the EPP: Address Write, Data Write, Address Read, and Data Read. All operations on the EPP device are performed asynchronously.

13.2.7.1. EPP Version 1.9 Operation

The EPP read/write operation can be completed under the following conditions:

a. If nWait is active low, the read cycle (nWrite inactive high, nDStrb/nAStrb active low) or write cycle (nWrite active low, nDStrb/nAStrb active low) starts, proceeds normally, and is completed when nWait goes inactive high.

b. If nWait is inactive high, the read/write cycle cannot start. It must wait until nWait changes to active low, at which time it starts as described above.

13.2.7.2. EPP Version 1.7 Operation

The EPP read/write cycle can start without checking whether nWait is active or inactive. Once the read/write cycle starts; however, it does not finish until nWait changes from active low to inactive high.

13.3 Extended Capabilities Parallel (ECP) Port

This port is software- and hardware-compatible with existing parallel ports, so the W83627DHG-P parallel port may be used in standard printer mode if ECP is not required. It provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward (host-to-peripheral) and reverse (peripheral-to-host) directions.

Small FIFOs are used in both forward and reverse directions to improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes. The ECP port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The ECP port hardware supports run-length-encoded (RLE) decompression. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. RLE compression is required; the hardware support is optional.

For more information about the ECP Protocol, please refer to the Extended Capabilities Port Protocol and ISA Interface Standard.

The W83627DHG-P ECP supports the following modes.

Table 13-4 ECP Mode Description

MODE	DESCRIPTION
000	SPP mode
001	PS/2 Parallel Port mode
010	Parallel Port Data FIFO mode

MODE	DESCRIPTION
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the CRF0h to select ECP/EPP mode)
101	Reserved
110	Test mode
111	Configuration mode

The mode selection bits are bits 7-5 of the Extended Control Register.

13.3.1 ECP Register and Bit Map

The next two tables list the registers used in the ECP mode and provide a bit map of the parallel port and ECP registers.

Table 13-5 ECP Register Addresses

NAME	ADDRESS	I/O	ECP MODES	FUNCTION
data	Base+000h	R/W	000-001	Data Register
ecpAFifo	Base+000h	R/W	011	ECP FIFO (Address)
dsr	Base+001h	R	All	Status Register
dcr	Base+002h	R/W	All	Control Register
cFifo	Base+400h	R/W	010	Parallel Port Data FIFO
ecpDFifo	Base+400h	R/W	011	ECP FIFO (DATA)
tFifo	Base+400h	R/W	110	Test FIFO
cnfgA	Base+400h	R	111	Configuration Register A
cnfgB	Base+401h	R/W	111	Configuration Register B
ecr	Base+402h	R/W	All	Extended Control Register

Note: The base addresses are specified by CR60 and 61, which are determined by the configuration register or the hardware setting.

Table 13-6 Bit Map of the ECP Registers

	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/RLE	Address or RLE field							2
Dsr	nBusy	nAck	PError	Select	nFault	1	1	1	1
Dcr	1	1	Directio	ackIntEn	SelectIn	nInit	Autofd	strobe	1
cFifo	Parallel Port Data FIFO								2
ecpDFifo	ECP Data FIFO								2
tFifo	Test FIFO								2
cnfgA	0	0	0	1	0	0	0	0	
cnfgB	compress	intrValue	1	1	1	1	1	1	
Ecr	MODE			nErrIntrEn	dmaEn	serviceIntr	full	empty	

Notes:

1. These registers are available in all modes.
2. All FIFOs use one common 16-byte FIFO.

Each register (or pair of registers, in some cases) is discussed below.

13.3.2 Data and ecpAFifo Port

Modes 000 (SPP) and 001 (PS/2) (Data Port)

During a write operation, the Data Register latches the contents of the data bus on the rising edge of the input, and the contents of this register are output to PD0-PD7. During a read operation, ports PD0-PD7 are read and output to the host. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Mode 011 (ECP FIFO-Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. This operation is defined only for the forward direction. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	ADDRESS/RLE	ADDRESS OR RLE						

13.3.3 Device Status Register (DSR)

These bits are logical 0 during a read of the Printer Status Register. The bits of this status register are defined as follows:

BIT	7	6	5	4	3	2	1	0
NAME	nBUSY	nACK	PERROR	SELECT	nFAULT	1	1	1

BIT	DESCRIPTION
7	**nBUSY.** This bit reflects the complement of the Busy input.
6	**nACK.** This bit reflects the nAck input.
5	**PERROR.** This bit reflects the PError input.
4	**SELECT.** This bit reflects the Select input.
3	**nFAULT.** This bit reflects the nFault input.
2-0	**RESERVED.** These three bits are not implemented and are always logical 1 during a read.

13.3.4 Device Control Register (DCR)

The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		DIRECTOR	ACKINTEN	SELECTIN	NINIT	AUTOFD	STROBE
DEFAULT	1	1	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7-6	**RESERVED.** These two bits are always read as logical 1 and cannot be written.
5	**DIRECTOR.** If the mode is 000 or 010, this bit has no effect and the direction is always out. In other modes, 0: The parallel port is in the output mode. 1: The parallel port is in the input mode.
4	**ACKINEN.** Interrupt Request Enable. When this bit is set to logical 1, it enables interrupt requests from the parallel port to the CPU on the low-to-high transition on ACK#.
3	**SELECTIN.** This bit is inverted and output to the SLIN# output. 0: The printer is not selected. 1: The printer is selected.
2	**NINIT.** This bit is output to the INIT# output.
1	**AUTOFD.** This bit is inverted and output to the AFD# output.
0	**STROBE.** This bit is inverted and output to the STB# output.

13.3.5 CFIFO (Parallel Port Data FIFO) Mode = 010

This mode is defined only for the forward direction. Bytes written or DMAed to this FIFO are transmitted by a hardware handshake to the peripheral using the standard parallel port protocol. Transfers to the FIFO are byte-aligned.

13.3.6 ECPDFIFO (ECP Data FIFO) Mode = 011

When the direction bit is 0, bytes written or DMAed to this FIFO are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte-aligned.

When the direction bit is 1, data bytes from the peripheral are read via automatic hardware handshake from ECP into this FIFO. Reads or DMAs from the FIFO return bytes of ECP data to the system.

13.3.7 TFIFO (Test FIFO Mode) Mode = 110

Data bytes may be read, written, or DMAed to or from the system to this FIFO in any direction. Data in the tFIFO is not transmitted to the parallel port lines. However, data in the tFIFO may be displayed on the parallel port data lines.

13.3.8 CNFGA (Configuration Register A) Mode = 111

This register is a read-only register. When it is read, 10h is returned indicating an 8-bit implementation.

13.3.9 CNFGB (Configuration Register B) Mode = 111

The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	COMPRESS	INTROVALUE	IRQX2	IRQX1	IRQX0	RESERVED		
DEFAULT	0	0	0	0	0	1	1	1

BIT	DESCRIPTION	
7	COMPRESS. This bit is read-only. It is logical 0 during a read, which means that this chip does not support hardware RLE compression.	
6	INTRVALUE. Returns the value on the ISA IRQ line to determine possible conflicts.	
5	IRQX2.	Reflects the IRQ resource assigned for the ECP port.
4	IRQX1.	
3	IRQX0.	
2-0	RESERVED. These bits are logical 1 during a read and can be written.	

cnfgB[5:3]	IRQ Resource
000	Reflects other IRQ resources selected by PnP register (Default)
001	IRQ7
010	IRQ9
011	IRQ10
100	IRQ11
101	IRQ14
110	IRQ15
111	IRQ5

13.3.10 ECR (Extended Control Register) Mode = all

This register controls the extended ECP parallel port functions. The bit definitions are follows:

BIT	7	6	5	4	3	2	1	0
NAME	MODE			nERRINTREN	DMAEN	SERVICE INTR	FULL	EMPTY
DEFAULT	0	0	0	1	0	1	0	1

BIT	DESCRIPTION
7-5	**MODE.** Read/Write. These bits select the mode. **Bits** **7 6 5** 0 0 0: **Standard Parallel Port (SPP) mode.** The FIFO is reset in this mode. 0 0 1: **PS/2 Parallel Port mode.** In addition to the functions of the SPP mode, this mode has an extra trait: Direction is able to tri-state the data lines. Furthermore, reading the data register returns the value on the data lines, not the value in the data register. 0 1 0: **Parallel Port FIFO mode.** This is the same as the SPP mode except that bytes are written or DMAed to the FIFO. FIFO data are automatically transmitted using the standard parallel port protocol. This mode functions only when the direction is 0. 0 1 1: **ECP Parallel Port Mode.** When the direction is 0 (forward direction), bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and automatically transmitted to the peripheral using the ECP Protocol. When the direction is 1 (reverse direction), bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo. 1 0 0: **EPP Mode.** The EPP mode is activated if the EPP mode is selected. 1 0 1: **Reserved.**

BIT	DESCRIPTION
	1 1 0: **Test Mode.** The FIFO may be written and read in this mode, but the data is not transmitted on the parallel port. 1 1 1: **Configuration Mode.** The confgA and confgB registers are accessible at 0x400 and 0x401 in this mode.
4	**nERRINTREN.** Read/Write (Valid only in the ECP mode) 1: Disables the interrupt generated on the asserting edge of nFault. 0: Enables the interrupt generated on the falling edge of nFault. This prevents interrupts from being lost in the time between the read and the write of the ECR.
3	**DMAEN.** Read/Write. 1: Enables DMA. 0: Disables DMA unconditionally.
2	**SERVICE INTR.** Read/Write. 1: Disables DMA and all of the service interrupts. Writing a logical 1 to this bit does not cause an interrupt. 0: Enables one of the following cases of interrupts. When one of the serviced interrupts occurs, this bit is set to logical 1 by the hardware. This bit must be reset to logical 0 to re-enable the interrupts. (a) dmaEn = 1: During DMA, this bit is set to logical 1 when terminal count is reached. (b) dmaEn = 0, direction = 0: This bit is set to logical 1 whenever there are writeIntr threshold or more bytes free in the FIFO. (c) dmaEn = 0, direction = 1: This bit is set to logical 1 whenver there are readIntr threshold or more valid bytes to be read from the FIFO.
1	**FULL.** Read only. 1: The FIFO is completely full. It cannot accept another byte. 0: The FIFO has at least one free byte.
0	**EMPTY.** Read only. 1: The FIFO is completely empty. 0: The FIFO contains at least one byte of data.

13.3.11ECP Pin Descriptions

NAME	TYPE	DESCRIPTION
NStrobe (HostClk)	O	This pin loads data or address into the slave on its asserting edge during write operations. This signal handshakes with Busy.
PD<7:0>	I/O	These signals contain address, data or RLE data.
nAck (PeriphClk)	I	This signal indicates valid data driven by the peripheral when asserted. This signal handshakes with nAutoFd in reverse.
Busy (PeriphAck)	I	This signal deasserts to indicate that the peripheral can accept data. In the reverse direction, it indicates whether the data lines contain ECP command information or data. Normal data are transferred when Busy (PeriphAck) is high, and an 8-bit command is transferred when it is low.
PError (nAckReverse)	I	This signal is used to acknowledge a change in the direction of the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus.

NAME	TYPE	DESCRIPTION
Select (Xflag)	I	Indicates printer on-line.
NautoFd (HostAck)	O	Requests a byte of data from the peripheral when it is asserted. In the forward direction, this signal indicates whether the data lines contain ECP address or data. Normal data are transferred when nAutoFd (HostAck) is high, and an 8-bit command is transferred when it is low.
nFault (nPeriphReuqest)	I	Generates an error interrupt when it is asserted. This signal is valid only in the forward direction. The peripheral is permitted (but not required) to drive this pin low to request a reverse transfer during ECP mode.
nInit (nReverseRequest)	O	This signal sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction.
nSelectIn (ECPMode)	O	This signal is always deasserted in ECP mode.

13.3.12 ECP Operation

The host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol before ECP operation. After negotiation, it is necessary to initialize some of the port bits.

(a) Set direction = 0, enabling the drivers.

(b) Set strobe = 0, causing the nStrobe signal to default to the deasserted state.

(c) Set autoFd = 0, causing the nAutoFd signal to default to the deasserted state.

(d) Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo, respectively.

13.3.12.1. Mode Switching

The software must handle P1284 negotiation and all operations prior to a data transfer in SPP or PS/2 modes (000 or 001). The hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port, only in the data transfer phase (mode 011 or 010).

If the port is in mode 000 or 001, it may switch to any other mode. If the port is not in mode 000 or 001, it can only be switched into mode 000 or 001. The direction can only be changed in mode 001.

In extended forward mode, the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In ECP reverse mode, the software should wait for all the data to be read from the FIFO before changing back to mode 000 or 001.

13.3.12.2. Command/Data

ECP mode allows the transfer of normal 8-bit data or 8-bit commands. In the forward direction, normal data are transferred when HostAck is high, and an 8-bit command is transferred when HostAck is low. The most significant bits of the command indicate whether it is a run-length count (for compression) or a channel address.

In the reverse direction, normal data are transferred when PeriphAck is high, and an 8-bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero.

13.3.12.3. Data Compression

The W83627DHG-P hardware supports RLE decompression and can transfer compressed data to a peripheral. Odd (RLE) compression is not supported in the hardware, however. In order to transfer data in ECP mode, the compression count is written to ecpAFifo and the data byte is written to ecpDFifo.

13.3.13 FIFO Operation

The FIFO threshold is set in LD0 CRO0, bit 6 ~ 3. All data transferred to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode, as indicated by the selected mode. The FIFO is used in Parallel Port FIFO mode or ECP Parallel Port Mode. After a reset, the FIFO is disabled.

13.3.14DMA Transfers

DMA transfers are always to or from the ecpDFifo, tFifo, or CFifo. DMA uses the standard PC DMA services. The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA empties or fills the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated, and serviceIntr is asserted, which will disable the DMA.

13.3.15 Programmed I/O (NON-DMA) Mode

The ECP and parallel port FIFOs can also be operated using interrupt-driven, programmed I/O. Programmed I/O transfers are

1. To the ecpDFifo at 400h and ecpAFifo at 000h
2. From the ecpDFifo located at 400h
3. To / from the tFifo at 400h.

The host must set dmaEn and serviceIntr to 0 and also must set the direction and state accordingly in the programmed I/O transfers.

The ECP requests programmed I/O transfers from the host by activating the IRQ pin. The programmed I/O empties or fills the FIFO using the appropriate direction and mode.

14. KEYBOARD CONTROLLER

The W83627DHG-P KBC (8042 with licensed KB BIOS) circuit is designed to provide the functions needed to interface a CPU with a keyboard and/or a PS/2 mouse and can be used with IBM®-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. Then, the controller asserts an interrupt to the system when data are placed in its output buffer. The keyboard and PS/2 mouse are required to acknowledge all data transmissions. No transmission should be sent to the keyboard or PS/2 mouse until an acknowledgement is received for the previous data byte.

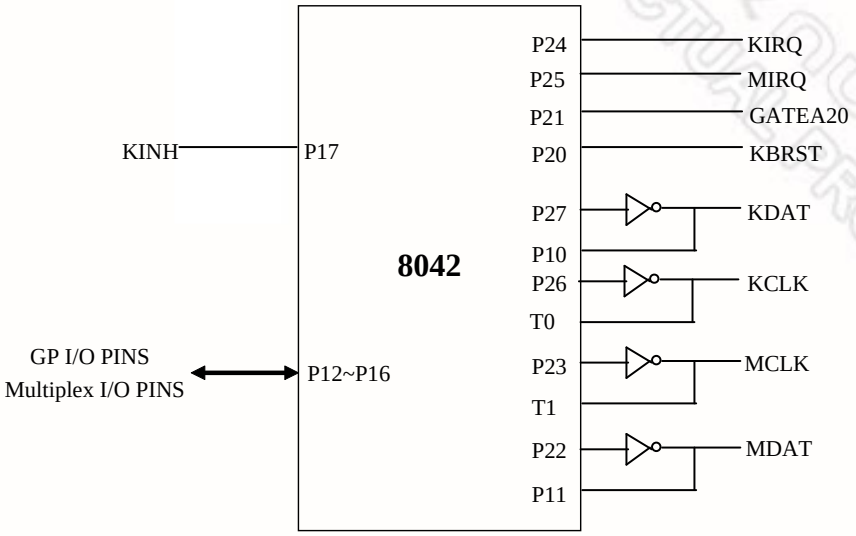


Figure 14-1 Keyboard and Mouse Interface

14.1 Output Buffer

The output buffer is an 8-bit, read-only register at I/O address 60h (Default, PnP programmable I/O address LD5-CR60 and LD5-CR61). The keyboard controller uses the output buffer to send the scan code (from the keyboard) and required command bytes to the system. The output buffer can only be read when the output buffer full bit in the register (in the status register) is logical 1.

14.2 Input Buffer

The input buffer is an 8-bit, write-only register at I/O address 60h or 64h (Default, PnP programmable I/O address LD5-CR60, LD5-CR61, LD5-CR62, and LD5-CR63). Writing to address 60h sets a flag to indicate a data write; writing to address 64h sets a flag to indicate a command write. Data written to I/O address 60h is sent to the keyboard (unless the keyboard controller is expecting a data byte) through the controller's input buffer only if the input buffer full bit (in the status register) is logical 0.

14.3 Status Register

The status register is an 8-bit, read-only register at I/O address 64h (Default, PnP programmable I/O address LD5-CR62 and LD5-CR63) that holds information about the status of the keyboard controller and interface. It may be read at any time.

Table 14-1 Bit Map of Status Register

BIT	BIT FUNCTION	DESCRIPTION
0	Output Buffer Full	0: Output buffer empty 1: Output buffer full
1	Input Buffer Full	0: Input buffer empty 1: Input buffer full
2	System Flag	This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller. It defaults to 0 after a power-on reset.
3	Command/Data	0: Data byte 1: Command byte
4	Inhibit Switch	0: Keyboard is inhibited 1: Keyboard is not inhibited
5	Auxiliary Device Output Buffer	0: Auxiliary device output buffer empty 1: Auxiliary device output buffer full
6	General Purpose Time-out	0: No time-out error 1: Time-out error
7	Parity Error	0: Odd parity 1: Even parity (error)

14.4 Commands

Table 14-2 KBC Command Sets

COMMAND	FUNCTION
20h	Read Command Byte of Keyboard Controller
60h	Write Command Byte of Keyboard Controller

BIT	BIT DEFINITION
7	Reserved
6	IBM Keyboard Translate Mode
5	Disable Auxiliary Device
4	Disable Keyboard
3	Reserve
2	System Flag
1	Enable Auxiliary Interrupt
0	Enable Keyboard Interrupt

<table>
<tr><th>COMMAND</th><th>FUNCTION</th></tr>
<tr><td>A4h</td><td>Test Password
Returns 0Fah if Password is loaded
Returns 0F1h if Password is not loaded</td></tr>
<tr><td>A5h</td><td>Load Password
Load Password until a logical 0 is received from the system</td></tr>
<tr><td>A6h</td><td>Enable Password
Enable the checking of keystrokes for a match with the password</td></tr>
<tr><td>A7h</td><td>Disable Auxiliary Device Interface</td></tr>
<tr><td>A8h</td><td>Enable Auxiliary Device Interface</td></tr>
<tr><td>A9h</td><td>Interface Test
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>00</td><td>No Error Detected</td></tr>
<tr><td>01</td><td>Auxiliary Device "Clock" line is stuck low</td></tr>
<tr><td>02</td><td>Auxiliary Device "Clock" line is stuck high</td></tr>
<tr><td>03</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
<tr><td>04</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
</table></td></tr>
<tr><td>AAh</td><td>Self-test
Returns 055h if self-test succeeds</td></tr>
<tr><td>ABh</td><td>Interface Test
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>00</td><td>No Error Detected</td></tr>
<tr><td>01</td><td>Keyboard "Clock" line is stuck low</td></tr>
<tr><td>02</td><td>Keyboard "Clock" line is stuck high</td></tr>
<tr><td>03</td><td>Keyboard "Data" line is stuck low</td></tr>
<tr><td>04</td><td>Keyboard "Data" line is stuck high</td></tr>
</table></td></tr>
<tr><td>ADh</td><td>Disable Keyboard Interface</td></tr>
<tr><td>AEh</td><td>Enable Keyboard Interface</td></tr>
<tr><td>C0h</td><td>Read Input Port (P1) and send data to the system</td></tr>
<tr><td>C1h</td><td>Continuously puts the lower four bits of Port1 into the STATUS register</td></tr>
<tr><td>C2h</td><td>Continuously puts the upper four bits of Port1 into the STATUS register</td></tr>
<tr><td>D0h</td><td>Send Port 2 value to the system</td></tr>
<tr><td>D1h</td><td>Only set / reset GateA20 line based on system data bit 1</td></tr>
<tr><td>D2h</td><td>Send data back to the system as if it came from the Keyboard</td></tr>
<tr><td>D3h</td><td>Send data back to the system as if it came from Auxiliary Device</td></tr>
<tr><td>D4h</td><td>Output next received byte of data from system to Auxiliary Device</td></tr>
<tr><td>E0h</td><td>Reports the status of the test inputs</td></tr>
<tr><td>FXh</td><td>Pulse only RC (the reset line) low for 6µs if the Command byte is even</td></tr>
</table>

14.5 Hardware GATEA20/Keyboard Reset Control Logic

The KBC includes hardware control logic to speed-up GATEA20 and KBRESET. This control logic is controlled by LD5-CRF0 as follows:

14.5.1 KB Control Register

BIT	7	6	5	4	3	2	1	0
NAME	KCLKS1	KCLKS0	Reserved			P92EN	HGA20	HKBRST#
DEFAULT	1	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7	**KCLKS1**	These two bits select the KBC clock rate. **Bits** **7 6** 0 0: Reserved. 0 1: Reserved. 1 0: KBC clock input is 12 MHz. 1 1: Reserved.
6	**KCLKS0**	
5-3	**RESERVED.**	
2	**P92EN. Port 92 Enable.** 1: Enable Port 92 to control GATEA20 and KBRESET. 0: Disable Port 92 functions.	
1	**HGA20. Hardware GATEA20.** 1: Selects hardware GATEA20 control logic to control GATE A20 signal. 0: Disable hardware GATEA20 control logic function.	
0	**HKBRST#. Hardware Keyboard Reset.** 1: Select hardware KB RESET control logic to control KBRESET signal. 0: Disable hardware KB RESET control logic function.	

When the KBC receives data that follows a "D1" command, the hardware control logic sets or clears GATEA20 according to received data bit 1. Similarly, the hardware control logic sets or clears KBRESET depending on received data bit 0. When the KBC receives an "FE" command, the KBRESET is pulse low for 6μs (Min.) with a 14μs (Min.) delay.

GATEA20 and KBRESET are controlled by either software or hardware logic, and they are mutually exclusive. Then, GATEA20 and KBRESET are merged with Port92 when the P92EN bit is set.

14.5.2 Port 92 Control Register

BIT	7	6	5	4	3	2	1	0
NAME	Res. (0)		Res. (1)	Res. (0)		Res. (1)	SGA20	PLKBRST#
DEFAULT	0	0	1	0	0	1	0	0

SGA20 (Special GATE A20 Control)

1: Drives GATE A20 signal to high.

0: Drives GATE A20 signal to low.

PLKBRST# (Pull-Low KBRESET)

A logical 1 on this bit causes KBRESET to drive low for 6 μS (Min.) with a 14 μS (Min.) delay. Before issuing another keyboard-reset command, the bit must be cleared.

BIT	DESCRIPTION
7-6	**Res. (0)**
5	**Res. (1)**
4-3	**Res. (0)**
2	**Res. (1)**
1	**SGA20. Special GATE A20 Control.** 1: Drives GATE A20 signal to high. 0: Drives GATE A20 signal to low.
0	**PLKBRST#. Pull-Low KBRESET.** A logical 1 on this bit causes KBRESET to drive low for 6 μS (Min.) with a 14 μS (Min.) delay. Before issuing another keyboard-reset command, the bit must e cleared.

15. POWER MANAGEMENT EVENT

The PME# (pin 86) signal is connected to the South Bridge and is used to wake up the system from S1 ~ S5 sleeping states.

One control bit and four registers in the W83627DHG-P are associated with the PME function. The control bit is at Logical Device A, CR [F2h], bit [0] and is for enabling or disabling the PME function. If this bit is set to "0", the W83627DHG-P won't output any PME signal when any of the wake-up events has occurred and is enabled. The four registers are divided into PME status registers and PME interrupt registers of wake-up events [Note.1].

1) The PME status registers of wake-up event:
   - At Logical Device A, CR [F3h] and CR [F4h]
   - Each wake-up event has its own status
   - The PME status should be cleared by writing a "1" before enabling its corresponding bit in the PME interrupt registers
2) The PME interrupt registers of wake-up event:
   - At Logical Device A, CR [F6h] and CR [F7h]
   - Each wake-up event can be enabled / disabled individually to generate a PME# signal

Note.1 PME wake-up events that the W83627DHG-P supports include:

- Mouse IRQ event *
- Keyboard IRQ event *
- GP30, GP31, and GP35 events *
- Printer IRQ event
- Floppy IRQ event
- UART A IRQ event
- UART B IRQ event
- Hardware Monitor IRQ event
- WDTO# event
- RIB (UARTB Ring Indicator) event

Note.2 All the above support both S0 and S1 states. Events with the "*" mark also support S3 and S5 states.

15.1 Power Control Logic

This chapter describes how the W83627DHG-P implements its ACPI function via these power control pins: PSIN# (Pin 68), PSOUT# (Pin 67), SUSB# (i.e. SLP_S3#; Pin 73) and PSON# (Pin 72). The following figure illustrates the relationships.

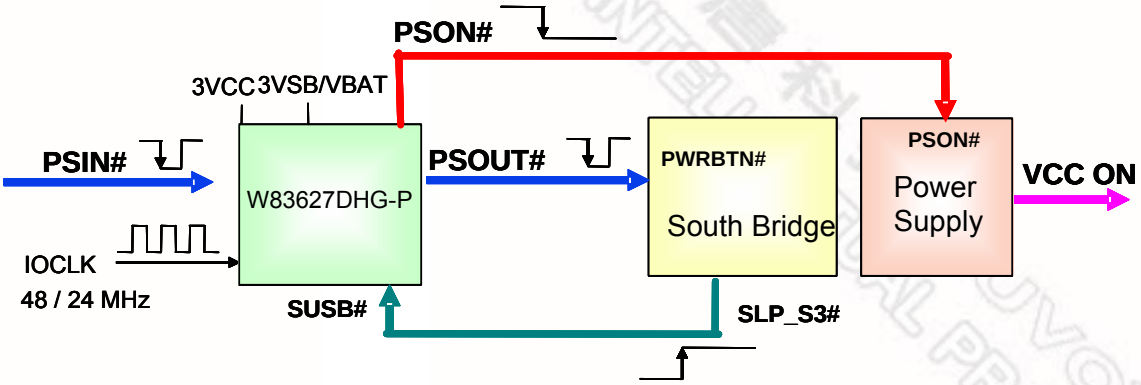


Figure 15-1 Power Control Mechanism

15.1.1 PSON# Logic

15.1.1.1. Normal Operation

The PSOUT# signal will be asserted low if the PSIN# signal is asserted low. The PSOUT# signal is held low for as long as the PSIN# is held low. The South Bridge controls the SUSB# signal through the PSOUT# signal. The PSON# is directly connected to the power supply to turn on or off the power.

Figure 15.2 shows the power on and off sequences.

The ACPI state changes from S5 to S0, then to S5

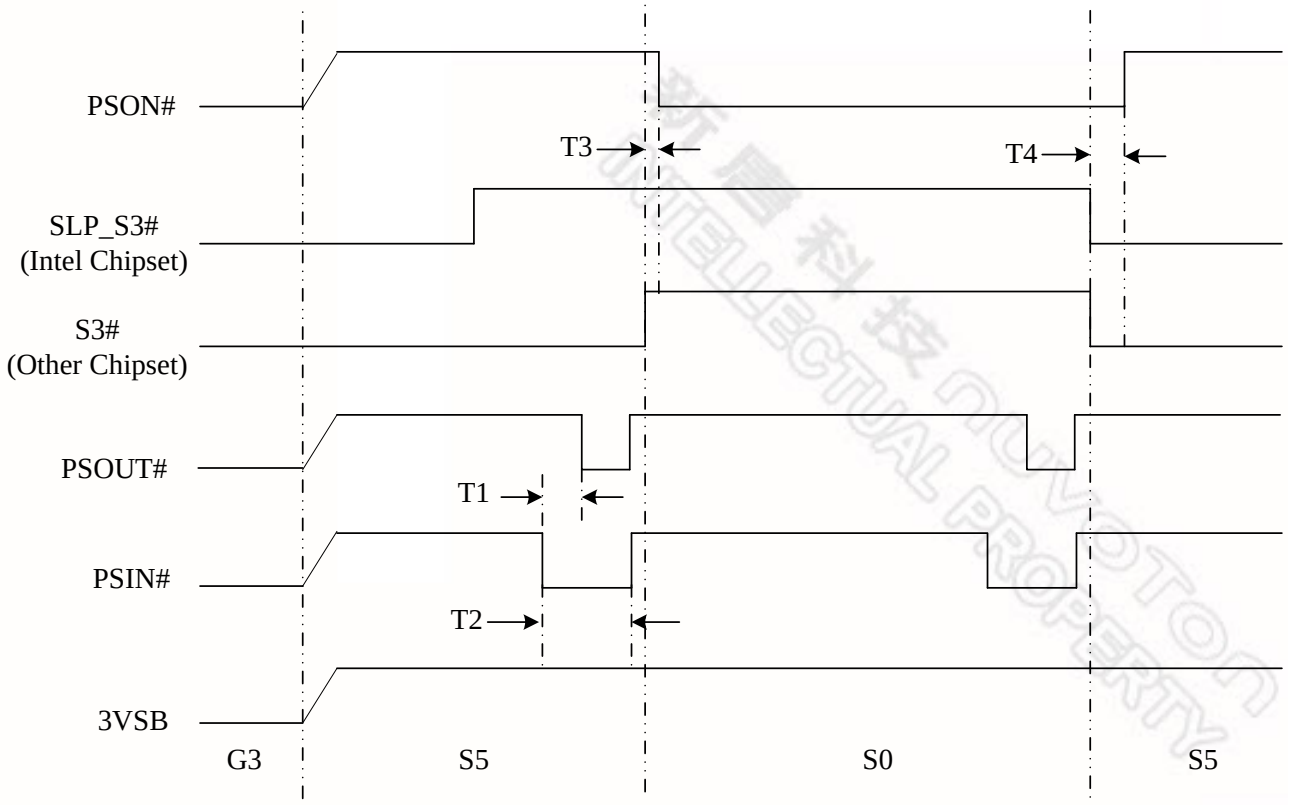


Figure 15-2 Power Sequence from S5 to S0, then Back to S5

15.1.2 AC Power Failure Resume

By definition, AC power failure means that the standby power is removed. The power failure resume control logic of the W83627DHG-P is used to recover the system to a pre-defined state after AC power failure. Two control bits at Logical Device A, CR [E4h], bits [6:5] indicate the pre-defined state. The definition of these two bits is listed in the following table:

Table 15-1 Bit Map of Logical Device A, CR [E4h], Bits [6:5]

LOGICAL DEVICE A, CR[E4H], BITS[6:5]	DEFINITION
00	System always turns off when it returns from AC power failure
01	System always turns on when it returns from AC power failure
10	System turns off / on when it returns from power failure depending on the state before the power failure. (Please see Note 1)
11	User defines the state before the power failure. (The previous state is set at CRE6 [4]. Please see Note 2)

Note1. The W83627DHG-P detects the state before power failure (on or off) through the SUSB# signal and the 3VCC power. The relation is illustrated in the following two figures.

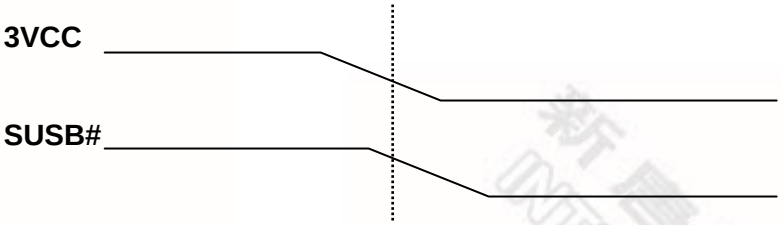


Figure 15-3 The previous state is “on” - 3VCC falls to 2.6V and SUSB# keeps at 2.0V

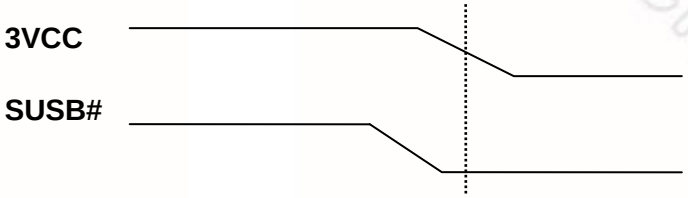


Figure 15-4 The previous state is “off” - 3VCC falls to 2.6V and SUSB# keeps at 0.8V

Note 2.

Logical Device A, CR[E6h] bit [4]	Definition
0	User defines the state to be “on”
1	User defines the state to be “off”

To ensure that VCC does not fall faster than VSB in various ATX Power Supplies, the W83627DHG-P adds the option of “user define mode” for the pre-defined state before AC power failure. BIOS can set the pre-defined state to be “On” or “Off”. According to this setting, the system is returned to the pre-defined state after the AC power recovery.

15.2 Wake Up the System by Keyboard and Mouse

The W83627DHG-P generates a low pulse through the PSOUT# pin to wake up the system when it detects a key code pressed or mouse button clicked. The following sections describe how the W83627DHG-P works.

15.2.1 Waken up by Keyboard events

The keyboard Wake-Up function is enabled by setting Logical Device A, CR [E0h], bit 6 to “1”.

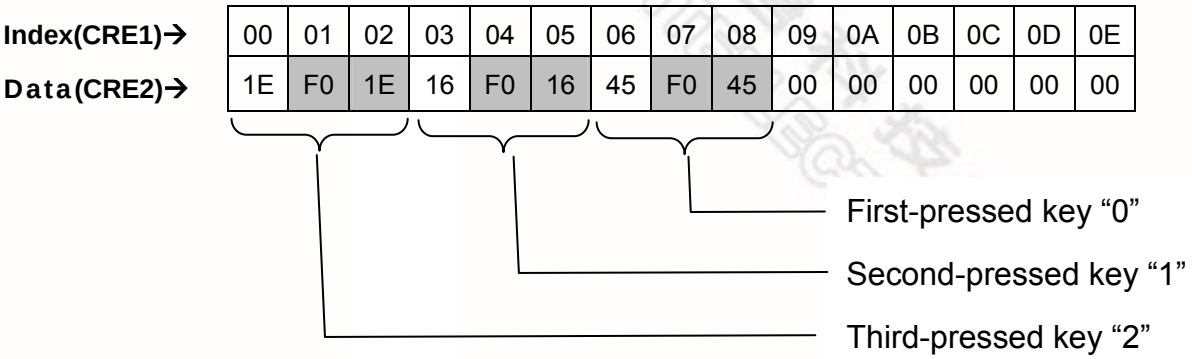
There are two keyboard events can be used for the wake-up

1) Any key – Set bit 0 at Logical Device A, CR [E0h] to “1” (Default).
2) Specific keys (Password) - Set bit 0 at Logical Device A, CR [E0h] to “0”.

Three sets of specific key combinations are stored at Logical Device A. CR [E1h] is an index register to indicate which byte of key code storage (0x00h ~ 0x0Eh, 0x30h ~ 0x3Eh, 0x40h ~ 0x4Eh) is going to be read or written through CR [E2h]. According to IBM 101/102 keyboard specification, a complete

key code contains a 1-byte make code and a 2-byte break code. For example, the make code of "0" is 0x45h, and the corresponding break code is 0xF0h, 0x45h.

The approach to implement Keyboard Password Wake-Up Function is to fill key codes into the password storage. Assume that we want to set "012" as the password. The storage should be filled as below. Please note that index 0x09h ~ 0x0Eh must be filled as 0x00h since the password has only three numbers.



15.2.2 Waken up by Mouse events

The mouse Wake-Up function is enabled by setting Logical Device A, CR [E0h], bit 5 to "1".

The following specific mouse events can be used for the wake-up:

- Any button clicked or any movement
- One click of the left or the right button
- One click of the left button
- One click of the right button
- Two clicks of the left button
- Two clicks of the right button.

Three control bits (ENMDAT_UP, MSRKEY, MSXKEY) define the combinations of the mouse wake-up events. Please see the following table for the details.

Table 15-2 Definitions of Mouse Wake-Up Events

ENMDAT_UP (LOGICAL DEVICE A, CR[E6H], BIT 7)	MSRKEY (LOGICAL DEVICE A, CR[E0H], BIT 4)	MSXKEY (LOGICAL DEVICE A, CR[E0H], BIT 1)	WAKE-UP EVENT
1	x	1	Any button clicked or any movement.
1	x	0	One click of the left or right button.
0	0	1	One click of the left button.
0	1	1	One click of the right button.
0	0	0	Two clicks of the left button.
0	1	0	Two clicks of the right button.

15.3 Resume Reset Logic

The RSMRST# (Pin 75) signal is a reset output and is used as the 3VSB power-on reset signal for the South Bridge.

When the W83627DHG-P detects the 3VSB voltage rises to "V1", it then starts a delay – "t1" before the rising edge of RSMRST# asserting. If the 3VSB voltage falls below "V2", the RSMRST# de-asserts immediately.

Timing and voltage parameters are shown in Figure 15-5 Mechanism of Resume Reset Logic and Figure 15-3 The previous state is "on" - 3VCC falls to 2.6V and SUSB# keeps at 2.0V.

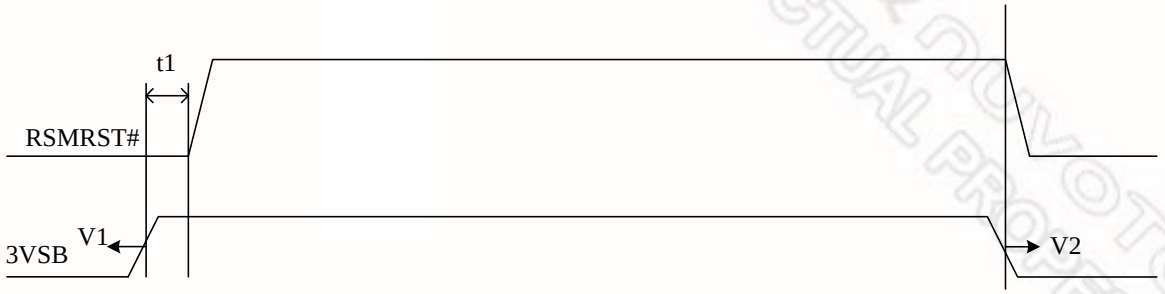


Figure 15-5 Mechanism of Resume Reset Logic

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V1	3VSB Valid Voltage	2.4	2.6	2.75	V
V2	3VSB Ineffective Voltage	2.25	2.4	2.55	V
t1	Valid 3VSB to RSMRST# inactive	100	-	200	mS

Table 15-3 Timing and Voltage Parameters of RSMRST#

15.4 PWROK Generation

The PWROK (Pin 71) signal is an output and is used as the 3VCC power-on reset signal.

When the W83627DHG-P detects the 3VCC voltage rises to "V3", it then starts a delay – "t2" before the rising edge of PWROK asserting. If the 3VCC voltage falls below "V4", the PWROK de-asserts immediately.

Timing and voltage parameters are shown in Figure 15-6 and Table 15-4.

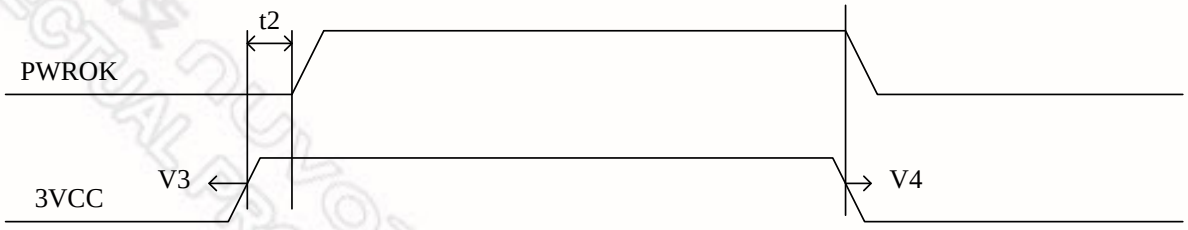


Figure 15-6

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V3	3VCC Valid Voltage	2.4	2.6	2.75	V
V4	3VCC Ineffective Voltage	2.25	2.4	2.55	V
t2	Valid 3VCC to PWROK active	300	-	500	mS

Table 15-4

Originally, the t2 timing is between 300 mS to 500 mS, but it can be changed to 200 mS to 300 mS by programming Logical Device A, CR [E6h], bit 3 to "1". Furthermore, the W83627DHG-P provides four different extra delay time of PWROK for various demands. The four extra delay time are designed at Logical Device A, CR [E6h], bits 2~1. The following table shows the definitions of Logical Device A, CR [E6h] bits 3 ~1.

Table 15-5 Bit Map of Logical Device A, CR [E6h], Bits [3:1]

LOGICAL DEVICE A, CR[E6H] BIT[3:1]	DEFINITION
3	PWROK_DEL (first stage) **(VSB)** Set the delay time when rising from PWROK_LP to PWROK_ST. 0: 300 ~ 500 mS. 1: 200 ~ 300 mS.
2~1	PWROK_DEL **(VSB)** Set the delay time when rising from PWROK_ST to PWROK. 00: No delay time. 01: Delay 32 mS 10: 96 mS 11: Delay 250 mS

For example, if Logical Device A, CR [E6h] bit 3 is set to "0" and bits 2~1 are set to "10", the range of t2 timing is from 396 (300 + 96) mS to 596 (500 + 96) mS.

15.4.1 The Relation among PWROK/PWROK2, ATXPGD and FTPRST#

PWROK and PWROK2 signals as well as ATXPGD and FTPRST# input signals are interrelated.

Once the FTPRST# signal changes from high to low then to high, the PWROK and PWROK2 signals will have the same transition after 28mS ~ 39mS delay. The relation and parameter are illustrated in the following figure and table.

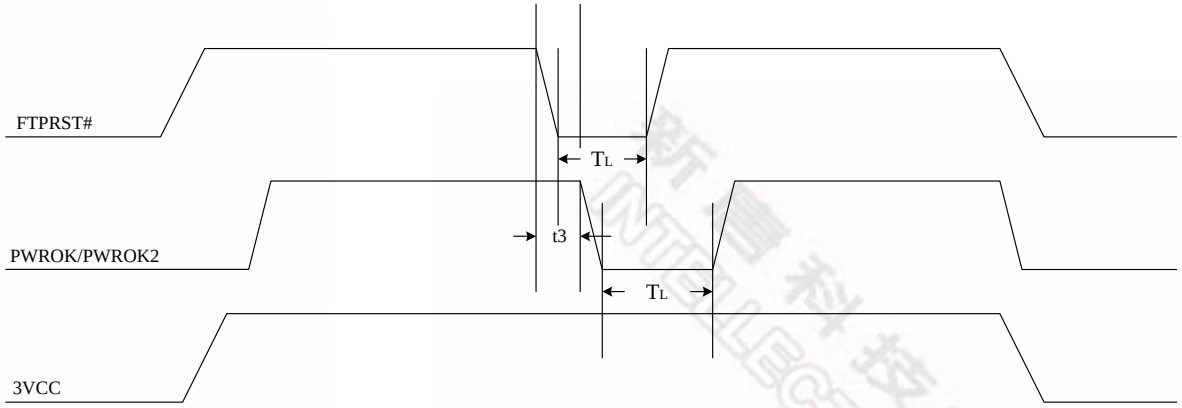


Figure 15-7

Table 15-6

SYMBOL	PARAMETER	MIN	MAX	UNIT
t3	FTPRST# active to PWROK active	28	39	mS

Note. 1. The values above are the worst-case results of R&D simulation

2. The length of T_L level is based on the length of the low level of FTPRST#

Additionally, the ATXPGD signal, too, is used to control the generation of PWROK and PWROK2. In Figure 15-8, the 3VCC voltage rises to "V3", and then starts a delay – "t2" for PWROK and PWROK2 generation. However, ATXPGD is still inactive after t2; therefore the delay time before the rising edge of PWROK and PWROK2 are t2 plus Td. The length of Td is based on when the ATXPGD signal is active. Once 3VCC falls below "V4" or the ATXPGD signal is inactive, PWROK and PWROK2 de-assert immediately.

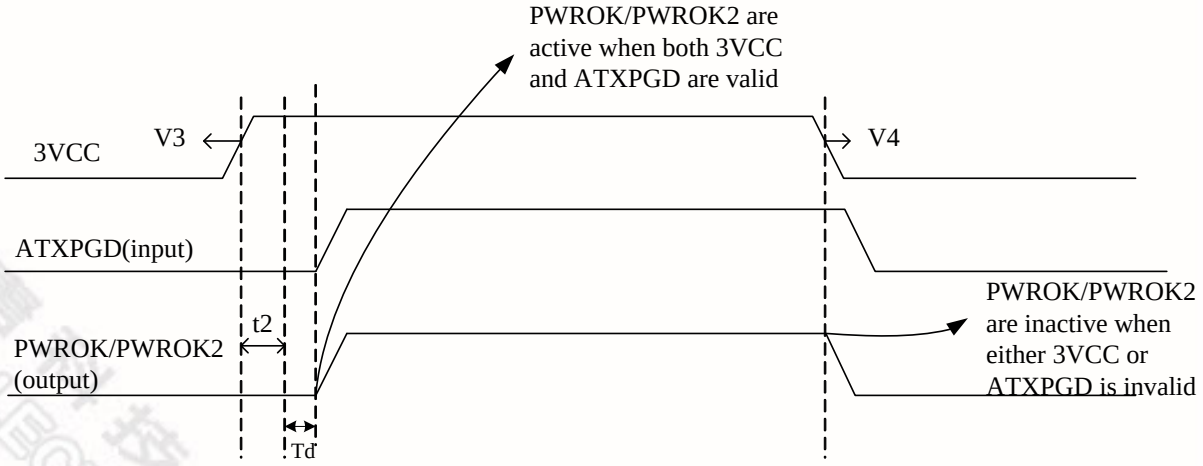


Figure 15-8

In Figure 15-9, the 3VCC voltage rises to "V3", and the ATXPGD is active during t2, so PWROK and PWROK2 assert after t2. The timing of t2 starts when 3VCC voltage rises to "V3". No matter the ATXPGD signal activation is during or after t2, PWROK and PWROK2 assert or de-assert according to the 3VCC voltage and the ATXPGD signal.

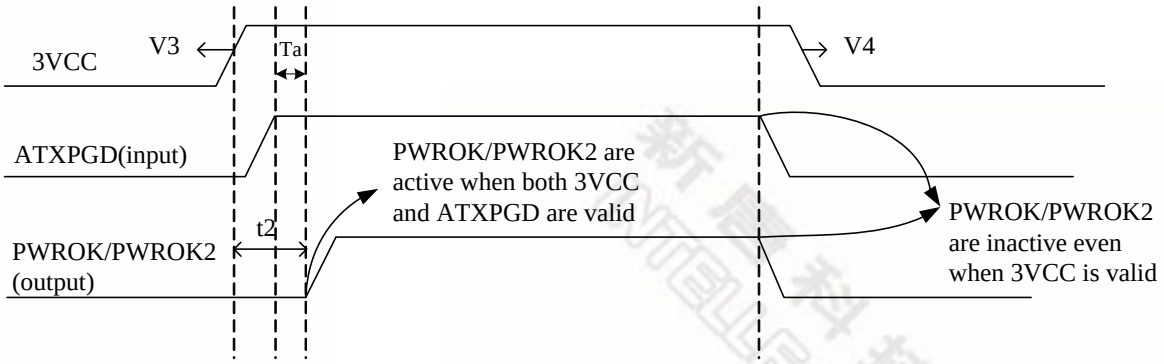


Figure 15-9

Timing and voltage parameters are shown in the following table.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V3	3VCC Valid Voltage	2.4	2.6	2.75	V
V4	3VCC Ineffective Voltage	2.25	2.4	2.55	V
t2	Starting from valid 3VCC	300	-	500	mS

16. SERIALIZED IRQ

The W83627DHG-P supports a serialized IRQ scheme. This allows a signal line to be used to report the parallel interrupt requests. Since more than one device may need to share the signal serial SERIRQ signal, an open drain signal scheme is employed. The clock source is the PCI clock. The serialized interrupt is transferred on the SERIRQ signal, one cycle consisting of three frames types: the Start Frame, the IRQ/Data Frame, and the Stop Frame.

16.1 Start Frame

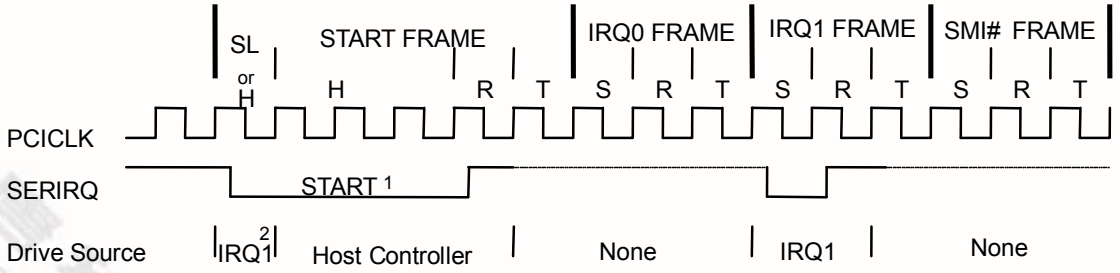
There are two modes of operation for the SERIRQ Start Frame: Quiet mode and Continuous mode.

In the Quiet mode, the W83627DHG-P drives the SERIRQ signal active low for one clock, and then tri-states it. This brings all the state machines of the W83627DHG-P from idle to active states. The host controller (the South Bridge) then takes over driving SERIRQ signal low in the next clock and continues driving the SERIRQ low for programmable 3 to 7 clock periods. This makes the total number of clocks low 4 to 8 clock periods. After these clocks, the host controller drives the SERIRQ high for one clock and then tri-states it.

In the Continuous mode, the START Frame can only be initiated by the host controller to update the information of the IRQ/Data Frame. The host controller drives the SERIRQ signal low for 4 to 8 clock periods. Upon a reset, the SERIRQ signal is defaulted to the Continuous mode for the host controller to initiate the first Start Frame.

Please see the diagram below for more details.

Start Frame Timing with source sampled a low pulse on IRQ1.



H=Host Control SL=Slave Control R=Recovery T=Turn-around S=Sample

Note:

1. The Start Frame pulse can be 4-8 clocks wide.
2. The first clock of Start Frame is driven low by the W83627DHG-P because IRQ1 of the W83627DHG-P needs an interrupt request. Then the host takes over and continues to pull the SERIRQ low.

16.2 IRQ/Data Frame

Once the Start Frame has been initiated, the W83627DHG-P must start counting frames based on the rising edge of the start pulse. Each IRQ/Data Frame has three clocks: the Sample phase, the Recovery phase, and the Turn-around phase.

During the Sample phase, the W83627DHG-P drives SERIRQ low if the corresponding IRQ is active. If the corresponding IRQ is inactive, then SERIRQ must be left tri-stated. During the Recovery phase, the W83627DHG-P device drives the SERIRQ high. During the Turn-around phase, the W83627DHG-P device leaves the SERIRQ tri-stated. The W83627DHG-P starts to drive the SERIRQ line from the beginning of "IRQ0 FRAME" based on the rising edge of PCICLK.

The IRQ/Data Frame has a specific numeral order, as shown in Table 16.1.

Table 16-1 SERIRQ Sampling Periods

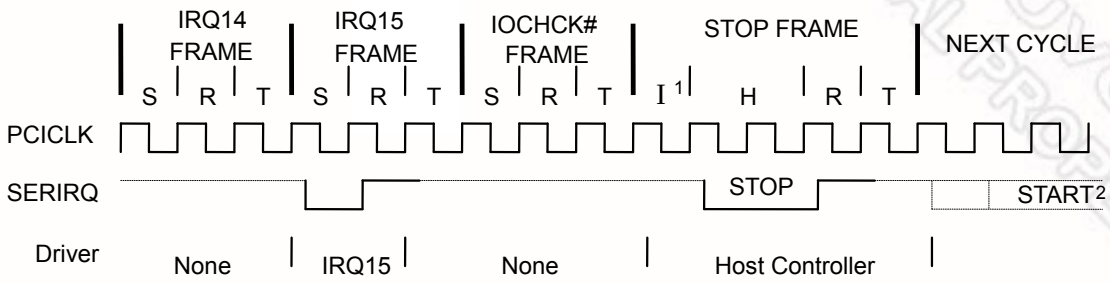
SERIRQ SAMPLING PERIODS			
IRQ/DATA FRAME	**SIGNAL SAMPLED**	**# OF CLOCKS PAST START**	**EMPLOYED BY**
1	IRQ0	2	Reserved
2	IRQ1	5	Keyboard
3	SMI#	8	H/W Monitor & SMI
4	IRQ3	11	UART B
5	IRQ4	14	UART A
6	IRQ5	17	-
7	IRQ6	20	FDC
8	IRQ7	23	LPT
9	IRQ8	26	-
10	IRQ9	29	-
11	IRQ10	32	-
12	IRQ11	35	-
13	IRQ12	38	Mouse
14	IRQ13	41	Reserved
15	IRQ14	44	-
16	IRQ15	47	-
17	IOCHCK#	50	-
18	INTA#	53	-
19	INTB#	56	-
20	INTC#	59	-
21	INTD#	62	-
32:22	Unassigned	95	-

16.3 Stop Frame

After all IRQ/Data Frames have completed, the host controller will terminates SERIRQ with a Stop frame. Only the host controller can initiate the Stop Frame by driving SERIRQ low for 2 or 3 clocks. If the Stop Frame is low for 2 clocks, the Sample mode of next SERIRQ cycle's Sample mode is the Quiet mode. If the Stop Frame is low for 3 clocks, the Sample mode of next SERIRQ cycle is the Continuous mode.

Please see the diagram below for more details.

Stop Frame Timing with Host Using 17 SERIRQ sampling period.



H=Host Control R=Recovery T=Turn-around S=Sample I= Idle.

Note:

1. There may be none, one or more Idle states during the Stop Frame.
2. The Start Frame pulse of next SERIRQ cycle may or may not start immediately after the turn-around clock of the Stop Frame.

17. WATCHDOG TIMER

The WDTO# pin is a multi-function pin with GP50 functions and is configured to the WDTO# function, if Configuration Register CR [2Dh], bit 0 is set to zero.

The Watchdog Timer of the W83627DHG-P consists of an 8-bit programmable time-out counter and a control and status register. The time-out counter ranges from 1 to 255 minutes in the minute mode, or 1 to 255 seconds in the second mode. The units of Watchdog Timer counter are selected at Logical Device 8, CR [F5h], bit [3]. The time-out value is set at Logical Device 8, CR [F6h]. Writing zero disables the Watchdog Timer function. Writing any non-zero value to this register causes the counter to load this value into the Watchdog Timer counter and start counting down.

The W83627DHG-P outputs a low signal to the WDTO# pin (pin 77) when a time-out event occurs. In other words, when the value is counted down to zero, the timer stops, and the W83627DHG-P sets the WDTO# status bit in Logical Device 8, CR [F7h], bit [4], outputting a low signal to the WDTO# pin (pin 77). Writing a zero will clear the status bit and the WDTO# pin returns to high. Writing a zero will clear the status bit. This bit will also be cleared if LRESET# or PWROK# signal is asserted.

Additionally, GP40 (pin 85), GP42 (pin 83), GP44 (pin 81) and GP46 (pin 79) provides an alternative WDTO# function. This function can be configured by the relative GPIO control register.

Please note that the output type of WDTO# (pin 77) and GP42 (pin 83) is push-pull and that of GP40 (pin 85), GP44 (pin 81) and GP46 (pin 79) is open-drain.

18. GENERAL PURPOSE I/O

The W83627DHG-P provides 40 input/output ports that can be individually configured to perform a simple basic I/O function or alternative, pre-defined function. GPIO port 6 is configured through control registers in Logical Device 7, and GPIO ports 2 ~ 5 in Logical Device 9. Users can configure each individual port to be an input or output port by programming respective bit in selection register (0 = output, 1 = input). Invert port value by setting inversion register (0 = non -inverse, 1 = inverse). Port value is read / written through data register.

In addition, only GP30, GP31 and GP35 are designed to be able to assert PSOUT# or PME# signal to wake up the system if any of them has any transitions. There are about 16mS debounced circuit inside these 3 GPIOs and it can be disabled by programming respective bit (LD9, CR [FEh] bit 4~6). Users can set what kind of event type, level or edge, and polarity, rising or falling, to perform the wake-up function. The following table gives a more detailed register map on GP30, GP31 and GP35.

	EVENTROUTE I (PSOUT#) **0: DISABLE** **1: ENABLE**	**EVENTROUTE II (PME#)** **0: DISABLE** **1: ENABLE**	**EVENT DEBOUNCED** **0 : ENABLE** **1 : DISABLE**	**EVENT TYPE** **0 : EDGE** **1: LEVEL**	**EVENT POLARITY** **0 : RISING** **1 : FALLING**	**EVENT STATUS**
GP30	LDA, CR[FEh] bit4	LDA, CR[FEh] bit0	LD9, CR[FEh] bit4	LD9, CR[FEh] bit0	LD9, CR[F2h] bit0	LD9, CR[E7h] bit0
GP31	LDA, CR[FEh] bit5	LDA, CR[FEh] bit1	LD9, CR[FEh] bit5	LD9, CR[FEh] bit1	LD9, CR[F2h] bit1	LD9, CR[E7h] bit1
GP35	LDA, CR[FEh] bit6	LDA, CR[FEh] bit2	LD9, CR[FEh] bit6	LD9, CR[FEh] bit2	LD9, CR[F2h] bit5	LD9, CR[E7h] bit5

19. VID INPUTS AND OUTPUTS

The W83627DHG-P provides eight pins for VID input or output function. The default function is VID input. These pins can be configured to VID output function by setting Logical Device B, CR [F0h], bit 7 to 0. The configuration is applied to the 8 pins as a group. None of them can be individually set to input or output.

19.1 VID Input Detection

The W83627DHG-P supports Intel VRM 9/10/11 and AMD VRM VID detections. H/W strapping and S/W programming can set the following three input levels. a) and b) can be set by H/W strapping or S/W programming, while c) can only be set by S/W programming.

a) TTL (Vih = 2 V; Vil = 0.8V) –

1) Add a pulled-down resistor at Pin 77(EN_GTL), or

2) Set Configuration Register CR [2Ch], bit 3 to “0”;

b) GTL (Vih = 0.6 V; Vil = 0.4 V) – (Default)

1) No extra pulled-up resistor needed, or

2) Set Configuration Register CR [2Ch], bit 3 to “1”;

c) AMD VRM (Vih = 1.4V; Vil = 0.8V) –

Set Configuration Register CR [2Ch], bit 3 to “1” and Logical Device B, CR [F0h], bit 6 to “1”.

The input data can be read in the data register at Logical Device B, CR [F1h], bit 7 ~ 0. It is a read/write register where bit 7~0 corresponds to VID pin 7~0. Please note that in the input mode, writes to this register have no effect.

19.2 VID Output Control

The output type of the eight VID pins is push-pull, and they drive to 3VCC (3.3V) when configured to the output mode. The output data can be set in the data register (Logical Device B, CR [F1h], bit 7 ~ 0). The written data can be read if Configuration Register CR [2Ch], bit 3 is set to “0”.

20. PCI RESET BUFFERS

The W83627DHG-P has five copies of LRESET# output buffers. LRESET# is LPC Interface Reset, to which PCI Reset is connected. The five copies of LRESET# in the W83627DHG-P are designated RSTOUT0#, RSTOUT1#, RSTOUT2#, RSTOUT3# and RSTOUT4#. All of them are powered by a 3VSB power.

RSTOUT0# is an open-drain output buffer of LRESET#. This signal needs an external pulled-up resistor of 3.3V or 5V.

RSTOUT1#, RSTOUT2#, RSTOUT3# and RSTOUT4# are push-pull output buffers of LRESET#. Each of them outputs 3.3V, voltage and the state is low when the 3VSB power is the only power source.

21. CONFIGURATION REGISTER

21.1 Chip (Global) Control Register

CR 02h. (Software Reset; Write Only)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	Write "1" Only	Software RESET.

CR 07h. (Logical Device; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Logical Device Number.

CR 20h. (Chip ID, High Byte; Read Only)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only	Chip ID number = B0h (high byte).

CR 21h. (Chip ID, Low Byte; Read Only)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only	Chip ID number = 7Xh (low byte). X is the IC version

CR 22h. (Device Power Down; Default FFh)

BIT	READ / WRITE	DESCRIPTION	
7	Reserved.		
6	R / W	HM Power Down.	0: Powered down. 1: Not powered down.
5	R / W	UARTB Power Down.	0: Powered down. 1: Not powered down.
4	R / W	UARTA Power Down.	0: Powered down. 1: Not powered down.
3	R / W	PRT Power Down.	0: Powered down. 1: Not powered down.
2~1	Reserved.		
0	R / W	FDC Power Down.	0: Powered down. 1: Not powered down.

CR 23h. (IPD; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	IPD (Immediate Power Down). When set to 1, the whole chip is put into power-down mode immediately.

CR 24h. (Global Option; Default 0100_0ss0b) s: value by strapping

BIT	READ / WRITE	DESCRIPTION
7	R / W	Select output type of CPUFANOUT1 =0 CPUFANOUT1 is Push-pull. (Default) =1 CPUFANOUT1 is Open-drain.
6	R / W	CLKSEL => Input clock rate selection = 0 The clock input on pin 18 is 24 MHz. = 1 The clock input on pin 18 is 48 MHz. (Default)
5	R / W	Select output type of AUXFANOUT =0 AUXFANOUT is Push-pull. (Default) =1 AUXFANOUT is Open-drain.
4	R / W	Select output type of SYSFANOUT =0 SYSFANOUT is Open-drain. (Default) =1 SYSFANOUT is Push-pull.
3	R / W	Select output type of CPUFANOUT0 =0 CPUFANOUT0 is Open-drain. (Default) =1 CPUFANOUT0 is Push-pull.
2	Read Only	ENKBC => Enable keyboard controller = 0 KBC is disabled after hardware reset. = 1 KBC is enabled after hardware reset. This bit is read-only, and it is set or reset by a power-on strapping pin (Pin 54, SOUTA).
1	R / W	ENROM => Enable Serial Peripheral Interface = 0 ROM is disabled after hardware reset. = 1 ROM is enabled after hardware reset. This bit is set or reset by a power-on strapping pin (Pin 52, DTRA#). **Note 1**
0	Reserved.	

Note1:

Disable Serial Peripheral Interface	Enable Serial Peripheral Interface
Pin 2 → GP23	**Pin 2 → SCK**
Pin 19 → GP22	**Pin 19 → SCE**
Pin 58 → AUXFANIN1	**Pin 58 → SI**
Pin 118→BEEP	**Pin 118→SO**

CR 25h. (Interface Tri-state Enable; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~6	Reserved.	
5	R / W	UARTBTRI
4	R / W	UARTATRI
3	R / W	PRTTRI

BIT	READ / WRITE	DESCRIPTION
2~1	Reserved.	
0	R / W	FDCTRI.

CR 26h. (Global Option; Default 0s000000b) s: value by strapping

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	HEFRAS => = 0 Write 87h to location 2E twice. = 1 Write 87h to location 4E twice. The corresponding power-on strapping pin is RTSA# (Pin 51).
5	R / W	LOCKREG => = 0 Enable R/W configuration registers. = 1 Disable R/W configuration registers.
4	Reserved.	
3	R / W	DSFDLGRQ => = 0 Enable FDC legacy mode for IRQ and DRQ selection. Then DO register (base address + 2) bit 3 is effective when selecting IRQ. = 1 Disable FDC legacy mode for IRQ and DRQ selection. Then DO register (base address + 2) bit 3 is not effective when selecting IRQ.
2	R / W	DSPRLGRQ => = 0 Enable PRT legacy mode for IRQ and DRQ selection. Then DCR register (base address + 2) bit 4 is effective when selecting IRQ. = 1 Disable PRT legacy mode for IRQ and DRQ selection. Then DCR register (base address + 2) bit 4 is not effective when selecting IRQ.
1	R / W	DSUALGRQ => = 0 Enable UART A legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable UART A legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.
0	R / W	DSUBLGRQ => = 0 Enable UART B legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable UART B legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.

CR 27h. (Reserved)

CR 28h. (Global Option; Default 50h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	

BIT	READ / WRITE	DESCRIPTION
6~5	R / W	Flash ROM size select = 00 1M = 01 2M = 10 4M (Default) = 11 8M
4	R / W	Select to enable/disable decoding of BIOS ROM range 000E xxxxh. = 0 Enable decoding of BIOS ROM range at 000E xxxxh. = 1 Disable decoding of BIOS ROM range at 000E xxxxh.
3	R / W	Select to enable/disable decoding of BIOS ROM range FFE xxxxx. = 0 Enable decoding of BIOS ROM range at FFE xxxxx. = 1 Disable decoding of BIOS ROM range at FFE xxxxx.
2~0	R / W	PRTMODS2 ~ 0 => = 0xx Parallel Port Mode. = 100 Reserved. = 101 External FDC Mode = 110 Reserved = 111 External two FDC Mode

CR 29h. (Multi-function Pin Selection; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	Pin 5 function select = 0 OVT# = 1 SMI#
5~4	Reserved.	
3	R / W	Pins 49 ~ 54, 56 ~ 57 function select = 0 Pins 49 ~ 54, 56 ~ 57 → UART A = 1 Pins 49 ~ 54, 56 ~ 57 → GPIO6
2~1	R / W	Pin 119 ~ 120 function select
0	Reserved.	

Bit-2	Bit-1	Pin 119 ~ 120 function
0	0	Pin 119 ~ 120 → CPUFANIN1, CPUFANOUT1 (Default)
0	1	Pin 119 ~ 120 → GP21, GP20

CR 2Ah. (SPI Configuration; Default 00h) **(VSB Power)**

BIT	READ / WRITE	DESCRIPTION
7~6	R / W	Serial Peripheral Interface Configuration bit. **(VSB)** = 00 Normal read. SPI clock is 16MHz. = 01 Normal read. SPI clock is 33MHz. = 10 Normal read. SPI clock is 22MHz. = 11 Reserved. ***Note: These two bits are ignored when CR24, bit 1 is "0" (SPI function is disabled).***
5~4	R / W	Serial Peripheral Interface configuration bit.**(VBAT)** = 00 Normal read. The clock rate is based on the setting of CR [2Ah], bits [7:6] = 01 Reserved = 10 Reserved = 11 Fast read with one dummy byte. The clock rate is 33MHz. If set to "11", CR [2Ah], bits [7:6] must be 0. ***Note: These two bits are ignored when CR24, bit 1 is "0". (SPI function is disabled)***
3	R/W	SDA_filter_EN: 0: Enable SDA input to a filter 1: Disable SDA input to a filter
2	R / W	SCL_filter_EN: 0: Enable SCL input to a filter 1: Disable SCL input to a filter
1	R / W	Pin 89, Pin 90 function select (I^2C interface) = 0 {Pin 89, Pin 90} → set by CR2C bits [6:5]. = 1 {Pin 89, Pin 90} → SDA, SCL.
0	R / W	KB, MS pin function select = 0 KB, MS function. = 1 GPIO function. (GP24, GP25, GP26 and GP27)

* Normal Read: Read 1-byte data.
  Fast Read: Read 4-byte data.

CR 2Bh. (Reserved)

CR 2Ch. (Multi-function Pin Selection; Default E2h) **(VSB Power)**

BIT	READ / WRITE	DESCRIPTION
7	R / W	Pin 88 Select = 0 GP34 = 1 RSTOUT4# (Default)
6	R / W	Pin 89 Select = 0 GP33 = 1 RSTOUT3# (Default) ***Note: This bit is ignored when CR2A, bit 1 is High.***

BIT	READ / WRITE	DESCRIPTION
5	R / W	Pin 90 Select = 0 GP32 = 1 RSTOUT2# (Default) ***Note: This bit is ignored when CR2A, bit 1 is High.***
4	Read Only	EN_ACPI status bit = 0 Particular ACPI functions are disabled. = 1 Particular ACPI functions are enabled. The bit is strapped by Pin 70 (GP55). While particular ACPI functions are enabled (EN_ACPI = 1), GPIO3 pins (pins 64, 69, 87, 91 and 92) are disabled and the particular ACPI functions are activated (SUSC#, FTPRST#, ATXPGD, VSBGATE# and PWROK2)
3	R / W	EN_GTL Configure bit = 0 VID input voltage is TTL. = 1 VID input voltage is GTL. The bit is strapped by Pin 77 (GP50).--- Internal Pull high to 3VSB.
2	R / W	EN_PWRDN. **(VBAT)** = 0 Thermal shutdown function is disabled. = 1 Enable thermal shutdown function.
1~0	R / W	Pins 78 ~ 85 function select

Bit-1	Bit-0	Pins 78 ~ 85 function
0	0	Pin 82 → Reserved (tri-state) Pin 83 → Reserved (always low) Others → GPIO4
0	1	Pin 82 → IRRX Pin 83 → IRTX Others → GPIO4
1	0	Pins 78 ~ 85 → GPIO4
1	1	Pins 78 ~ 85 → UART B

CR 2Dh. (Multi-function Pin Selection; default 21h) **(VSB Power)**

BIT	READ / WRITE	DESCRIPTION
7	R / W	Pin 67 Select (reset by RSMRST#) = 0 PSOUT# = 1 GPIO57
6	R / W	Pin 68 Select (reset by RSMRST#) = 0 PSIN# = 1 GPIO56
5	R / W	Pin 70 Select (reset by RSMRST#) = 0 SUSLED = 1 GPIO55

BIT	READ / WRITE	DESCRIPTION
4	R / W	Pin 71 Select (reset by RSMRST#) = 0 PWROK = 1 GPIO54
3	R / W	Pin 72 Select (reset by RSMRST#) = 0 PSON# = 1 GPIO53
2	R / W	Pin 73 Select (reset by RSMRST#) = 0 SUSB# = 1 GPIO52
1	R / W	Pin 75 Select (reset by RSMRST#) = 0 RSMRST# = 1 GPIO51
0	R / W	Pin 77 Select (reset by RSMRST#) = 0 WDTO# = 1 GPIO50

CR 2Eh. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Test Mode Bits: Reserved for Nuvoton.

CR 2Fh. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Test Mode Bits: Reserved for Nuvoton.

21.2 Logical Device 0 (FDC)

CR 30h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Activate the logical device.

CR 60h, 61h. (Default 03h,F0h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select FDC I/O base address <100h: FF8h> on 8 bytes boundary.

CR 70h. (Default 06h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for FDC.

CR 74h. (Default 02h)

BIT	READ / WRITE	DESCRIPTION
7~3	Reserved.	
2~0	R / W	These bits select DRQ resource for FDC. 000: DMA0. 001: DMA1. 010: DMA2. 011: DMA3. 1xx: No DMA active.

CR F0h. (Default 8Eh)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	This bit determines the polarity of all FDD interface signals. 0: FDD interface signals are active low. 1: FDD interface signals are active high.
5	R / W	When this bit is logic 0, indicates a second drive is installed and is reflected in status register A. (PS2 mode only)
4	R / W	Swap Drive 0, 1 Mode => 0: No Swap. 1: Drive and Motor select 0 and 1 are swapped.
3~2	R / W	Interface Mode. 00: Model 30. 01: PS/2. 10: Reserved. 11: AT Mode
1	R / W	FDC DMA Mode. 0: Burst Mode is enabled 1: Non-Burst Mode.

BIT	READ / WRITE	DESCRIPTION
0	R / W	Floppy Mode. 0: Normal Floppy Mode. 1: Enhanced 3-mode FDD.

CR F1h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~6	R / W	Boot Floppy. 00: FDD A. 01: Reserved. 10: Reserved. 11: Reserved.
5~4	R / W	Media ID1, Media ID0. These bits will be reflected on FDC's Tape Drive Register bit 7, 6.
3~2	R / W	Density Select. 00: Normal. 01: Normal. 10: 1 (Forced to logic 1). 11: 0 (Forced to logic 0).
1	R / W	DISFDDWR => 0: Enable FDD write. 1: Disable FDD write (forces pins WE, WD to stay high).
0	R / W	SWWP => 0: Normal, use WP to determine whether the FDD is write protected or not. 1: FDD is always write-protected.

CR F2h. (Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~2	Reserved.	
1~0	R / W	FDD A Drive Type.

CR F4h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	0: Enable FDC Pre-compensation. 1: Disable FDC Pre-compensation.
5	Reserved.	
4~3	R / W	Data Rate Table selection (Refer to TABLE A). 00: Select regular drives and 2.88 format. 01: 3-mode drive. 10: 2 Meg Tape. 11: Reserved.
2	Reserved.	
1~0	R / W	Drive Type selection (Refer to TABLE B).

CR F5h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Same as FDD0 of CR F5h.

TABLE A

DRIVE RATE TABLE SELECT		DATA RATE		SELECTED DATA RATE		SELDEN
DRTS1	DRTS0	DRATE1	DRATE0	MFM	FM	
0	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	300K	150K	0
		1	0	250K	125K	0
0	1	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	500K	250K	0
		1	0	250K	125K	0
1	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	2Meg	---	0
		1	0	250K	125K	0

TABLE B

DTYPE0	DTYPE1	DRVDEN0 (pin 2)	DRIVE TYPE
0	0	SELDEN	4/2/1 MB 3.5”“ 2/1 MB 5.25” 2/1.6/1 MB 3.5” (3-MODE)
0	1	DRATE1	
1	0	$\overline{\text{SELDEN}}$	
1	1	DRATE0	

21.3 Logical Device 1 (Parallel Port)

CR 30h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	*0: Logical device is inactive. 1: Activate the logical device. *: If customer need EXTFDC function, bit 0 should be 0.

CR 60h, 61h. (Default 03h, 78h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select PRT I/O base address. <100h: FFCh> on 4-byte boundary (EPP not supported) or <100h: FF8h> on 8-byte boundary (all modes supported, EPP is only available when the base address is on 8-byte boundary).

CR 70h. (Default 07h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for PRT.

CR 74h. (Default 04h)

BIT	READ / WRITE	DESCRIPTION
7~3	Reserved.	
2~0	R / W	These bits select DRQ resource for PRT. 000: DMA0. 001: DMA1. 010: DMA2. 011: DMA3. 1xx: No DMA active.

CR F0h. (Default 3Fh)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6~3	R / W	ECP FIFO Threshold.
2~0	R / W	Parallel Port Mode selection (CR28 bit2 PRTMODS2 = 0). 000: Standard and Bi-direction (SPP) mode. 001: EPP – 1.9 and SPP mode. 010: ECP mode. 011: ECP and EPP – 1.9 mode. 100: Printer Mode. 101: EPP – 1.7 and SPP mode. 110: Reserved. 111: ECP and EPP – 1.7 mode.

21.4 Logical Device 2 (UART A)

CR 30h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Activate the logical device.

CR 60h, 61h. (Default 03h, F8h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select Serial Port 1 I/O base address <100h: FF8h> on 8 bytes boundary.

CR 70h. (Default 04h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for Serial Port 1.

CR F0h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~2	Reserved.	
1~0	R / W	00: UART A clock source is 1.8462 MHz (24 MHz / 13). 01: UART A clock source is 2 MHz (24 MHz / 12). 10: UART A clock source is 24 MHz (24 MHz / 1). 11: Reserved

21.5 Logical Device 3 (UART B)

CR 30h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Activate the logical device.

CR 60h, 61h. (Default 02h, F8h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select Serial Port 2 I/O base address <100h: FF8h> on eight-byte boundary.

CR 70h. (Default 03h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for Serial Port 2.

CR F0h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3	R / W	0: No reception delay when SIR is changed from TX mode to RX mode. 1: Reception delayed for 4 characters' time (40 bit-time) when SIR is changed from TX mode to RX mode.
2	R / W	0: No transmission delay when SIR is changed from RX mode to TX mode. 1: Transmission delayed for 4 characters' time (40 bit-time) when SIR is changed from RX mode to TX mode.
1~0	R / W	00: UART B clock source is 1.8462 MHz (24 MHz / 13). 01: UART B clock source is 2 MHz (24 MHz / 12). 10: UART B clock source is 24 MHz (24 MHz / 1). 11: Reserved

CR F1h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	Reserved.
6	R / W	IRLOCSEL => IR I/O pins' location selection. 0: Through SINB / SOUTB. 1: Through IRRX / IRTX.
5~3	R / W	IRMODE => IR function mode selection. See the table below.
2	R / W	IR half / full duplex function selection. 0: IR function is Full Duplex. 1: IR function is Half Duplex.
1	R / W	0: SOUTB pin of UART B function or IRTX pin of IR function in normal condition. 1: Inverse SOUTB pin of UART B function or IRTX pin of IR function.
0	R / W	0: SINB pin of UART B function or IRRX pin of IR function in normal condition. 1: Inverse SINB pin of UART B function or IRRX pin of IR function.

IR MODE	IR FUNCTION	IRTX	IRRX
00X	Disable	Tri-state	High
010*	IrDA	Active pulse 1.6 μS	Demodulation into SINB/IRRX
011*	IrDA	Active pulse 3/16 bit time	Demodulation into SINB/IRRX
100	ASK-IR	Inverting IRTX/SOUTB pin	Routed to SINB/IRRX
101	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Routed to SINB/IRRX
110	ASK-IR	Inverting IRTX/SOUTB	Demodulation into SINB/IRRX
111*	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Demodulation into SINB/IRRX

Note: The notation is normal mode in the IR function.

21.6 Logical Device 5 (Keyboard Controller)

CR 30h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h. (Default 00h,60h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select the first KBC I/O base address <100h: FFFh> on 1-byte boundary.

CR 62h, 63h. (Default 00h,64h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select the second KBC I/O base address <100h: FFFh> on 1 byte boundary.

CR 70h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for KINT. (Keyboard interrupt)

CR 72h. (Default 0Ch)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for MINT. (PS/2 Mouse interrupt)

CR F0h. (Default83h)

BIT	READ / WRITE	DESCRIPTION
7~6	R / W	KBC clock rate 00: Reserve 01: Reserve 10: 12MHz 11: Reserve
5~3	Reserved.	
2	R / W	0: Port 92 disable. 1: Port 92 enable.
1	R / W	0: Gate A20 software control. 1: Gate A20 hardware speed up.

BIT	READ / WRITE	DESCRIPTION
0	R / W	0: KBRST# software control. 1: KBRST# hardware speed up.

21.7 Logical Device 6 (Serial Peripheral Interface)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Serial Peripheral Interface is inactive. 1: Activate Serial Peripheral Interface.

CR 62h, 63h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select Serial Peripheral Interface I/O base address <100h: FF8h> on 1 byte boundary.

21.8 Logical Device 7 (GPIO6)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3	R / W	0: GPIO6 is inactive. 1: GPIO6 is active.
2~0	Reserved.	

CR F4h. (GPIO6 I/O Register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO6 I/O register 0: The respective GPIO6 PIN is programmed as an output port 1: The respective GPIO6 PIN is programmed as an input port.

CR F5h. (GPIO6 Data Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO6 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR F6h. (GPIO6 Inversion Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO6 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

CR F7h. (Status Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only Read-Clear	GPIO6 Event Status Bit 7-0 corresponds to GP67-GP60, respectively. 0 : No active edge(rising/falling) has been detected 1 : An active edge(rising/falling) has been detected Read the status bit clears it to 0.

CR F8h. (GPIO6 Multi-function Select Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO67 1: GPIO67 → PLED

BIT	READ / WRITE	DESCRIPTION
6	R / W	0: GPIO66 1: GPIO66 → PLED
5	R / W	0: GPIO65 1: GPIO65 → PLED
4	R / W	0: GPIO64 1: GPIO64 → PLED
3	R / W	0: GPIO63 1: GPIO63 → PLED
2	R / W	0: GPIO62 1: GPIO62 → PLED
1	R / W	0: GPIO61 1: GPIO61 → PLED
0	R / W	0: GPIO60 1: GPIO60 → PLED

21.9 Logical Device 8 (WDTO# & PLED)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: WDTO# and PLED are inactive. 1: Activate WDTO# and PLED.

CR F5h. (WDTO#, PLED and KBC P20 Control Mode Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~5	R / W	Select Power LED mode. 000: Power LED pin is driven high. 001: Power LED pin outputs 0.5Hz pulse with 50% duty cycle. 010: Power LED pin is driven low. 011: Power LED pin outputs 2Hz pulse with 50% duty cycle. 100: Power LED pin outputs 1Hz pulse with 50% duty cycle. 101: Power LED pin outputs 4Hz pulse with 50% duty cycle. 110: Power LED pin outputs 0.25Hz pulse with 50% duty cycle. 111: Power LED pin outputs 0.25Hz pulse with 50% duty cycle.
4	R / W	WDTO# count mode is 1000 times faster. 0: Disable. 1: Enable. (If bit-3 is in Seconds Mode, the count mode is 1/1000 sec.) (If bit-3 is in Minutes Mode, the count mode is 1/1000 min.)
3	R / W	Select WDTO# count mode. 0: Second Mode. 1: Minute Mode.
2	R / W	Enable the rising edge of a KBC reset (P20) to issue a time-out event. 0: Disable. 1: Enable.
1	R / W	Disable / Enable the WDTO# output low pulse to the KBRST# pin (PIN60) 0: Disable. 1: Enable.
0	Reserved.	

CR F6h. (WDTO# Counter Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Watch Dog Timer Time-out value. Writing a non-zero value to this register causes the counter to load the value into the Watch Dog Counter and start counting down. If CR F7h, bits 7 and 6 are set, any Mouse Interrupt or Keyboard Interrupt event causes the previously-loaded, non-zero value to be reloaded to the Watch Dog Counter and the count down resumes. Reading this register returns the current value in the Watch Dog Counter, not the Watch Dog Timer Time-out value. 00h: Time-out Disable 01h: Time-out occurs after 1 minute only. 02h: Time-out occurs after 2 second/minutes 03h: Time-out occurs after 3 second/minutes ……..... FFh: Time-out occurs after 255 second/minutes (The deviation is approx 1 second.)

CR F7h. (WDTO# Control & Status Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	Mouse interrupt reset enables watch-dog timer reload 0: Watchdog timer is not affected by mouse interrupt. 1: Watchdog timer is reset by mouse interrupt.
6	R / W	Keyboard interrupt reset enables watch-dog timer reload 0: Watchdog timer is not affected by keyboard interrupt. 1: Watchdog timer is reset by keyboard interrupt.
5	Write “1” Only	Trigger WDTO# event. This bit is self-clearing.
4	R / W Write “0” Clear	WDTO# status bit 0: Watchdog timer is running. 1: Watchdog timer issues time-out event.
3~0	R / W	These bits select the IRQ resource for the WDTO#. (02h for SMI# event.)

21.10 Logical Device 9 (GPIO2, GPIO3, GPIO4, GPIO5)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION	
7~4	Reserved.		
3	R / W	0: GPIO5 is inactive.	1: GPIO5 is active
2	R / W	0: GPIO4 is inactive.	1: GPIO4 is active.
1	R / W	0: GPIO3 is inactive.	1: GPIO3 is active.
0	R / W	0: GPIO2 is inactive.	1: GPIO2 is active.

CR E0h. (GPIO5 I/O Register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO5 I/O register 0: The respective GPIO5 PIN is programmed as an output port 1: The respective GPIO5 PIN is programmed as an input port.

CR E1h. (GPIO5 Data Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO5 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For input ports, the respective bits can only be read by the pins. Write accesses are ignored.

CR E2h. (GPIO5 Inversion Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO5 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

CR E3h. (GPIO2 Register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO2 I/O register 0: The respective GPIO2 PIN is programmed as an output port 1: The respective GPIO2 PIN is programmed as an input port

CR E4h. (GPIO2 Data Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO2 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For input ports, the respective bits can only be read by the pins. Write accesses are ignored.

CR E5h. (GPIO2 Inversion Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO2 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

CR E6h. (GPIO2 Status Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only Read-Clear	GPIO2 Event Status Bit 7-0 corresponds to GP27-GP20, respectively. 0 : No active edge(rising/falling) has been detected 1 : An active edge(rising/falling) has been detected Read the status bit clears it to 0.

CR E7h. (GPIO3 Status Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only Read-Clear	GPIO3 Event Status Bit 7-0 corresponds to GP37-GP30, respectively. 0 : No active edge(rising/falling) has been detected 1 : An active edge(rising/falling) has been detected Read the status bit clears it to 0.

CR E8h. (GPIO4 Status Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only Read-Clear	GPIO4 Event Status Bit 7-0 corresponds to GP47-GP40, respectively. 0 : No active edge(rising/falling) has been detected 1 : An active edge(rising/falling) has been detected Reading the status bit clears it to 0.

CR E9h. (GPIO5 Status Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	Read Only Read-Clear	GPIO5 Event Status Bit 7-0 corresponds to GP57-GP50, respectively. 0 : No active edge(rising/falling) has been detected 1 : An active edge(rising/falling) has been detected Reading the status bit clears it to 0.

CR F0h. (GPIO3 I/O Register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO3 I/O register 0: The respective GPIO3 PIN is programmed as an output port 1: The respective GPIO3 PIN is programmed as an input port.

CR F1h. (GPIO3 Data Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO3 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For input ports, the respective bits can only be read by the pins. Write accesses are ignored.

CR F2h. (GPIO3 Inversion Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO3 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

CR F3h. (Suspend LED Mode Register; Default 00h) **(VBAT power)**

BIT	READ / WRITE	DESCRIPTION
7~5	R / W	Select Suspend LED mode.(SUSLED) 000: Suspend LED pin is driven high. 001: Suspend LED pin outputs 0.5Hz pulse with 50% duty cycle. 010: Suspend LED is driven low. 011: Suspend LED pin outputs 2Hz pulse with 50% duty cycle. 100: Suspend LED pin outputs 1Hz pulse with 50% duty cycle. 101: Suspend LED pin outputs 4Hz pulse with 50% duty cycle. 110: Suspend LED pin outputs 0.25Hz pulse with 50% duty cycle. 111: Suspend LED pin outputs 0.25Hz pulse with 50% duty cycle.
4~0	Reserved.	

CR F4h. (GPIO4 I/O Register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO4 I/O register 0: The respective GPIO4 PIN is programmed as an output port 1: The respective GPIO4 PIN is programmed as an input port.

CR F5h. (GPIO4 Data Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO4 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For input ports, the respective bits can only be read by the pins. Write accesses are ignored.

CR F6h. (GPIO4 Inversion Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO4 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

CR F7h. (GPIO4 Multi-function Select Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO47 1: GPIO47 → SUSLED
6	R / W	0: GPIO46 1: GPIO46 → WDTO#
5	R / W	0: GPIO45 1: GPIO45 → SUSLED
4	R / W	0: GPIO44 1: GPIO44 → WDTO#
3	R / W	0: GPIO43 1: GPIO43 → SUSLED
2	R / W	0: GPIO42 1: GPIO42 → WDTO#
1	R / W	0: GPIO41 1: GPIO41 → SUSLED
0	R / W	0: GPIO40 1: GPIO40 → WDTO#

CR F8h. (GPIO2 Multi-function Select Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO27 1: GPIO27 → SUSLED
6	R / W	0: GPIO26 1: GPIO26 → SUSLED
5	R / W	0: GPIO25 1: GPIO25 → SUSLED
4	R / W	0: GPIO24 1: GPIO24 → SUSLED
3	R / W	0: GPIO23 1: GPIO23 → PLED
2	R / W	0: GPIO22 1: GPIO22 → PLED
1	R / W	0: GPIO21 1: GPIO21 → PLED
0	R / W	0: GPIO20 1: GPIO20 → PLED

CR F9h. (GPIO3 Multi-function Select Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO37 1: GPIO37 → SUSLED
6	R / W	0: GPIO36 1: GPIO36 → SUSLED
5	R / W	0: GPIO35 1: GPIO35 → SUSLED
4	R / W	0: GPIO34 1: GPIO34 → SUSLED
3	R / W	0: GPIO33 1: GPIO33 → SUSLED
2	R / W	0: GPIO32 1: GPIO32 → SUSLED
1	R / W	0: GPIO31 1: GPIO31 → SUSLED
0	R / W	0: GPIO30 1: GPIO30 → SUSLED

CR FAh. (GPIO5 Multi-function Select Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO57 1: GPIO57 → SUSLED
6	R / W	0: GPIO56 1: GPIO56 → SUSLED
5	R / W	0: GPIO55 1: GPIO55 → SUSLED
4	R / W	0: GPIO54 1: GPIO54 → SUSLED
3	R / W	0: GPIO53 1: GPIO53 → SUSLED
2	R / W	0: GPIO52 1: GPIO52 → SUSLED
1	R / W	0: GPIO51 1: GPIO51 → SUSLED
0	R / W	0: GPIO50 1: GPIO50 → SUSLED

CR FEh. (GPIO3 Input Detected Type Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	Reserved.
6	R / W	0: Enable GP35 input de-bouncer 1: Disable GP35 input de-bouncer
5	R / W	0: Enable GP31 input de-bouncer 1: Disable GP31 input de-bouncer
4	R / W	0: Enable GP30 input de-bouncer 1: Disable GP30 input de-bouncer
3	Reserved.	
2	R / W	0: GP35 trigger type : edge 1: GP35 trigger type : level
1	R / W	0: GP31 trigger type : edge 1: GP31 trigger type : level
0	R / W	0: GP30 trigger type : edge 1: GP30 trigger type : level

21.11 Logical Device A (ACPI)

(CR30, CR70 are VCC powered; CRE0~F7 are VRTC powered)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical Device A CR70h function is inactive. 1: Logical Device A CR70h function is active.

CR 70h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select the IRQ resource for PME#.

CR E0h. (Default 01h) (VBAT power)

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>DIS_PSIN => Disable the panel switch input to turn on the system power supply.
0: PSIN is wire-AND and connected to PSOUT#.
1: PSIN is blocked and cannot affect PSOUT#.</td></tr>
<tr><td>6</td><td>R / W</td><td>Enable KBC wake-up
0: Disable keyboard wake-up function via PSOUT#.
1: Enable keyboard wake-up function via PSOUT#.</td></tr>
<tr><td>5</td><td>R / W</td><td>Enable Mouse wake-up
0: Disable mouse wake-up function via PSOUT#.
1: Enable mouse wake-up function via PSOUT#.</td></tr>
<tr><td>4</td><td>R / W</td><td>MSRKEY =>
Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please see the following table for the details.
<table>
<tr><th>ENMDAT_UP</th><th>MSRKEY</th><th>MSXKEY</th><th>Wake-up event</th></tr>
<tr><td>1</td><td>x</td><td>1</td><td>Any button clicked or any movement.</td></tr>
<tr><td>1</td><td>x</td><td>0</td><td>One click of left or right button.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>One click of the left button.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>One click of the right button.</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Two clicks of the left button.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Two clicks of the right button.</td></tr>
</table></td></tr>
<tr><td>3</td><td>Reserved.</td><td></td></tr>
</table>

BIT	READ / WRITE	DESCRIPTION
2	R / W	Keyboard / Mouse swap enable 0: Normal mode. 1: Keyboard / Mouse ports are swapped.
1	R / W	MSXKEY => Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please check out the table in CRE0[4] for the detailed.
0	R / W	KBXKEY => 0: Only the pre-determined key combination in sequence can wake up the system. 1: Any character received from the keyboard can wake up the system.

CR E1h. (KBC Wake-Up Index Register; Default 00h) (VSB power)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Keyboard wake-up index register. This is the index register of CRE2, which is the access window for the keyboard's pre-determined key key-combination characters. The first set of wake-up keys is in of 0x00 – 0x0E, the second set 0x30 – 0x3E, and the third set 0x40 – 0x4E. Incoming key combinations can be read through 0x10 – 0x1E.

CR E2h. (KBC Wake-Up Data Register; Default FFh) (VSB power)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Keyboard wake-up data register. This is the data register for the keyboard's pre-determined key-combination characters, which is indexed by CRE1.

CR E3h. (Event Status Register; Default 08h)

BIT	READ / WRITE	DESCRIPTION
7~6	Reserved.	
5	Read Only Read-Clear	This status flag indicates VSB power off/on.
4	Read Only Read-Clear	This bit is always 0 0: When power-loss occurs and the VSB power is on, turn on system power.
3	Read Only Read-Clear	Thermal shutdown status. 0: No thermal shutdown event issued. 1: Thermal shutdown event issued.
2	Read Only Read-Clear	PSIN_STS 0: No PSIN event issued. 1: PSIN event issued.

BIT	READ / WRITE	DESCRIPTION
1	Read Only Read-Clear	MSWAKEUP_STS => The bit is latched by the mouse wake-up event. 0: No mouse wake-up event issued. 1: Mouse wake-up event issued.
0	Read Only Read-Clear	KBWAKEUP_STS => The bit is latched by the keyboard wake-up event. 0: No keyboard wake-up event issued. 1: Keyboard wake-up event issued.

CR E4h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6~5	R / W	Power-loss control bits => (**VBAT**) 00: System always turns off when it returns from power-loss state. 01: System always turns on when it returns from power-loss state. 10: System turns off / on when it returns from power-loss state depending on the state before the power loss. 11: User defines the state before power loss.(i.e. the last state set of CRE6[4])
4	R / W	VSBGATE# Enable bit => 0: Disable. 1: Enable.
3	R / W	Keyboard wake-up options. **(LRESET#)** 0: Password or sequence hot keys programmed in the registers. 1: Any key.
2	R / W	Enable the hunting mode for all wake-up events set in CRE0. This bit is cleared when any wake-up events is captured. **(LRESET#)** 0: Disable. 1: Enable.
1~0	Reserved.	

CR E5h. (GPIOs Reset Source Register; Default 00))

BIT	READ / WRITE	DESCRIPTION
7~ 5	Reserved.	
4	R / W	VID_MRST 0: VID reset by LRESET#. 1: VID reset by PWROK.
3	R / W	GP23_MRST 0: GP23 reset by LRESET#. 1: GP23 reset by PWROK.
2	R / W	GP22_MRST 0: GP22 reset by LRESET#. 1: GP22 reset by PWROK.

BIT	READ / WRITE	DESCRIPTION
1	R / W	PWROK source selection. 0: PSON# 1: SUSB#
0	R / W	ATXPGD signal to control PWROK and PWROK2 generation 0: Enable. 1: Disable.

CR E6h. (Default 1Ch)

BIT	READ / WRITE	DESCRIPTION
7	R / W	ENMDAT => **(VSB)** Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please see the table in CRE0, bit 4 for the details.
6	Reserved.	
5	R / W	CASEOPEN Clear Control. **(VSB)** Write 1 to this bit to clear CASEOPEN status. This bit will not clear the status itself. Please write 0 after an event is cleared. The function is the same as Index 46h bit 7 of H/W Monitor part.
4	R / W	Power-loss Last State Flag. **(VBAT)** 0: ON 1: OFF.
3~1	R / W	PWROK_DEL **(VSB)** Set the delay time when rising from 3VCC to PWROK **Bits** **3 2 1** 0 0 0: 300 ~ 600mS 0 0 1: 330 ~ 670mS 0 1 0: 390 ~ 730mS 0 1 1: 520 ~ 860mS 1 0 0: 200 ~ 300mS 1 0 1: 230 ~ 370mS 1 1 0: 290 ~ 430mS 1 1 1: 420 ~ 560mS
0	R / W-Clear	PWROK_TRIG => Write 1 to re-trigger the PWROK signal from low to high.

CR E7h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	ENKD3 => **(VSB)** Enable the third set of keyboard wake-up key combination. Its values are accessed through keyboard wake-up index register (CRE1) and keyboard wake-up data register (CRE2) at the index from 40h to 4eh. 0: Disable the third set of the key combinations. 1: Enable the third set of the key combinations.
6	R / W	ENKD2 => **(VSB)** Enable the second set of keyboard wake-up key combination. Its values are accessed through keyboard wake-up index register (CRE1) and keyboard wake-up data register (CRE2) at the index from 30h to 3eh. 0: Disable the second set of the key combinations. 1: Enable the second set of the key combinations.
5	R / W	ENWIN98KEY => **(VSB)** Enable Win98 keyboard dedicated key to wake-up system via PSOUT# when keyboard wake-up function is enabled. 0: Disable Win98 keyboard wake-up. 1: Enable Win98 keyboard wake-up.
4	R / W	EN_ONPSOUT **(VBAT)** Disable/Enable to issue a 0.5s delay PSOUT# level when system returns from power loss state and is supposed to be on as described in CRE4[6:5], logic device A. (for SiS & VIA chipsets) 0: Disable. 1: Enable.
3	R / W	Select WDTO# reset source **(VSB)** 0: Watchdog timer is reset by LRESET#. 1: Watchdog timer is reset by PWROK.
2~1	Reserved.	
0	R / W	Hardware Monitor RESET source select **(VBAT)** 0: PWROK. 1: LRESET#.

CR E8h. (Reserved)

CR E9h. (Reserved)

CR F2h. (Default 7Ch) (VSB Power)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	Enable RSTOUT4# function. 0: Disable RSTOUT4#. 1: Enable RSTOUT4#.

BIT	READ / WRITE	DESCRIPTION
5	R / W	Enable RSTOUT3# function. 0: Disable RSTOUT3#. 1: Enable RSTOUT3#.
4	R / W	Enable RSTOUT2# function. 0: Disable RSTOUT2#. 1: Enable RSTOUT2#.
3	R / W	Enable RSTOUT1# function. 0: Disable RSTOUT1#. 1: Enable RSTOUT1#.
2	R / W	Enable RSTOUT0# function. 0: Disable RSTOUT0#. 1: Enable RSTOUT0#.
1	Reserved.	
0	R / W	EN_PME => 0 : Disable PME. 1 : Enable PME.

CR F3h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~6	Reserved.	
5	R / W-Clear	PME status of the Mouse IRQ event. Write 1 to clear this status.
4	R / W-Clear	PME status of the KBC IRQ event. Write 1 to clear this status.
3	R / W-Clear	PME status of the PRT IRQ event. Write 1 to clear this status.
2	R / W-Clear	PME status of the FDC IRQ event. Write 1 to clear this status.
1	R / W-Clear	PME status of the URA IRQ event. Write 1 to clear this status.
0	R / W-Clear	PME status of the URB IRQ event. Write 1 to clear this status.

CR F4h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3	R / W-Clear	PME status of the HM IRQ event. Write 1 to clear this status.
2	R / W-Clear	PME status of the WDTO# event. Write 1 to clear this status.
1	Reserved.	

BIT	READ / WRITE	DESCRIPTION
0	R / W-Clear	PME status of the RIB event. Write 1 to clear this status.

CR F6h. (Default 00h) (VSB Power)

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Disable KB, MS PME interrupt of the KBC password event. 1: Enable KB, MS PME interrupt of the KBC password event.
6	Reserved.	
5	R / W	0: Disable PME interrupt of the Mouse IRQ event. 1: Enable PME interrupt of the Mouse IRQ event.
4	R / W	0: Disable PME interrupt of the KBC IRQ event. 1: Enable PME interrupt of the KBC IRQ event.
3	R / W	0: Disable PME interrupt of the PRT IRQ event. 1: Enable PME interrupt of the PRT IRQ event.
2	R / W	0: Disable PME interrupt of the FDC IRQ event. 1: Enable PME interrupt of the FDC IRQ event.
1	R / W	0: Disable PME interrupt of the URA IRQ event. 1: Enable PME interrupt of the URA IRQ event.
0	R / W	0: Disable PME interrupt of the URB IRQ event. 1: Enable PME interrupt of the URB IRQ event.

CR F7h. (Default 00h) (VSB Power)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3	R / W	0: Disable PME interrupt of the HM IRQ event. 1: Enable PME interrupt of the HM IRQ event.
2	R / W	0: Disable PME interrupt of the WDTO# event. 1: Enable PME interrupt of the WDTO# event.
1	Reserved.	
0	R / W	0: Disable PME interrupt of the RIB event. 1: Enable PME interrupt of the RIB event.

CR Feh. (GPIO3 Event Route Selection Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	Reserved.
6	R / W	0: Disable GP35 event route to PSOUT#. 1: Enable GP35 event route to PSOUT#.
5	R / W	0: Disable GP31 event route to PSOUT#. 1: Enable GP31 event route to PSOUT#.

BIT	READ / WRITE	DESCRIPTION
4	R / W	0: Disable GP30 event route to PSOUT#. 1: Enable GP30 event route to PSOUT#.
3	Reserved.	
2	R / W	0: Disable GP35 event route to PME#. 1: Enable GP35 event route to PME#.
1	R / W	0: Disable GP31 event route to PME#. 1: Enable GP31 event route to PME#.
0	R / W	0: Disable GP30 event route to PME#. 1: Enable GP30 event route to PME#.

21.12 Logical Device B (Hardware Monitor)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Logical device is active.

CR 60h, 61h. (Default 00h, 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select the HM base address <100h : FFEh> along a two-byte boundary.

CR 70h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select the IRQ resource for HM.

CR F0h. (VID Control Register; Default 81h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	VID I/O Control 0: VID output mode. 1: VID input mode.
6	R / W	VIDAMD input level select 0: VID is GTL level. 1: VID is AMD VRM level.
5	R / W	0: Disable AUXFANIN1 input de-bouncer. 1: Enable AUXFANIN1 input de-bouncer.
4	R / W	0: Disable CPUFANIN1 input de-bouncer. 1: Enable CPUFANIN1 input de-bouncer.
3	R / W	0: Disable AUXFANIN0 input de-bouncer. 1: Enable AUXFANIN0 input de-bouncer.
2	R / W	0: Disable CPUFANIN0 input de-bouncer. 1: Enable CPUFANIN0 input de-bouncer.
1	R / W	0: Disable SYSFANIN input de-bouncer. 1: Enable SYSFANIN input de-bouncer.
0	Reserved.	

CR F1h. (VID Data Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	VID[7:0] Data Register. (For Input/Output both use)

CR F2h. (FAN Strapping Status Register; Default 00h) (VCC Power)

BIT	READ / WRITE	DESCRIPTION
7~2	Reserved.	
1	Read Only	FAN_SET2 strapping status. This bit is strapped by pin 83(SOUTB). 0: Initial speed is 100%. 1: Initial speed is 50%.
0	Read Only	FAN_SET strapping status. This bit is strapped by pin 117(PLED). 0: Initial speed is 100%. 1: Initial speed is 50%.

21.13 Logical Device C (PECI, SST)

CR E0h. (Agent Configuration Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	Agt4EN (Agent 4 Enable Bit) 0: Agent 4 is disabled. 1: Agent 4 is enabled.
6	R / W	Agt3EN (Agent 3 Enable Bit) 0: Agent 3 is disabled. 1: Agent 3 is enabled.
5	R / W	Agt2EN (Agent 2 Enable Bit) 0: Agent 2 is disabled. 1: Agent 2 is enabled.
4	R / W	Agt1EN (Agent 1 Enable Bit) 0: Agent 1 is disabled. 1: Agent 1 is enabled.
3	R / W	RTD4 0: Agent 4 always returns the relative temperature from domain 0. 1: Agent 4 always returns the relative temperature from domain 1.
2	R / W	RTD3 (Agent 3 Return Domain 1 Enable Bit. Functions only when Agt3D1 is set to 1) 0: Agent 3 always returns the relative temperature from domain 0. 1: Agent 3 always returns the relative temperature from domain 1.
1	R / W	RTD2 (Agent 2 Return Domain 1 Enable Bit. Functions only when Agt2D1 is set to 1) 0: Agent 2 always returns the relative temperature from domain 0. 1: Agent 2 always returns the relative temperature from domain 1.
0	R / W	RTD1 (Agent 1 Return Domain 1 Enable Bit. Functions only when Agt1D1 is set to 1) 0: Agent 1 always returns the relative temperature from domain 0. 1: Agent 1 always returns the relative temperature from domain 1.

CR E1h. (Agent 1 Tbase Register; Default 48h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6~0	R / W	Agent 1 Tbase (Range: 0~127). (Note 1)

CR E2h. (Agent 2 Tbase Register; Default 48h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6~0	R / W	Agent 2 Tbase (Range: 0~127). (note 1)

CR E3h. (Agent 3 Tbase Register; Default 48h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6~0	R / W	Agent 3 Tbase (Range: 0~127). (Note 1)

CR E4h. (Agent 4 Tbase Register; Default 48h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6~0	R / W	Agent 4 Tbase (Range: 0~127). (Note 1)

Note 1: Tbase is a temperature refernce based on the experiment of processor actual temperature. For more details, please refer to 8.5 PECI.

CR E5h. (PECI Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	Agt4D1 (Agent 4 Domain 1 Enable Bit) 0: Agent 4 does not have domain 1. 1: Agent 4 has domain 1.
6	R / W	Agt3D1 (Agent 3 Domain 1 Enable Bit) 0: Agent 3 does not have domain 1. 1: Agent 3 has domain 1.
5	R / W	Agt2D1 (Agent 2 Domain 1 Enable Bit) 0: Agent 2 does not have domain 1. 1: Agent 2has domain 1.
4	R / W	Agt1D1 (Agent 1 Domain 1 Enable Bit) 0: Agent 1 does not have domain 1. 1: Agent 1 has domain 1.
3	R / W	PECI_1.1°_en 0: Normal PECI transmission. (Default) 1: PECI _1.1a transmission with PECI_REQ#.
2	Reserved	
1	R / W	Return High Temperature 0: The temperature of each agent is returned from domain 0 or domain 1, which is controlled by CRE0 bit 0~3. 1: Return the highest temperature in domain 0 and domain 1 of individual Agent.

BIT	READ / WRITE	DESCRIPTION
0	R / W	PECISB_EN 0: PECI host is controlled by IO. 1: PECI host is another device (e.g. South Bridge)

CR E8h. (PECI Warning Flag Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	Read Only	**Agent 4 Alert Bit** (When CR E8[3] is 0) 0: Agent 4 has valid FCS. 1: Agent 4 has invalid FCS in the previous 3 transactions.
		Agent 4 Absent Bit (When CR E8[3] is 1) 0: Agent 4 is detected. 1: Agent 4 cannot be detected.
6	Read Only	**Agent 3 Alert Bit** (When CR E8[3] is 0) 0: Agent 3 has valid FCS. 1: Agent 3 has invalid FCS in the previous 3 transactions.
		Agent 3 Absent Bit (When CR E8[3] is 1) 0: Agent 3 is detected. 1: Agent 3 cannot be detected.
5	Read Only	**Agent 2 Alert Bit** (When CR E8[3] is 0) 0: Agent 2 has valid FCS. 1: Agent 2 has invalid FCS in the previous 3 transactions.
		Agent 2 Absent Bit (When CR E8[3] is 1) 0: Agent 2 is detected. 1: Agent 2 cannot be detected.
4	Read Only	**Agent 1 Alert Bit** (When CR E8[3] is 0) 0: Agent 1 has valid FCS. 1: Agent 1 has invalid FCS in the previous 3 transactions.
		Agent 1 Absent Bit (When CR E8[3] is 1) 0: Agent 1 is detected. 1: Agent 1 cannot be detected.
3~2	R / W	**Bank Select.** These two bits are used in Bank index selection. The relative data delivered over PECI interface and PECI Agent Absent Bit can be read from the registers below by setting Bank selection. The relative data delivered over PECI interface can be read in CR EE and CR EF, and the PECI warning flag can be read in CR E8 bit 7~4.
1~0	R / W	**PECI Speed Select.** **Bits** **1 0** 0 0: The PECI speed is 1.5 MHz 0 1: The PECI speed is 750 KHz 1 0: The PECI speed is 375 KHz 1 1: The PECI speed is 187 KHz

CR E9h. (Reserved)

CR EAh. (PECI_1.1[a] Status Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	Read_Only	Reserved
		Agent 4 Alert toggle bit (When CR E8[2] is 1) 0: PECI Alert bit never occurred. 1: PECI Alert bit occurred once. (Read clear)
6	Read_Only	Reserved
		Agent 3 Alert toggle bit (When CR E8[2] is 1) 0: PECI Alert bit never occurred. 1: PECI Alert bit occurred once. (Read clear)
5	Read_Only	Reserved
		Agent 2 Alert toggle bit (When CR E8[2] is 1) 0: PECI Alert bit never occurred. 1: PECI Alert bit occurred once. (Read clear)
4	Read_Only	Reserved
		Agent 2 Alert toggle bit (When CR E8[2] is 1) 0: PECI Alert bit never occurred. 1: PECI Alert bit occurred once. (Read clear)
3~0	Read_Only	Reserved. (When CR E8[2] is 0)

CR ECh. (PECI_1.1a Status Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~3	R / W	Reserved.
2~0	R / W	PECI Transmission cycle time: **Bits** **2 1 0** 0 0 0 : Finish one PECI message transmission every 0.0625sec(16Hz) 0 0 1 : Finish one PECI message transmission every 0.125sec(8Hz) 0 1 0 : Finish one PECI message transmission every 0.25sec(4Hz) 0 1 1 : Finish one PECI message transmission every 0.5sec(2Hz) 1 0 0 : Finish one PECI message transmission every 1sec(1Hz) 1 0 1 : Finish one PECI message transmission every 2sec(1/2Hz) 1 1 0 : Finish one PECI message transmission every 4sec(1/4Hz)

CR EEh. (SST Device ID Low Byte; Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	SST Device ID Low Byte. (Note 3)

CR EFh. (SST Device ID High Byte; Default 5Ah)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	SST Device ID High Byte. (Note 3)

Note 2: Vendor ID identifies the device from a specific vendor. The PCI SIG or TBA assigns the contents of this value.

Note 3: This value is assigned by vendor and must be exclusive to that vendor and to the device. It will be used in conjunction with the Vendor ID to associate the correct software driver with the sensor.

CR F1h. (SST Address Register; Default 48h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	SST address

CR F2h. (SST Vendor ID Low Byte; Default 50h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	SST Vendor ID Low Byte. (Note 2)

CR F3h. (SST Vendor ID High Byte; Default 10h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	SST Vendor ID High Byte. (Note 2)

CR FEh. (PECI Agent Relative High Byte Temperature Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only	This register shows the retrieved High Byte raw data from PECI interface. When Bank Select (CR E8 bit 3~2) **Bits** **3 2** = 0 0 Agt1RelTemp (High Byte) = 0 1 Agt2RelTemp (High Byte) = 1 0 Agt3RelTemp (High Byte) = 1 1 Agt4RelTemp (High Byte)

CR FFh. (PECI Agent Relative Low ByteTemperature Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only	This register shows the retrieved High Byte raw data from PECI interface. When Bank Select (CR E8 bit 3~2) **Bits** **3 2** = 0 0 Agt1RelTemp (Low Byte) = 0 1 Agt2RelTemp (Low Byte) = 1 0 Agt3RelTemp (Low Byte) = 1 1 Agt4RelTemp (Low Byte)

22. SPECIFICATIONS

22.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNIT
3VCC	Power Supply Voltage (3.3V)	-0.3 to 3.6	V
VI	Input Voltage	-0.3 to 3Vcc+0.3	V
	Input Voltage (5V tolerance)	-0.3 to 5.5	V
TA	Operating Temperature	0 to +70	°C
		-40 to +85	°C
TSTG	Storage Temperature	-55 to +150	°C

Note1: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Note2: Both W83627DHG-P and W83627DHG-PT supports the IC operating temperature from 0℃ to +70℃. Only W83627DHG-PT supports the IC operating temperature from -40℃ to +85℃.

22.2 Hardware Monitor Ratings

(T_a = 0°C to 70°C, V_{DD} = 3.3V ± 5%, V_{SS} = 0V)

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
External Temperature Measurement Accuracy		-3	±1	+3	℃	0℃≦T_a≦70℃

22.3 DC CHARACTERISTICS

(T_a = 0°C to 70°C, V_{DD} = 3.3V ± 5%, V_{SS} = 0V)

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
RTC Battery Quiescent Current	I_{BAT}			2.4	μA	V_{BAT} = 2.5 V CASEOPEN Pull-Up to V_{BAT}
ACPI Stand-by Power Supply Quiescent Current	I_{SB}			2.0	mA	V_{SB} = 3.3 V CASEOPEN Pull-Up to V_{BAT}

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
VCC Quiescent Current	I_{VCC}			25	mA	V_{SB} = 3.3V V_{CC} (AVCC) = 3.3V LRESET = High IOCLK = 48MHz CASEOPEN Pull-Up to V_{BAT}
Vtt Quiescent Current	I_{VTT}			1	mA	V_{SB} = 3.3V V_{CC} (AVCC) = 3.3V V_{TT} = 1.2V LRESET = High IOCLK = 48MHz CASEOPEN Pull-Up to V_{BAT}
I/O_{8t} – TTL–level, bi-directional pin with 8mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = - 8 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O_{12t} – TTL-level, bi-directional pin with 12mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O_{24t} – TTL-level, bi-directional pin with 24mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O_{12tp3} – 3.3V TTL-level, bi-directional pin with 12mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O_{12ts} – TTL–level, Schmitt-trigger, bi-directional pin with 12mA source-sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{CC}=3.3V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O_{24ts} – TTL–level, Schmitt-trigger, bi-directional pin with 24mA source-sink capability						

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{CC}= 3.3V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O_{24tsp3} – 3.3V TTL-level, Schmitt-trigger, bi-directional pin with 24mA source-sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{CC}=3.3V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/OD_{12t} – TTL–level, bi-directional pin and open-drain output with 12mA sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/OD_{16t} – TTL–level, bi-directional pin and open-drain output with 16mA sink capability						

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD_{24t} – TTL–level, bi-directional pin and open-drain output with 24mA sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{12tp3} – 3.3V TTL–level, bi-directional pin and open-drain output with 12mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
$I/OD16_{ts}$ – TTL–level, Schmitt-trigger, bi-directional pin and open-drain output with 16mA sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Hystersis	V_{TH}	0.5	1.2		V	V_{CC}=3.3V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD_{24ts} – TTL level, Schmitt-trigger, bi-directional pin and open-drain output with 24mA sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{CC}=3.3V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
$I/OD12_{cs}$ – CMOS–level, Schmitt-trigger, bi-directional pin and open-drain output with 12mA sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
$I/OD16_{cs}$ – CMOS–level, Schmitt-trigger, bi-directional pin and open-drain output with 16mA sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
I/OD12$_{csd}$ – CMOS–level, Schmitt-trigger, bi-directional pin with internal pulled-down resistor and open-drain output with 12mA sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
I/OD12$_{csu}$ – CMOS–level, Schmitt-trigger, bi-directional pin with internal pulled-up resistor and open-drain output with 12mA sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
O4 – Output pin with 4mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4 mA

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -4 mA
O_8 – Output pin with 8mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -8 mA
O_{12} – Output pin with 12mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
O_{16} – Output pin with 16mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -16 mA
O_{24} – Output pin with 24mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
O_{12p3} – 3.3V output pin with 12mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
O_{24p3} – 3.3V output pin with 24mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
OD_{12} – Open-drain output pin with 12mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
OD_{24} – Open-drain output pin with 24mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
OD_{12p3} – 3.3V open-drain output pin with 12mA sink capability						

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
In_t – TTL-level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
In_{tp3} – 3.3V TTL-level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
In_{td} – TTL-level input pin with internal pulled-down resistor						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
In_{tu} – TTL-level input pin with internal pulled-up resistor						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
In_{ts} – TTL–level, Schmitt-trigger input pin						

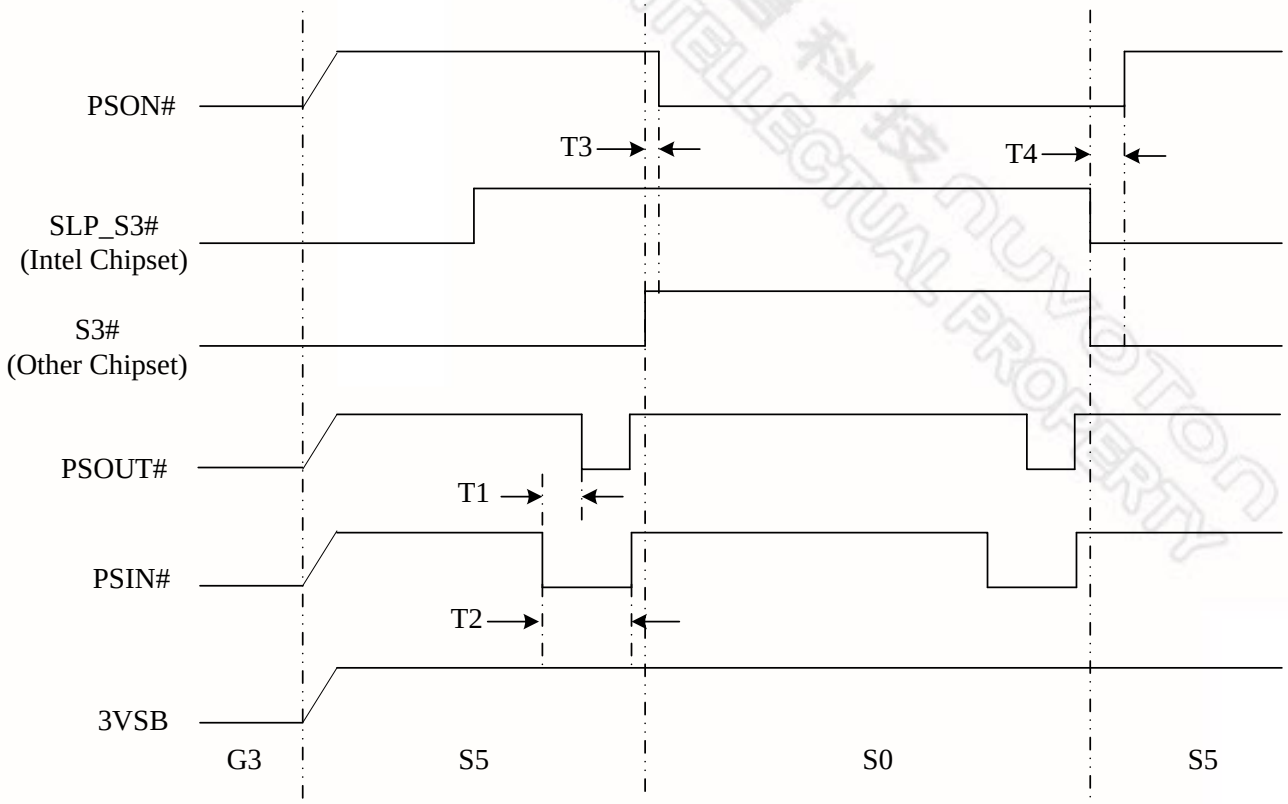
PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
In_{tsp3} – 3.3 V TTL-level, Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
In_{c} – CMOS-level input pin						
Input Low Voltage	VIL			0.3 V_{CC}	V	
Input High Voltage	VIH	0.7 V_{CC}			V	
Input High Leakage	ILIH			+10	µA	VIN = V_{CC} = 3.3V
Input Low Leakage	ILIL			-10	µA	VIN = 0 V
In_{cd} – CMOS-level input pin with internal pulled-down resistor						
Input Low Voltage	V_{IL}			0.3 V_{CC}	V	
Input High Voltage	V_{IH}	0.7 V_{CC}			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = V_{CC} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
Input Low Voltage	V_{IL}			0.3 V_{CC}	V	

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
In_{cu} – CMOS-level input pin with internal pulled-up resistor						
Input High Voltage	V_{IH}	0.7 V_{CC}			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = V_{CC} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
In_{cs} – CMOS–level, Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	1.3	1.5	1.7	V	V_{CC} = 3.3V
Hystersis	V_{TH}	1.5	2		V	V_{CC} = 3.3V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
In_{csu} – CMOS–level, Schmitt-trigger input pin with internal pulled-up resistor						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
AOUT – Analog output						
		N.A.				
IN_{V1S} – VID input pin for INTEL® VRM10.0, and VRM11 design						
Input Low Voltage	V_{IL}			0.4	V	
Input High Voltage	V_{IH}	0.6			V	
IN_{V2S} – VID input pin for AMD™VRM design						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	1.4			V	

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
I/O_{V3} – Bi-direction pin with source capability of 6 mA and sink capability of 1 mA for INTEL® PECI						
Input Low Voltage	V_{IL}	0.275Vtt		0.5Vtt	V	
Input High Voltage	V_{IH}	0.55Vtt		0.725Vtt	V	
Output Low Voltage	V_{OL}			0.25Vtt	V	
Output High Voltage	V_{OH}	0.75Vtt			V	
Hysterisis	V_{Hys}	0.1Vtt			V	
I/O_{V4} – Bi-direction pin with source capability of 6 mA and sink capability of 1 mA for INTEL® SST						
Input Low Threshold Voltage	Vt-	0.4		0.65	V	V_{CC} = 1.5 V
Input High Threshold Voltage	Vt+	0.75		1.1	V	V_{CC} = 1.5 V
Input High Leakage	I_{LIH}			+10	μA	$V_{IN} = V_{CC}$
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
Hysteresis	V_{TH}	0.15			V	V_{CC} = 1.5 V

22.4 AC CHARACTERISTICS

22.4.1 Power On / Off Timing

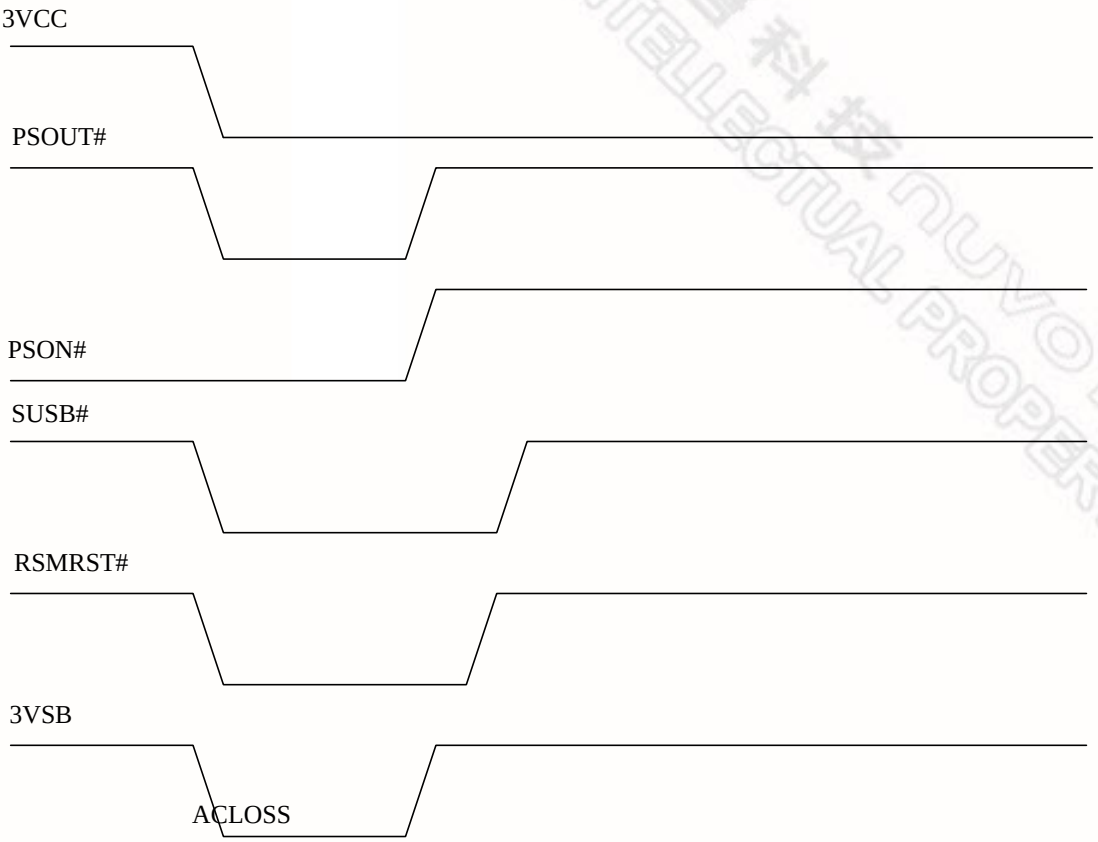


	T1	T2	T3	T4
IDEAL TIMING (SEC)	64ms	Over 64ms at least	< 10ns	32ms

22.4.2 AC Power Failure Resume Timing

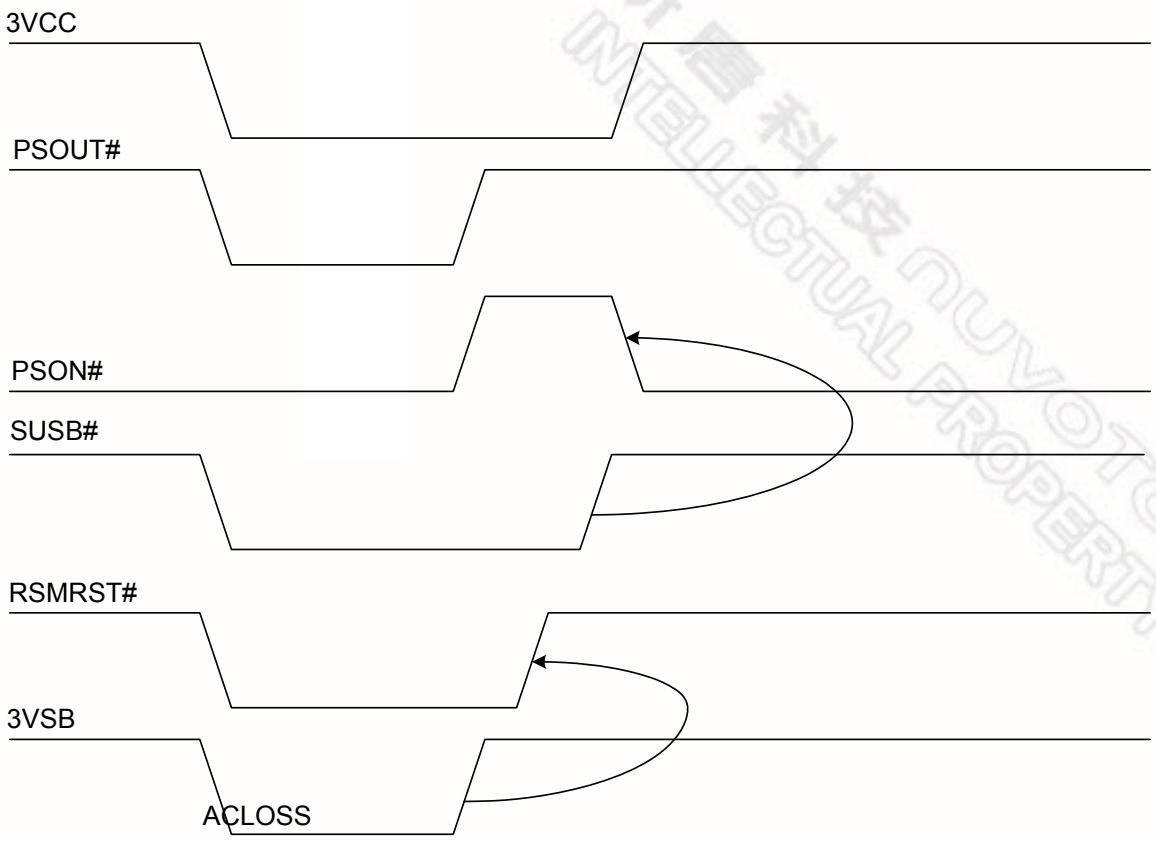
2. Logical Device A, CR [E4h] bits [6:5] =00 means “OFF” state

(“OFF” means the system is always turned off after the AC power loss recovered.)



3. Logical Device A, CR [E4h] bits [6:5]=01 means “ON” state.

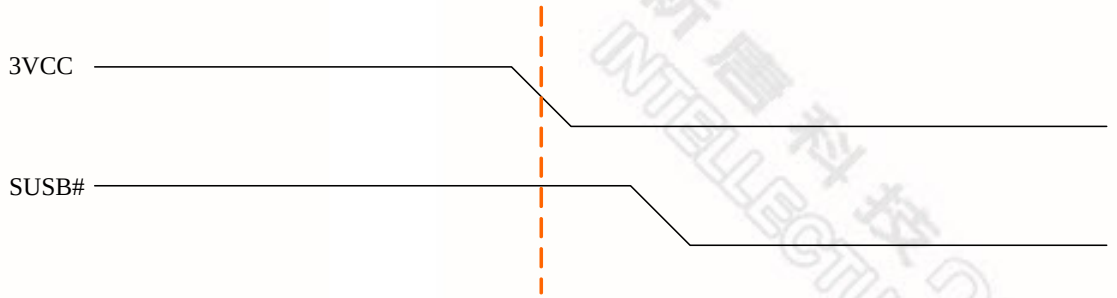
(“ON” means the system is always turned on after AC power loss recovered.)



**** What's the definition of former state at AC power failure?**

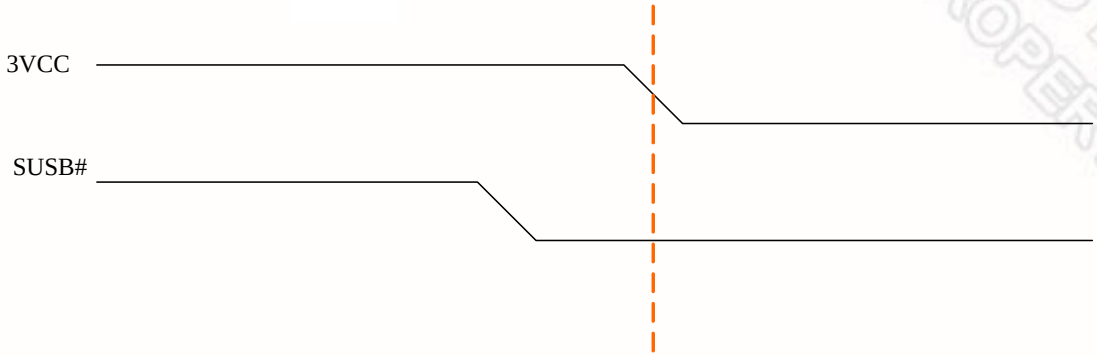
1) The previous state is "ON"

3VCC falls to 2.6V and SUSB# keeps at VIH 2.0V



2) The previous state is "OFF"

3VCC falls to 2.6V and SUSB# keeps at VIL 0.8V



To ensure that VCC does not fall faster than VSB in various ATX Power Supplies, the W83627DHG-P adds the option of "user define mode" for the pre-defined state before AC power failure. BIOS can set the pre-defined state for the system to be "On" or "Off". According to this setting, the system chooses the state after the AC power recovery.

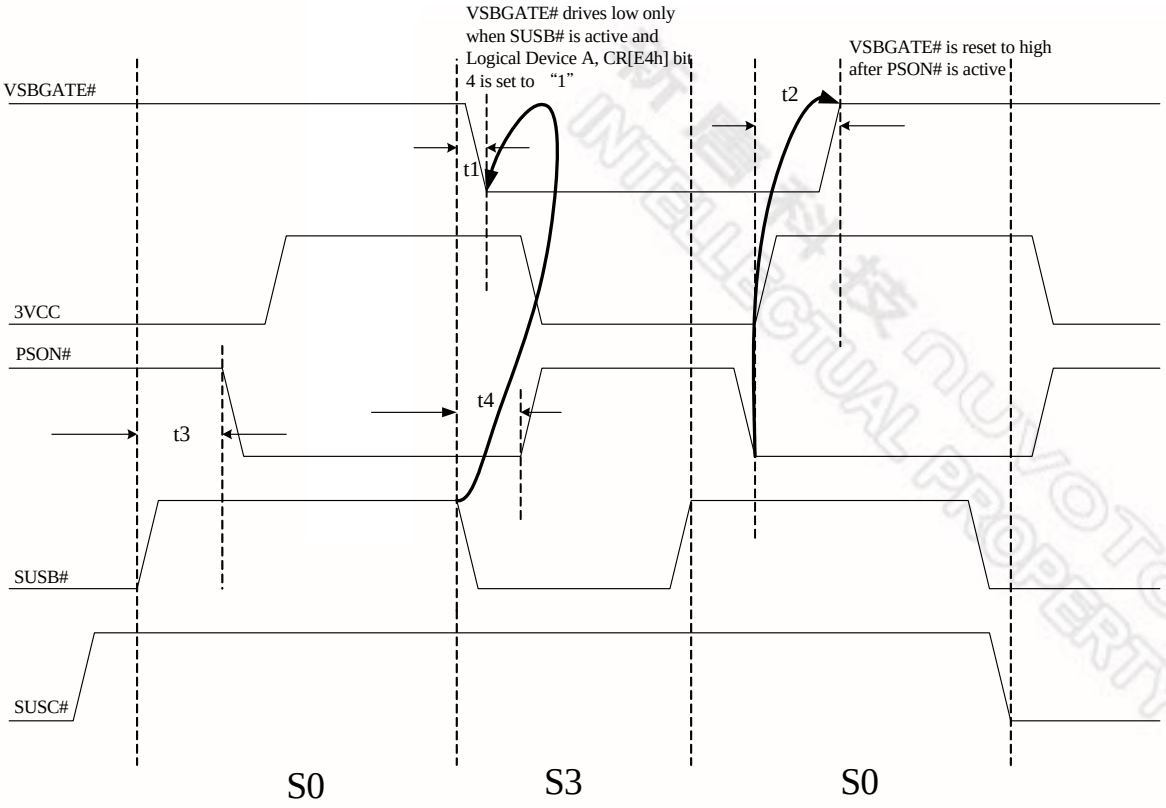
Logical Device A, CR E4h

BIT	READ / WRITE	DESCRIPTION
6~5	R / W	Power-loss control bits => (**VBAT**) 00: System always turns off when it returns from power-loss state. 01: System always turns on when it returns from power-loss state. 10: System turns off / on when it returns from power-loss state depending on the state before the power loss. 11: User defines the state before the power loss.(The previous state is set at CRE6[4])

Logical Device A, CR E6h

BIT	READ / WRITE	DESCRIPTION
4	R / W	Power loss Last State Flag. **(VBAT)** 0: ON 1: OFF

22.4.3 VSBGATE# Timing

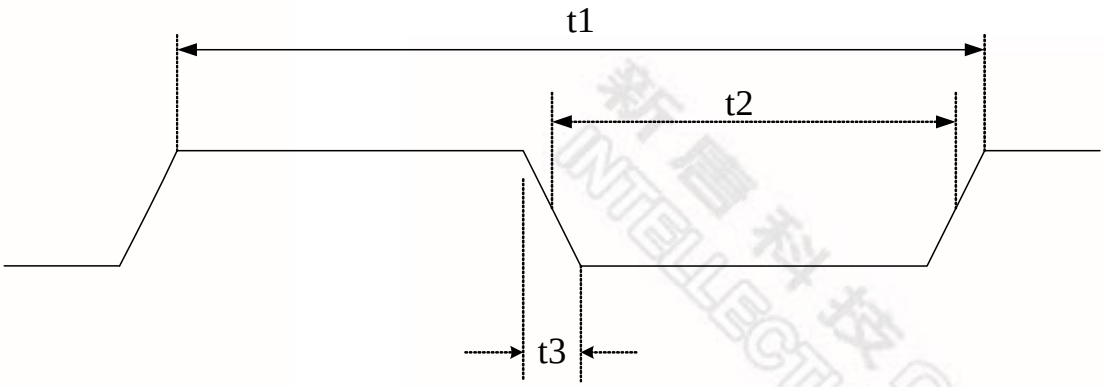


SYMBOL	PARAMETER	MIN	MAX	UNIT
t1	SUSB# active to VSBGATE# active	0	80	nS
t2	PSON# active to VSBGATE# inactive	90	142	mS
t3	SUSB# inactive to PSON# active	0	80	nS
t4	SUSB# active to PSON# inactive	28	39	mS

Note. The values above the worst-case results of R&D simulation

22.4.4 Clock Input Timing

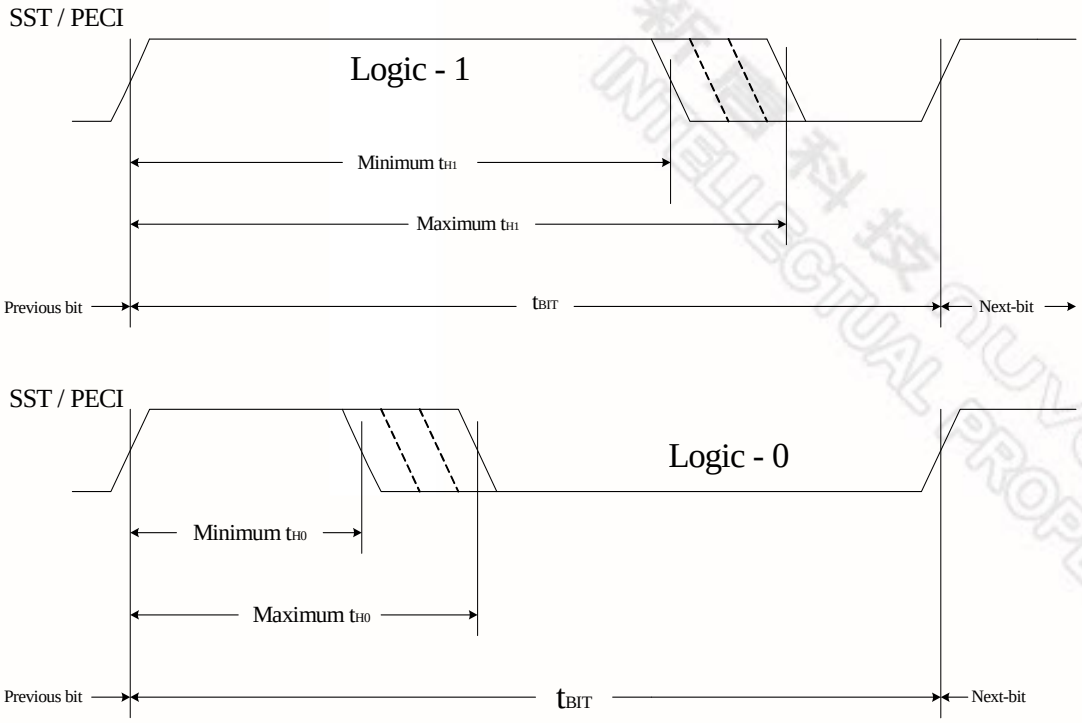
PARAMETER	48MHZ / 24MHZ		UNIT
	MIN	MAX	
Cycle to cycle jitter		300/500	ps
Duty cycle	45	55	%



PARAMETER	DESCRIPTION	48MHZ / 24MHZ			UNIT
		MIN	TYP	MAX	
t1	Clock cycle time		20.8 / 41.7		ns
t2	Clock high time/low time	8.094 / 19	10 / 21		ns
t3	Clock rising time/falling time (0.4V~2.4V)			3	ns

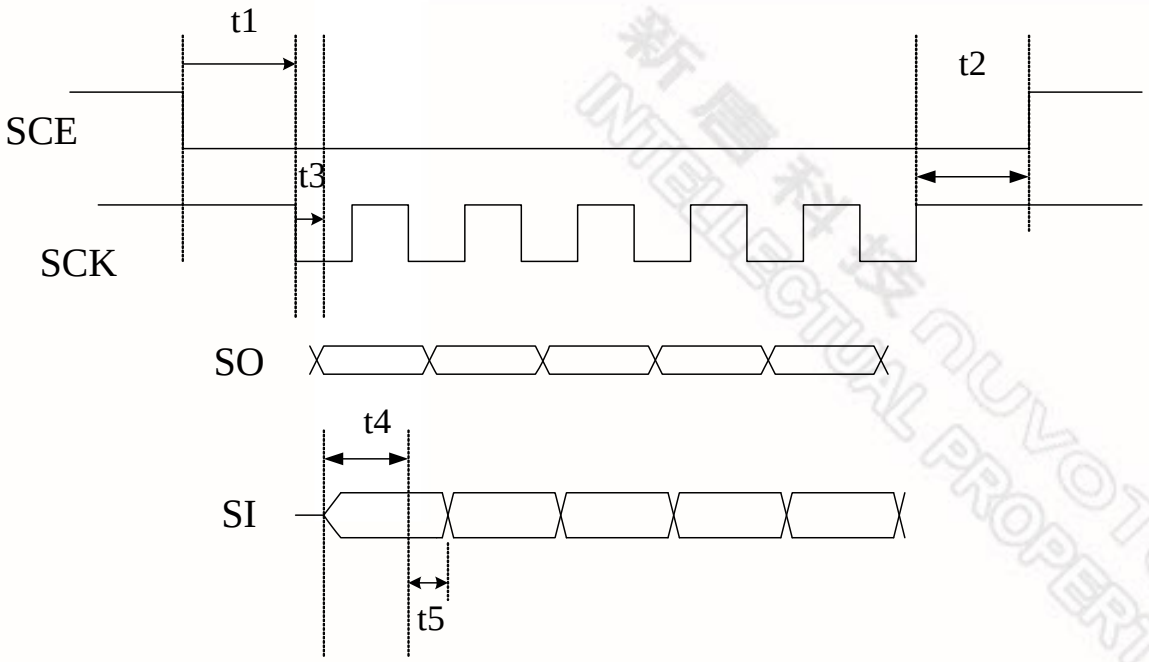
Note: t2 measure from the voltage (VIH+VIL)/2=(2.0+0.8)/2=1.4V

22.4.5 PECI and SST Timing



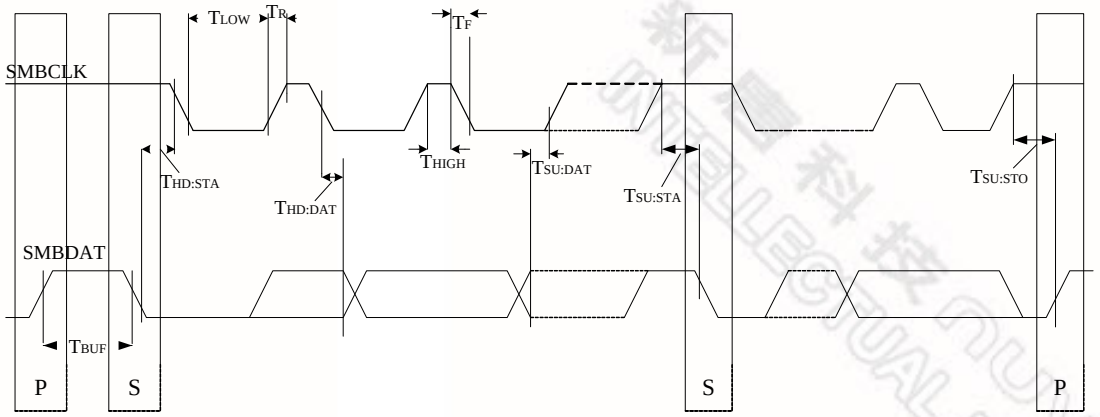
SYMBOL		MIN	TYP	MAX	UNITS
t_{BIT}	Client	0.495		500	μs
	Originator	0.495		250	
t_{H1}		0.6	3/4	0.8	× t_{BIT}
t_{H0}		0.2	1/4	0.4	× t_{BIT}

22.4.6 SPI Timing



DESCRIPTION	SYMBOL	MIN	TYP	MAX
Enable to first clock falling	t1	25ns	-	35ns
Disable after last clock rising	t2	40ns	-	50ns
Output hold time	t3	-	-	5ns
Input setup time	t4	5ns	-	-
Input hold time	t5	6ns	-	-

22.4.7 SMBus Timing



SYMBOL	PARAMETER	MIN.	MAX.:	UNITS
T_{BUF}	Bus Free Time between Stop and Start Condition	4.7	-	uS
$T_{HD:STA}$	Hold time after (Repeated) Start Condition. After this period, the first clock is generated	4.0	-	uS
$T_{SU:STA}$	Repeated Start Condition setup time	4.7	-	uS
$T_{SU:STO}$	Stop Condition setup time	4.0	-	uS
$T_{HD:DAT}$	Data hold time	300	-	nS
$T_{SU:DAT}$	Data setup time	250	-	nS
T_{LOW}	Clock low period	4.7	-	uS
T_{HIGH}	Clock high period	4.0	50	uS
T_F	Clock/Data Falling Time	-	300	nS
T_R	Clock/Data Rising Time	-	1000	nS

22.4.8 Floppy Disk Drive Timing

FDC: Data rate = 1MB, 500KB, 300KB, 250KB/sec.

PARAMETER	SYM.	MIN.	TYP. (NOTE 1)	MAX.	UNIT
DIR# setup time to STEP#	TDST	1.0/1.6 /2.0/4.0			µS
DIR# hold time from STEP#	TSTD	24/40 /48/96			µS
STEP# pulse width	TSTP	6.8/11.5	7/11.7	7.2/11.9	µS

PARAMETER	SYM.	MIN.	TYP. (NOTE 1)	MAX.	UNIT
		/13.8/27.8	/14/28	/14.2/28.2	
STEP# cycle width	TSC	NOTE 2	NOTE 2	NOTE 2	mS
INDEX# pulse width	TIDX	125/250 /417/500			nS
RDATA# pulse width	TRD	40			nS
WD# pulse width	TWD	100/185 /225/475	125/210 /250/500	150/235 /275/525	nS

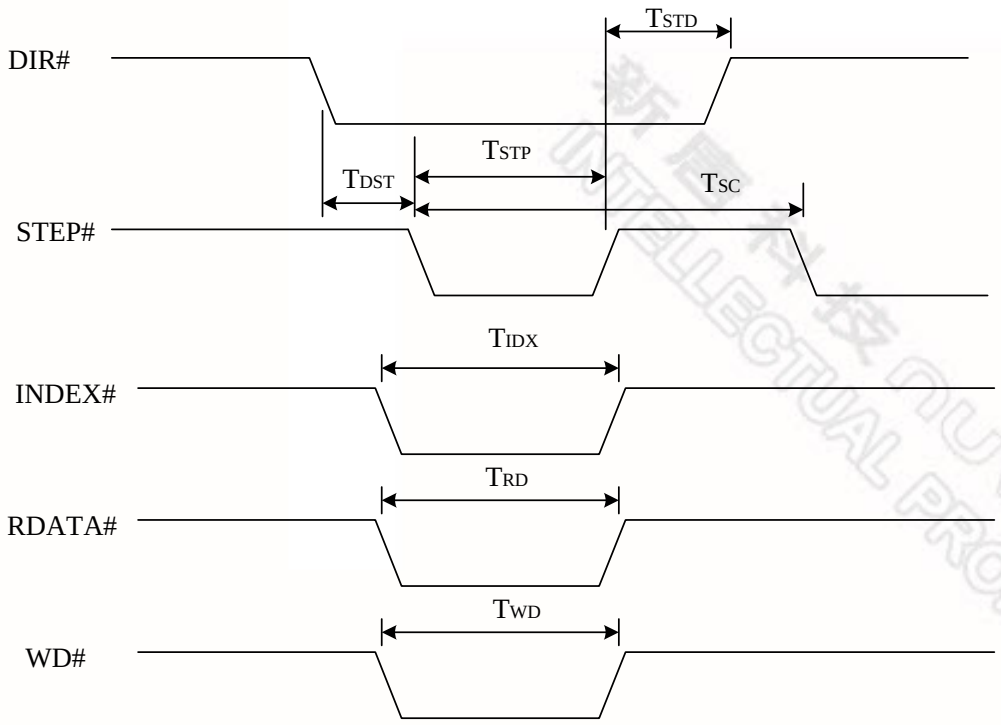
Notes:

1. Typical values for T = 25°C and normal supply voltage.
2. Programmable from 0.5 mS through 32 mS as described in step rate table. (Please refer to the description of the SPECIFY command set.)

Step Rate Table

DATA RATE / SRT	1MB/S	500KB/S	300KB/S	250KB/S
0	8	16	26.7	32
1	7.5	15	25	30
…	…	…	…	…
E	1.0	2	3.33	4
F	0.5	1	1.67	2

Floppy Disk Driving Timing

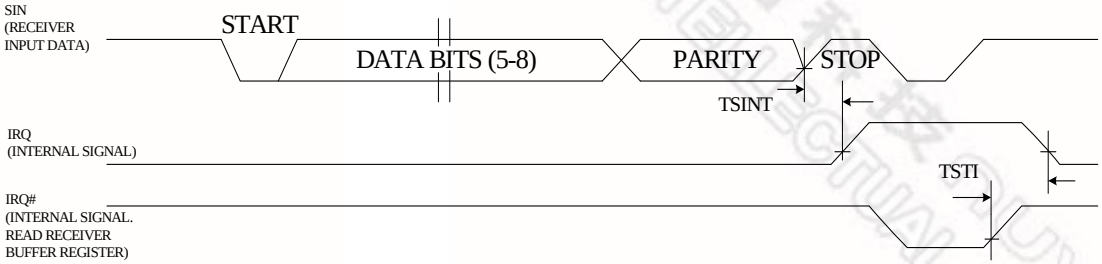


22.4.9 UART/Parallel Port

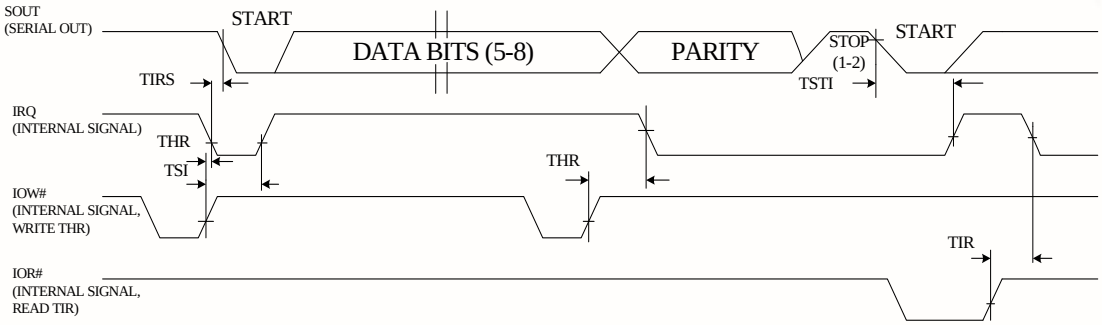
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Delay from Stop to Set Interrupt	TSINT		9/16		Baud Rate
Delay from $\overline{IOR}$ Reset Interrupt	TRINT		9	1000	nS
Delay from Initial IRQ Reset to Transmit Start	TIRS		1/16	8/16	Baud Rate
Delay from to Reset interrupt	THR			175	nS
Delay from Initial $\overline{IOW}$ to interrupt	TSI		9/16	16/16	Baud Rate
Delay from Stop to Set Interrupt	TSTI			8/16	Baud Rate
Delay from $\overline{IOR}$ to Reset Interrupt	TIR		8	250	nS
Delay from $\overline{IOR}$ to Output	TMWO		6	200	nS
Set Interrupt Delay from Modem Input	TSIM		18	250	nS
Reset Interrupt Delay from $\overline{IOR}$	TRIM		9	250	nS
Baud Divisor	N	100 pF Loading		2^{16}-1	

UART Receiver Timing

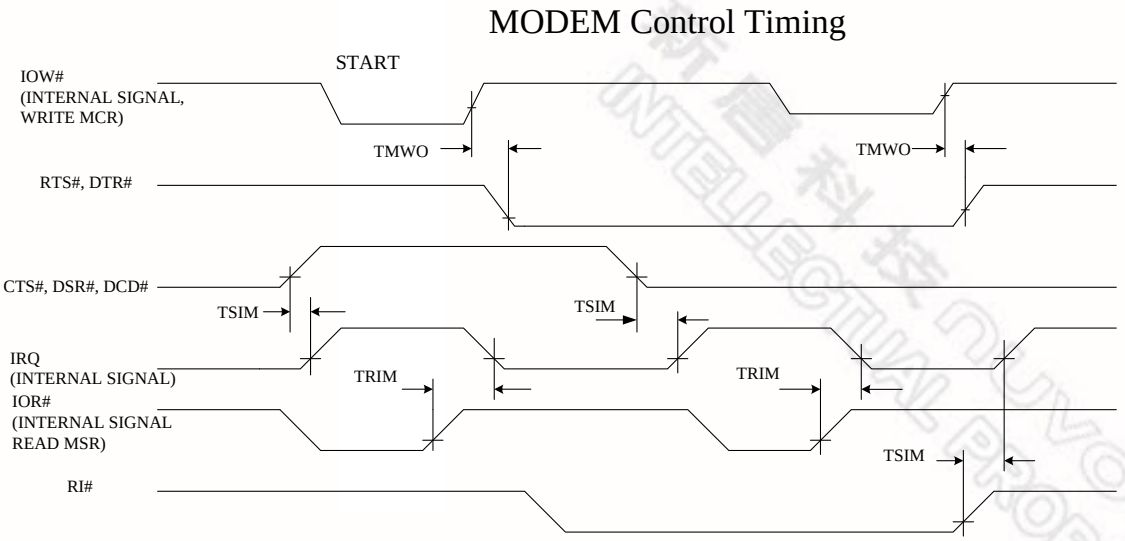
Receiver Timing



UART Transmitter Timing



22.4.9.1. Modem Control Timing

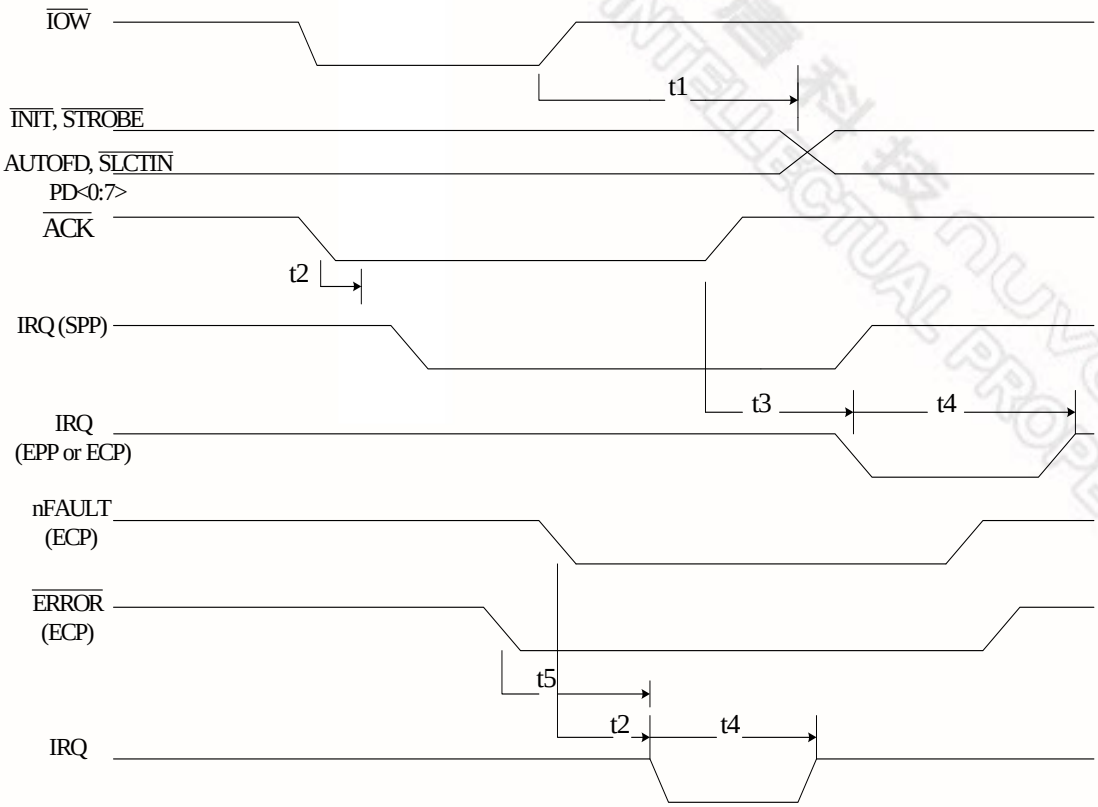


22.4.10 Parallel Port Mode Parameters

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
PD0-7, $\overline{\text{INDEX}}$, $\overline{\text{STROBE}}$, $\overline{\text{AUTOFD}}$ Delay from $\overline{\text{IOW}}$	t1			100	nS
IRQ Delay from $\overline{\text{ACK}}$, nFAULT	t2			60	nS
IRQ Delay from $\overline{\text{IOW}}$	t3			105	nS
IRQ Active Low in ECP and EPP Modes	t4	200		300	nS
$\overline{\text{ERROR}}$ Active to IRQ Active	t5			105	nS
PARAMETER	**SYM.**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
PD0-7, $\overline{\text{INDEX}}$, $\overline{\text{STROBE}}$, $\overline{\text{AUTOFD}}$ Delay from $\overline{\text{IOW}}$	t1			100	nS
IRQ Delay from $\overline{\text{ACK}}$, nFAULT	t2			60	nS
IRQ Delay from $\overline{\text{IOW}}$	t3			105	nS
IRQ Active Low in ECP and EPP Modes	t4	200		300	nS
$\overline{\text{ERROR}}$ Active to IRQ Active	t5			105	nS

22.4.11Parallel Port

22.4.11.1. Parallel Port Timing



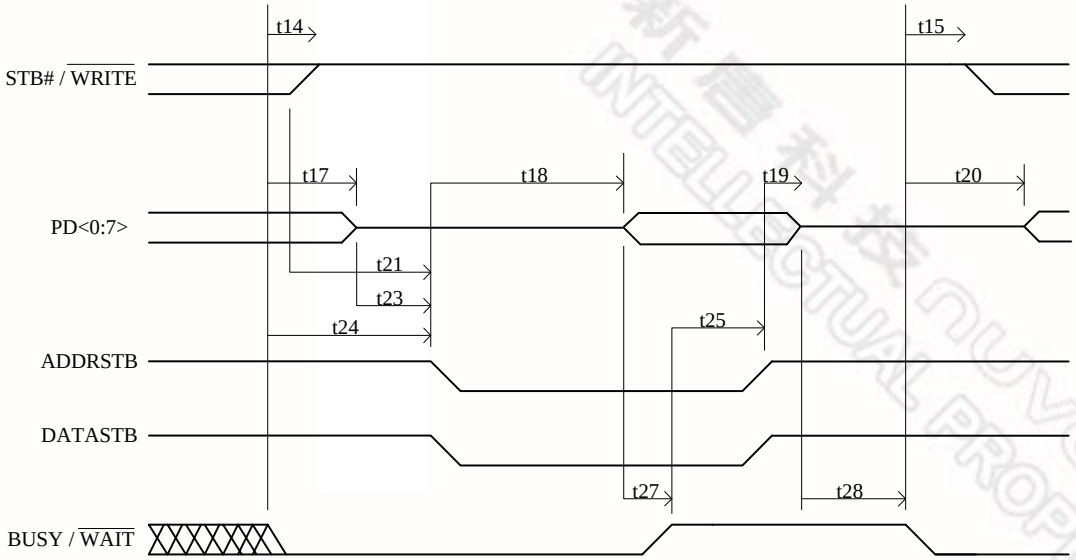
22.4.11.2. EPP Data or Address Read Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
WAIT Asserted to WRITE Deasserted	t14	0	185	nS
Deasserted to WRITE Modified	t15	60	190	nS
WAIT Asserted to PD Hi-Z	t17	60	180	nS
Command Asserted to PD Valid	t18	0		nS
Command Deasserted to PD Hi-Z	t19	0		nS
WAIT Deasserted to PD Drive	t20	60	190	nS
WRITE Deasserted to Command	t21	1		nS
PBDIR Set to Command	t22	0	20	nS
PD Hi-Z to Command Asserted	t23	0	30	nS
Asserted to Command Asserted	t24	0	195	nS
WAIT Deasserted to Command Deasserted	t25	60	180	nS

PARAMETER	SYM.	MIN.	MAX.	UNIT
Time out	t26	10	12	nS
PD Valid to $\overline{WAIT}$ Deasserted	t27	0		nS
PD Hi-Z to $\overline{WAIT}$ Deasserted	t28	0		μS
PARAMETER	SYM.	MIN.	MAX.	UNIT
Ax Valid to $\overline{IOR}$ Asserted	t1	40		nS
IOCHRDY Deasserted to $\overline{IOR}$ Deasserted	t2	0		nS
$\overline{IOR}$ Deasserted to Ax Valid	t3	10	10	nS
$\overline{IOR}$ Deasserted to $\overline{IOW}$ or $\overline{IOR}$ Asserted	t4	40		
$\overline{IOR}$ Asserted to IOCHRDY Asserted	t5	0	24	nS
PD Valid to SD Valid	t6	0	75	nS
$\overline{IOR}$ Deasserted to SD Hi-Z (Hold Time)	t7	0	40	μS
SD Valid to IOCHRDY Deasserted	t8	0	85	nS
$\overline{WAIT}$ Deasserted to IOCHRDY Deasserted	t9	60	160	nS
PD Hi-Z to PDBIR Set	t10	0		nS
$\overline{WRITE}$ Deasserted to $\overline{IOR}$ Asserted	t13	0		nS
$\overline{WAIT}$ Asserted to $\overline{WRITE}$ Deasserted	t14	0	185	nS
Deasserted to $\overline{WRITE}$ Modified	t15	60	190	nS
$\overline{IOR}$ Asserted to PD Hi-Z	t16	0	50	nS
$\overline{WAIT}$ Asserted to PD Hi-Z	t17	60	180	nS
Command Asserted to PD Valid	t18	0		nS
Command Deasserted to PD Hi-Z	t19	0		nS
$\overline{WAIT}$ Deasserted to PD Drive	t20	60	190	nS
$\overline{WRITE}$ Deasserted to Command	t21	1		nS
PBDIR Set to Command	t22	0	20	nS
PD Hi-Z to Command Asserted	t23	0	30	nS
Asserted to Command Asserted	t24	0	195	nS
$\overline{WAIT}$ Deasserted to Command Deasserted	t25	60	180	nS
Time out	t26	10	12	nS
PD Valid to $\overline{WAIT}$ Deasserted	t27	0		nS
PD Hi-Z to $\overline{WAIT}$ Deasserted	t28	0		μS

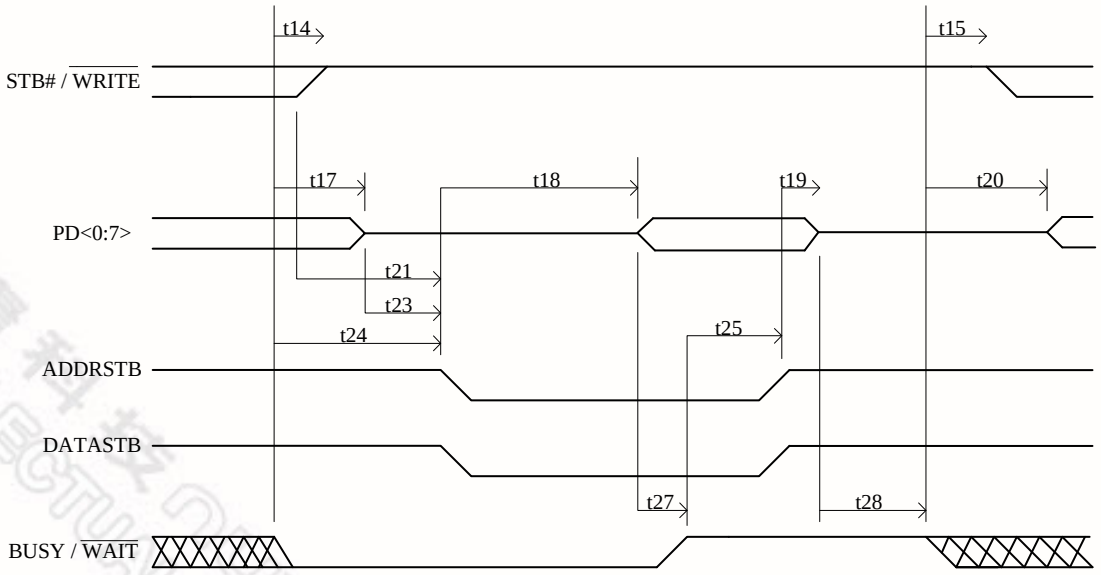
22.4.11.3. EPP Data or Address Read Cycle (EPP Version 1.9)

EPP Data or Address Read Cycle (EPP Version 1.9)



22.4.11.4. EPP Data or Address Read Cycle (EPP Version 1.7)

EPP Data or Address Read Cycle (EPP Version 1.7)



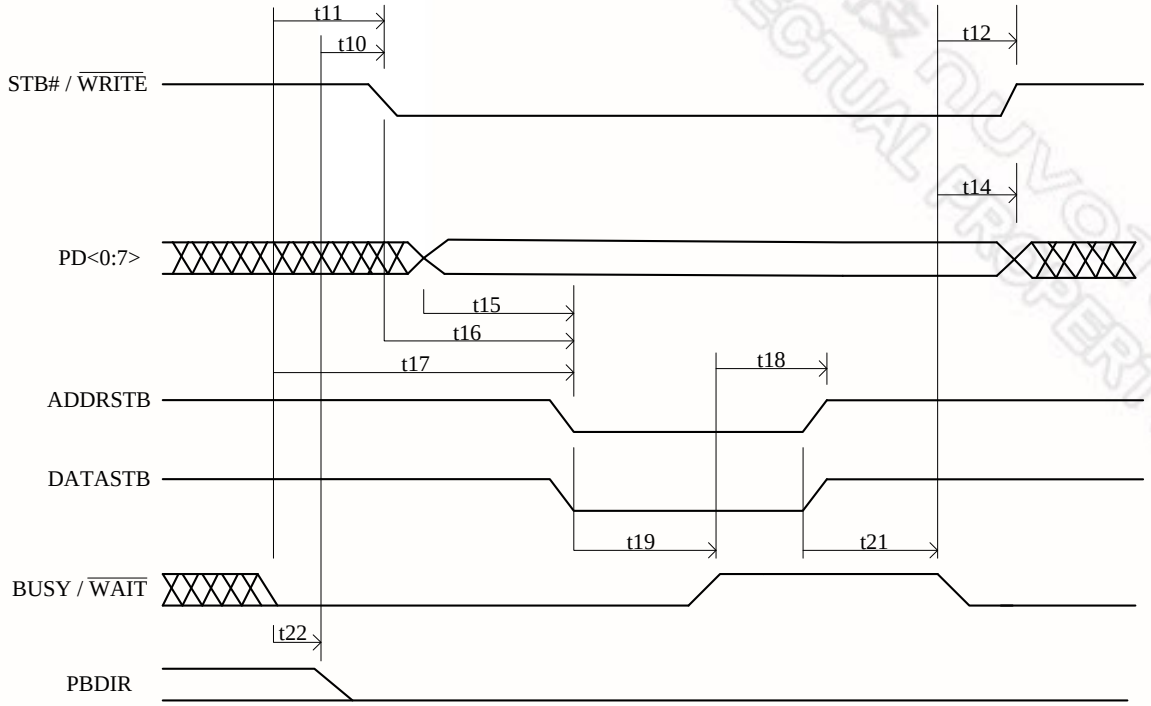
22.4.11.5. EPP Data or Address Write Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
PBDIR Low to $\overline{\text{WRITE}}$ Asserted	t10	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Asserted	t11	60	185	nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Change	t12	60	185	nS
$\overline{\text{WAIT}}$ Asserted to PD Invalid	t14	0		nS
PD Invalid to Command Asserted	t15	10		nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t17	60	210	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t18	60	190	nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t19	0	10	μS
Time out	t20	10	12	μS
Command Deasserted to $\overline{\text{WAIT}}$ Asserted	t21	0		nS
PARAMETER	**SYM.**	**MIN.**	**MAX.**	**UNIT**
Ax Valid to $\overline{\text{IOW}}$ Asserted	t1	40		nS
SD Valid to Asserted	t2	10		nS
$\overline{\text{IOW}}$ Deasserted to Ax Invalid	t3	10		nS
$\overline{\text{WAIT}}$ Deasserted to IOCHRDY Deasserted	t4	0		nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t5	10		nS
$\overline{\text{IOW}}$ Deasserted to $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ Asserted	t6	40		nS
IOCHRDY Deasserted to $\overline{\text{IOW}}$ Deasserted	t7	0	24	nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t8	60	160	nS
$\overline{\text{IOW}}$ Asserted to $\overline{\text{WAIT}}$ Asserted	t9	0	70	nS
PBDIR Low to $\overline{\text{WRITE}}$ Asserted	t10	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Asserted	t11	60	185	nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Change	t12	60	185	nS
$\overline{\text{IOW}}$ Asserted to PD Valid	t13	0	50	nS
$\overline{\text{WAIT}}$ Asserted to PD Invalid	t14	0		nS
PD Invalid to Command Asserted	t15	10		nS
$\overline{\text{IOW}}$ to Command Asserted	t16	5	35	nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t17	60	210	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t18	60	190	nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t19	0	10	μS
Time out	t20	10	12	μS
Command Deasserted to $\overline{\text{WAIT}}$ Asserted	t21	0		nS

PARAMETER	SYM.	MIN.	MAX.	UNIT
$\overline{IOW}$ Deasserted to $\overline{WRITE}$ Deasserted and PD invalid	t22	0		nS
$\overline{WRITE}$ to Command Asserted	t16	5	35	nS

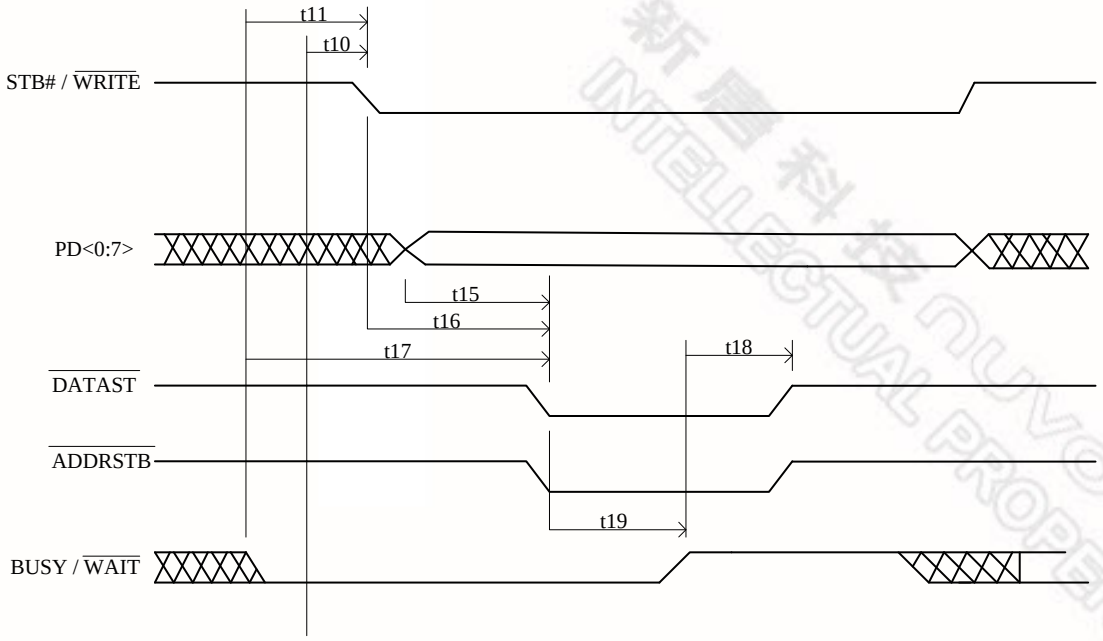
22.4.11.6. EPP Data or Address Write Cycle (EPP Version 1.9)

EPP Data or Address Write Cycle (EPP Version 1.9)



22.4.11.7. EPP Data or Address Write Cycle (EPP Version 1.7)

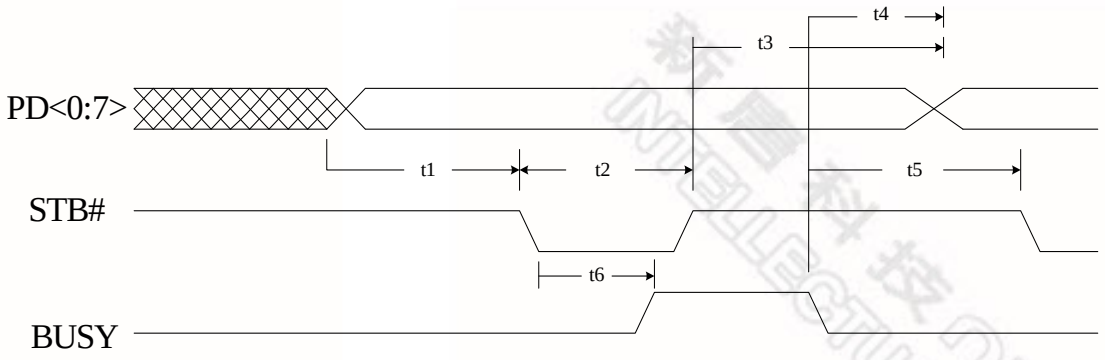
EPP Data or Address Write Cycle (EPP Version 1.7)



22.4.11.8. Parallel Port FIFO Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DATA Valid to nSTROBE Active	t1	600		nS
nSTROBE Active Pulse Width	t2	600		nS
DATA Hold from nSTROBE Inactive	t3	450		nS
BUSY Inactive to PD Inactive	t4	80		nS
BUSY Inactive to nSTROBE Active	t5	680		nS
nSTROBE Active to BUSY Active	t6		500	nS

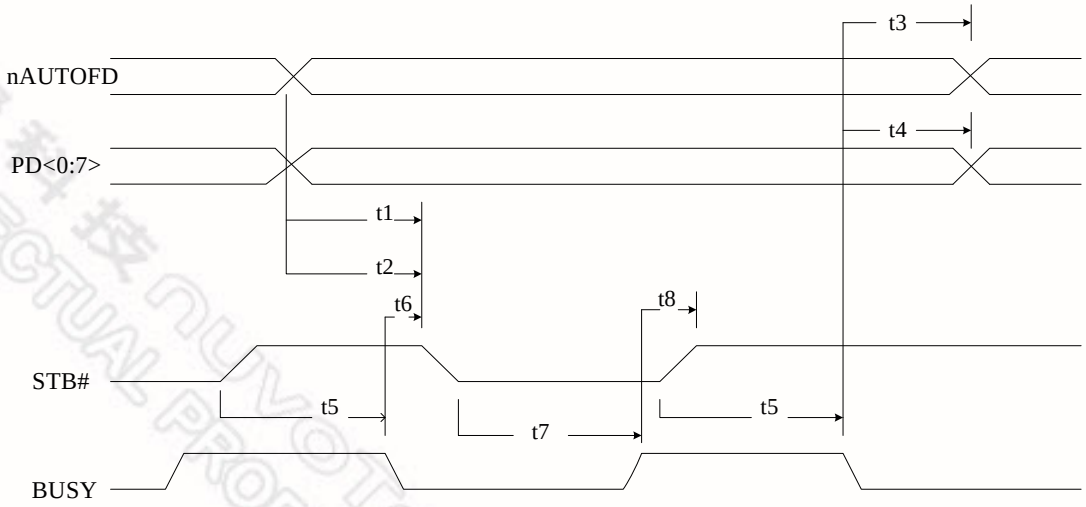
22.4.11.9. Parallel FIFO Timing



22.4.11.10. ECP Parallel Port Forward Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
nAUTOFD Valid to nSTROBE Asserted	t1	0	60	nS
PD Valid to nSTROBE Asserted	t2	0	60	nS
BUSY Deasserted to nAUTOFD Changed	t3	80	180	nS
BUSY Deasserted to PD Changed	t4	80	180	nS
nSTROBE Deasserted to BUSY Deasserted	t5	0		nS
BUSY Deasserted to nSTROBE Asserted	t6	80	200	nS
nSTROBE Asserted to BUSY Asserted	t7	0		nS
BUSY Asserted to nSTROBE Deasserted	t8	80	180	nS

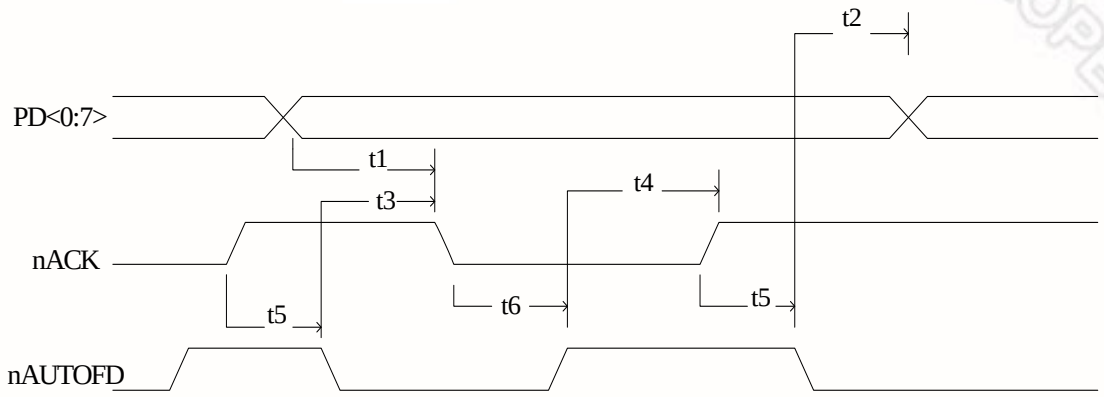
22.4.11.11. ECP Parallel Port Forward Timing



22.4.11.12. ECP Parallel Port Reverse Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
PD Valid to nACK Asserted	t1	0		nS
nAUTOFD Deasserted to PD Changed	t2	0		nS
nAUTOFD Asserted to nACK Asserted	t3	0		nS
nAUTOFD Deasserted to nACK Deasserted	t4	0		nS
nACK Deasserted to nAUTOFD Asserted	t5	80	200	nS
PD Changed to nAUTOFD Deasserted	t6	80	200	nS

22.4.11.13. ECP Parallel Port Reverse Timing

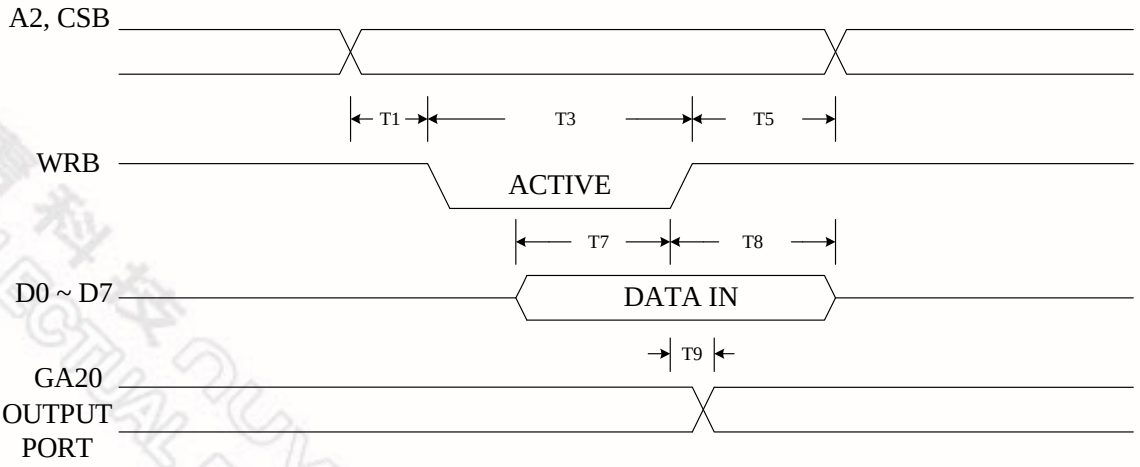


22.4.12KBC Timing Parameters

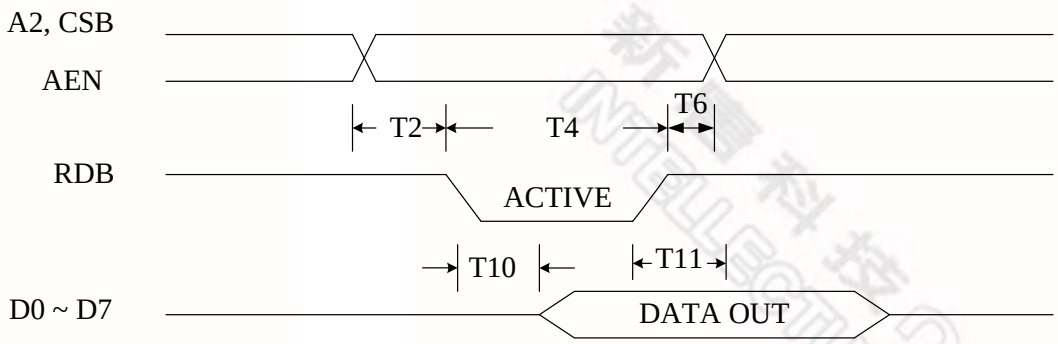
SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T1	Address Setup Time from WRB	0		nS
T2	Address Setup Time from RDB	0		nS
T3	WRB Strobe Width	20		nS
T4	RDB Strobe Width	20		nS
T5	Address Hold Time from WRB	0		nS
T6	Address Hold Time from RDB	0		nS
T7	Data Setup Time	50		nS
T8	Data Hold Time	0		nS
T9	Gate Delay Time from WRB	10	30	nS
T10	RDB to Drive Data Delay		40	nS

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T11	RDB to Floating Data Delay	0	20	nS
T12	Data Valid After Clock Falling (SEND)		4	μS
T13	K/B Clock Period	20		μS
T14	K/B Clock Pulse Width	10		μS
T15	Data Valid Before Clock Falling (RECEIVE)	4		μS
T16	K/B ACK After Finish Receiving	20		μS
T19	Transmit Timeout		2	mS
T20	Data Valid Hold Time	0		μS
T21	Input Clock Period (6–16 Mhz)	63	167	nS
T22	Duration of CLK inactive	30	50	μS
T23	Duration of CLK active	30	50	μS
T24	Time from inactive CLK transition, used to time when the auxiliary device sample DATA	5	25	μS
T25	Time of inhibit mode	100	300	μS
T26	Time from rising edge of CLK to DATA transition	5	T28-5	μS
T27	Duration of CLK inactive	30	50	μS
T28	Duration of CLK active	30	50	μS
T29	Time from DATA transition to falling edge of CLK	5	25	μS

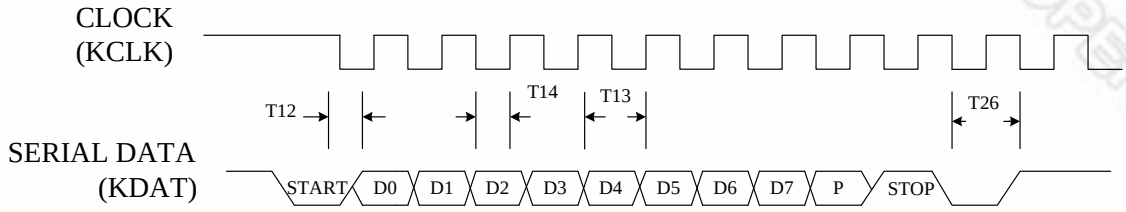
22.4.12.1. Writing Cycle Timing



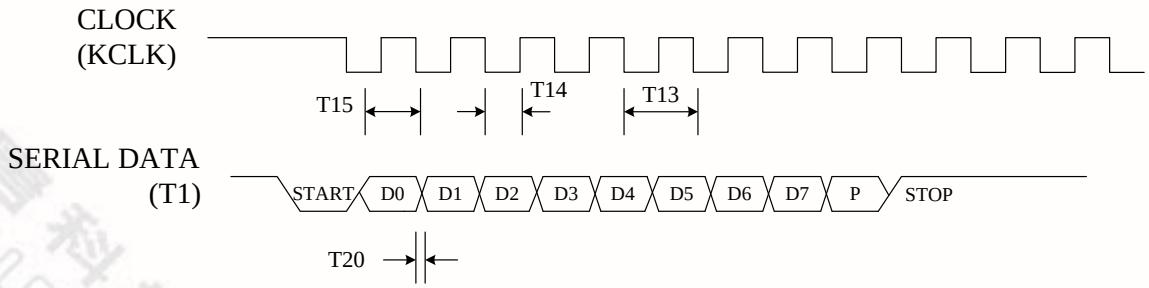
22.4.12.2. Read Cycle Timing



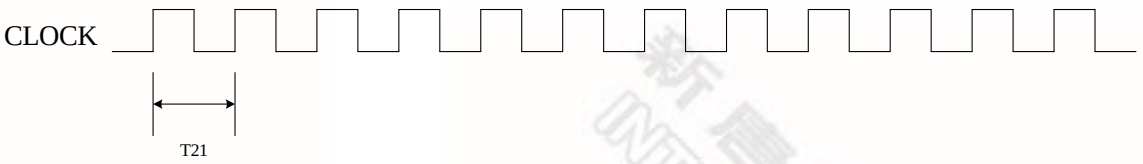
22.4.12.3. Send Data to K/B



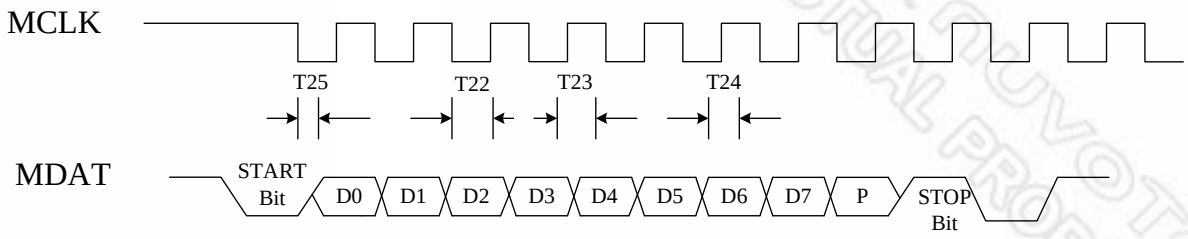
22.4.12.4. Receive Data from K/B



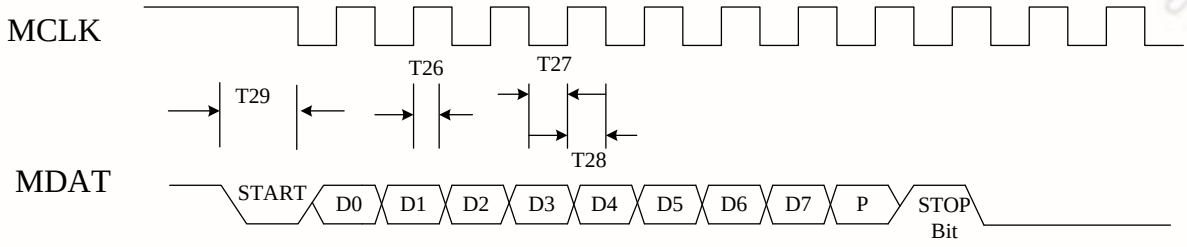
22.4.12.5. Input Clock



22.4.12.6. Send Data to Mouse



22.4.12.7. Receive Data from Mouse



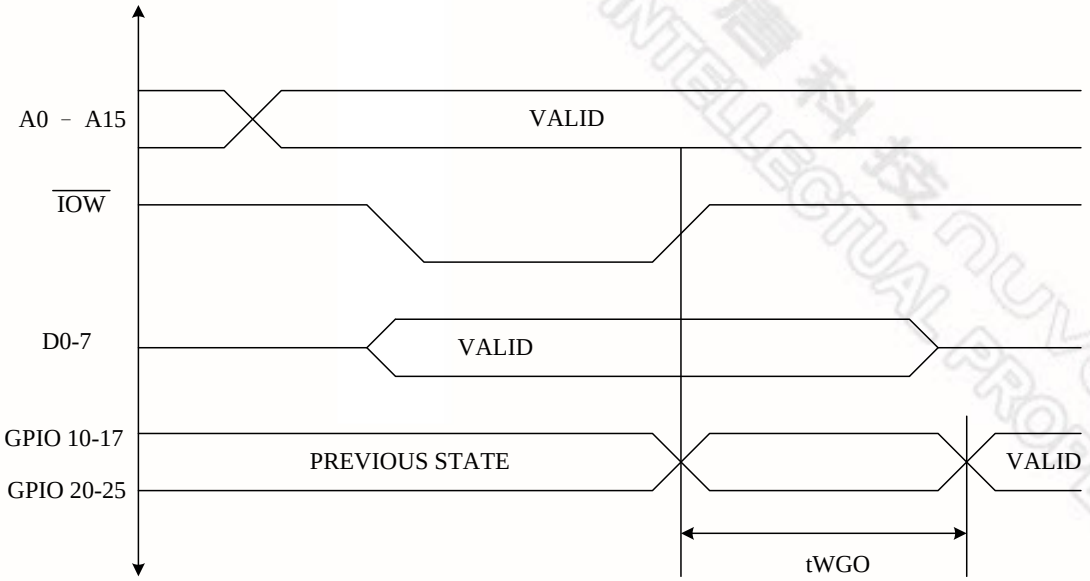
22.4.13 GPIO Timing Parameters

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WGO}	Write data to GPIO update		300(Note 1)	ns
t_{SWP}	SWITCH pulse width	16		msec

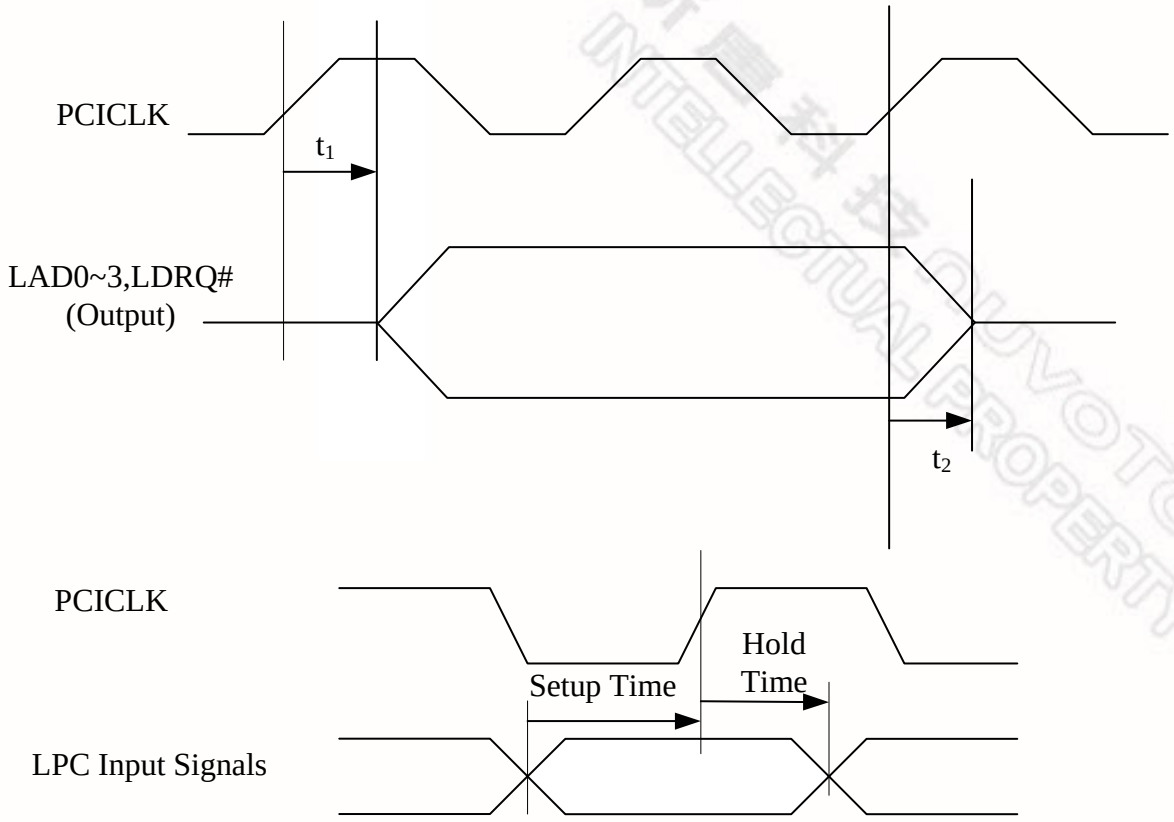
Note: Refer to Microprocessor Interface Timing for Read Timing.

22.4.13.1. GPIO Write Timing

GPIO Write Timing diagram



22.5 LPC Timing

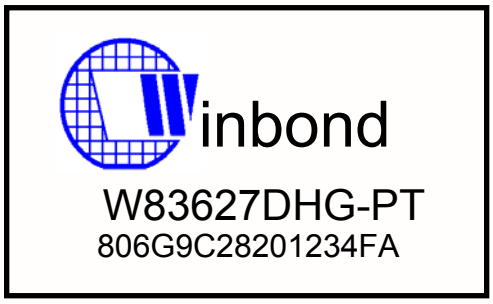


SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
t_1	Output Valid Delay	4	11	nS
t_2	Float Delay	4	11	nS
t_3	LAD[3:0] Setup Time	14		nS
t_4	LAD[3:0] Hold Time	0		nS
t_5	LFRAME# Setup Time	12		nS
t_6	LFRAME# Hold Time	0		nS

23. TOP MARKING SPECIFICATIONS

1st line: Nuvoton logo
2nd line: part number: W83627DHG-P (Pb-free package)
3rd line: tracking code 806G9C28201234FA

806: packages made in '08, week 06
G: assembly house ID; G means GR, A means ASE, etc.
9: code version; 9 means code 009
C: IC revision; A means version A; B means version B, and C means version C
28201234: wafer production series lot number
FA: Nuvoton internal use.



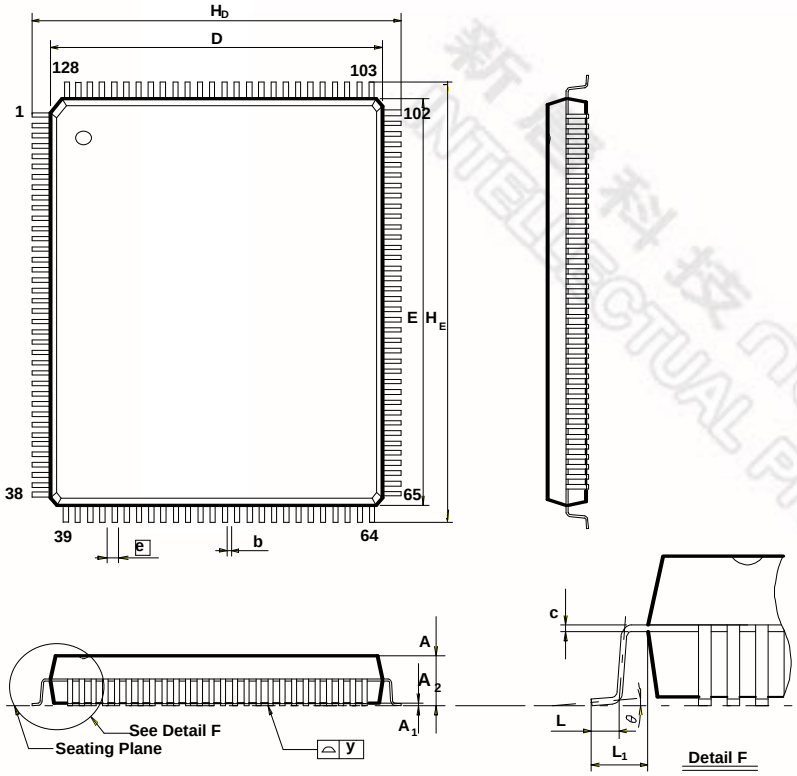
1st line: Nuvoton logo
2nd line: part number: W83627DHG-PT (Pb-free package)
3rd line: tracking code 806G9C28201234FA

806: packages made in '08, week 06
G: assembly house ID; G means GR, A means ASE, etc.
9: code version; 9 means code 009
C: IC revision; A means version A; B means version B, and C means version C
28201234: wafer production series lot number
FA: Nuvoton internal use.

24. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83627DHG-P	128Pin QFP (PB-free package)	Commercial, 0°C to +70°C
W83627DHG-PT	128Pin QFP (PB-free package)	Industrial standard, -40°C to 85°C

25. PACKAGE SPECIFICATION



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.134	—	—	3.40
A_1	0.004	—	—	0.10	—	—
A_2	0.101	0.107	0.113	2.57	2.72	2.87
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.010	0.10	0.15	0.25
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.783	0.787	0.791	19.90	20.00	20.10
e		0.020			0.50	
H_D	0.669	0.677	0.685	17.00	17.20	17.40
H_E	0.905	0.913	0.921	23.00	23.20	23.40
L	0.023	0.031	0.039	0.60	0.80	1.00
L_1	0.055	0.063	0.071	1.40	1.60	1.80
y	—	—	0.004	—	—	0.10
θ	0°	—	12°	0°	—	12°

128-pin (QFP, 14x20x2.75mm foot print 3.2mm)

26. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
1.0	12/04/2007	N.A.	1. First published version.
1.1	01/28/2008	N.A.	1. Add section 7.6.3.4 SMART FAN™ III+ and the descriptions of Shut-down Mode in section 7.7.1.3 2. Add the register descriptions of SMART FAN™ III+, SMART FAN™ III+-2, and Shut-down Mode in Chapter 8 Hardware Monitor Register Set 3. Update the descriptions of 21.1 Absolute Maximum Ratings and 21.2 DC Characteristics. 4. Add the block diagram for PECI 1.1a to section 7.5 PECI. 5. Correct the data in 20.8 Logical Device 7 (GPIO6), 20.9 Logical Device 8 (WDTO&PLED), 20.10 Logical Device 9 (GPIO2, GPIO3, GPIO4, GPIO5), and 20.13 Logical Device C (PECI, SST).
1.2	02/19/2008	6, 38, 173	1. Correct the pin names in Chapter 4 Pin Layout. 2. Update the PECI 1.1a diagram in section 7.5 PECI. 3. Correct the information in Table 15.1 SERIRQ Sampling Periods.
1.3	02/25/2008	216-222	1. Correct 20.13 Logical Device C (PECI, SST).
1.4	04/14/2008	23-25, 40, 41, 55, 97-99, 105-107, 116-121, 244, 226	1. Add Chapter 6 ACPI Glue Logical Application Notice. 2. Update the descriptions in 8.5 PECI. 3. Correct the table of Display Registers – in SMART FAN™ III+ Mode in 8.6.3.4 SMART FAN™ III+. 4. Update register descriptions of Chapter 9 Hardware Monitor Register Set. 5. Add 22.3.1 Power On/Off Timing. 6. Update the description of CR[E5h] bit3 in 21.13 Logical Device C.
1.41	05/14/2008.	6, 16, 38-41, 82, 120-121, 156, 232	1. Update Chapter 4 Pin Layout. 2. Remove all descriptions of “PECI_AVL”. 3. Update 8.5 PECI descriptions. 4. Correct the descriptions of 9.39, and 9.130 to 9.134. 5. Correct Table 13-1. 6. Update 22.2 DC Characteristics.

VERSION	DATE	PAGE	DESCRIPTION
1.42	08/19/2008	22-24, 36, 82, 224, 228, 232, 251	1. Update the figures and the title of Chapter 6 ACPI Glue Logic. 2. Update Figure 8-7. 3. Correct the description in 9.39. 4. Update CR[F0h] of 21.12 Logical Device B (Hardware Monitor). 5. Update CR[E5h] and CR[E8h] of 21.13 Logical Device C (PECI, SST). 6. Update 22.1 Absolute Maximum Ratings. 7. Correct 22.3.4 Clock Input Timing. 8. Change Winbond logo to Nuvoton.
1.43	09/16/2008	109	1. Correct the description of bit 3-1 of 9.98 FANCTRL6 SMART FAN™ III+ input source & output FAN select Register – Index 5Eh (Bank 1).
1.5	10/14/2008	89, 91, 216, 218, 219, 220, 245, 246, 247	1. Update the descriptions of 9.50 and 9.53. 2. Modify the descriptions of CR30h, bit 7 of CRE4h, bit 1 of CRE5h, bits 3-1 of CRE6h, and bit 4 of CRE7h of 21.11 Logical Device A (ACPI). 3. Update the descriptions of 22.3.1 AC Power Failure Resume Timing.
1.6	11/10/2008	17, 232	1. Define SMBus Interface in Chapter 5.11; GPIO in Chapter 5.12 2. Add Hardware Monitor Ratings in Chapter 22.2
1.7	02/23/2009	3, 9, 10, 11, 12, 84, 106, 111, 112, 194, 201, 203	1. Remove KBC clock rate selection. 2. Add LPT support FDD function, include pin description and register setting. 3. Add / modify the function description in Chapter 9.39, 9.85, 9.86, 9.99 and 9.100.
1.8	04/02/2009	N.A.	1. Add part number W83627DHG-PT, supporting -40℃ ~ 85℃ operation temperature. 2. Add Chapter 24, Ordering Information. 3. Update Chapter 25, Package Specification.
1.9	04/27/2009	82,92	1. Modify Bank0 CR46[2.1] name. 2. Modify Bank0 CR59 description.
1.91	05/21/2009	252	1. Modify clock cycle time and add t3.
1.92	06/11/2009	178, 247 203, 204 123 ~ 125	1. Correct ACPI power sequence timing. 2. Correct UART A & UART B registers. 3. Correct Hardware Monitor registers.
1.93	06/25	252	1. Correct Clock input timing data.
1.94	07/09/2009	2, 158, 203, 204	Reserve one UART source clock.

Important Notice

Nuvoton products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Furthermore, Nuvoton products are not intended for applications wherein failure of Nuvoton products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Nuvoton customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nuvoton for any damages resulting from such improper use or sales.