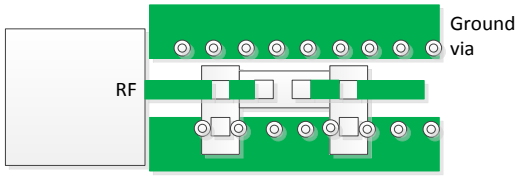
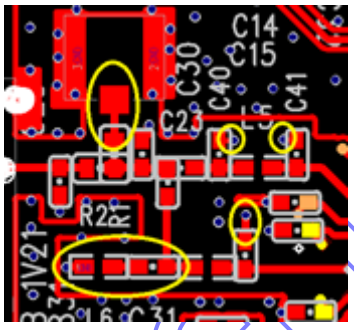
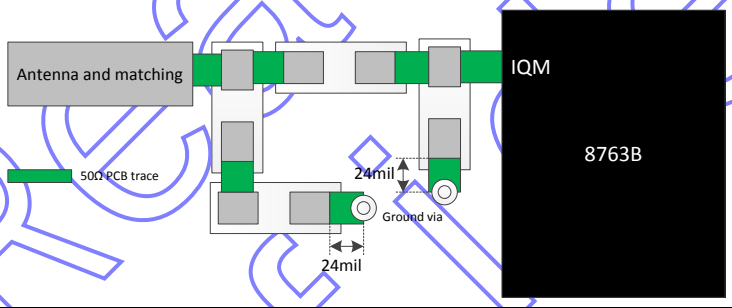
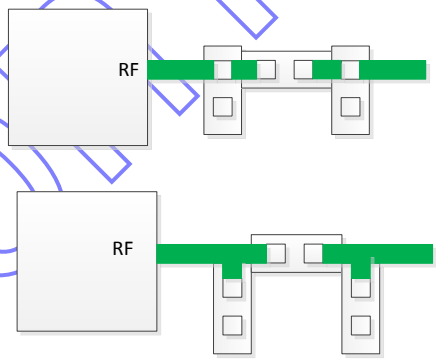
Realtek Semiconductor Corp.

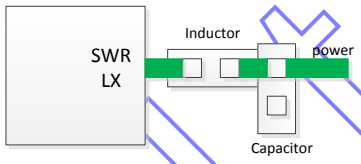
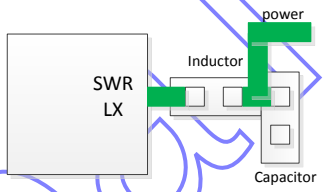
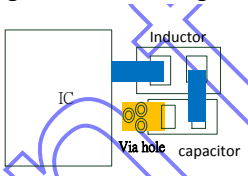
Document P/N: [ ]

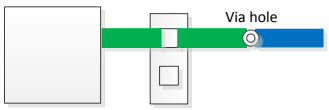
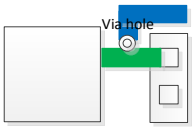
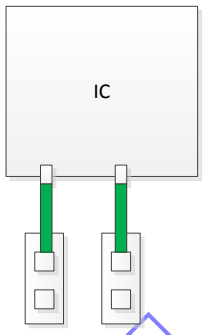
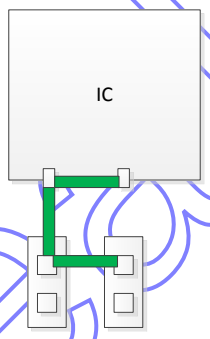
RTL8753BAU Layout check list v1.2

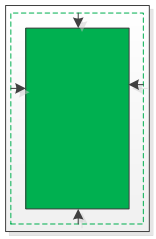
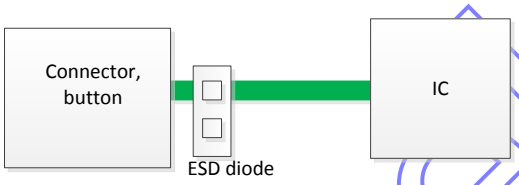
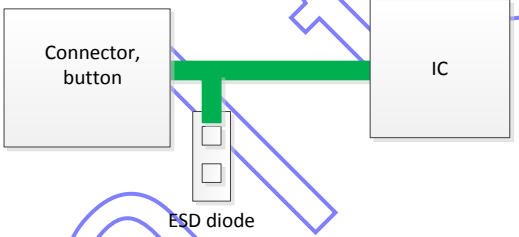
Project:	PCB layout Version:	Customer:
Review by:	Approval by:	Date:

	Content	PASS	Fail	N/A	Note
Components placement ordering					
1	Key components placement, decide first (1) Decide the antenna, RF and antenna matching components placement (2) Decide the RTL8753BAU placement (3) Decide the crystal placement (4) Decide the SPI flash placement Peripheral power components (1) HV cap placement first, as close to RTL8753BAU as possible (2) Please let the HV capacitor (pin28)away to voice mic (3) Switching regulator inductor and capacitor (4) The capacitor of VBAT and ADP_IN pin (5) The related capacitor				
RF circuit					
2	The RF π-matching network should be as close to the chip as possible.				
3	Check the RF trace impedance, use RF impedance calculation tool to check, must include board thickness information, and the RF trace is suggested to be over 8mil in order to cover the uncertainty of the PCB etching, or the RF impedance measurement at the PCB maker is suggested.				
4	Board grounding check – 2 layer PCB The grounding should be as completed as possible, refer to RTK hardware instruction guide.				
5	Board grounding check – 4 layer PCB The layer next to the BT chip (defined as top layer) must be ground layer, and the distance between the two layers is suggested to be 5mil				
6	There should be no any signal to be on the reference layer under the RF circuit and trace				
7	Check the clearance of the antenna, there should no copper or any metal close to the antenna				

8	A complete ground via array is suggested to next to the RF trace 				
9	Notice the ground via hole in the RF π-matching , the distance from the components pad to via hole should follow the requirement below. The ground via should be connected to layer2 (ground layer) directly, **do not** connect to the ground copper in top layer (e.g. same layer of the main chip)  				
10	The IC RF matching is suggested to follow RTK guideline, and the layout must be straight-forward.  Correct NG				
11	Use 0402 (1005) type components for the RF network, if the PCB size is too small, use 0201 type components, no components in the				

	matching network could be ignored and removed.				
Analog and Digital Circuit					
12	VBAT The battery to VBAT pin must be as wide as possible, at least 12mil wide (20mil if possible) and a big cap must be close to the chip input.				
13	Buck SWR: The switching signal LX must be as short and as wide (at least 12mil) as possible Suggested to be over 10mil				
14	Buck SWR: The SWR capacitor must be next to the inductor, after this capacitor, it could be called as 1V2 power and could be for the system. Before this cap, it is not allowed to use for any purpose. Correct  NG 				
15	The ground terminal of the buck circuit 4.7uF capacitor should be close to the chip EP pad as possible to shorten the ground loop, place more ground via at the ground pin of 4.7uF capacitor. 				
17	There should be no ground metal or signal under the buck inductor body, and in the next layer, should be a complete ground plan (layer2)				
18	The crystal oscillator placement should be as close to the chip as possible, and the layout trace is suggested to be over 6mil This include 40MHz and 32768Hz crystal.				
19	The capacitor next to the power pin should be as close as possible. The relation of the via and component should be as below.				

	Correct  NG 				
20	The power cap should be connected individually, do not connect on chip directly. Correct  NG 				
22	USB differential signal: The trace width is suggested to be 6mil wide and the spacing is 5mil between the differential signal, the clearance to the other signal should be at least 8mil				
20	Audio differential signal: Both the speaker out and microphone signal, if it is in differential mode, the trace width is suggested to be at least 8mil wide and the spacing is 5mil between the differential signal, the clearance to the other signal should be at least 8mil				
21	Audio amp: The power cut for digital ground and audio drive ground is suggested.				
22	ESD: For ESD consideration, the ground layer could be shrinkage and the				

	sensitive signal should not close to the board edge. 				
23	ESD diode The ESD diode should be at the connector, and as close as possible. The ESD diode must be on the correct trace. Correct  NG 				
24	HW_RST pin: If there is any signal trace nearby, the distance between HW_RST and signal trace should be at least 10 mils				
MISC					
25	Check the silkscreen.				
26	The ground via under the EP pad, the ground via must average to place. For 6x6 or 8x8mm^2 package: 16 via holes				
27	The chip EP pad dimension is suggested to follow the information in the RTL8753BAU datasheet.				
PASS：the design is correct。 FAIL：Not properly, need to describe the reason. N/A：No such request					