RTL8763B/ RTL8753B/ RTL8773B
BLUETOOTH SOC
PCB Layout Guide

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

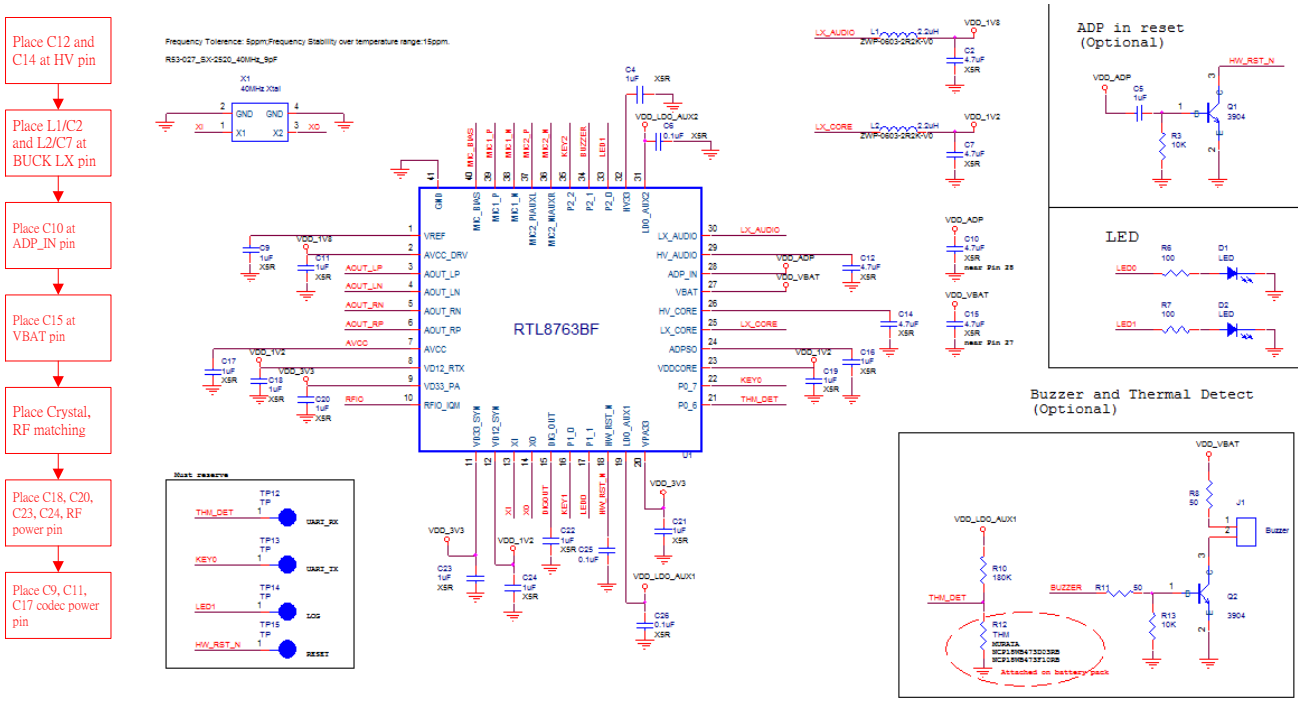
REVISION HISTORY

Revision	Release Date	Summary
1.0	2017/11	First release.
1.1	2018/02/06	In page12, add audio layout rule for single end and CAPLESS mode
1.2	2019/10/2	In page12 and 13, add the MIC layout and design notice
1.3	2020/5/22	Add RTL8753 and RTL8773

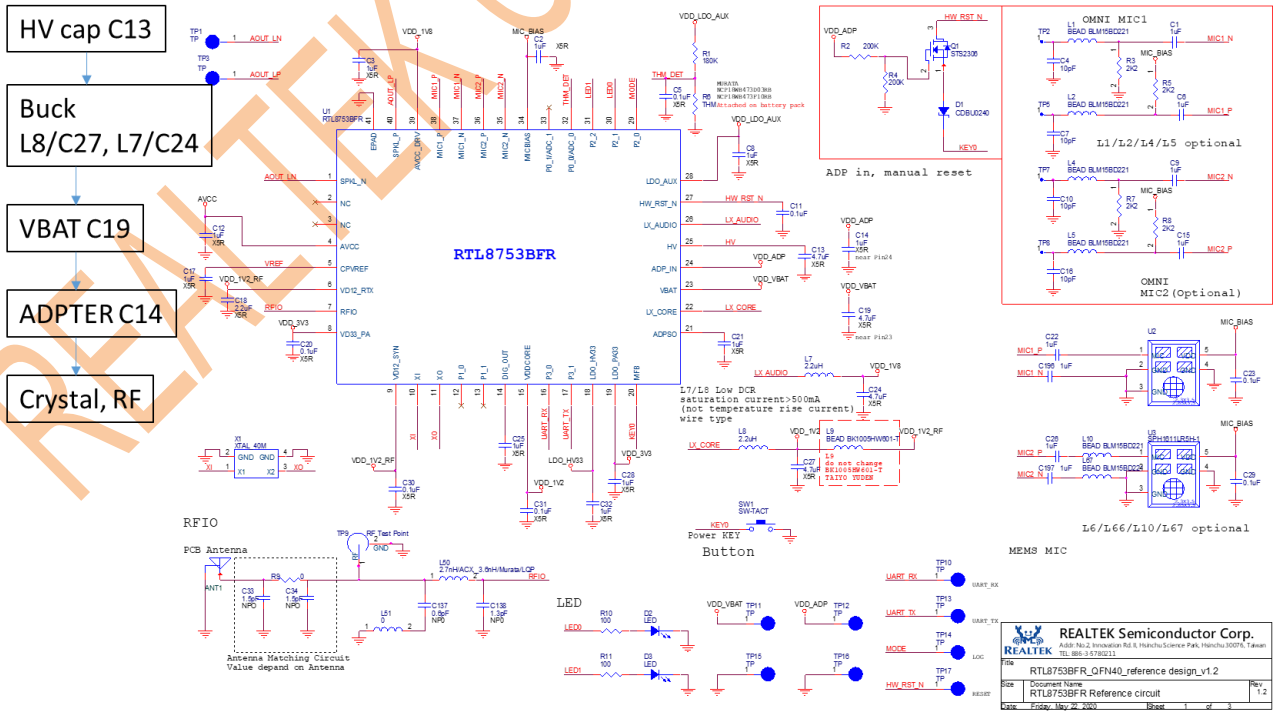
➢ Placement Priority, IMPORTANT!!

- **The priority here means close to chip as possible.**

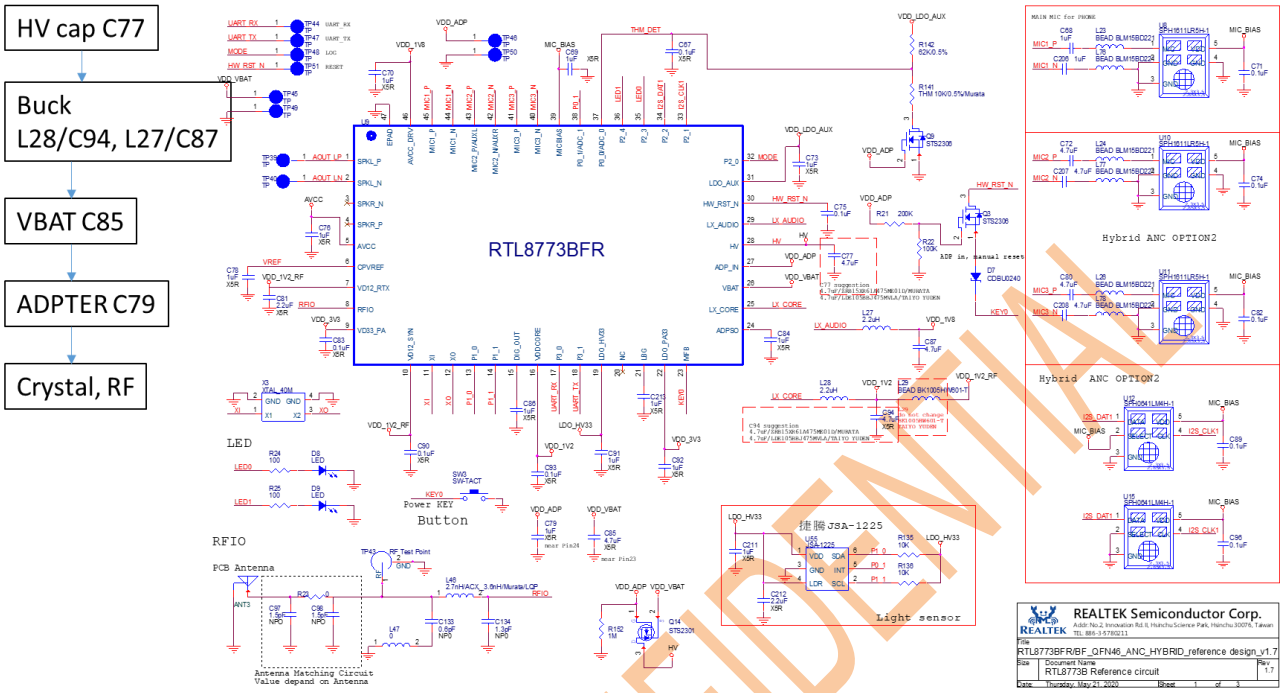
RTL8763B



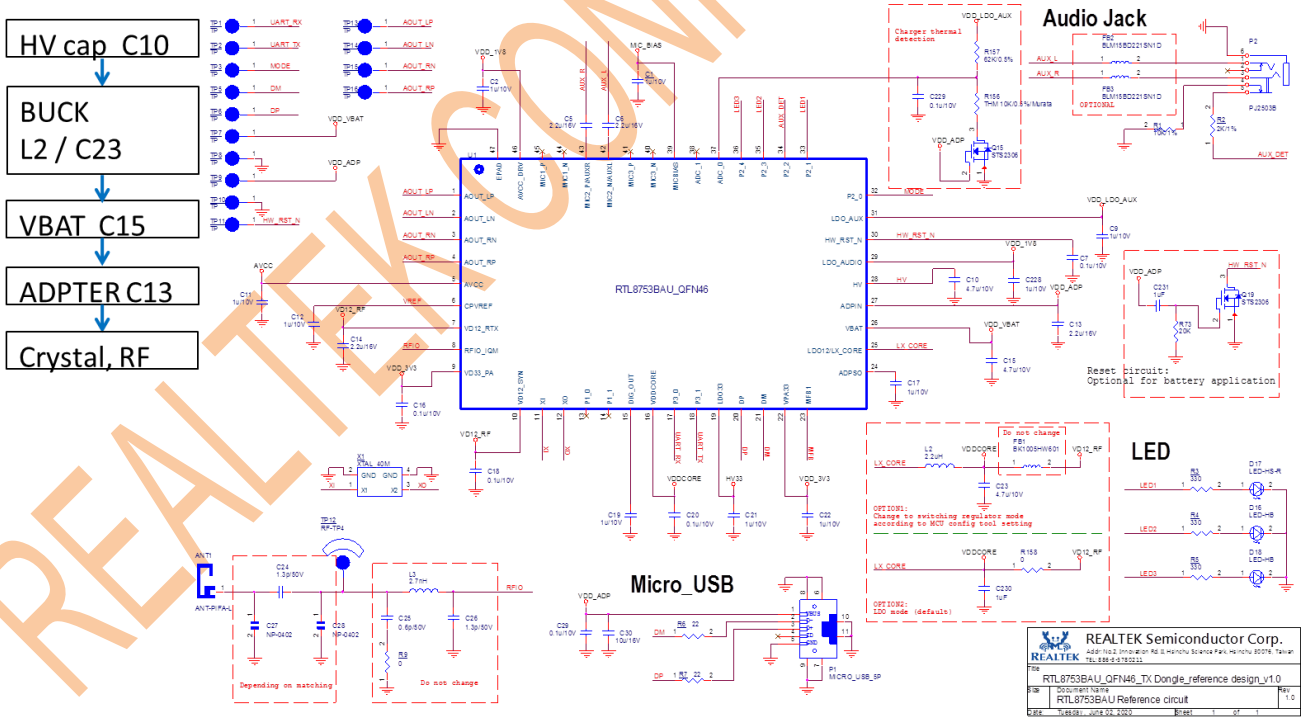
RTL8753B



RTL8773

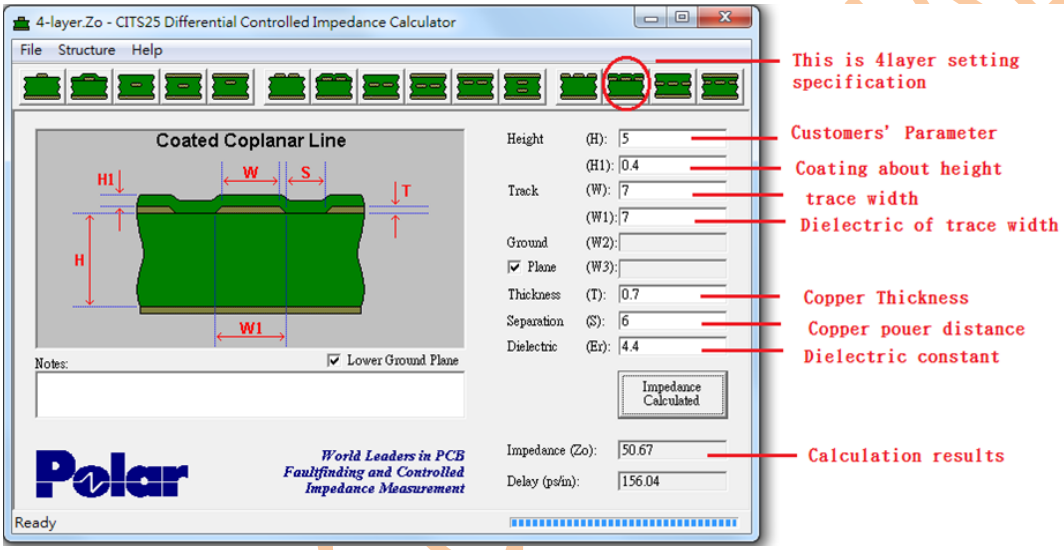


8753BAU

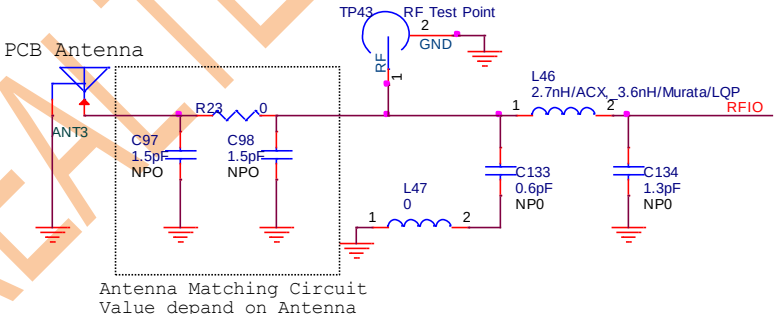


➢ RF placement rule

- ➢ Use the RF impedance tool to calculate 50 Ohm impedance.
  - ■ The parameters include the distance from the RF trace to the reference layer(H), the coating thickness(H1), trace width(W), deviation of trace width due to PCB etching(W1), copper thickness(T), ground copper separation from the RF trace(S), dielectric constant(Er).
  - ■ Example below: use the tool to calculate impedance (Zo) and select appropriate parameters according the PCB maker's capability. It is important all the parameters should be selected reasonably, if not, you may need to find a very high-end PCB maker and cause the high PCB charge.



  - ■ We suggest the RF trace should be no less than 8mil to avoid the large variation of RF impedance.
  - ■ The RF trace here include RF output (RFIO include IQM and TPM) from chip to antenna, all of the trace should be carefully controlled. It will impact the RF performance a lot if the impedance is not within 50Ω+/-10%.



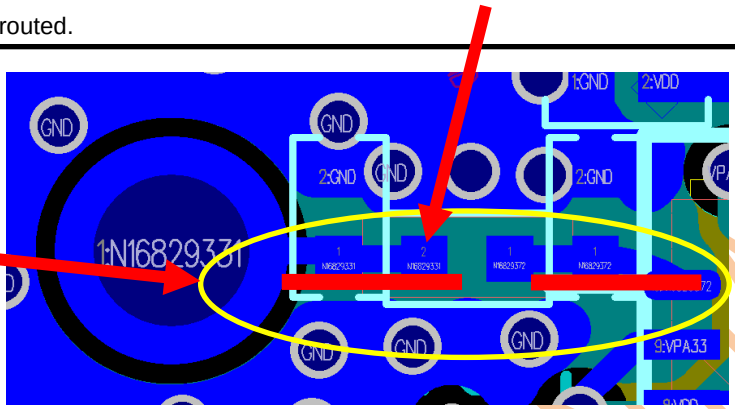
- ➢ Be sure to communicate with the PCB maker to final check if the parameters are all right.
- ➢ The RF test point TP9 is not suggested to be on an extra branch, if it is on back side, the via should be on the path.

- The RF matching components must be closed to IC RFIO pin, as close as possible.

The component and trace should be placed following the route example below, the RF trace should go straight forward and appropriately routed.

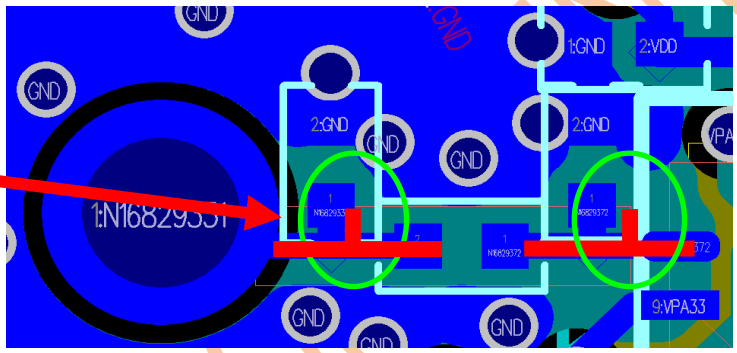
CORRECT

Follow the route example, the trace must be straight forward.



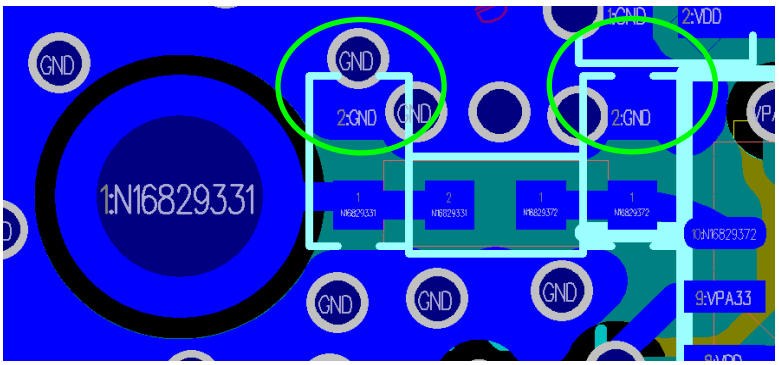
NG

An extra branch trace to the matching is not allowed.



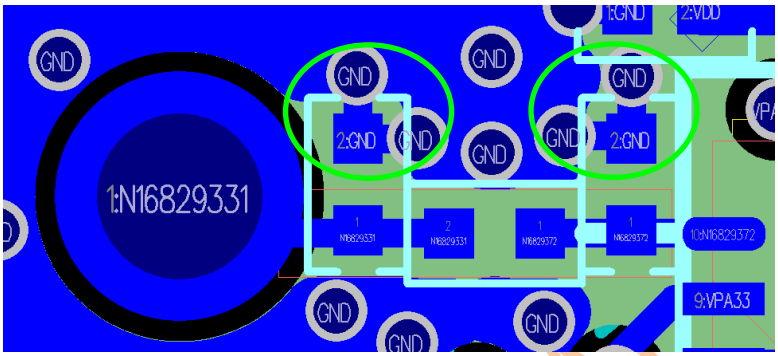
- The PCB layer with BT CHIP is defined as top layer, the layer next to top layer must be ground layer as a reference in a 4 or 6 layer design.
- There should be no other signal to go through the reference layer under the RF area.
- Keep clearance at the antenna area, no copper, no trace below the antenna.
- The ground via of the RF components should be as close to the soldering pad as possible, and use cross-over connection.

NG

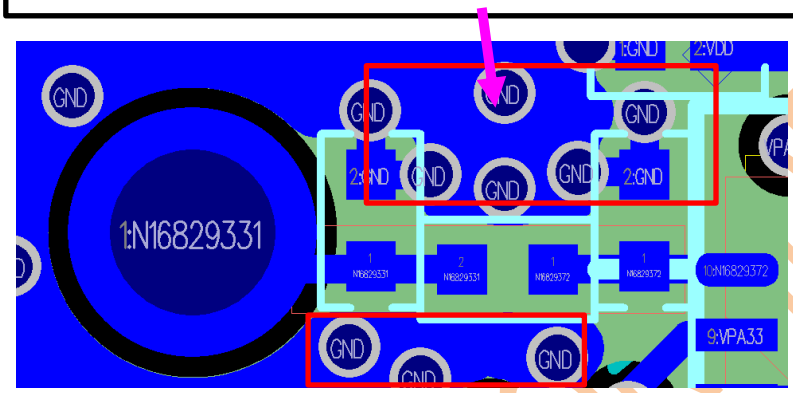


Correct

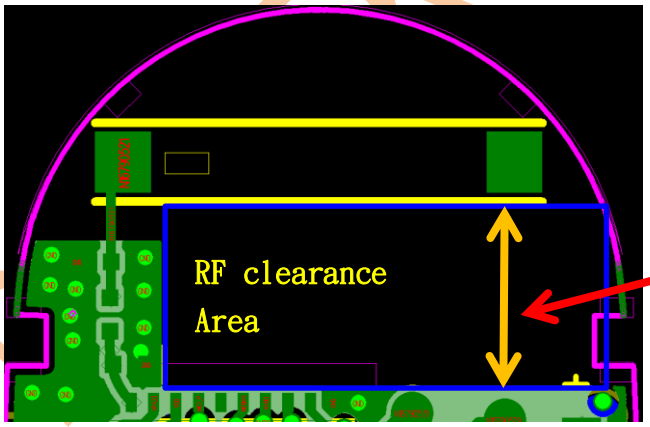
For the RF matching components, the grounding should be cross connected.



- A complete ground via array is suggested to protect the RF trace.(shown in red rectangular mark below)

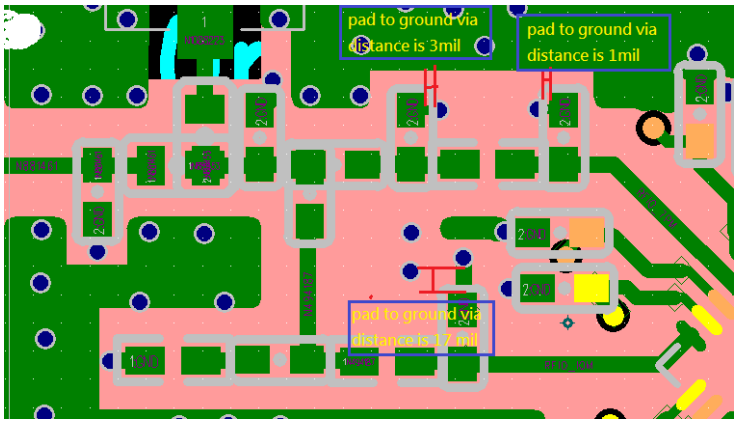


- The layout and placement should be as concentrated as possible to reserve more space for a bigger antenna with good bandwidth and radiation efficiency, and keep more RF clearance area. (As the picture below)



The minimum distance (clearance) between the antenna and ground copper should follow antenna datasheet to achieve a well radiation pattern and efficiency.

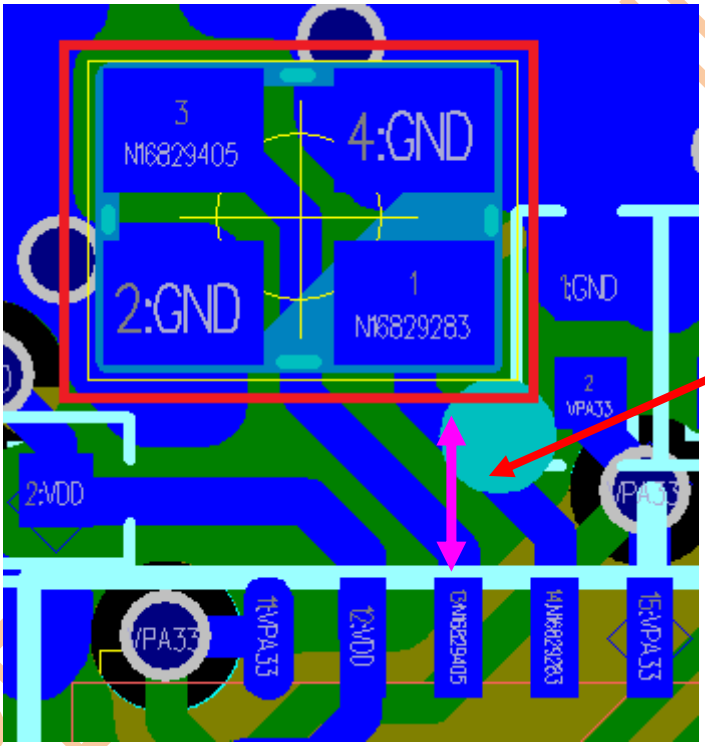
- RF component ground pad to via hole trace distance of as shown below. Trace width is the same as the RF 50 Ohm trace.



- RF ground via not connected to the first layer of copper, directly connected to the ground layer

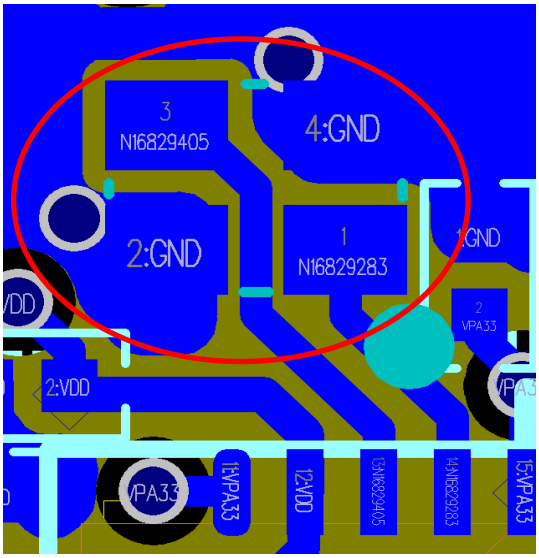
Crystal Placement & Layout Rule

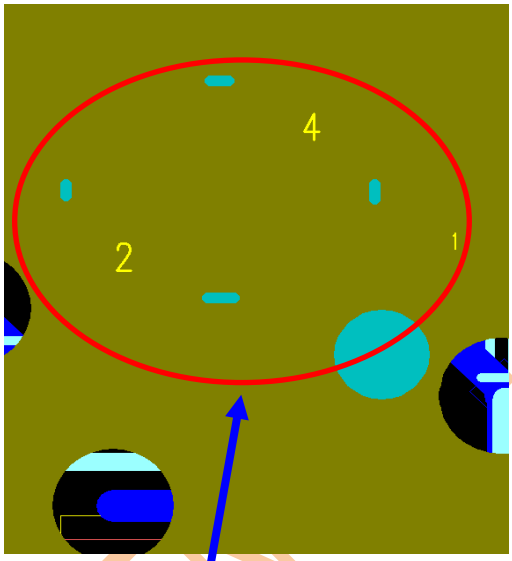
- If there is no mechanical restrictions, crystal and BT CHIP is best to be in the same layer.
- Crystal should be closed to BT CHIP to keep a short routing path, the trace width should be 6mil at least.



The distance of crystal and BT CHIP should be as short as possible.

- If this is a two layer PCB board, try to keep a complete ground reference at the next reference layer (bottom side)





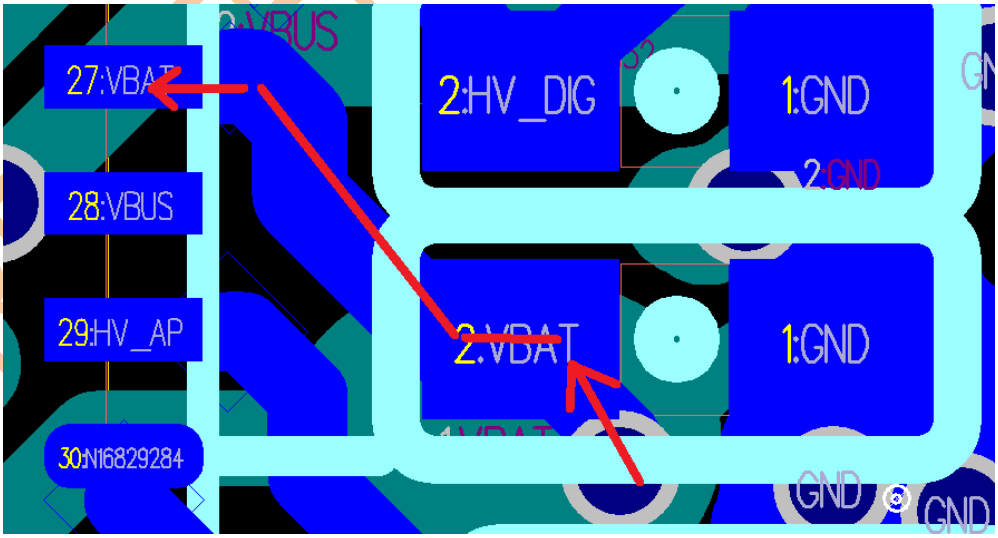
TOP Layer:

The Range of Crystal

The bottom layer of crystal:

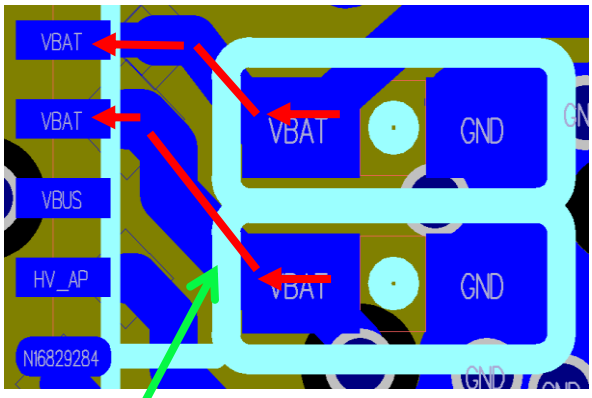
Forbidden any trace, and keep the copper plan complete.

- **VBAT Power Supply**
  - The capacitor of VBAT should place near the input of CHIP.
  - The trace routed must go to the capacitor first, and then go into the input of CHIP. The Trace width suggested to be 15mil at least.

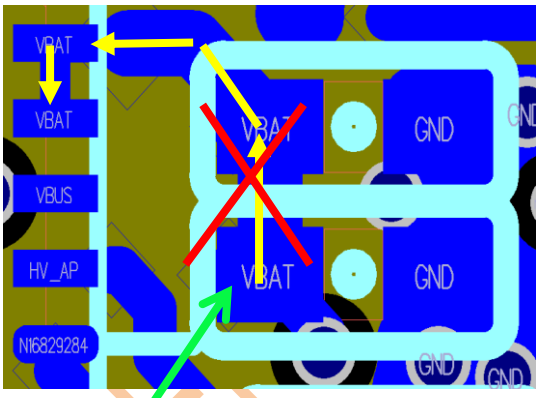


- If there are two pins nearby with the same net name, there should be two bypass capacitors, one for each individually and the power trace should be routed separately. Do not use the NG example.

CORRECT **NG**



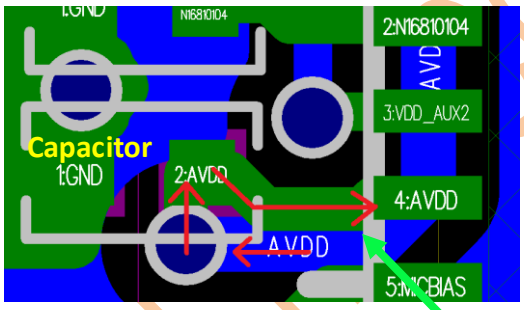
The capacitor component must connect with CHIP pin individually.

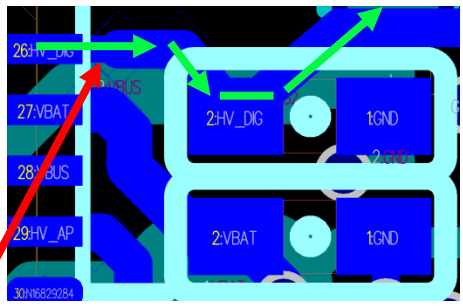


Do not connect together before reaching the chip.

- The capacitor of the power supply pin should be placed close to the power pin.

All of the power trace should go through capacitor first, and then go outside.



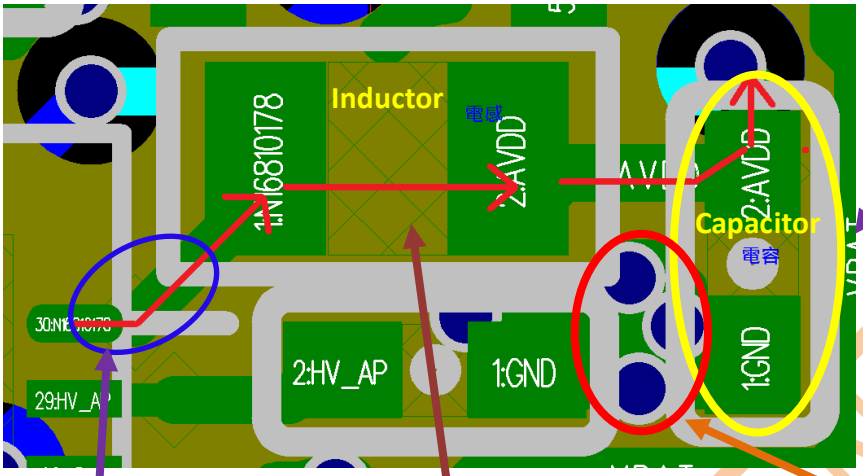


Be sure to follow current flow

Buck Placement & Layout Rule

- The inductor of switching regulator (buck) and capacitor is suggested to be close to BT chip.
- The switching regulator power pin LX goes through the inductor 2.2uH and a capacitor 4.7uF to form a stable, low noise power source, do not pull out this power without going through the 4.7uF capacitor, it is strictly prohibited to pull out the power without going through the 4.7uF capacitor. The trace of LX should be short and wide for the consideration of EMI issue, the trace width is suggested to be 15mil at least.

- The ground terminal of the 4.7uF capacitor should be close to the chip EP pad as possible to shorten the ground loop, place more ground via the ground pin of 4.7uF capacitor.



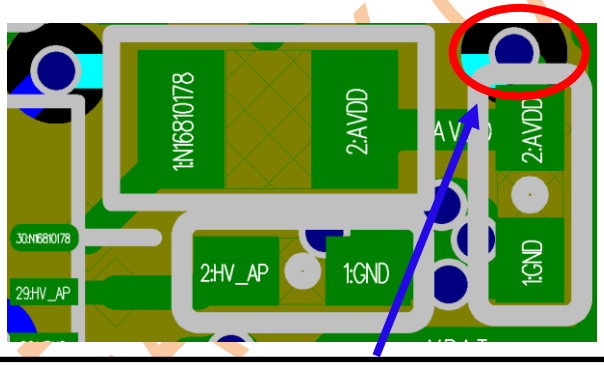
The capacitor must place next to the inductor

The switching signal LX must be short and wide.

The LX must go through the inductor, through the capacitor and then branch out.

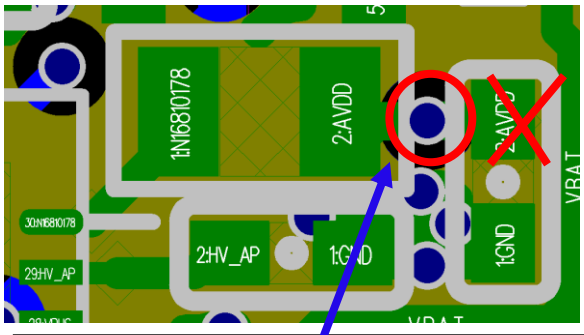
Put more than one ground via at the ground pad of 4.7uF capacitor.

- CORRECT



Buck SWR LX goes through inductor and capacitor → power via should be after the capacitor.

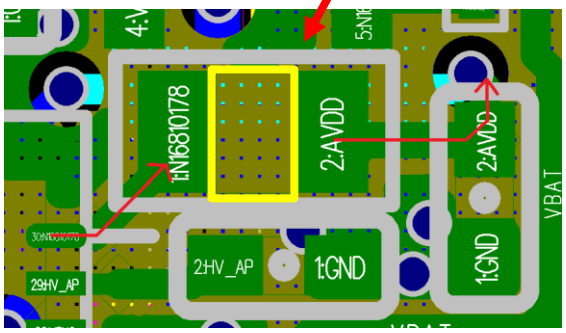
NG

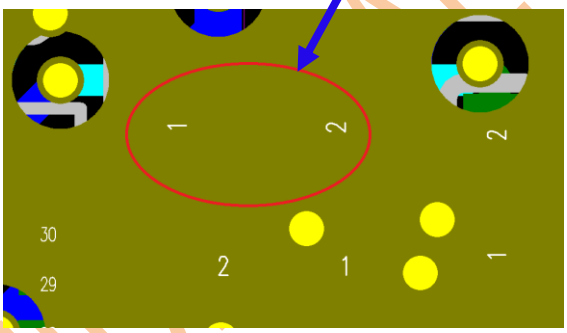


Buck SWR through inductor →the add Via before the capacitor.

- There should be no signal at the reference layer of buck inductor (under the buck inductor body, make reference plane of the back layer(BOT) complete.

- There is no GND copper between the pads of wire wound inductor.(as yellow rectangular mark)



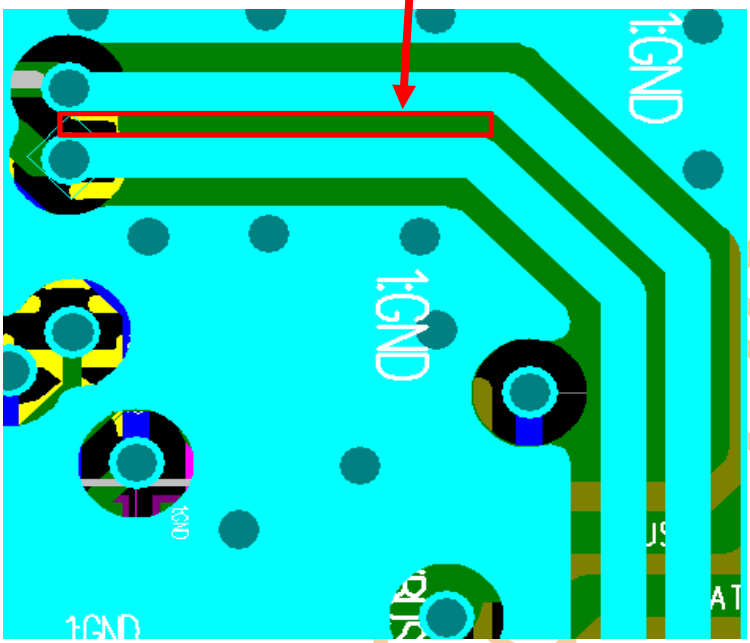


- If it is a 2-layer board, there should be no any signal trace under the inductor, keep copper plane of the back layer (BOT) complete.

➢ Audio Layout Rule

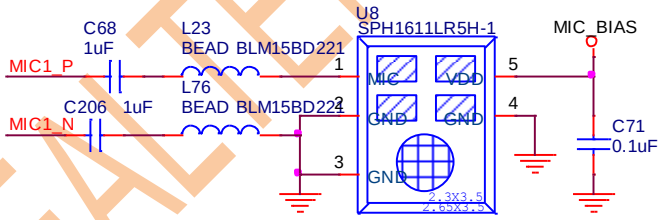
➢ If SPK+/- and MIC+/- (Both ECM and analog MEMS type) are differential pairs, the trace width is suggested to be 8mil at least.

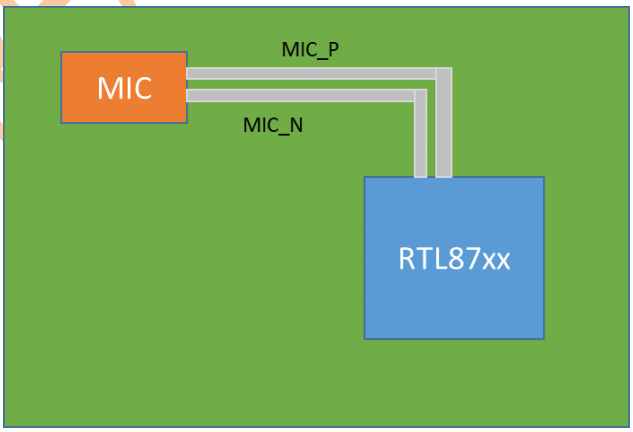
The distance between the differential signals is 5mil **(as the red frame)**, the clearance to the other signal should be at least 8mil (both single end mode and differential mode), and add GND via holes around the trace to protect the audio signal.



➢ MEMS MIC

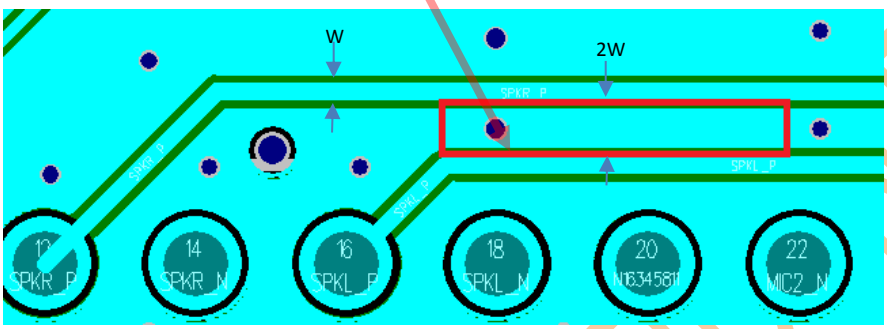
The MEMS MIC, though only single end output, we still suggest to route the MIC signal as P/N pair, a reference ground goes with the MIC signal from MIC to the chip. L23 and L76 is optional.





- AUXIN_R and AUXIN_L are not a differential pair, do not route the two as differential signals.

- If single end and CAPLESS mode, the trace width is suggested to be 8mil (W) at least. The clearance to the other signal should be at least 2W **(as the red frame)** and add GND via hole around the trace to protect the audio signal. To avoid interference, audio trace should to be keep away from power trace and power inductor (BUCK converter circuit). It is suggested the area above and below the audio signal (for example, if audio is in layer3, the upper layer is layer2, lower layer is bottom layer, layer4) should not be clock and noisy power trace.

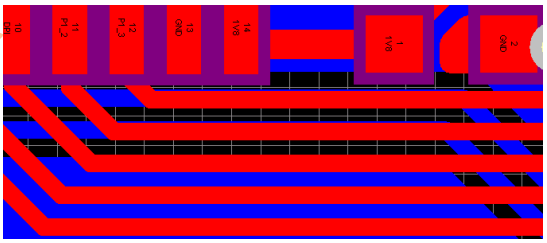


MISC-1

- Avoid the trace at two nearby layers to be in parallel.

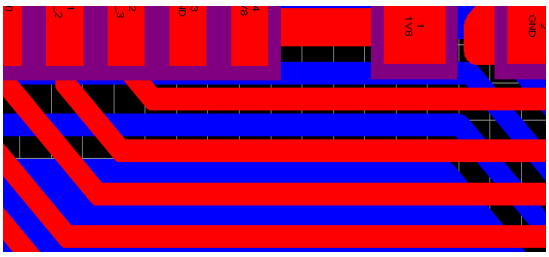
Error:

Parallel traces at layer1 and layer2.



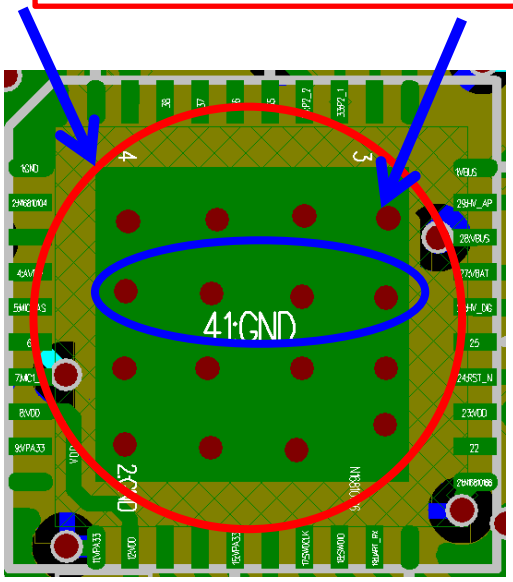
Correct:

Fine tune the trace not to be in parallel at the two nearby layers.

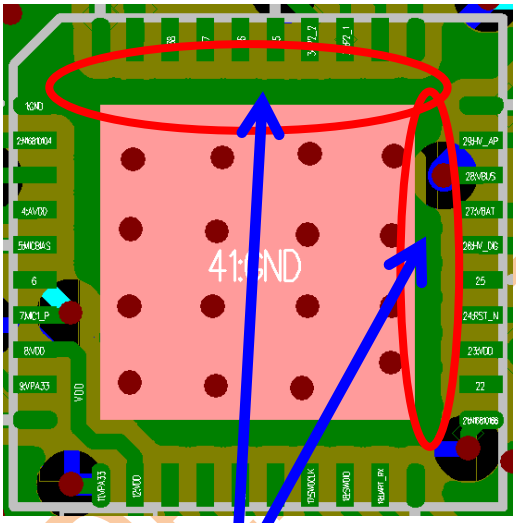


- Do not use copper pour at the area in between the IC PIN and EP PAD, the GND via at EP pad must connect directly to the GND Layer.

- Add enough GND Via in the EP PAD, and connect with GND Layer directly.



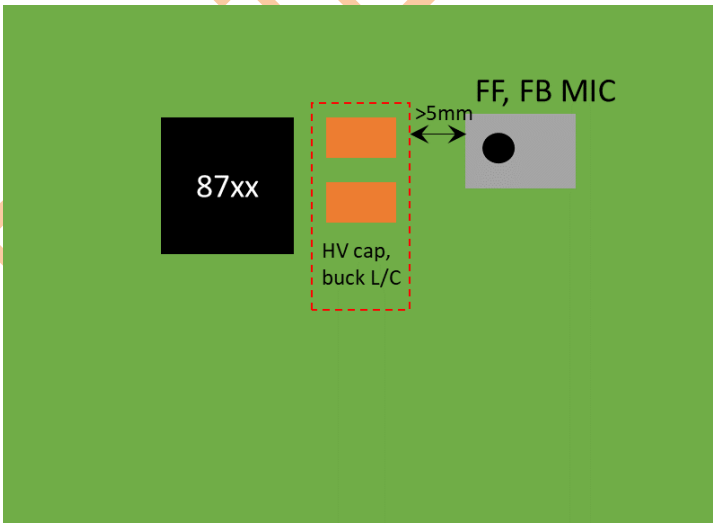
CORRECT



NG

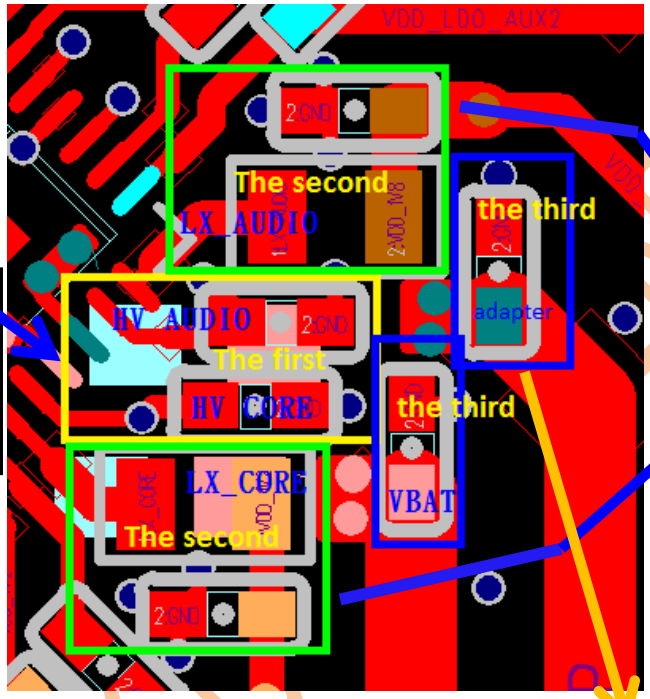
- **MISC-2**

HV cap, buck L/C, VBAT caps are noisy components, keep away from MIC, audio related components, especially FF MIC, FB MIC, at least >5mm away.



- Placement Priority order:

1. HV AUDIO and HV CORE capacitor is first priority to do placement, capacitor put close BT CHIP as possible, The route should be short and the distance suggest do not exceed 100mil.
2. The second is Buck inductor and capacitor, LX trace width > 15mil.
3. The third is the capacitor of adapter and battery



HV AUDIO and HV CORE is the first priority to do placement.

The second is LX Audio and LX CORE.

The third is adapter and battery.