

# REALTEK

## RTL8763BO

### BLUETOOTH 5 DUAL MODE SOC

For HerzTek Internal Use Only.

#### PRELIMINARY DATASHEET (CONFIDENTIAL: Development Partners Only)

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## USING THIS DOCUMENT

This document is intended for the software engineer’s reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

## ELECTROSTATIC DISCHARGE (ESD) WARNING

This product can be damaged by Electrostatic Discharge (ESD). When handling, care must be taken. Damage due to inappropriate handling is not covered by warranty.

Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

- Use an approved anti-static mat to cover your work surface.
- Use a conductive wrist strap attached to a good earth ground
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

## REVISION HISTORY

Revision	Release Date	Summary
0.92	2017/12/06	Preliminary Release.

Revision	Release Date	Summary
0.93	2017/12/07	<ol style="list-style-type: none"><li>1. Modify chip tape and reel information</li><li>2. Remove DSP MIPS information</li><li>3. Update the reference circuit, correct the UART RX/TX</li></ol>
0.94	2017/12/08	<ol style="list-style-type: none"><li>1. Correct P3_0/P3_1 to AUX_LDO1 domain</li><li>2. Add tray indication</li></ol>
0.95	2017/12/14	<ol style="list-style-type: none"><li>1. Modify the power block in figure.2</li><li>2. Add GPIO input/output level</li><li>3. Add SPI and SDHOST pin description, assign dedicate GPIO</li><li>4. Modify reference circuit, the cap by Vref is changed to 0.1uF</li></ol>

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## 1. General Description

The RT8763BO is a single-chip Bluetooth audio solution for SDK applications. The RT8763BO is composed of an ARM core and an ultra-low power DSP core with high efficiency computing power, high performance audio codec, power management unit, ADC, ultra-low current RF transceiver, and smart I/O distribution controller.

The parameter configuration tools, the EVB kits, and the MP kits, including controller hardware and software, provide a simple and flexible procedure for customers to quickly design and proceed to mass production with Realtek's new generation of audio solutions. This complete total solution provides a fast and highly reliable development path with a very competitive R-BOM.

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## 2. Features

### General Features

- Bluetooth 5 specification compliant
- Supports HFP 1.7, HSP 1.2, A2DP 1.3, AVRCP 1.6, SPP 1.2. and PBAP 1.0
- Single-end RF radio output with high performance 10dBm of transmitter power and -94dBm 2M EDR receiver sensitivity
- Supports Bluetooth classic (BDR/EDR)
- Supports Bluetooth Low Energy (BLE)
  - ◆ Generic access service
  - ◆ Device information service
  - ◆ Proprietary services for data communication
  - ◆ Apple Notification Center Service (ANCS)
- Real Wireless Stereo (RWS)
- Supports USB type-C audio
- Supports local play application with eMMC
- Supports iAP2
- Realtek's latest RCV (Real Clear Voice) technology for narrowband and wideband voice connection, including wind noise reduction
- Supports high resolution audio codec up to 24bits, 192kHz audio data format
- Supports dual analog and digital MIC, AUX-IN, I2S digital audio, analog output
- Supports high speed UART, I2C, SPI and USB2.0 compatible interface
- Supports high resolution 12-bits multi-channel ADC
- Supports PWM I/O and smart LED controller
- Supports USB BC1.2 battery charging
- Smart I/O distribution scheme with MUX

- Built-in 16Mbits FLASH memory
- Integrated dual switch mode power regulator, linear regulators, and battery charger; charging current up to 400mA
- Built-in battery voltage monitoring and thermal protection scheme with external thermal resistor
- SBC, AAC decoder support
- Package: 4.5x6mm BGA 88 balls [8x11 ]
- Supports OTA and USB firmware upgrade
- GSM 217Hz interference block out design
- Low BOM cost
- Green (RoHS compliant and no antimony or halogenated flame retardants)
- Supports PTA (Packet Traffic Arbiter) when co-existing with Wi-Fi

### Baseband Features

- 40MHz main clock
- Supports serial flash for FW storage and parameter upgrade
- Adaptive Frequency Hopping (AFH)
- Multi-link support
- Supports Serial Copy Management System (SCMS-T) content protection

### RAM and ROM Size

- ROM size 768KB
- MCU RAM size 96KB Data RAM + 64KB Buffer RAM + 16KB cache RAM
- DSP RAM 240KB

### RF

- Supports TX +10dBm (typ.) maximum output power for Bluetooth classic
- Supports TX +10dBm (typ.) maximum output power for Bluetooth BLE

- Supports TX +4dBm (typ.) maximum output power for Bluetooth BLE low power TPM mode
- Receive sensitivity: -94dBm (2Mbps EDR)
- Receive sensitivity: -97dBm (BLE)
- Receiver sensitivity: -106.5dBm (125K BLE long range)
- Single-end TX/RX RF port without matching component required (when TX power is below +4dBm and using PIFA type PCB antenna)
- Crystal oscillator with built-in integrated capacitor for clock offset digital tuning (0~20pF), could save 2-compensation CL cap following Realtek design guidelines

#### MCU

- 32-bit ARM Cortex-M4F Processor
- Supports hardware Floating Point Unit (FPU)
- Supports Memory Protect Unit (MPU)
- Supports SWD debug interface
- Executed external SPI flash
- 4-way association cache controller

#### DSP Audio Processing

- Enhanced Tensilica Hi-Fi-mini compatible 24-bit DSP core
- 2 single-cycle MACs: 24 x 24-bit multiplier and 56-bit accumulator
- Supports G.711 A-Law, μ-Law, continuous-variable-slope-delta (CVSD) and mSBC voice codecs
- Supports 8/16 kHz 1/2-mic noise suppression and echo cancellation
- Packet Loss Concealment (PLC) for voice processing
- SBC, and AAC-LC audio codecs supported for BT audio streaming

#### Audio Codec

- Dual operation voltage range 2.8V and 1.8V
- Supports cap-less, single-ended, and differential mode at the DAC path
- Supports 16ohm and 32ohm speaker loading
- Stereo 24-bit digital-to-analog (DAC) with 102dBA SNR
- Stereo 24-bit analog-to-digital (ADC) with 97dBA SNR
- 5-band configurable EQ at both DAC/ADC paths
- Sampling rates of 8, 16, 32, 44.1, 48, 88.2, and 96kHz are supported.
- Built-in MIC bias generator

#### Digital Audio Interface

- Supports two PDM digital MIC inputs
- Supports 24-bit, 192kHz on I2S digital audio
- Sampling frequency  
8/16/32/44.1/48/88.2/96/176.4/192kHz

#### Radio

- Compliant with Bluetooth Core Specification including BR/EDR/LE-1M/LE-2M/LE-Coded (Long Range)
- Fully integrated balun and synthesizer minimizes external components.
- RF circuit design minimizes power-consumption while keeping excellent performance

#### PMU

- Highly integrated PMU design for the system application
- Dual switching mode regulator for digital core, radio and audio codec respectively
- Built-in LDO for the I/O and FLASH memory
- Built-in Li-Ion battery charger with up to 400mA charger current capability

- Supports ambient thermal detection to detect the battery temperature
- Built-in OVP, OCP, UVP protection to protect the system.

#### Operating Condition

- Operating voltage: 2.8V to 4.35V (VBAT)

- Temperature range: -40°C to +85°C

#### Package

- 4.5mmx6mm BGA88

### 3. System Applications

- Mono headset
- Stereo headset
- Real Wireless Stereo (RWS) headset
- Mono speaker
- Stereo speaker
- SDK customized application including MCU and DSP

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## 4. Block Diagram

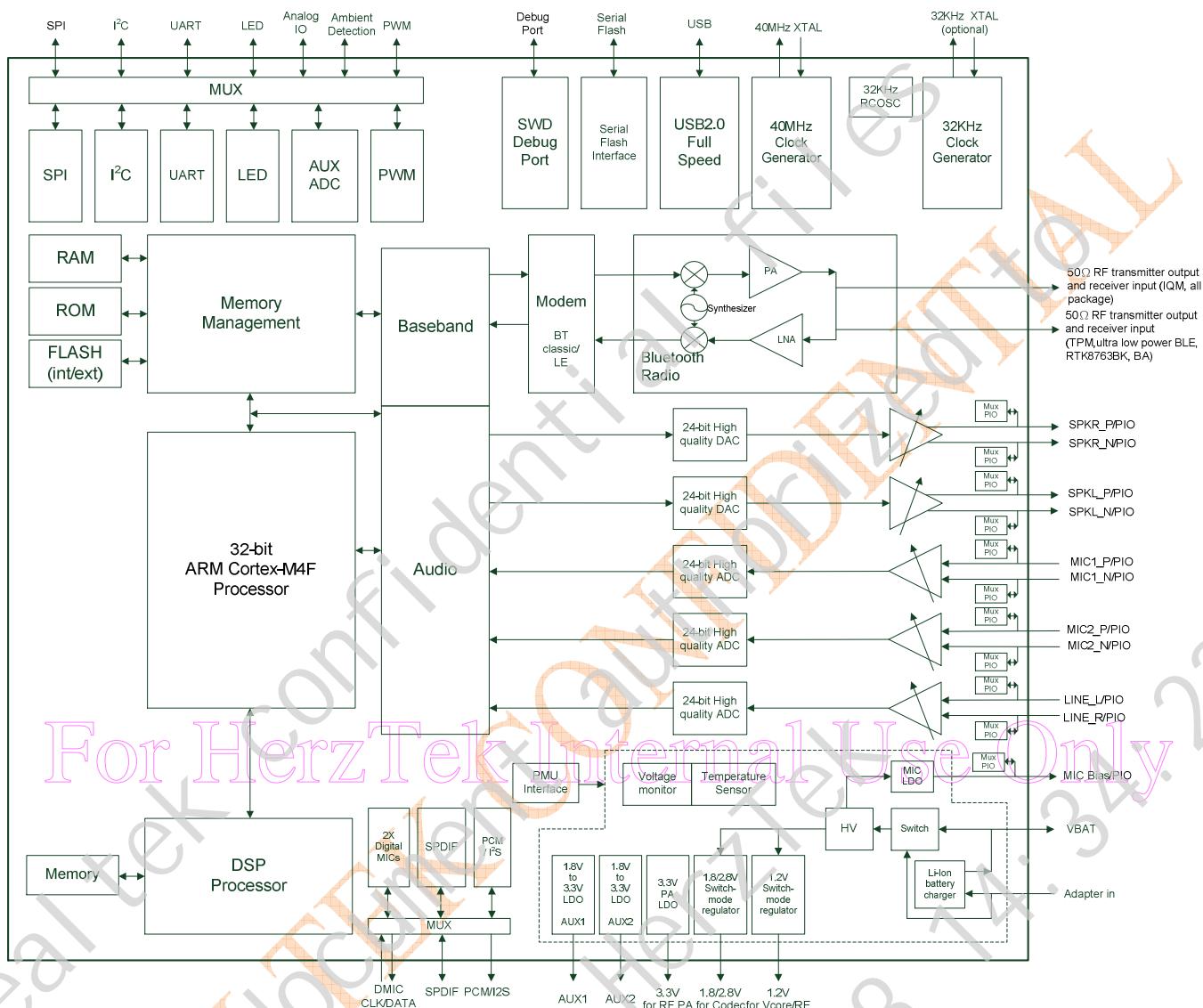


Figure 1. Block Diagram

## 5. Power Tree

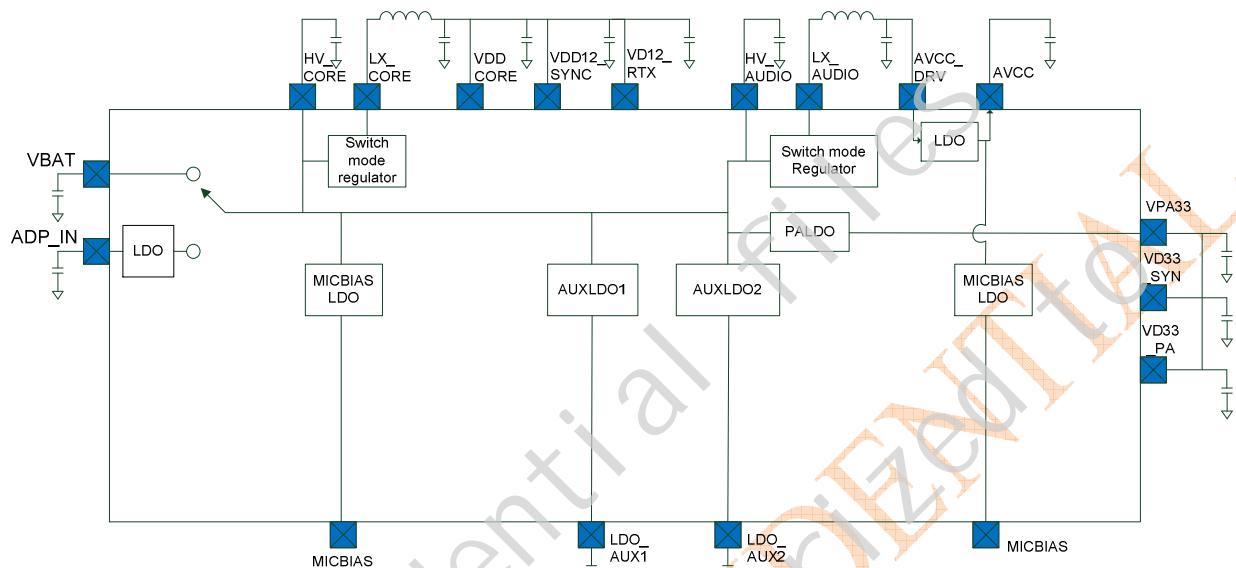


Figure 2. Power Tree-1

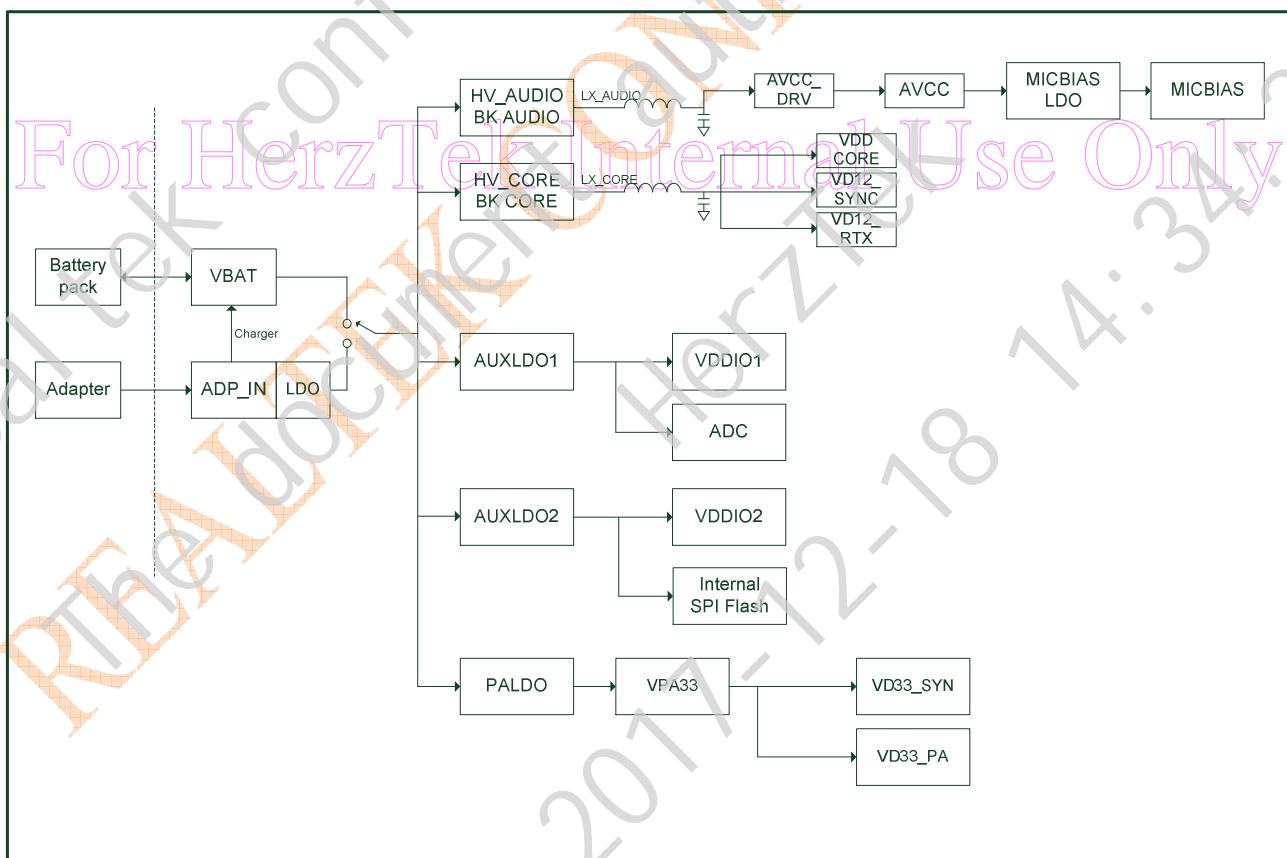


Figure 3. Power Tree-2

## 5.1. Power On Sequence-Battery Mode

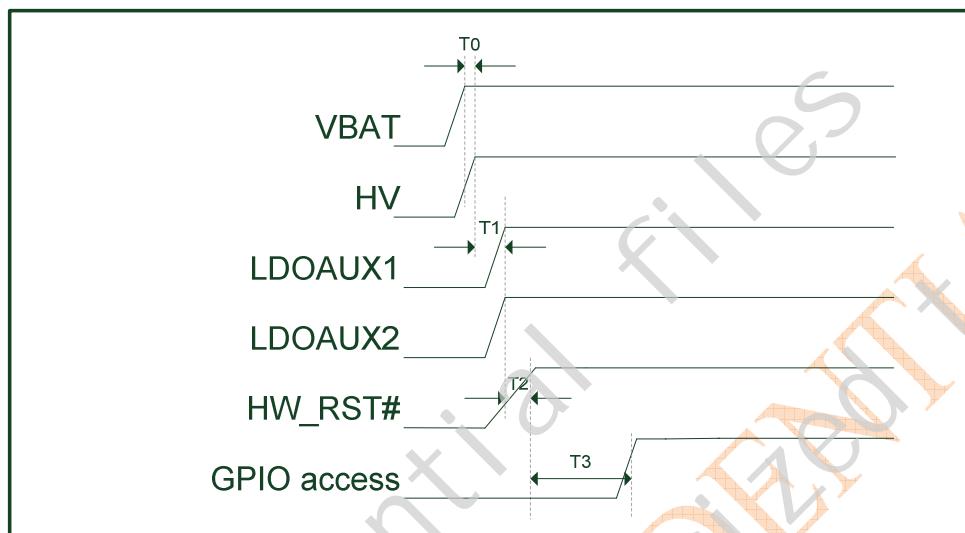


Figure 4. Power-On Sequence-Battery Mode

Table 1. Power-On Sequence-Battery Mode

Parameter	Min.	Typ.	Max.	Unit
T0	-	58.5	-	mS
T1	-	6.7	-	mS
T2	-	10	-	mS
T3	-	TBD	-	-

## 5.2. Power On Sequence-Adapter Mode



Figure 5. Power-On Sequence-Adapter Mode

Table 2. Power-On Sequence-Battery Mode

Parameter	Min.	Typ.	Max.	Unit
T0	100	-	-	mS

## 6. Clock Tree

### 6.1. Overview

The RTL8763BO is composed of two clock oscillator circuits, 40MHz and 32.768kHz. 40MHz is for the system main clock in active mode, while 32.768kHz is for a low power clock when in sleep mode.

A low power clock from an external 32.768kHz crystal and its circuitry is optional for consideration of minimum power consumption in deep sleep mode. The low power clock could also be derived from the internal RCOSC block for cost efficiency and PCB design area optimization.

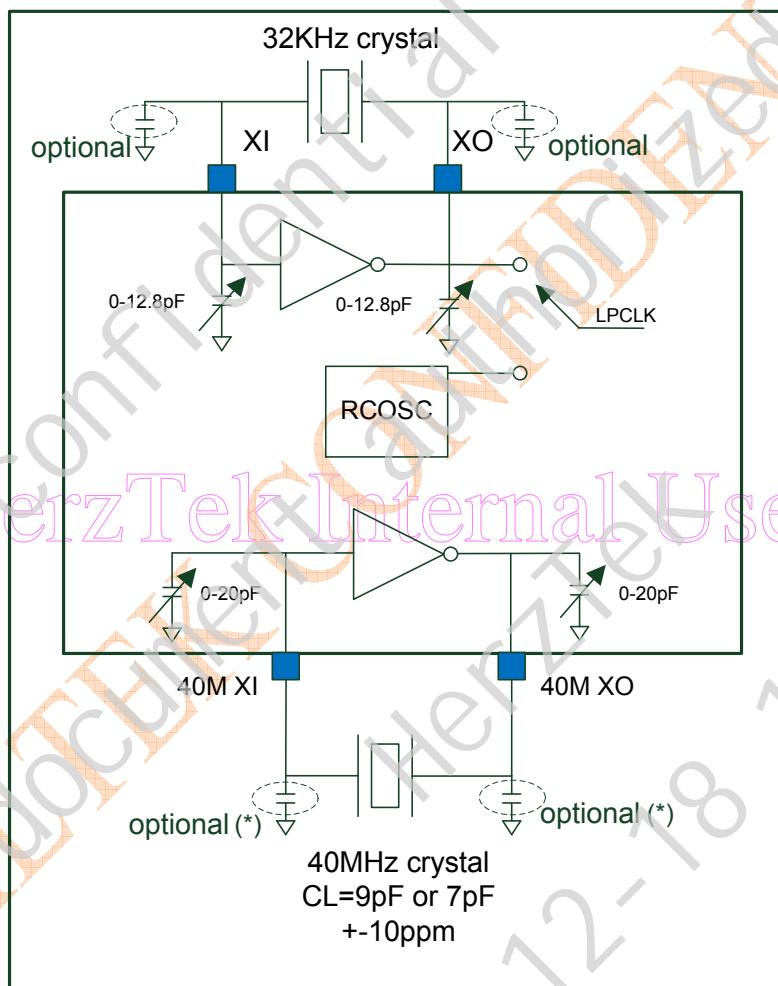


Figure 6. Clock Tree

The RTL8763BO is composed of multiple clock domains. A clock MUX inside the chip distributes the clock source under various user scenarios.

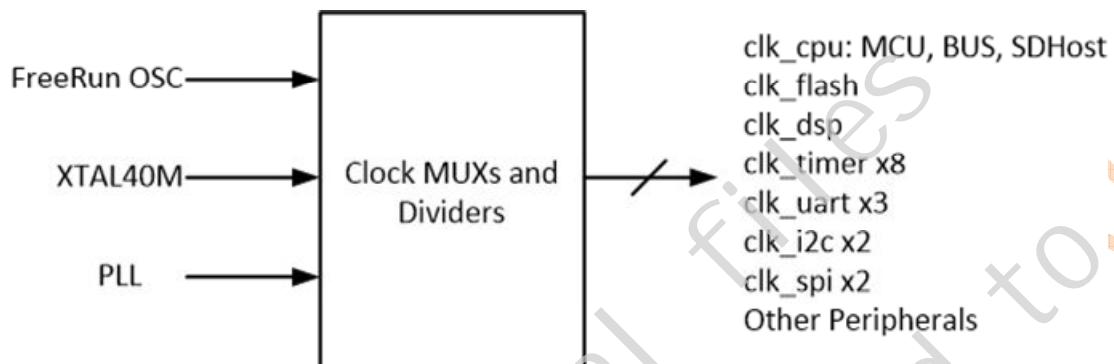


Figure 7. Clock Mux-1

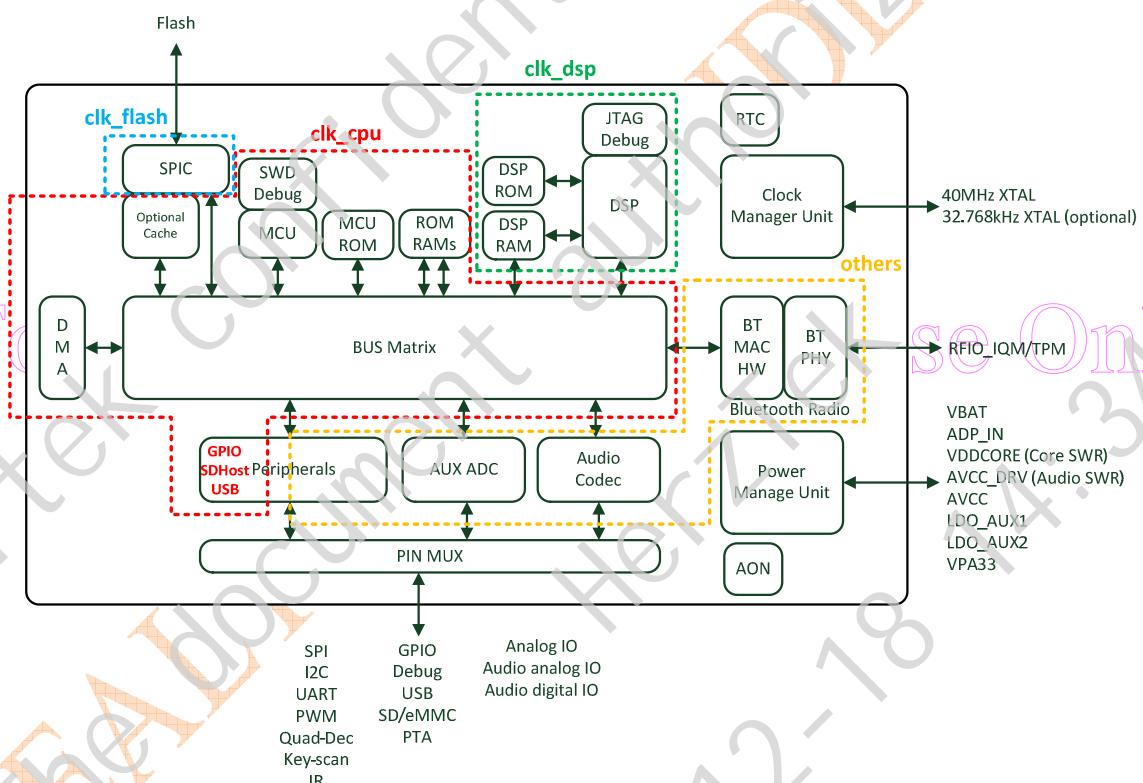


Figure 8. Clock Mux-2

## 6.2. Reset

The RTL8763BO integrates multiple-reset protections to guarantee the system is working under the defined power range, and to avoid system hang up or FLASH memory corruption issues. The external reset IC is optional if the reset threshold defined by the customer is higher than 1.8V. If the customer would like to add an external reset IC, an OPEN drain type is required as the I/O power domain is different from the HV port.

The HW\_RST# pin is active low to trigger reset behavior, and the drive low should be longer than 8ms ( $>8\text{ms}$ ) to avoid unconditional rest noise from the PCB board.

This high reliability design can stabilize the whole system and save the BOM of an external reset.

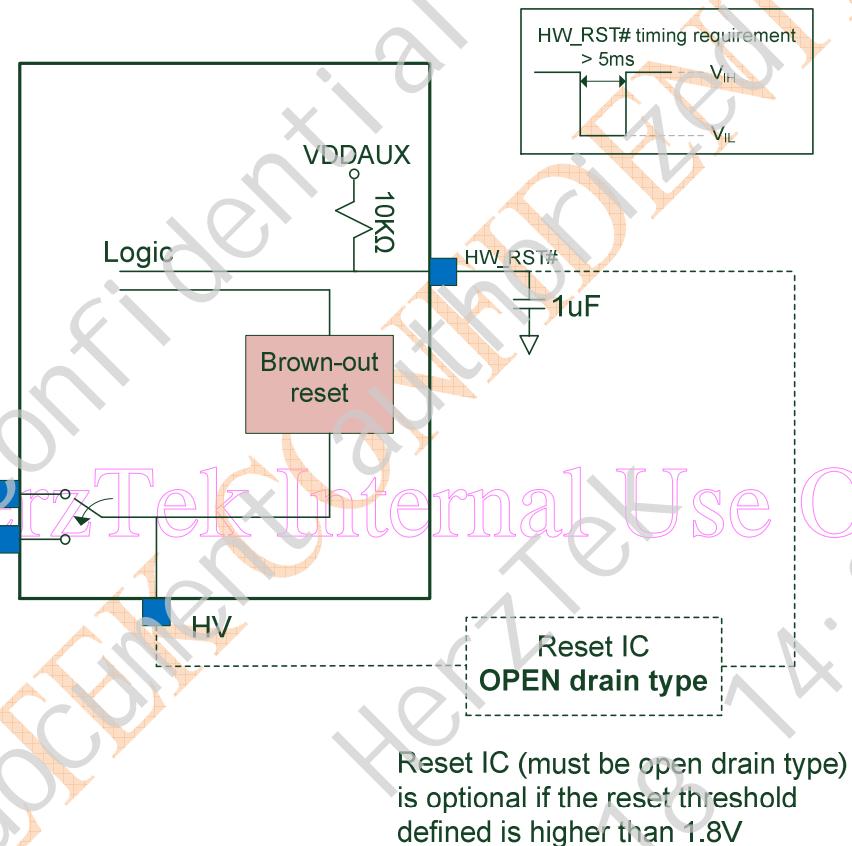


Figure 9. Reset

## 7. Pin Assignments

### 7.1. Package Identification

Green package is indicated by the 'G' in GXXXV (Figure 10). The version is shown in the location marked 'V'.



Figure 10. Package Identification

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RMC

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2017-12-18 14:34:23

## 7.2. Pin Out (Top View) RTL8763BO BGA88

1    2    3    4    5    6    7    8    9    10    11



Figure 11. Pin Out (Top View) RTL8763BO BGA88

## 8. Pin Descriptions

### 8.1. RF Interface

**Table 3. RF Interface**

Pin Name	Pad Type	Ball	Description
RFIO_IQM	RF	H1	Bluetooth radio 50Ω transmitter output and receiver input (dual mode)
RFIO TPM	RF	E1	Bluetooth radio 50Ω transmitter output and receiver input (BLE)

### 8.2. Crystal Oscillator

**Table 4. Crystal Oscillator**

Pin Name	Pad Type	Ball	Description
XI	A	H4	40MHz Crystal input, main clock
XO	A	G4	40MHz Crystal output, main clock
32KXI	A	D8	32KHz crystal input, low power clock
32KXO	A	E8	32KHz crystal output, low power clock

A: Analog

### 8.3. General Purpose I/Os

**Table 5. General Purpose I/Os**

Pin Name	Pad Type	Ball	Description
P0_0/ADC_0	I/O PU_A	H10	Programmable GPIO. Can be programmed as ADC input pin Pull high/low input configurable Belongs to LDO_AUX1 domain
P0_1/ADC_1	I/O PU_A	H11	Programmable GPIO. Can be programmed as ADC input pin Pull high/low input configurable Belongs to LDO_AUX1 domain
P0_2/ADC_2	I/O PU_A	G8	Programmable GPIO. Can be programmed as ADC input pin Pull high/low input configurable Belongs to LDO_AUX1 domain
P0_3/ADC_3	I/O PU_A	F8	Programmable GPIO. Can be programmed as ADC input pin Pull high/low input configurable Belongs to LDO_AUX1 domain
P0_4/ADC_4	I/O PU_A	G9	Programmable GPIO. Can be programmed as ADC input pin Pull high/low input configurable Belongs to LDO_AUX1 domain
P0_5/ADC_5	I/O PU_A	G10	Programmable GPIO. Can be programmed as ADC input pin Pull high/low input configurable Belongs to LDO_AUX1 domain

Pin Name	Pad Type	Ball	Description
P0_6/ADC_6	I/O PU_A	F9	Programmable GPIO. Can be programmed as ADC input pin Pull high/low input configurable Belongs to LDO_AUX1 domain
P0_7/ADC_7	I/O PU_A	E7	Programmable GPIO. Can be programmed as ADC input pin Pull high/low input configurable Belongs to LDO_AUX1 domain
P1_0	I/O PU	F3	Programmable GPIO and MFB for power on and off Pull high/low input configurable Belongs to LDO_AUX1 domain  SWDCLK
P1_1	I/O PU	E3	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX1 domain  SWDIO
P1_2	I/O PU	F4	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX1 domain  SPI: CSN(SPI0_msater) SCK(SPI0_slave) SD HOST: SDH_CLK
P1_3	I/O PU	E4	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX1 domain  SPI: MISO(SPI0_msater) MOSI(SPI0_slave) SD HOST: SDH_CMD
P1_4	I/O PU	F5	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX1 domain  SPI: SCK(SPI0_msater) MISO(SPI0_slave) SD HOST: SDH_IO0
P1_5	I/O PU	F6	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX1 domain  SPI: MOSI(SPI0_msater) CSN(SPI0_slave) SDHOST SDH_IO1

Pin Name	Pad Type	Ball	Description
P1_6	I/O PU	H7	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX1 domain SDHOST: SDH_IO2
P1_7	I/O PU	F7	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX1 domain SDHOST: SDH_IO3
P2_0	I/O PU	B9	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX1 domain
P2_1	I/O PU	A8	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX2 domain SPI: CSN(SPI1_msater)
P2_2	I/O PU	C9	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX2 domain SPI: MISO(SPI1_msater)
P2_3	I/O PU	B8	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX2 domain SPI: MOSI(SPI1_msater)
P2_4	I/O PU	C8	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX2 domain SPI: SCK(SPI1_msater)
P2_5	I/O PU	D7	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX2 domain
P2_6	I/O PU	A7	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX2 domain
P2_7	I/O PU	B7	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX2 domain
P3_0	I/O PU	G6	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX1 domain

Pin Name	Pad Type	Ball	Description
P3_1	I/O PU	G5	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX1 domain
P4_0	I/O PU	C7	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX2 domain
P4_1	I/O PU	C6	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX2 domain

I/O: Bidirectional digital pad

I/O PU: Bidirectional digital pad with pull high resistor inside when in input mode

I/O PD: Bidirectional digital pad with pull low resistor inside when in input mode

I/O A: Bidirectional digital pad and programmable ADC

## 8.4. Audio Codec

Table 6. Audio Codec

Pin Name	Pad Type	Ball	Description
MIC1_N	AH	A3	MIC1 input negative pad, used as main MIC in dual MIC application. Programmable digital I/O, refer to MUX table
MIC1_P	AH	B3	MIC1 input positive pad, used as main MIC in dual MIC application. Programmable digital I/O, refer to MUX table
MIC2_N	AH	B4	MIC2 input negative pad, used as 2 <sup>nd</sup> MIC in dual MIC application. Programmable digital I/O, refer to MUX table (*) AUX input right channel pad. Programmable digital I/O, refer to MUX table
MIC2_P	AH	C4	MIC2 input positive pad, used as 2 <sup>nd</sup> MIC in dual MIC application. Programmable digital I/O, refer to MUX table (**) AUX input left channel pad. Programmable digital I/O, refer to MUX table
SPKR_N	AH	D3	Right channel speaker output negative Programmable digital I/O, refer to MUX table
SPKR_P	AH	C2	Right channel speaker output positive Programmable digital I/O, refer to MUX table
SPKL_N	AH	C3	Left channel speaker output negative Programmable digital I/O, refer to MUX table
SPKL_P	AH	D4	Left channel speaker output positive Programmable digital I/O, refer to MUX table
MICBIAS	PO	B2	Microphone bias output
VREF	PO	A2	Codec bandgap reference output, add a 1uF cap as close as possible.
AUXIN_R	AH	A5	AUX input right channel pad. Programmable digital I/O, refer to MUX table
AUXIN_L	AH	A4	AUX input left channel pad. Programmable digital I/O, refer to MUX table

AH: Analog and digital hybrid programmable

PO: Power output

## 8.5. Power Management

Table 7. Power Management

Pin Name	Pad Type	Ball	Description
VBAT	PIO	D11	Battery input when battery only Battery charge output when in charger mode with adapter in
ADP_IN	PI	C11	Adapter input for battery charge
HV_CORE	PO	F11	Switch output for switch mode regulator, add a 4.7uF cap as close as possible
LX_CORE	PO	E11	Switch mode regulator output, connect to a 2.2uH inductor as close as possible
VDDCORE	PI	G11	Switch mode regulator sense input and digital core power input
HV_AUDIO	PO	B11	Switch output for switch mode regulator, add a 4.7uF cap as close as possible
LX_AUDIO	PO	A11	Switch mode regulator output, connect to a 2.2uH inductor as close as possible
AVCC	PO	C1	Switch mode regulator sense input and power input for codec digital circuitry, 1.8V or 2.8V
AVCC_DRV	PI	B1	Power input for codec drive stage, 1.8V or 2.8V
VD33_PA	PI	H9	3.3V power input for RF PA
VD33_SYN	PI	H2	3.3V power input for RF synthesizer
VPA33	PO	G1	3.3V linear regulator output
VD12_SYN	PI	H3	1.2V power input for RF synthesizer
VD12_RTX	PI	F1	1.2V power input for RF circuitry
LDO_AUX1	PO	H8	Programmable linear regulator output for I/O
LDO_AUX2	PO	A9	Programmable linear regulator output for I/O
V33_USB	PO	A6	Power output, add 1uF cap
TADPSO	PO	F10	Power output, add 1uF cap
DIG_OUT	PO	H6	Power output, add 1uF cap
HV33	PO	C10	Power output, add 1uF cap
HV33_AON	PO	D9	Power output, add 1uF cap
SW_GND	GND	A10, B10, E10	Ground of switching power regulator
AGND	GND	D10	Ground of PMU analog block
DGND	GND	E9, D5, D6, E5, E6	Ground of digital circuitry
USB_GND	GND	B6	Ground of USB circuitry
RFGND	GND	D2, E2, F2, G2, G3	Ground of RF circuitry
XTAL_GND	GND	H5	Ground of crystal oscillator

PO: Power Output

PI: Power Input

PIO: Power Input and Output

## 8.6. System

**Table 8. System**

Pin Name	Pad Type	Ball	Description
HW_RST#	I_PU	G7	System reset input with internal pull high, low active with at least 5ms low to trigger system reset
USB_DP	AI/O	C5	USB signal positive
USB_DN	AI/O	B5	USB signal negative

*I\_PU: Input with internal pull high inside*

## 9. RF Radio

### 9.1. RF Radio

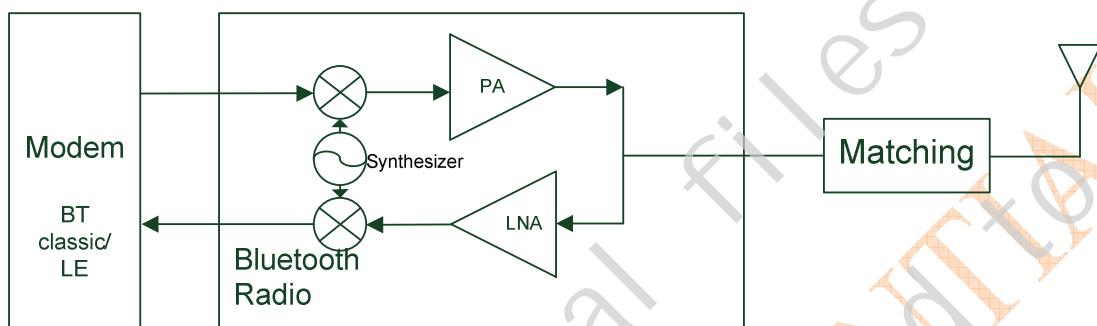


Figure 12. RF Radio

#### 9.1.1. Transceiver

Fully integrated radio transceiver compliant with Bluetooth SIG test specification. Designed for low power consumption and excellent transmit and receive performance in the ISM band.

#### 9.1.2. Transmitter

The Transmit mixer translates the baseband input signal to form the RF signal. It is designed to provide good stability and modulation characteristics.

The power amplifier integrated in the chip can provide up to 10 dBm in the ISM band.

#### 9.1.3. Receiver

This is a Low Noise Amplifier. It amplifies a low energy RF signal to the desired level without significantly increasing the noise power. When input power is high, the designed limits non-linearity.

The Receive mixer is a device whose input is an RF signal, and the output is an IF signal. The IF signal is then passed along the IF path to the demodulator.

The Synthesizer is a control loop to compare the crystal and VCO during their phases. If the VCO frequency shifts, then the phase difference produces an error signal for the control loop.

## 9.1.4. RF IQM and TPM

### 9.1.4.1 RF IQM

The RTL8763BO supports Bluetooth classic and Bluetooth BLE for all packages (known as the RF\_IQM path). TX radiation power is up to +10 dBm.

### 9.1.4.2 RF TPM

The RTL8763BO supports RF TPM, which is an extra low current consumption RF path for Bluetooth BLE. TX radiation power is up to +4 dBm.

In order to combine RF\_IQM and RF TPM into one antenna port, an SPDT circuit is required; refer to the RTL8763BO hardware instructions or the RTL8763BO reference circuit.

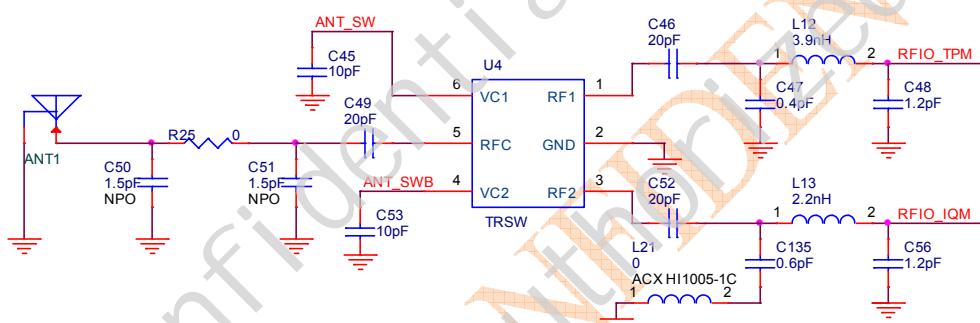


Figure 13. Reference Circuit

For HerzTek Internal Use Only.

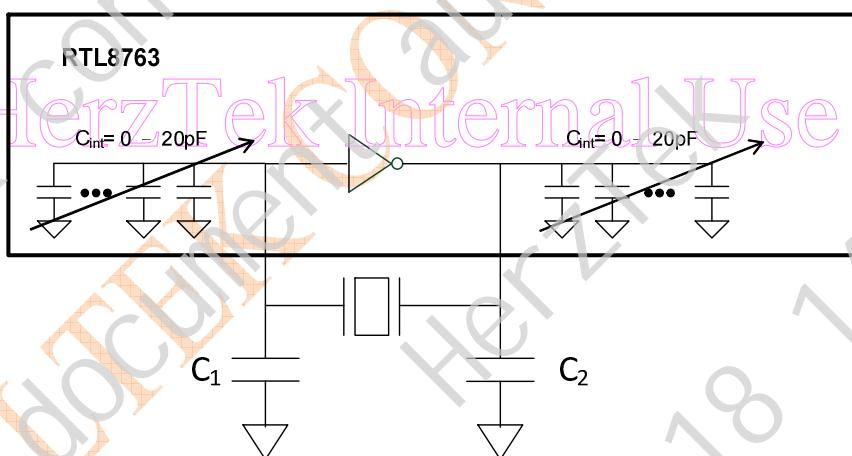
## 9.2. Crystal Oscillator

The RTL8763BO series has a built-in 40MHz crystal oscillation circuit to provide a stable, controllable system clock. With the built-in capacitor, the clock offset can be fine-tuned in the mass production process. The maximum internal cap is 20pF typically, and we suggest following the Realtek crystal design specification and QVL.

The external capacitors, C1 and C2, can be replaced by an internal cap, reducing the BOM cost, minimizing PCB dimensions, and providing flexibility for clock fine-tuning. The clock offset calibration procedure is supported with Realtek's MP GU hardware; contact Realtek's FAE for details.

**Table 9. Crystal Oscillator**

Parameter	Min.	Typ.	Max.
Frequency (MHz)	-	40	-
Frequency tolerance (ppm)	-	-	$\pm 10$
Frequency stability (ppm) over operating temperature	-	-	$\pm 10$
Load capacitance (pF)	7	9	-
Drive Level ( $\mu$ W)	-	-	300
Equivalent Series Resistance (Ohm)	-	-	$50\Omega @ 7\text{pF}$ $40\Omega @ 9\text{pF}$
Insulation Resistance (MOhm)	500	-	-



**Figure 14. 40MHz Crystal Specification Suggestion**

Example:

For a crystal with specification CL=9pF

$CL = [(C1 \times C2) / (C1 + C2)] + (C_{int} / 2) + C_{parasitic}$ , the parasitic capacitor  $C_{parasitic}$  can be observed on the PCB trace and IC SMT soldering pad....etc.

Rule of thumb says ' $C1 + C_{int}$ ' is typically 12~15pF, hence the external capacitor C1 and C2 can be replaced by the internal capacitor  $C_{int}$ , which can be 20pF at the maximum setting to cover the needs of external capacitors.

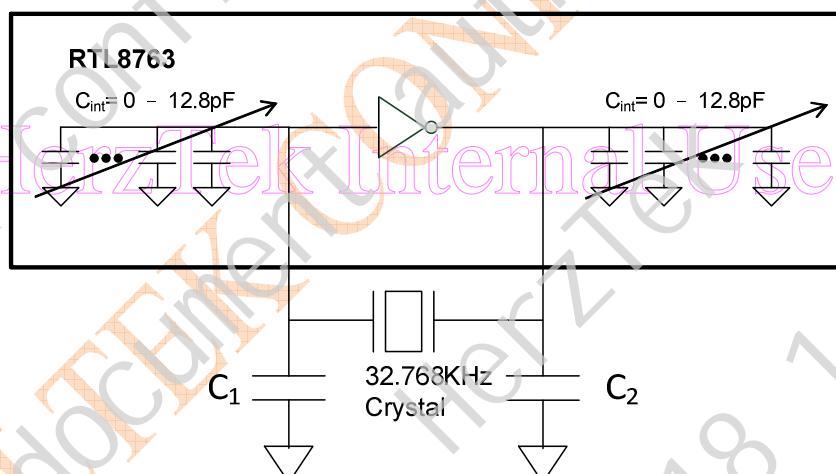
### 9.3. Crystal Oscillator 32.768kHz

The RTL8763BO has a built-in 32768Hz crystal oscillation circuit to provide a stable, controllable low power clock. With the internal built-in capacitor, the clock offset can be fine-tuned. The maximum internal cap is 12.8pF typically, and we suggest following the Realtek crystal design specifications and QVL.

If the CL specification of the crystal is 7pF, the external capacitor, C1 and C2, can be replaced by an internal cap, reducing the BOM cost, minimizing PCB dimensions, and providing flexibility for clock fine-tuning

**Table 10. Crystal Oscillator**

Parameter	Min.	Typ.	Max.
Frequency (kHz)	-	32.768	-
Frequency tolerance (ppm)	-	-	$\pm 20$
Load capacitance (pF)	-	7	-
Drive Level ( $\mu$ W)	-	-	0.5
Equivalent Series Resistance (KOhm)	-	-	90
Insulation Resistance (MOhm)	500	-	-



**Figure 15. 32.768kHz Crystal Specification Suggestion**

Example:

For a crystal with specification  $C_L=7\text{pF}$

$C_L = [(C_A \times C_B) / (C_A + C_B)] + C_{\text{parasitic}}$ , the parasitic capacitor  $C_{\text{parasitic}}$  can be observed on the PCB trace and IC SMT soldering pad....etc.

$$C_A = C_1 + C_{\text{int}}$$

$$C_B = C_2 + C_{\text{int}}$$

## 9.4. DSP

The RTL8763BO platform incorporates a Tensilica Hi-Fi DSP core to enable high-performance signal processing functions for Bluetooth audio/voice data streaming. With customized powerful instructions designed in the DSP, Figure 16 illustrates the DSP architecture and interfaces with other hardware functional blocks.

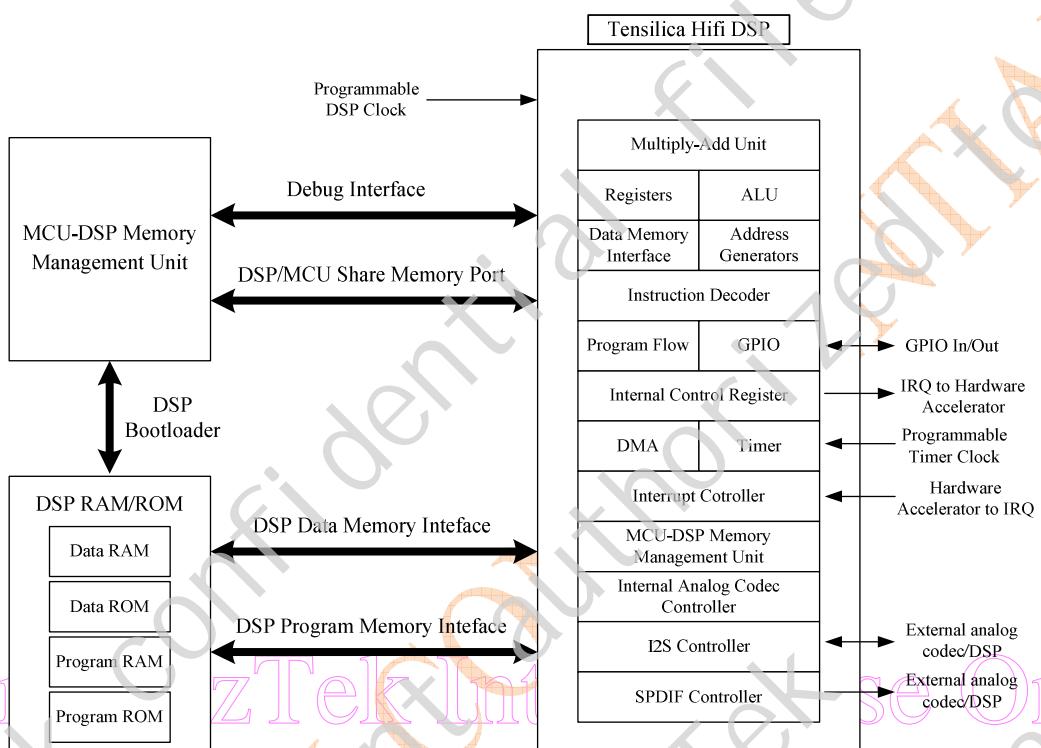


Figure 16. DSP Interfaces in RTL86xx IC Platform

**Key features of this DSP core include:**

- 160 MHz clock max
- Dual-issue VLIW architecture
- 32-bit ALU fixed-point DSP core
- Single-cycle flexible multiply-and-add (MAC) supporting capability:
  - Dual 24x24-bit MAC units with 56-bit accumulator
  - Single 32x16-bit MAC unit with 56-bit accumulator
- Variable-length (8/16/32/64-bit) data memory fetch
- Zero overhead looping
- Zero overhead circular buffering indexing
- Single cycle barrel shifter supporting up to 56-bit operation.
- Multi-cycle 32-bit divide
- Low overhead interrupt

## 9.5. Audio CODEC: DAC

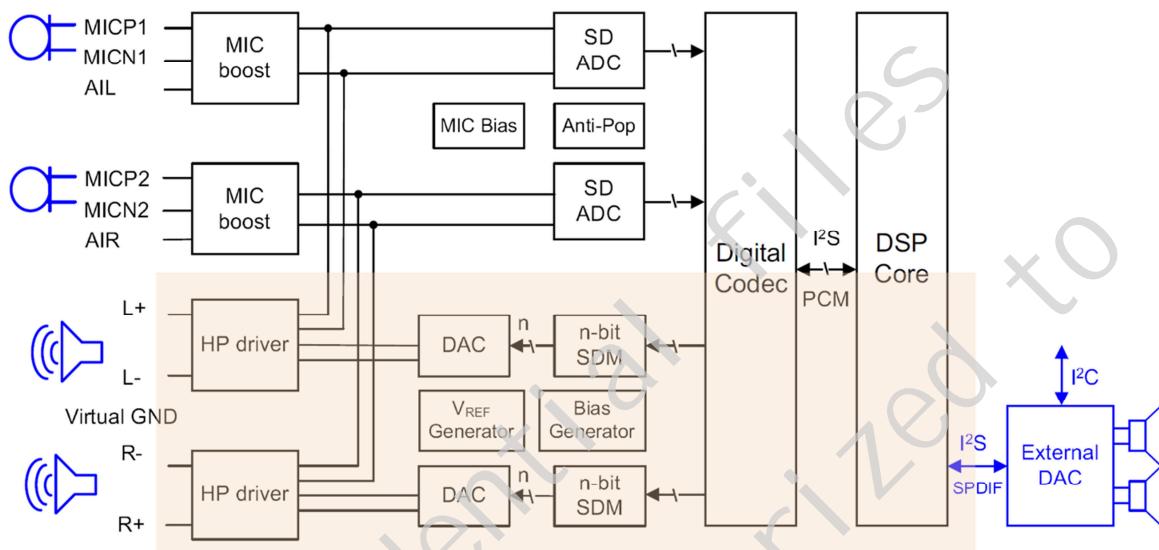


Figure 17. Codec and DAC Block Diagram

The RTL8763BO supports three types of analog audio output format

- Single-ended output
- Cap-less output
- Differential output

### 9.5.1. Single-Ended Output

In single-ended output mode, only SPK\_P drives the audio signal and bias on VREF DC level. An external 100 $\mu$ F capacitor is needed to do DC decoupling. The DC voltage must be eliminated as:

- DC voltage will create a large DC current on the speaker unit, which is designed for 16 or 32ohm, and result in power consumption issues
- The large DC current will result in heat issues on the speaker unit and possible burn out

The 100 $\mu$ F cap can be adjusted according to end product requirements.

## RTL8763BO MONO

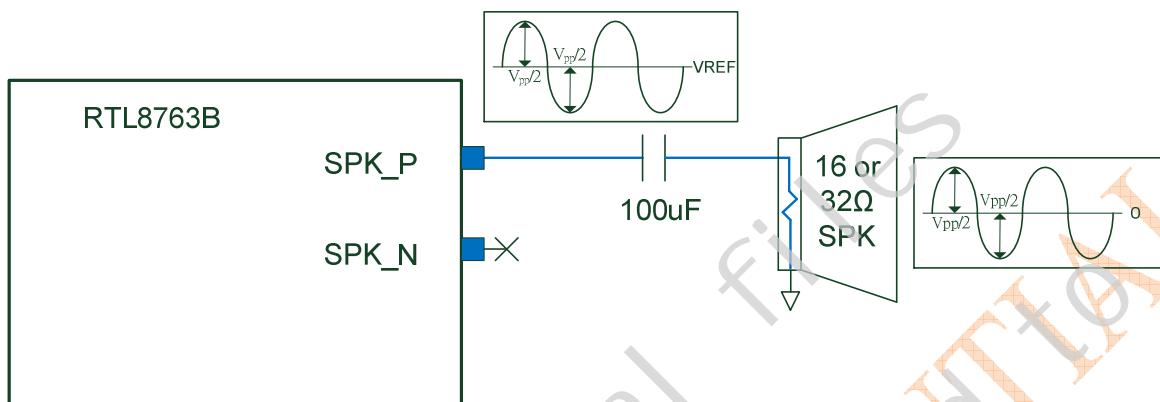


Figure 18. RTL8763BO MONO

## RTL8763BO STEREO

Crosstalk isolation between Right channel and Left channel should be below -80dB

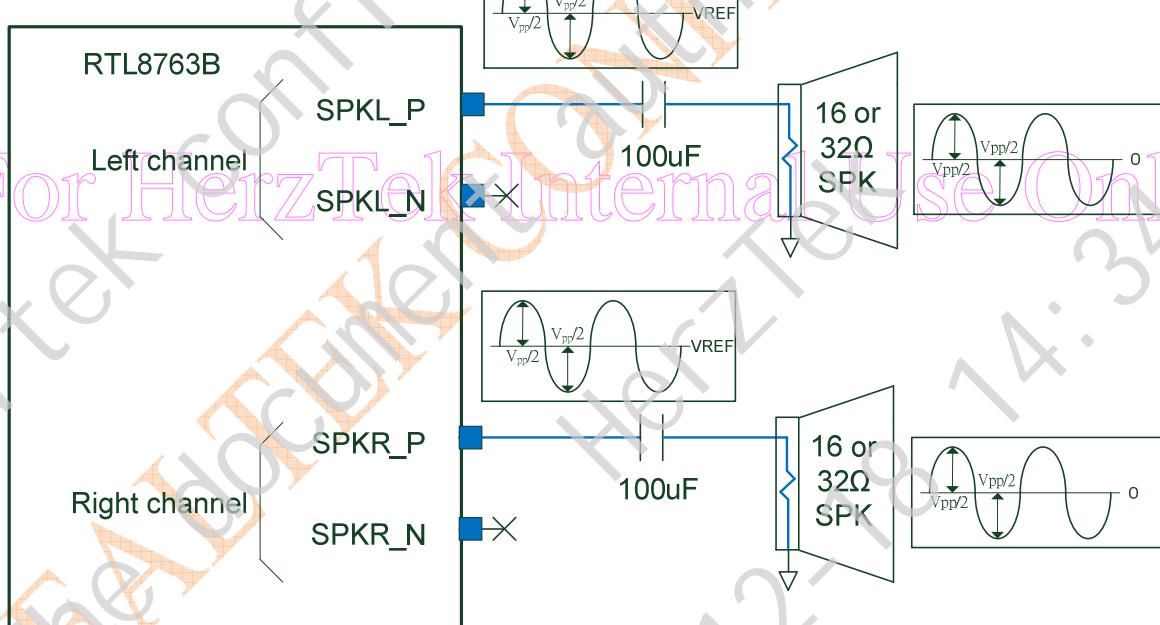


Figure 19. RTL8763BO STEREO

### 9.5.2. Cap-Less Output

In cap-less mode, SPK\_P drives the audio signal and bias on the VREF DC level. SPK\_N drives a bias VREF DC signal. Both SPK\_P and SPK\_N are connected to the speaker unit ‘PLUS’ and ‘MINUS’ nodes respectively. The DC signal can be cancelled without the need for a DC decoupling capacitor. The low frequency response is not degraded because there is no decoupling DC on the PCB path; hence the low frequency response is not changed.

The advantage: save one or two big capacitors in the BOM, save PCB design area and good audio low frequency response. The main application is for audio products, mono headset, and stereo headset.

#### RTL8763BO MONO

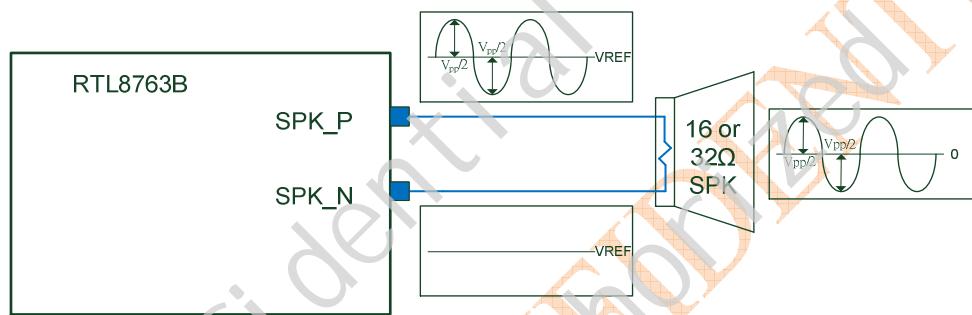


Figure 20. RTL8763BO MONO

#### RTL8763BO STEREO

Crosstalk isolation between Right channel and Left channel is lessened; approximately -50dB ~ -60dB only.

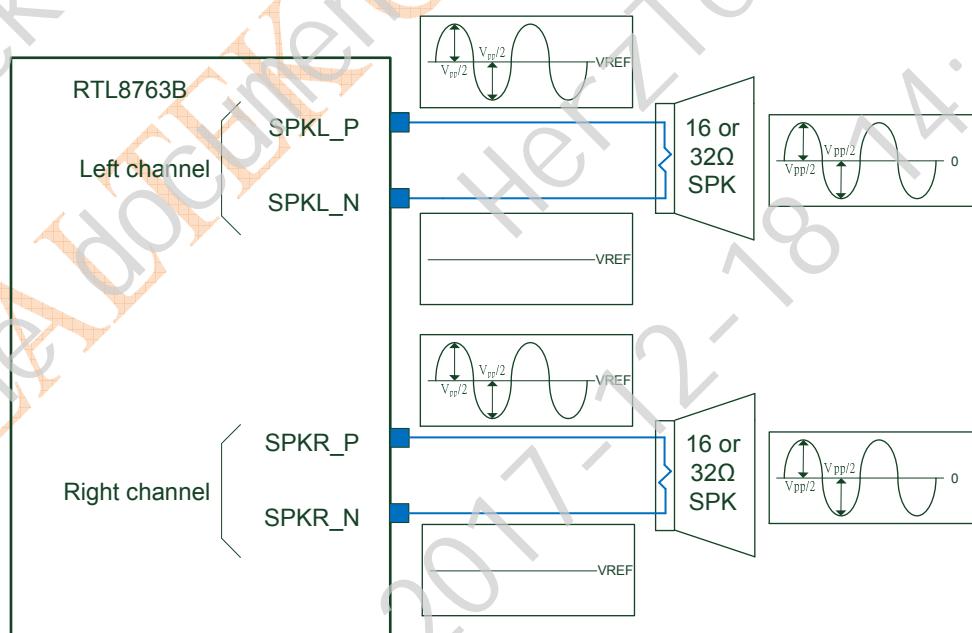


Figure 21. RTL8763BO STEREO

### 9.5.3. Differential Output

In differential mode, both SPK\_P and SPK\_N drive the audio signal and bias on VREF DC level. SPK\_P and SPK\_N are in one differential pair and drive a signal with  $180^\circ$  difference (reverse). The anti-interference performance is best when the signals are routed on the PCB. Both SPK\_P and SPK\_N are connected to speaker unit 'PLUS' and 'MINUS' node respectively. The DC signal can be cancelled without the need for a DC decoupling capacitor, and the signal swing (peak to peak Vpp) on the speaker unit will be doubled.

The low frequency response is not degraded as there is no decoupling capacitor on the path, hence the low frequency response is not changed. The advantage: save one or two big capacitors in the BOM, save PCB design area, good audio low frequency response, good anti-interference performance, and good crosstalk isolation between Right and Left channels. The solution is especially good for headband headset, and neckband headset.

#### RTL8763BO MONO

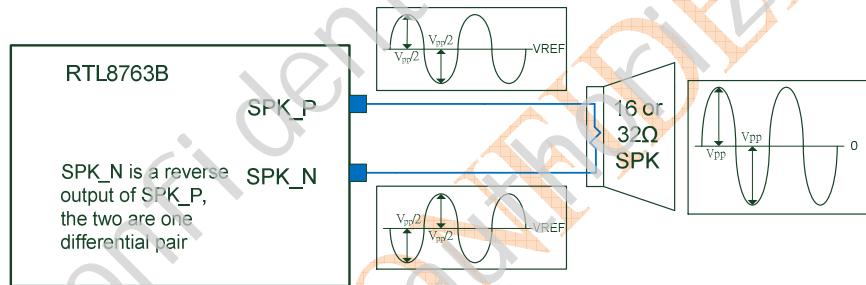


Figure 22. RTL8763BO MONO

#### RTL8763BO STEREO

Crosstalk isolation between Right channel and Left channel should be below -80dB

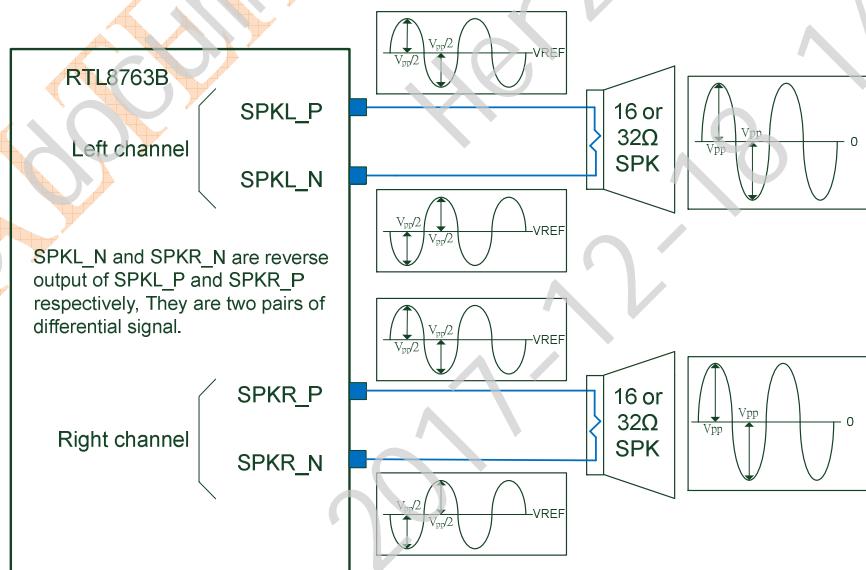


Figure 23. RTL8763BO STEREO

## 9.6. Audio CODEC: ADC

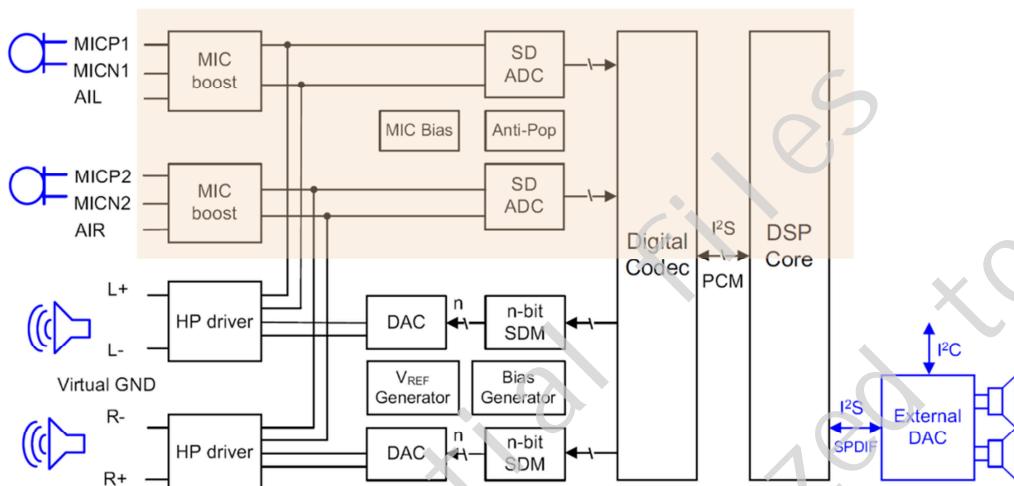


Figure 24. Codec and ADC Block Diagram

The RTL8763BO supports dual analog microphones, MIC2 and MIC1. MIC1 is treated as main microphone always, and MIC2 as the 2<sup>nd</sup> auxiliary in dual microphone applications. If MIC2 is not used, it can be configured as analog line input (AUX IN).

	1-MIC Application	2-MIC Application	Note
Main MIC	MIC1	MIC1	-
2 <sup>nd</sup> MIC	-	MIC1 MIC2	-
Audio line in (AUX IN)	MIC2	-	-

### Microphone Application with Biasing

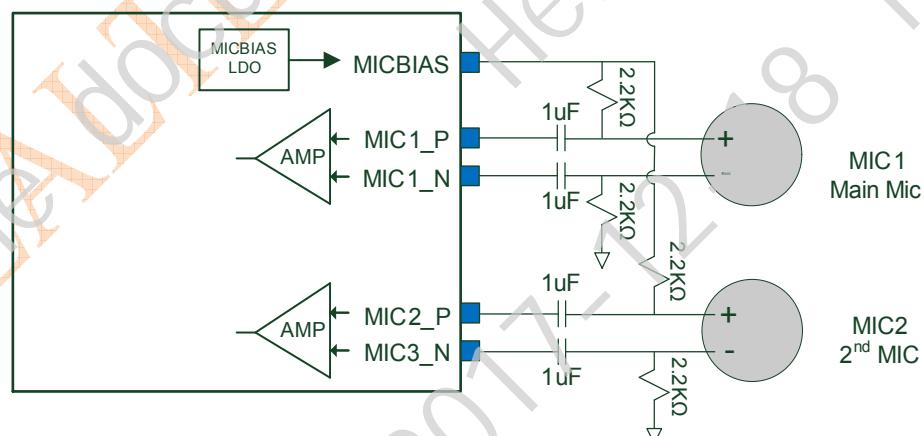
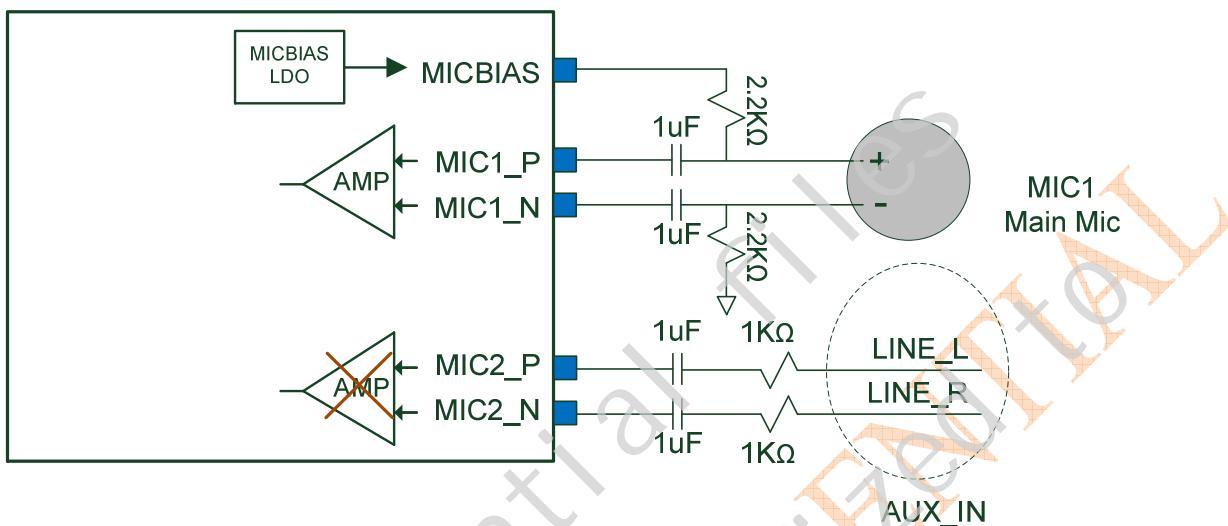


Figure 25. RTL8763BO Dual Microphone Reference

Note: UI configuration to enable MIC1 and MIC2 function; DSP configuration to set the AMP gain.

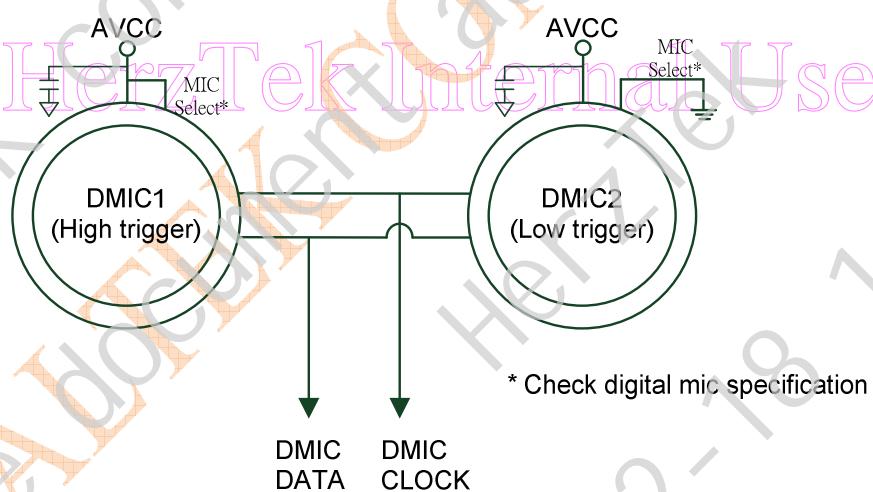
### RTL8763BO One Microphone and One AUX-IN



**Figure 26. RTL8763BO One Microphone and One AUX-IN Reference**

Note: UI configuration to enable MIC1 and AUX\_IN function; DSP configuration to set the AMP gain.

### 9.7. Audio Digital Microphone



**Figure 27. Audio Digital Microphone**

### Audio Digital Microphone Timing Diagram

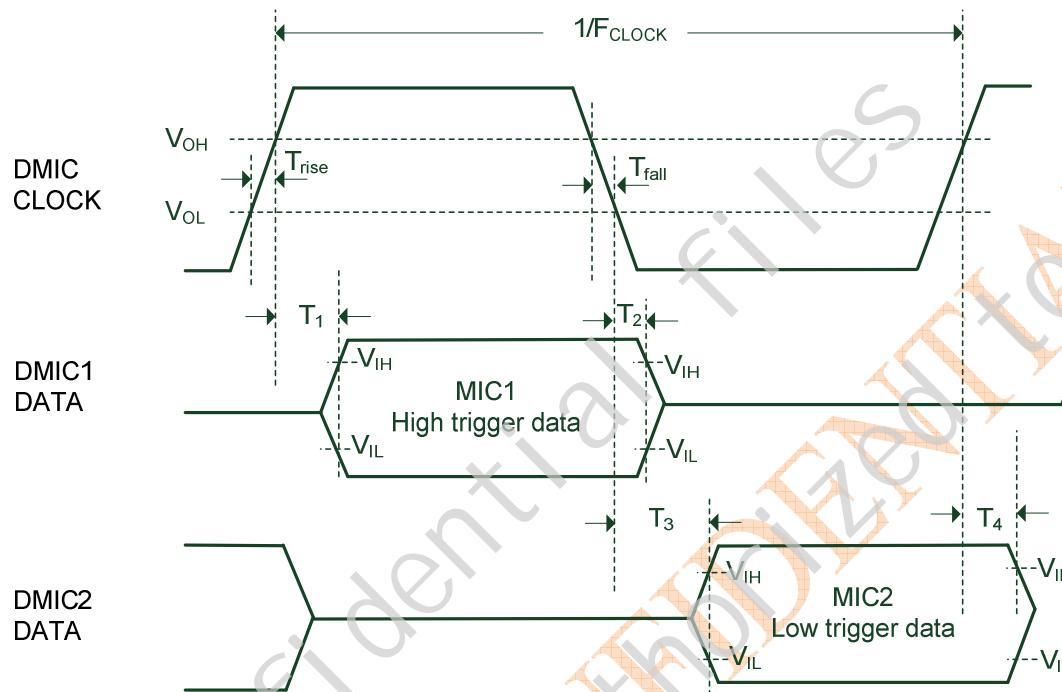


Figure 28. Audio Digital Microphone Timing Diagram

Table 11.1 Audio Digital Microphone Timing

	Min.	Typ.	Max.	Note
F <sub>CLOCK</sub>	312.5kHz	2.5MHz	5MHz	Supports five clock rates, 312.5K, 625K, 1.25M, 2.5M, 5M
Clock Duty	40%	-	60%	-
T <sub>rise</sub>	5	-	20	-
T <sub>fall</sub>	5	-	20	-
T1 (ns)	8	15	100	-
T2 (ns)	8	15	100	-
T3 (ns)	8	15	100	-
T4 (ns)	8	15	100	-

## 9.8. PCM I2S

The RTL8763BO supports two PCM/I2S digital audio output interfaces. The sampling rate can be from 8kHz to 192kHz to support middle quality and high quality I2S DAC. A MCLK for external DSP chip as main clock is also available from the RTL8763BO PLL, and can be enabled from the I/O MUX table in the UI tool. The MCLK can be programmed as 128\*BCLK or 256\*BCLK depending on the DSP specification, and with the I2C controller interface it provides a complete I2S control interface.

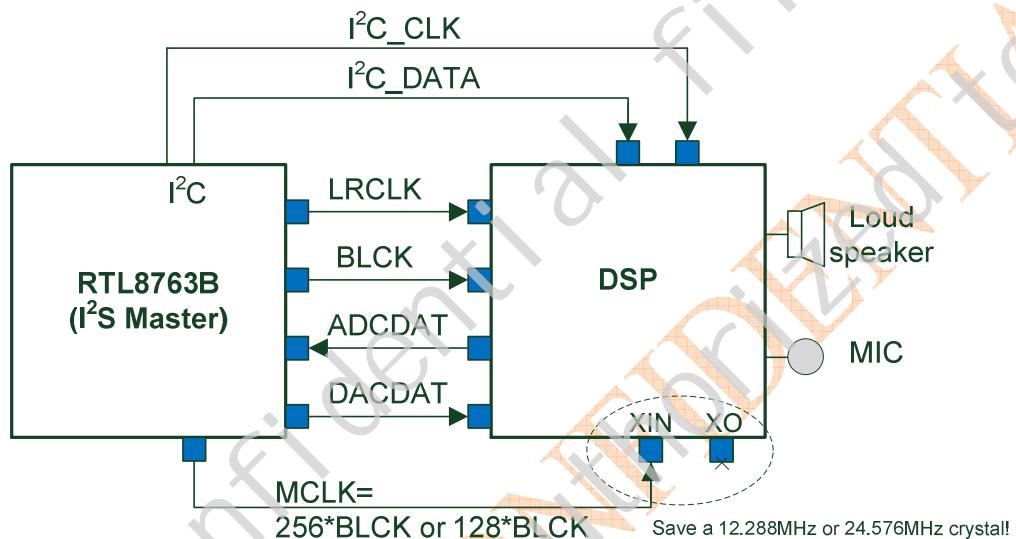


Figure 29. I2S Connection; RTL8763BO in Master Mode

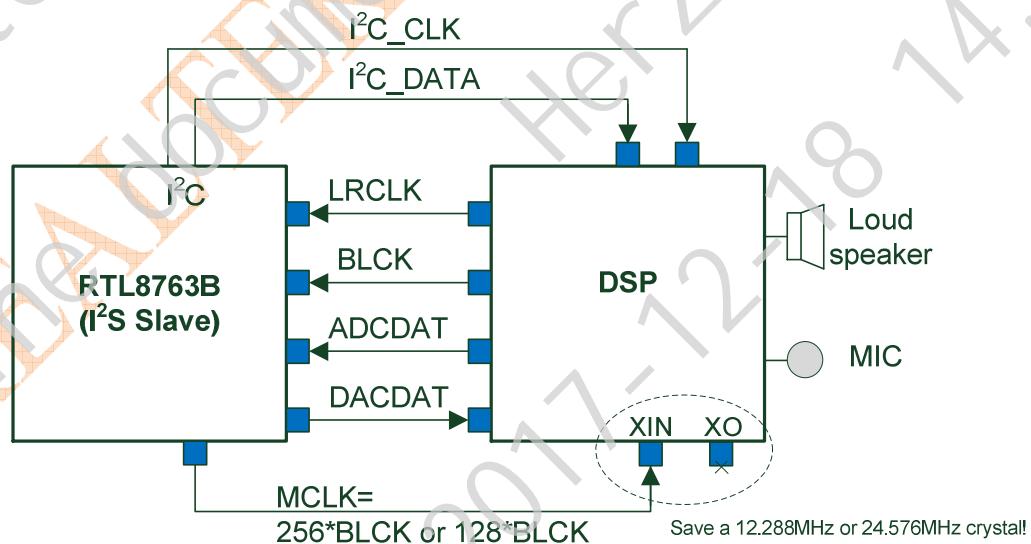
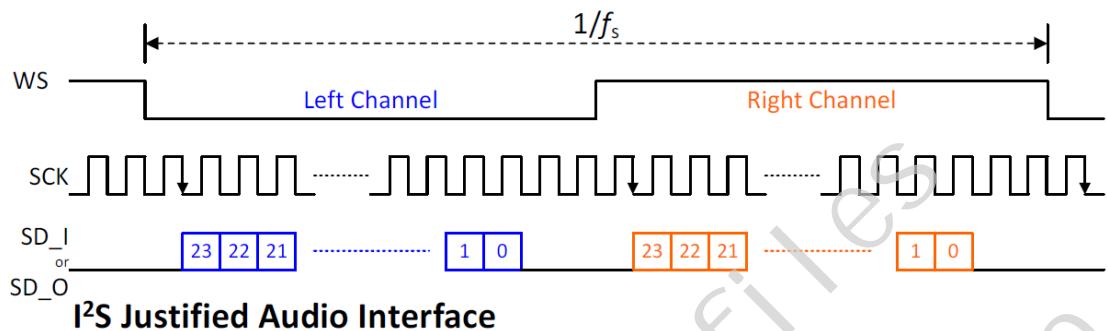
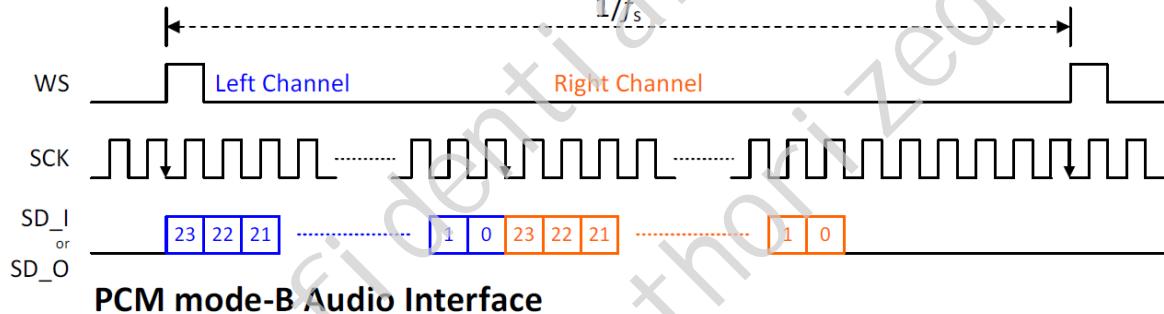
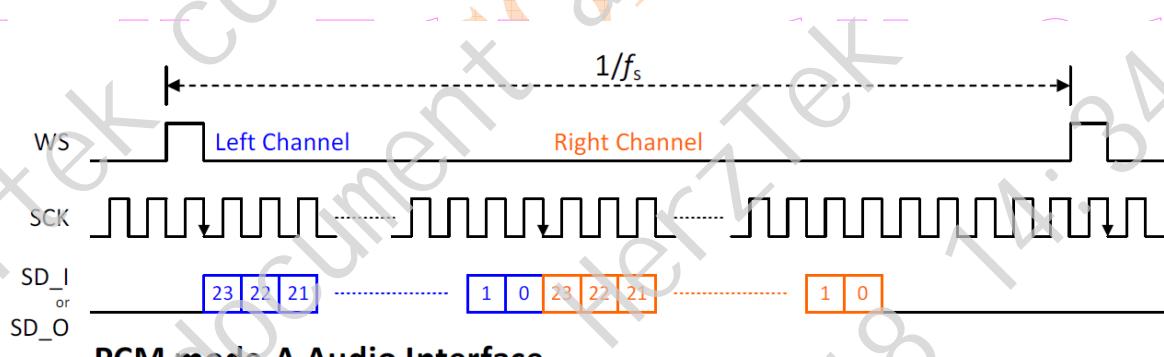


Figure 30. I2S Connection; RTL8763BO in Slave Mode


**I<sup>2</sup>S Justified Audio Interface**

**PCM mode-B Audio Interface**

**PCM mode-A Audio Interface**
**Figure 31. Timing Diagram**

Note: 'SCK' may to be inverted at any time if required.

## 9.9. *UART Interface*

The RTL8763BO supports a UART interface for FLASH memory parameter programming, and UART commands for MCU application. For the UART command application, refer to the ‘Realtek UART command set’ document.

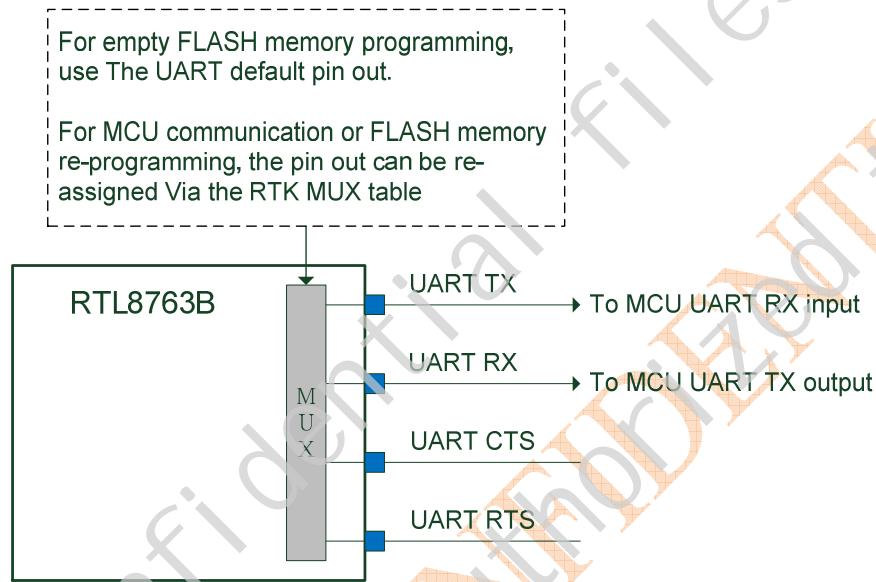


Figure 32. **UART Interface**

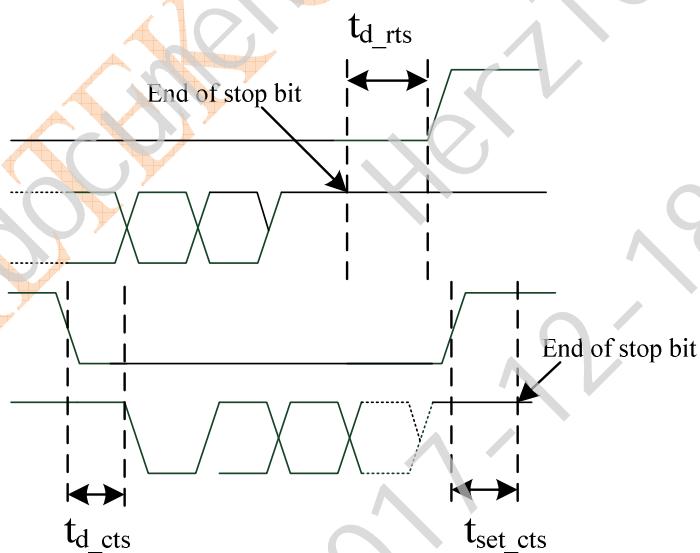


Figure 33. **UART Interface Timing Diagram**

**Table 12. UART Timing Characteristics**

Parameter	Symbol	Min	Typical	Max
Timing between RX Stop bit and RTS go high when RX FIFO is full (symbol time)	$t_{d\_rts}$	-	-	0.5
Timing between CTS go low and device send first bit (ns)	$t_{d\_cts}$	-	-	25
Timing between CTS go high and TX send stop bit (ns)	$t_{set\_cts}$	75	-	-

**Table 13. UART Data Error Rate Estimation Based On Various Baud Rates**

UART Classification	Baud rate	Error
-	1200	0.08%
-	9600	0.08%
-	14400	0.08%
-	19200	0.4%
-	28800	0.28%
-	38400	0.15%
-	57600	0.02%
-	76800	0.01%
Default Rate	115200	0.08%
-	128000	0
-	153600	0.22%
-	230400	0.08%
-	460800	0.11%
-	500000	0
-	921600	0.11%
-	1000000	0
-	1843200	0.14%
-	2000000	0
-	3000000	0.3%
Maximum Rate	4000000	0

**Table 14. UART (Base Address: 0x4001\_2000)**

Offset	Bit	Access	INI	Symbol	Description
<b>DLL</b>					
0x00	[31:8]	-	-	Reserved	-
	[7:0]	R/W	0	DLL	This register is the baud rate divisor[7:0], can be programmed only when the DLAB bit of LCR bit [7] = 1.

Offset	Bit	Access	INI	Symbol	Description
<b>DLH_INTCR</b>					
0x04	[31:0]	R/W	0	DLH	This register is the baud rate divisor[15:8], can be programmed only when the DLAB bit of LCR bit [7] = 1. 7:0 dlm RW Divisor [15:8]; accessible when DLAB = 1 31:8 Rsvd Reserved
	[3]	R/W	0	INTCR(edssi)	Enable Modem Status Interrupt (EDSSI) (modem status transition) 0: Disabled 1: Enabled
	[2]	R/W	0	INTCR(elsi)	Enable Receiver Line Status Interrupt (ELSI) (receiver line status) 0: Disabled 1: Enabled
	[1]	R/W	0	INTCR(etbei)	This register allows enabling and disabling interrupt generation by the UART. It can be accessed only when the DLAB bit of LCR bit [7] = 0. Enable Transmitter FIFO Empty interrupt (ETBEI) (tx fifo empty) 0: Disabled 1: Enabled
	[0]	R/W	0	INTCR(erbi)	This register allows enabling and disabling interrupt generation by the UART. It can be accessed only when the DLAB bit of LCR bit [7] = 0. enable Received Data Available Interrupt (ERBFI) (rx trigger or timeout) 0: Disabled 1: Enabled
<b>INTID_FCR</b>					
0x08	[12:8]	W	0	rxfifo_trigger_level	Define the 32-entries Receiver FIFO Interrupt trigger level 1~32 bytes
	[7:4]		-	Reserved	-
	[3]	W	-	dma_mode	Support dma mode. (cooperate with DW DDMA in the data path)
	[2]	W1C	-	clear_txfifo	Writing a Logic 1 clears the Transmitter FIFO and resets its logic. The shift register is not cleared, i.e., transmitting of the current character continues.
	[1]	W1C	-	clear_rxfifo	Writing a Logic 1 to Bit 1 clears the Receiver FIFO and resets its logic. But it does not clear the shift register, i.e. receiving of the current character continues.

Offset	Bit	Access	INI	Symbol	Description
0x0C	[3:1]	R	0	int_id[2:0]	<p>Bit3~Bit1 displays the list of possible interrupts along with the bits they enable, priority, and their source and reset control.</p> <p>3'b011: Interrupt Priority: 1st priority (int_3)  Interrupt Type: Receiver Line Status (read lsr)</p> <p>3'b010: Interrupt Priority: 2nd priority  Interrupt Type: Receiver Data Available or trigger level reached.(int_2)</p> <p>3'b110: Interrupt Priority: 2nd priority  Interrupt Type: Timeout Indication</p> <p>3'b001: Interrupt Priority: 3rd priority  Interrupt Type: Transmitter holding register TXFIFO empty</p> <p>3'b000: Interrupt Priority: 4th priority  Interrupt Type: Modem Status</p>
	[0]	R	0	int_pend	Indicates whether an interrupt is pending 0: an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine 1: no interrupt is pending
<b>LCR</b>					
0x0C	[7]	R/W	0	dlab	<p>Divisor Latch Access bit  0: the divisor latches can not be accessed  1: The divisor latches can be accessed  Note: DLL/DLM only can be access when dlab bit = 1  IER only can be access when dlab bit = 0  THR/RBR don't care about dlab bit value.</p>
	[6]	R/W	0	break_ctrl	<p>Break Control bit  '0' – break is disabled  '1' – the serial out is forced into logic '0' (break state).  Break control bit causes a break condition to be transmitted to the receiving UART. When it is set to a logic 1, the serial output (Sout) is forced to the Spacing ( logic 0 ) state.  The break is disabled by setting bit 6 to a logic 0. The Break Control bit acts only on SOUT and has no effect on the transmitter logic</p>
	[5]	R/W	0	stickParity	<p>Stick Parity bit.  1: Stick Parity bit as 1'b1  0: Stick Parity bit as 1'b0</p>

Offset	Bit	Access	INI	Symbol	Description
	[4]	R/W	0	even_parity_sel	Even Parity select 0: Odd number of Logic 1 is transmitted and checked in each word ( data and parity combined). In other words, if the data has an even number of 1 in it, then the parity bit is 1 1: Even number of 1 is transmitted in each word.
	[3]	R/W	0	parity_en	Parity Enable 0: No parity 1: Parity bit is generated on each outgoing character and is checked on each incoming one.
	[2]	R/W	0	stb	This bit specifies the number of Stop bits transmitted and received in each serial character. 0: 1 stop bits. 1: 2 stop bits. Note that the receiver always checks the first stop bit only.
	[0]	R/W	1	wls0	Word length selection 0 0: data is 7 bit word length. 1: data is 8 bit word length.

**MCR**

0x10	[7:6]	-	-	Reserved	-
	[5]	R/W	0	autoflow_en	AutoFlow Enable (AFE) This Bit (AFE) is the auto flow control enable.
	[4:2]	-	-	RESERVED	-
	[1]	R/W	0	rts	Request to Send (RTS) signal control 0 RTS is logic 1 1 RTS is logic 0 This bit controls the Request to Send (RTS_) output. Bit 1 affects the RTS_ output in a manner identical to that described above for bit 0.
	[0]	-	-	RESERVED	-
	<b>LSR</b>				
0x14	[7]	R	0	rxfifo_err	Uart_rx_error

Offset	Bit	Access	INI	Symbol	Description
	[6]	R	1	TXFIFO_empty	Transmitter Empty (TEMT) indicator 0:Otherwise 1: This bit is set to logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to one whenever the transmitter FIFO and shift register are both empty.
	[5]	R	1	TXFIFO empty indicator	TXFIFO empty indicator. 0: Otherwise 1: It indicates that the UART is ready to accept a new character for transmission
	[4]	R	0	break_err_int	Break Interrupt (BI) indicator 0: No break condition in the current character 1: set to logic 1 whenever the received data input is held in the Spacing ( logic 0) state for a longer than a full word transmission time
	[3]	R	0	framing_err	Framing Error (FE) indicator 0: No framing error in the current character 1: The received character at the top of the FIFO did not have a valid stop bit.
	[2]	R	0	parity_err	Parity Error (PE) indicator 0: No parity error in current character 1: Indicates that the received data character does not have the correct even or odd parity
	[1]	R	0	overrun_err	Overrun Error (OE) indicator 0: No Overrun state 1: Indicates that data in the Receiver Buffer Register RX FIFO not read by the CPU
	[0]	R	0	rxfifo_datardy	Data Ready (DR) indicator 0: No characters in the Receiver FIFO 1: At least one character has been received and transferred into the Receiver Buffer Register or the FIFO.
<b>SPR</b>					
0x1C	[31:27 ]	-	-	Reserved	-
	[26:16]	R/W	0	xfactor_adj[10:0]	One factor of Baud rate calculation, i.e., the ovsr_adj[10:0] of following formula.
	[15:8]	-	-	Reserved	-

Offset	Bit	Access	INI	Symbol	Description
0x20	[7]	R/W	0	-	rx break signal interrupt status Write one clear.
	[6]	R/W	0	-	rx break signal interrupt enable
	[5]	R/W	0	-	fl_set_bit_err
	[4]	R/W	0	-	fl_frame_err
	[3:0]	-	-	Reserved	-
<b>STSReg</b>					
0x20	[7:4]	R/W	0xb	xfactor	factor of Baud rate calculation, i.e., the ovsr[3:0] of following formula.
	[3]	R/W	0	Reset_rcv	Reset Uart Receiver
	[2:0]	-	-	Reserved	-
<b>RB THR</b>					
0x24	[7:0]	R	0	RX data	0 rxdatabit0 R Rx data bit 0 Note: Bit 0 is the least significant bit. It is the first bit serially received. 1 rxdatabit1 R Rx data bit 1 2 rxdatabit2 R Rx data bit 2 3 rxdatabit3 R Rx data bit 3 4 rxdatabit4 R Rx data bit 4 5 rxdatabit5 R Rx data bit 5 6 rxdatabit6 R Rx data bit 6 7 rxdatabit7 R Rx data bit 7 31:8 Rsvd Reserved
	[7:0]	W	-	TX data	0 txdatabit0 W Tx data bit 0 Note: Bit 0 is the least significant bit. It is the first bit serially transmitted. 1 txdatabit1 W Tx data bit 1 2 txdatabit2 W Tx data bit 2 3 txdatabit3 W Tx data bit 3 4 txdatabit4 W Tx data bit 4 5 txdatabit5 W Tx data bit 5 6 txdatabit6 W Tx data bit 6 7 txdatabit7 W Tx data bit 7 31:8 Rsvd Reserved
<b>MISCR</b>					
0x28	[12:8]	R/W	0	rxdma_burstsize	Rxdma burstsize
	[7:3]	R/W	0	txdma_burstsize	Txdma burstsize
	[2]	R/W	0	rxdma_en	1: rxdma is enabled (valid when dma_mode in FCR is 1'b1) 0: rxdma is disabled
	[1]	R/W	0	txdma_en	1: txdma is enabled (valid when dma_mode in FCR is 1'b1) 0: txdma is disabled
	[0]	-	-	Reserved	-

Offset	Bit	Access	INI	Symbol	Description
<b>RX_IDLE_INTCR</b>					
0x40	[31]	R/W	0	RX_IDLE_TIMEOUT_EN	RX_IDLE_TIMEOUT Enable, default 0.
	[30:4]	-	-	Reserved	-
	[3:0]	R/W	0	RXIDLE_Timeout_Value[3:0]	Default 0. 4'd0: 8 bit time. (1*8) 4'd1: 16 bit time. (2*8) 4'd2: 32 bit time. (2^2*8) 4'd3: 64 bit time. (2^3*8) 4'd4: 128 bit time. (2^4*8) 4'd5: 256 bit time. (2^5*8) 4'd6: 512 bit time. (2^6*8) 4'd7: 1024 bit time. (2^7*8) 4'd8: 2048 bit time. (2^8*8) 4'd9: 4096 bit time. (2^9*8) 4'd10: 8192 bit time. (2^10*8) 4'd11: 16384 bit time. (2^11*8) 4'd12: 32768 bit time. (2^12*8) 4'd13: 65535 bit time. (2^13*8) 4'd14: 131072 bit time. (2^14*8) 4'd15: 262144 bit time. (2^15*8)
<b>RX_IDLE_SR</b>					
0x44	[31:1]	-	-	Reserved	-
	[0]	R W1C	0	RXIDLE_TIMEOUT_INT_STS	interrupt status of RX IDLE timeout. Write 1 to clear.
<b>RXIDLE_INTCR</b>					
0x48	[31:1]	-	-	Reserved	-
	[0]	R/W	0	RXIDLE_TIMEOUT_INT_EN	RX idle timeout interrupt enable
<b>FIFO_LEVEL</b>					
0x4c	[13:8]	R	0	RX_FIFO_LEVEL	rx fifo character count
	[4:0]	R	0	TX_FIFO_LEVEL	tx fifo character count

## 9.10. I2C Interface

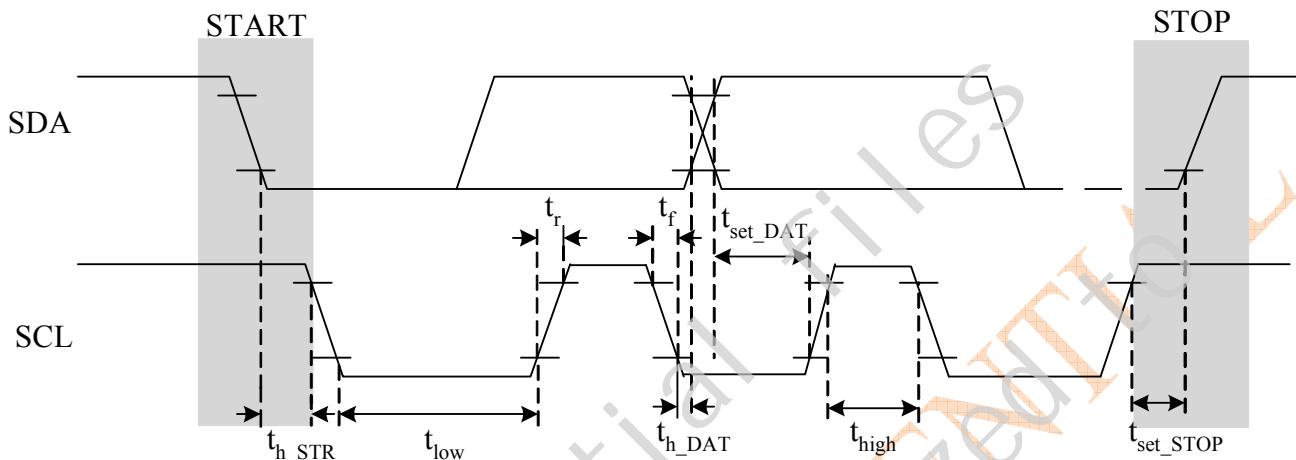


Figure 34. I2C Interface Timing Diagram

Table 15. I2C Timing Characteristics

Parameter	Symbol	Min	Typical	Max
SCL clock frequency (kHz)	-	-	-	400
High period of SCL (ns)	$t_{high}$	600	-	-
Low period of SCL (ns)	$t_{low}$	1300	-	-
Hold time of START (ns)	$t_{h\_STR}$	600	-	-
Hold time of DATA (ns)	$t_{h\_DAT}$	0	-	-
Setup time of STOP (ns)	$t_{set\_STOP}$	600	-	-
Setup time of DATA (ns)	$t_{set\_DAT}$	100	-	-
Rise time of SCL and SDA (ns) (with 4.7k ohm resistor pulled high)	$t_r$	See note	-	-
Fall time of SCA and SDA (ns)	$t_f$	See note	-	-

Note: Depends on the external bus pull up resistor.

Table 16. I2C (Base Address: 0x4001\_5000(I2C0) & 0x4001\_5400(I2C1))

Offset	Bit	Access	INI	Symbol	Description
IC_CON					
0x00	[15:7]	-	-	Reserved	-
	[6]	R/W	0x1	IC_SLAVE_DISABLE	Controls whether I2C has its slave disabled 0: Slave is enabled 1: Slave is disabled
	[5]	R/W	0x1	IC_RESTART_EN	Determines Whether RESTART Conditions May Be Sent When Acting As A Master 0: Disable 1: Enable

Offset	Bit	Access	INI	Symbol	Description
0x04	[4]	R	0x1	IC_10BITADDR_MASTER_RD_ONLY	Function of this bit is handled by bit 12 of IC_TAR register, and this bit is read-only 0: 7-bit addressing 1: 10-bit addressing
	[3]	R/W	0x1	IC_10BITADDR_SLAVE	When acting as a slave, this bit controls whether the I2C responds to 7- or 10-bit addresses. 0: 7-bit addressing. 1: 10-bit addressing.
	[2:1]	R/W	0x3	SPEED	These bits control at which speed the I2C operates; its setting is relevant only if one is operating the I2C in master mode. 1: Standard mode (0 to 100 kbit/s) 2: Fast mode ( $\leq$ 400 kbit/s) 3: Reserved
	[0]	R/W	0x1	MASTER_MODE	This bit controls whether the I2C master is enabled. 0: Master disabled 1: Master enabled
<b>IC_TAR</b>					
0x04	[15:13]	-	-	RESERVED	-
	[12]	R/W	0x1	IC_10BITADDR_MASTER	controls whether the I2C starts its transfers in 7- or 10-bit addressing mode when acting as a master. 0: 7-bit addressing 1: 10-bit addressing
	[11:10]	-	-	RESERVED	-
	[9:0]	R/W	0x55	IC_TAR	This is the target address for any master transaction
<b>IC_SAR</b>					
0x08	[9:0]	R/W	0x55	IC_SAR	The IC_SAR holds the slave address when the I2C is operating as a slave.
<b>RESERVED</b>					
0x0C	-	-	-	-	-
<b>IC_DATA_CMD</b>					
0x10	[15:11]	-	-	Reserved	-
	[10]	W	-	RESTART	This bit controls whether a RESTART is issued before the byte is sent or received. 1: If IC_RESTART_EN is 1, a RESTART is issued before the data is 0: If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.

Offset	Bit	Access	INI	Symbol	Description
	[9]	W	-	STOP	This bit controls whether a STOP is issued after the byte is sent or received. 1: STOP is issued after this byte, regardless of whether or not the Tx FIFO is empty. 0: STOP is not issued after this byte
	[8]	W	-	CMD	This bit controls whether a read or a write is performed. This bit does not control the direction when the I2C acts as a slave. It controls only the direction when it acts as a master. 1: Read 0: Write
	[7:0]	R/W	0	DATA	This register contains the data to be transmitted or received on the I2C bus.
<b>IC_SS_SCL_HCNT</b>					
0x14	[15:0]	R/W	0x190	IC_SS_SCL_HCNT	Standard speed I2C Clock SCL High Count
<b>IC_SS_SCL_LCNT</b>					
0x18	[15:0]	R/W	0x1d6	IC_SS_SCL_LCNT	Standard speed I2C Clock SCL Low Count
<b>IC_FS_SCL_HCNT</b>					
0x1C	[15:0]	R/W	0x3c	IC_FS_SCL_HCNT	Fast speed I2C Clock SCL High Count
<b>IC_FS_SCL_LCNT</b>					
0x20	[15:0]	R/W	0x82	IC_FS_SCL_LCNT	Fast speed I2C Clock SCL Low Count
<b>IC_INTR_STAT</b>					
0x2C	[15:12]	-	-	Reserved	-
	[11]	R	0	-	R_GEN_CALL
	[10]	R	0	-	R_START_DET
	[9]	R	0	-	R_STOP_DET
	[8]	R	0	-	R_ACTIVITY
	[7]	R	0	-	R_RX_DONE
	[6]	R	0	-	R_TX_ABRT
	[5]	R	0	-	R_RD_REQ
	[4]	R	0	-	R_TX_EMPTY
	[3]	R	0	-	R_TX_OVER
	[2]	R	0	-	R_RX_FULL
	[1]	R	0	-	R_RX_OVER
	[0]	R	0	-	R_RX_UNDER
<b>IC_INTR_MASK</b>					
0x30	[15:12]	-	-	Reserved	-
	[11]	R/W	1	-	M_GEN_CALL
	[10]	R/W	0	-	M_START_DET

Offset	Bit	Access	INI	Symbol	Description
[9]	R/W	0	-	M_STOP_DET	
	R/W	0	-	M_ACTIVITY	
	R/W	1	-	M_RX_DONE	
	R/W	1	-	M_TX_ABRT	
	R/W	1	-	M_RD_REQ	
	R/W	1	-	M_TX_EMPTY	
	R/W	1	-	M_TX_OVER	
	R/W	1	-	M_RX_FULL	
	R/W	1	-	M_RX_OVER	
	R/W	1	-	M_RX_UNDER	
<b>IC_RX_TL</b>					
0x38	[7:0]	R/W	0xb	RX_TL	I2C Receive FIFO Threshold Controls the level of entries (or above) that triggers the RX_FULL interrupt
<b>IC_TX_TL</b>					
0x3C	[7:0]	R/W	0x3	TX_TL	I2C Transmit FIFO Threshold Controls the level of entries (or below) that trigger the TX_EMPTY interrupt
<b>IC_CLR_INTR</b>					
0x40	[0]	R	-	IC_CLR_INTR	Clear Combined and Individual Interrupts Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register
<b>IC_CLR_RX_UNDER</b>					
0x44	[0]	R	-	IC_CLR_RX_UNDER	Read this register to clear the RX_UNDER interrupt
<b>IC_CLR_RX_OVER</b>					
0x48	[0]	R	-	IC_CLR_RX_OVER	Read this register to clear the RX_OVER interrupt
<b>IC_CLR_TX_OVER</b>					
0x4C	[0]	R	-	IC_CLR_TX_OVER	Read this register to clear the TX_OVER interrupt
<b>IC_CLR_RD_REQ</b>					
0x50	[0]	R	-	IC_CLR_RD_REQ	Read this register to clear the RD_REQ interrupt
<b>IC_CLR_TX_ABRT</b>					
0x54	[0]	R	-	IC_CLR_TX_ABRT	Read this register to clear the TX_ABRT interrupt
<b>IC_CLR_RX_DONE</b>					
0x58	[0]	R	-	IC_CLR_RX_DONE	Read this register to clear the RD_DONE interrupt

Offset	Bit	Access	INI	Symbol	Description
<b>IC_CLR_ACTIVITY</b>					
0x5C	[0]	R	-	IC_CLR_ACTIVITY	<p>Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore.</p> <p>If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set.</p> <p>It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus</p>
<b>IC_CLR_STOP_DET</b>					
0x60	[0]	R	-	IC_CLR_STOP_DET	Read this register to clear the STOP_DET interrupt
<b>IC_CLR_START_DET</b>					
0x64	[0]	R	-	IC_CLR_START_DET	Read this register to clear the START_DET interrupt
<b>IC_ENABLE</b>					
0x6C	[0]	R/W	0	IC_ENABLE	<p>Controls whether the I2C is enabled.</p> <p>0: Disables I2C (TX and RX FIFOs are held in an erased state)</p> <p>1: Enables I2C</p>
<b>IC_STATUS</b>					
0x70	[31:7]	-	-	Reserved	-
	[6]	R	0	SLV_ACTIVITY	<p>Slave FSM Activity Status.</p> <p>0: Slave FSM is in IDLE</p> <p>1: Slave FSM is active</p>
	[5]	R	0	MST_ACTIVITY	<p>Master FSM Activity Status</p> <p>0: Master FSM is in IDLE</p> <p>1: Master FSM is active</p>
	[4]	R	0	RFF	<p>Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set</p> <p>0: Receive FIFO is not full</p> <p>1: Receive FIFO is full</p>
	[3]	R	0	RFNE	<p>Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries</p> <p>0: Receive FIFO is empty</p> <p>1: Receive FIFO is not empty</p>
	[2]	R	1	TFE	<p>Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set</p> <p>0: Transmit FIFO is not empty</p> <p>1: Transmit FIFO is empty</p>
	[1]	R	1	TFNF	<p>Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations</p> <p>0: Transmit FIFO is full</p> <p>1: Transmit FIFO is not full</p>

Offset	Bit	Access	INI	Symbol	Description
	[0]	R	0	ACTIVITY	I2C Activity Status.
<b>IC_TXFLR</b>					
0x74	[4:0]	R	0	TXFLR	Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.
<b>IC_RXFLR</b>					
0x78	[4:0]	R	0	RXFLR	Receive FIFO Level. Contains the number of valid data entries in the Receive FIFO.
<b>IC_SDA_HOLD</b>					
0x7C	[15:0]	R/W	0x1	IC_SDA_HOLD	Controls the amount of hold time on the SDA signal after a negative edge of SCL in both master and slave mode, in units of ic_clk period
<b>IC_TX_ABRT_SOURCE</b>					
0x80	[31:16]	-	-	Reserved	-
	[15]	R	0	ABRT_SLVRD_INTX	1: When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register.
	[14]	R	0	ABRT_SLV_ARBLOST	1: Slave lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time.
	[13]	R	0	ABRT_SLVFLUSH_TXFIFO	1: Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.
	[12]	R	0	ARB_LOST	1: Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration.
	[11]	R	0	ABRT_MASTER_DIS	1: User tried to initiate a Master operation with the Master mode disabled.
	[10]	R	0	ABRT_10B_RD_NORSTRT	1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode.
	[9]	R	0	ABRT_SBYTE_NORSTRT	1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte.

Offset	Bit	Access	INI	Symbol	Description
	[8]	R	0	ABRT_HS_NORSTRT	1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode.
	[7]	R	0	ABRT_SBYTE_ACKDET	1: Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).
	[6]	R	0	ABRT_HS_ACKDET	1: Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior).
	[5]	R	0	ABRT_GCALL_READ	1: I2C in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus
	[4]	R	0	ABRT_GCALL_NOACK	1: I2C in master mode sent a General Call and no slave on the bus acknowledged the General Call.
	[3]	R	0	ABRT_TXDATA_NOACK	1: This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
	[2]	R	0	ABRT_10ADDR2_NOACK	1: Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.
	[1]	R	0	ABRT_10ADDR1_NOACK	1: Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.
	[0]	R	0	ABRT_7B_ADDR_NOACK	1: Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.
<b>IC_SLV_DATA_NACK_ONLY</b>					
0x84	[0]	R/W	0	NACK	Generate NACK. This NACK generation only occurs when I2C is a slave receiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received. 1: generate NACK after data byte received 0: generate NACK/ACK normally

Offset	Bit	Access	INI	Symbol	Description
<b>IC_DMA_CR</b>					
0x88	[1]	R/W	0	TDMAE	Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel. 0: Transmit DMA disabled 1: Transmit DMA enabled This can be programmed regardless of the state of IC_ENABLE
	[0]	R/W	0	RDMAE	Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel. 0: Receive DMA disabled 1: Receive DMA enabled This can be programmed regardless of the state of IC_ENABLE
<b>IC_DMA_TDLR</b>					
0x8C	[4:0]	R/W	0	DMATDL	DMA Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level
<b>DMA Receive Data Level Register (IC_DMA_RDLR)</b>					
0x90	[4:0]	R/W	0	DMARDL	DMA Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1
<b>IC_SDA_SETUP</b>					
0x94	[7:0]	R/W	0x64	SDA_SETUP	controls the amount of time delay (in terms of number of ic_clk clock periods) introduced in the rising edge of SCL—relative to SDA changing—by holding SCL low when I2C services a read request while operating as a slave-transmitter.
<b>RESERVED</b>					
0x98	-	-	-	-	-
<b>IC_ENABLE_STATUS</b>					
0x9C	-	-	-	-	-
	[2]	R	0	SLV_RX_DATA_LOST	This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0.
	[1]	R	0	SLV_DISABLED_WHILE_BUSY	This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0.

Offset	Bit	Access	INI	Symbol	Description
	[0]	R	0	IC_EN	The register is used to report the I2C hardware status when the IC_ENABLE register is set from 1 to 0; When read as 1, I2C is deemed to be in an enabled state. When read as 0, I2C is deemed completely inactive.

## 9.11. SPI Interface

The RTL8763BO supports industrial SPI (Serial Peripheral Interface), in both master and slave mode (SPI0, refer to pin description chapter) or in master mode (SPI1).

The SPI function can be enabled using the I/O MUX settings in the UI tool. Refer to the MUX function table in the I/O MUX section (page 84).

Table 17. SPI0/SPI1 Master

Offset	Bit	Access	INI	Symbol	Description
<b>CTRLR0</b>					
0x00	[31]	R/W	0	SS_T	When SCPH is 1 0: ss_n_out does not toggle between successive frames 1: ss_n_out does toggle between successive frames
	[24]	R/W	0	RxBitSwap	0: Order of receive bit does not swap 1: Order of receive bit does swap
	[23]	R/W	0	RxByteSwap	0: Order of receive byte does not swap 1: Order of receive byte does swap
	[22]	R/W	0	TxBitSwap	0: Order of transmit bit does not swap 1: Order of transmit bit does swap
	[21]	R/W	0	TxByteSwap	0: Order of transmit byte does not swap 1: Order of transmit byte does swap
	[20:16]	R/W	0	DFS_32	Data Frame Size in 32-bit mode Used to select the data frame size in 32-bit mode
	[15:10]	-	-	RESERVED	-
	[9:8]	R/W	0	TMOD	Transfer Mode. Selects the mode of transfer for serial communication. 00: Transmit & Receive 01: Transmit Only 10: Receive Only 11: EEPROM Read
	[7]	R/W	-	SCPOL	Serial Clock Polarity 0: Inactive state of serial clock is low 1: Inactive state of serial clock is high
	[6]	R/W	-	SCPH	Serial Clock Phase 0: Serial clock toggles in middle of first data bit 1: Serial clock toggles at start of first data bit
	[5:0]	-	-	RESERVED	-

Offset	Bit	Access	INI	Symbol	Description
<b>CTRLR1</b>					
0x04	[15:0]	R/W	0	NDF	Number of Data Frames. When TMOD = 10 or TMOD = 11, this register field sets the number of data frames to be continuously received by SPI master.
<b>SSIEN</b>					
0x08	[0]	R/W	0	SSI_EN	SSI Enable
<b>SER</b>					
0x10	[2:0] for SPI1 [0] for SPI0	R/W	0	SER	Slave Select Enable Flag. Each bit in this register corresponds to a slave select line (ss_x_n) from SPI master 1: Selected 0: Not Selected
<b>Baud Rate Select (BAUDR)</b>					
0x14	[15:0]	R/W	0	SCKDV	SSI Clock Divider. If the value is 0, the serial output clock (sclk_out) is disabled. The frequency of the sclk_out is derived from the following equation: $F_{sclk\_out} = F_{ssi\_clk}/SCKDV$ where SCKDV is any even value between 2 and 65534
<b>TXFTLR</b>					
0x18	[5:0]	R/W	0	TFT	Transmit FIFO Threshold. Controls the level of entries (or below) at which the transmit FIFO controller triggers an interrupt. When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered.
<b>RXFTLR</b>					
0x1C	[5:0]	R/W	0	RFT	Receive FIFO Threshold. Controls the level of entries (or above) at which the receive FIFO controller triggers an interrupt. When the number of receive FIFO entries is greater than or equal to this value + 1, the receive FIFO full interrupt is triggered.
<b>TXFLR</b>					
0x20	[31:0]	R	0	TXTFL	Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.
<b>RXFLR</b>					
0x24	[31:0]	R	0	RXTFL	Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

Offset	Bit	Access	INI	Symbol	Description
<b>SR</b>					
0x2C	[4]	R	0	RFF	Receive FIFO Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. 0: Receive FIFO is not full 1: Receive FIFO is full
	[3]	R	0	RFNE	Receive FIFO Not Empty. Set when the receive FIFO contains one or more entries and is cleared when the receive FIFO is empty. 0: Receive FIFO is empty 1: Receive FIFO is not empty
	[2]	R	1	TFE	Transmit FIFO Empty. When the transmit FIFO is completely empty, this bit is set. When the transmit FIFO contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty
	[1]	R	1	TFNF	Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. 0: Transmit FIFO is full 1: Transmit FIFO is not full
	[0]	R	0	BUSY	SPI Busy Flag. When set, indicates that a serial transfer is in progress; when cleared indicates that the SPI is idle or disabled. 0: SPI is idle or disabled 1: SPI is actively transferring data
<b>IMR</b>					
0x2C	[5]	R/W	1	MSTIM	Multi-Master Contention Interrupt Mask. This bit field is not present if SPI is configured as a serial-slave device. 0: ssi_mst_intr interrupt is masked 1: ssi_mst_intr interrupt is not masked
	[4]	R/W	1	RXFIM	Receive FIFO Full Interrupt Mask 0: ssi_rxf_intr interrupt is masked 1: ssi_rxf_intr interrupt is not masked
	[3]	R/W	1	RXOIM	Receive FIFO Overflow Interrupt Mask 0: ssi_rxo_intr interrupt is masked 1: ssi_rxo_intr interrupt is not masked
	[2]	R/W	1	RXUIM	Receive FIFO Underflow Interrupt Mask 0: ssi_rxu_intr interrupt is masked 1: ssi_rxu_intr interrupt is not masked
	[1]	R/W	1	TXOIM	Transmit FIFO Overflow Interrupt Mask 0: ssi_txo_intr interrupt is masked 1: ssi_txo_intr interrupt is not masked

Offset	Bit	Access	INI	Symbol	Description
	[0]	R/W	1	TXEIM	Transmit FIFO Empty Interrupt Mask 0: ssi_txe_intr interrupt is masked 1: ssi_txe_intr interrupt is not masked
<b>ISR</b>					
0x30	[5]	R	0	MSTIS	Multi-Master Contention Interrupt Status. This bit field is not present if SPI is configured as a serial-slave device. 0: ssi_mst_intr interrupt not active after masking 1: ssi_mst_intr interrupt is active after masking
	[4]	R	0	RXFIS	Receive FIFO Full Interrupt Status 0: ssi_rxf_intr interrupt is not active after masking 1: ssi_rxf_intr interrupt is full after masking
	[3]	R	0	RXOIS	Receive FIFO Overflow Interrupt Status 0: ssi_rxo_intr interrupt is not active after masking 1: ssi_rxo_intr interrupt is active after masking
	[2]	R	0	RXUIS	Receive FIFO Underflow Interrupt Status 0: ssi_rxu_intr interrupt is not active after masking 1: ssi_rxu_intr interrupt is active after masking
	[1]	R	0	TXOIS	Transmit FIFO Overflow Interrupt Status 0: ssi_txo_intr interrupt is not active after masking 1: ssi_txo_intr interrupt is active after masking
	[0]	R	0	TXEIS	Transmit FIFO Empty Interrupt Status 0: ssi_txe_intr interrupt is not active after masking 1: ssi_txe_intr interrupt is active after masking
<b>TXOICR</b>					
0x38	[0]	R	-	TXOICR	Clear Transmit FIFO Overflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_txo_intr interrupt; writing has no effect.
<b>RXOICR</b>					
0x3C	[0]	R	-	RXOICR	Clear Receive FIFO Underflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_rxu_intr interrupt; writing has no effect.
<b>RXUICR</b>					
0x40	[0]	R	-	RXUICR	Clear Transmit FIFO Overflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_txo_intr interrupt; writing has no effect.
<b>MSTICR</b>					
0x44	[0]	R	-	MSTICR	Clear Multi-Master Contention Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_mst_intr interrupt; writing has no effect.
<b>ICR</b>					
0x48	[0]	R	-	ICR	Clear Interrupts. This register is set if any of the interrupts below are active. A read clears the ssi_txo_intr, ssi_rxu_intr, ssi_rxo_intr, and the ssi_mst_intr interrupts. Writing to this register has no effect.

Offset	Bit	Access	INI	Symbol	Description
<b>DMACR</b>					
0x4C	[1]	R/W	0	TDMAE	Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel. 0: Transmit DMA disabled 1: Transmit DMA enabled.
	[0]	R/W	0	RDMAE	Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel 0: Receive DMA disabled 1: Receive DMA enabled.
<b>DMATDLR</b>					
0x50	[31:0]	R/W	0	DMATDLR	Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level
<b>DMARDLR</b>					
0x54	[31:0]	R/W	0	DMARDLR	Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1
<b>DR</b>					
0x60	[31:0]	R/W	0	DR	Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

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**Table 18. SPI0 Slave**

Offset	Bit	Access	INI	Symbol	Description
<b>Control Register 0 (CTRLR0)</b>					
0x00	[10]	R/W	0	SLV_OE	Slave Output Enable. Relevant only when the SPI is configured as a serial-slave device. When configured as a serial master, this bit field has no functionality. 0: Slave txd is enabled 1: Slave txd is disabled
	[9:8]	R/W	0	TMOD	Transfer Mode. Selects the mode of transfer for serial communication. This field does not affect the transfer duplexity. Only indicates whether the receive or transmit data are valid. 00: Transmit & Receive 01: Transmit Only 10: Receive Only 11: EEPROM Read
	[7]	R/W	0	SCPOL	Serial Clock Polarity 0: Inactive state of serial clock is low 1: Inactive state of serial clock is high

Offset	Bit	Access	INI	Symbol	Description
	[6]	R/W	0	SCPH	Serial Clock Phase 0: Serial clock toggles in middle of first data bit 1: Serial clock toggles at start of first data bit
	[5:4]	-	RESERVED	-	-
	[3:0]	R/W	0x7	DFS	Selects the data frame length
<b>SSI Enable Register (SSIEN)</b>					
0x08	[0]	R/W	0	SSI_EN	SSI Enable. Enables and disables all SPI operations.
<b>Transmit FIFO Threshold Level (TXFTLR)</b>					
0x18	[5:0]	R/W	0	TFT	Transmit FIFO Threshold. Controls the level of entries (or below) at which the transmit FIFO controller triggers an interrupt. When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered.
<b>Receive FIFO Threshold Level (RXFTLR)</b>					
0x1C	[5:0]	R/W	0	RFT	Receive FIFO Threshold. Controls the level of entries (or above) at which the receive FIFO controller triggers an interrupt. When the number of receive FIFO entries is greater than or equal to this value + 1, the receive FIFO full interrupt is triggered.
<b>Transmit FIFO Level Register (TXFLR)</b>					
0x20	[5:0]	R	0	TXTFL	Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.
<b>Receive FIFO Level Register (RXFLR)</b>					
0x24	[5:0]	R	0	RXTFL	Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.
<b>Status Register (SR)</b>					
0x28	[5]	R	0	TXE	Transmission Error. Set if the transmit FIFO is empty when a transfer is started. This bit can be set only when the SPI is configured as a slave device. This bit is cleared when read. 0: No error 1: Transmission error
	[4]	R	0	RFF	Receive FIFO Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. 0: Receive FIFO is not full 1: Receive FIFO is full

Offset	Bit	Access	INI	Symbol	Description
	[3]	R	0	RFNE	Receive FIFO Not Empty. Set when the receive FIFO contains one or more entries and is cleared when the receive FIFO is empty. 0: Receive FIFO is empty 1: Receive FIFO is not empty
	[2]	R	1	TFE	Transmit FIFO Empty. When the transmit FIFO is completely empty, this bit is set. When the transmit FIFO contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty
	[1]	R	1	TFNF	Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. 0: Transmit FIFO is full 1: Transmit FIFO is not full
	[0]	R	0	BUSY	SSI Busy Flag. When set, indicates that a serial transfer is in progress; when cleared indicates that the SPI is idle or disabled. 0: SPI is idle or disabled 1: SPI is actively transferring data

**Interrupt Mask Register (IMR)**

0x2C	[7]	R/W	1	SSRIM	SS_N Rising Edge Detect Interrupt Mask for SPI0 slave
	[4]	R/W	1	RXFIM	Receive FIFO Full Interrupt Mask 0: ssi_rxf_intr interrupt is masked 1: ssi_rxf_intr interrupt is not masked
	[3]	R/W	1	RXOIM	Receive FIFO Overflow Interrupt Mask 0: ssi_rxo_intr interrupt is masked 1: ssi_rxo_intr interrupt is not masked
	[2]	R/W	1	RXUIM	Receive FIFO Underflow Interrupt Mask 0: ssi_rxu_intr interrupt is masked 1: ssi_rxu_intr interrupt is not masked
	[1]	R/W	1	TXOIM	Transmit FIFO Overflow Interrupt Mask 0: ssi_txo_intr interrupt is masked 1: ssi_txo_intr interrupt is not masked
	[0]	R/W	1	TXEIM	Transmit FIFO Empty Interrupt Mask 0: ssi_txe_intr interrupt is masked 1: ssi_txe_intr interrupt is not masked

Offset	Bit	Access	INI	Symbol	Description
<b>Interrupt Status Register (ISR)</b>					
0x30	[7]	R	0	SSRIS	SS_N Rising Edge Detect Interrupt Status
	[4]	R	0	RXFIS	Receive FIFO Full Interrupt Status 0: ssi_rxf_intr interrupt is not active after masking 1: ssi_rxf_intr interrupt is full after maskingd
	[3]	R	0	RXOIS	Receive FIFO Overflow Interrupt Status 0: ssi_rxo_intr interrupt is not active after masking 1: ssi_rxo_intr interrupt is active after masking
	[2]	R	0	RXUIS	Receive FIFO Underflow Interrupt Status 0: ssi_rxu_intr interrupt is not active after masking 1: ssi_rxu_intr interrupt is active after masking
	[1]	R	0	TXOIS	Transmit FIFO Overflow Interrupt Status 0: ssi_txo_intr interrupt is not active after masking 1: ssi_txo_intr interrupt is active after masking
	[0]	R	0	TXEIS	Transmit FIFO Empty Interrupt Status 0: ssi_txe_intr interrupt is not active after masking 1: ssi_txe_intr interrupt is active after masking
<b>Transmit FIFO Overflow Interrupt Clear Register</b>					
0x38	[0]	R	-	TXOICR	Clear Transmit FIFO Overflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_txo_intr interrupt; writing has no effect.
<b>Receive FIFO Overflow Interrupt Clear Register</b>					
0x3C	[0]	R	-	RXOICR	Clear Receive FIFO Underflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_rxu_intr interrupt; writing has no effect.
<b>Receive FIFO Underflow Interrupt Clear Register</b>					
0x40	[0]	R	-	RXUICR	Clear Transmit FIFO Overflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_txo_intr interrupt; writing has no effect.

Offset	Bit	Access	INI	Symbol	Description
<b>Interrupt Clear Register</b>					
0x48	[0]	R	-	ICR	Clear Interrupts. This register is set if any of the interrupts below are active. A read clears the ssi_txo_intr, ssi_rxu_intr, ssi_rxo_intr, and the ssi_mst_intr interrupts. Writing to this register has no effect.
<b>DMA Control Register (DMACR)</b>					
0x4C	[1]	R/W	0	TDMAE	Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel. 0: Transmit DMA disabled 1: Transmit DMA enabled
	[0]	R/W	0	RDMAE	Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel. 0: Receive DMA disabled 1: Receive DMA enabled.
<b>DMA Transmit Data Level (DMATDLR)</b>					
0x50	[5:0]	R/W	0	DMATDLR	Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level
<b>DMA Receive Data Level (DMARDLRL)</b>					
0x54	[5:0]	R/W	0	DMARDLRL	Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDLRL
<b>SS_N Rising Edge Detect Interrupt Clear Register</b>					
0x5C	0	R	-	SSRICR	Clear SS_N Rising Edge Detect Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_ssri_intr interrupt; writing has no effect.
<b>Data Register</b>					
0x60	[31:0]	R/W	0	DR	Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

## 9.12. NFC

NFC (Near Field Communication) is a technology to simplify the establishment of a Bluetooth link between a Bluetooth host and a Bluetooth device. This is often used in smartphone applications with a smartphone APP.

The RTL8763BO supports the NFC feature to power on the whole system and connect with smart phone automatically by touching the two devices together.

The NFC application circuit in the RTL8763B reference circuit is very simple and cost effective with minimum BOM required. In mass production flow, an MP tool also supports an easy way to synchronize the BD ADDR in the NFC tag with the memory in the RTL8763B.

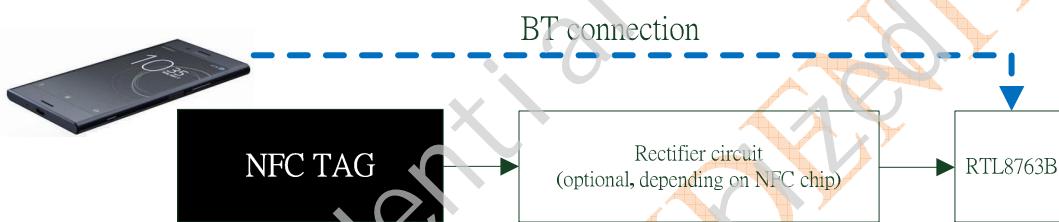


Figure 35. Near Field Communication

## 9.13. USB Interface

The RTL8763BO supports a USB2.0 full speed interface and the USB BC1.2 USB charger specification.

The USB ports on personal computers, laptop PCs, and USB adapters are convenient for portable devices to draw current for the audio device to charge the battery. When a device attaches to the USB ports, the USB2.0 specification requires that after connecting a device must draw current less than:

- 2.5mA average if the USB bus is suspended
- 100mA if the bus is not suspended and not configured
- 500mA if the bus is not suspended and configured for 500mA
- Support USB charger with a DCP, such as wall adapter or car power adapter

The RTL8763BO follows the USB2.0 and USB BC1.2 specification to draw the charging current from the USB ports and adjust the current under different USB port states accordingly.

The USB port also supports a FLASH memory parameter update process; refer to MP tool guidelines.

## 9.14. S/PDIF Interface

The RTL8763BO supports S/PDIF (SONY/PHILIPS Digital Interface) output; the purpose is to transfer digital audio data among digital devices with minimum loss.

### Bluetooth Speaker Application

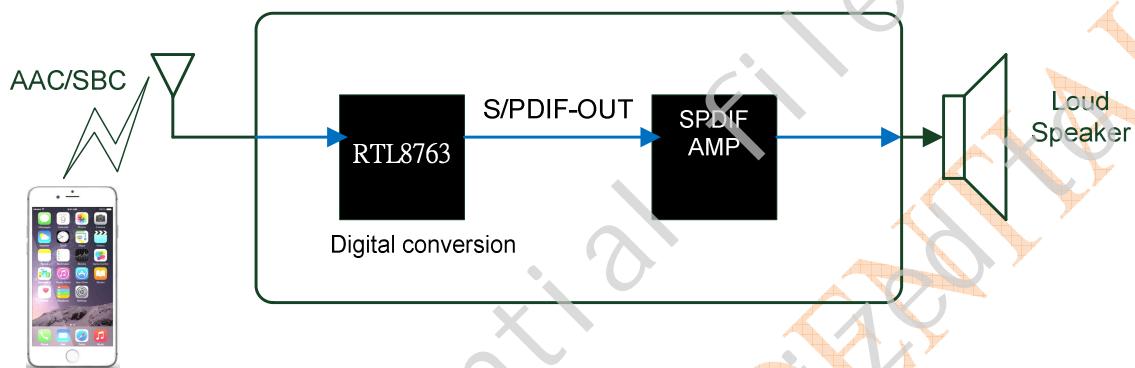


Figure 36. Bluetooth Speaker Application

### Bluetooth Audio Receiver Application

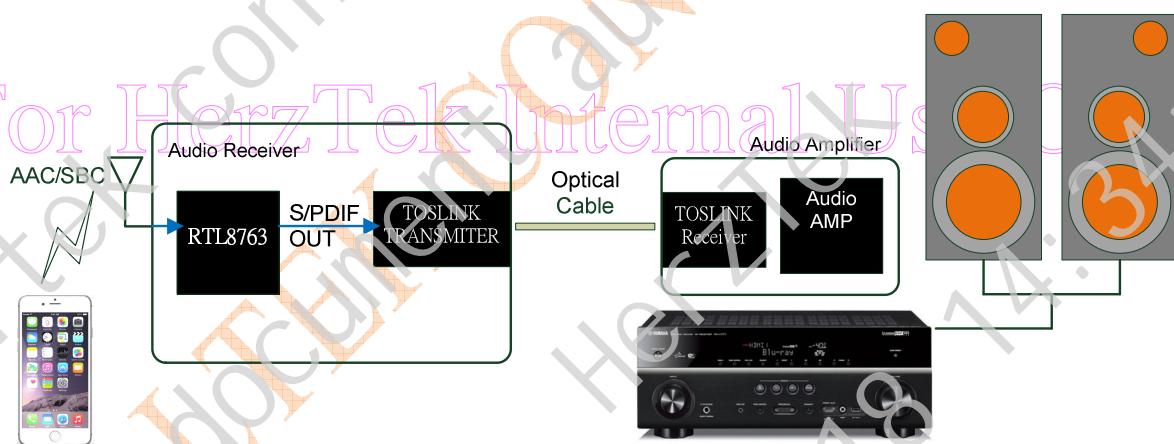


Figure 37. Bluetooth Audio Receiver Application

## 9.15. Auxiliary ADC Interface

The RTL8763BO supports high quality ADC input, designed-in 12-bit, and can be multiplexed with the digital GPIO function. The allowable input swing is from 0V to min (VDDIO, 3V) in normal mode.

The allowable input swing is from 0V to 1 in bypass mode.

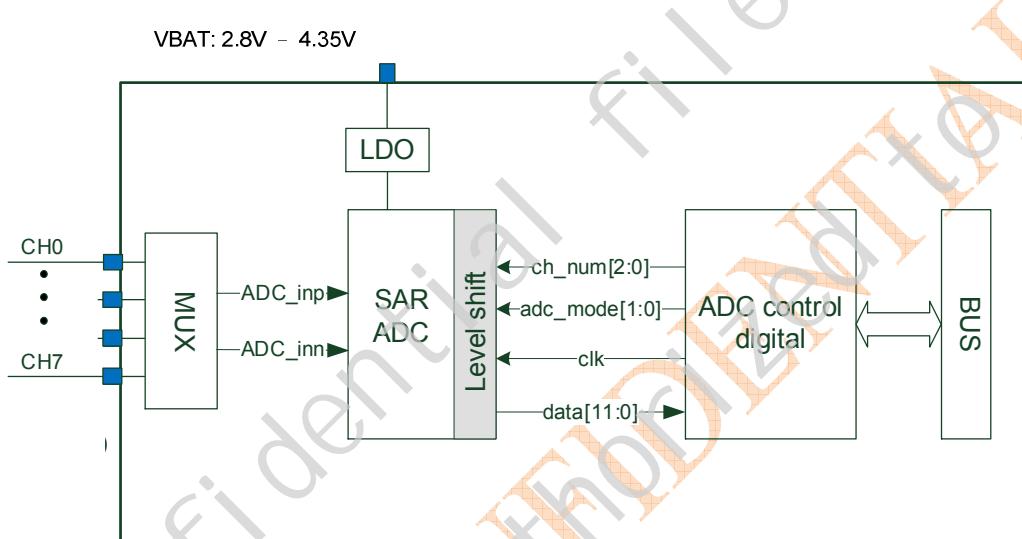


Figure 38. Auxiliary ADC Interface Application

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## 9.16. BT Wi-Fi Co-Existence (PTA)

The RTL8763BO supports a BT/Wi-Fi co-existence scheme, PTA (Packet Traffic Arbiter)

PTA is a handshake algorithm between Wi-Fi and Bluetooth in a Wi-Fi and Bluetooth co-existence system.

PTA is used to control the priority of the Wi-Fi and Bluetooth traffic by accessing a 3-wire MAILBOX block to avoid packet collisions in the same shared 2.4GHz ISM frequency band.

The PTA and mailbox signals can be defined via the PIN MUX table in the UI tool.

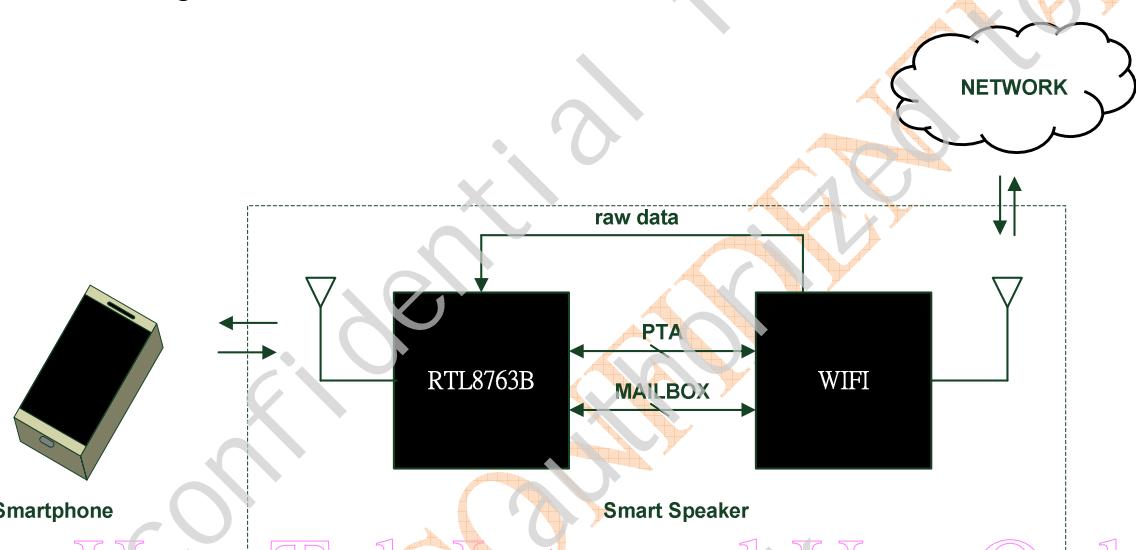


Figure 39. BT Wi-Fi Co-Existence (PTA)

3-wire MAILBOX	I2C_SCL
	I2C_INIT
	I2C_SDA
PTA	BT_CK
	BT_ACT
	BT_WLAN_ACT
	BT_STE

Figure 40. PTA and MAILBOX Connection

## 9.17. KEY Scan

The RTL8763BO supports a programmable 12x20 key matrix with keyscan engine. All GPIOs can use pin multiplexing for easy configuration. The PAD structure is pull-up resistor.

**Table 19. Hardware KeyScan (Base Address: 0x40005000)**

Offset	Bit	Access	INI	Symbol	Description
<b>CLKDIV</b>					
0x00	[31:24]	-	-	RESERVED	-
	[18:8]	R/W	0x27	keyscan_clk_div	System clock/(SCAN_DIV+1)=scan clock SCAN_DIV:11bit
	[3:0]	R/W	0x1	keyscan_delay_div	Delay clock= scan clock/(DELAY_DIV+1)
<b>TIMERCR</b>					
0x04	[31]	R/W	0x1	keyscan_deb_timer_en	Enable debounce function for key row 0x1: Enable debounce timer 0x0 : Disable debounce timer
	[30]	R/W	0x1	keyscan_interval_timer_en	Enable Scan interval timer 0x1: Scan interval timer 0x0 : Scan interval timer
	[29]	R/W	0x0	keyscan_release_timer_en	Enable Release detect timer 0x1: Enable Release detect timer 0x0 : Disable Release detect timer
	[23:16]	R/W	0x10	keyscan_deb_timer_cnt	Debounce counter n*delay_clk_cyle
	[15:8]	R/W	0x10	keyscan_interval_timer_cnt	Scan interval counter n*delay_clk_cyle
	[7:0]	R/W	0x10	keyscan_release_timer_cnt	Release detect counter n*delay_clk_cyle
<b>CR</b>					
0x08	[31]	R/W	0x1	keyscan_run_enable	Enable internal key scan clock. The key scan clock enable must be after key scan configuration is done 0x1: Enable key scan clock (HW FSM start run) 0x0 : Disable key scan clock (HW FSM stop)
	[30]	R/W	0x1	keyscan_work_mode	Scan mode: 0: manual scan - scan once, then trigger scan finish interrupt 1: Automatic scan - auto scan according to scan interval
	[29]	-	-	RESERVED	-
	[28]	R/W	0x1	keyscan_fifo_ov_ctrl	FIFO overflow control 0x0 : Rejects the new scan data when FIFO is full 0x1: Discard the oldest scan data when FIFO is full

Offset	Bit	Access	INI	Symbol	Description
	[27:23]	R/W	0x0	keyscan_fifo_limit	Limit the max. allowable key data in one scan 0x0 : No limit 0x1: Only one scan data is allowable in each key scan ... 0x1a : Max 26 scan data is allowable in each key scan 0x1b ~ 0x1f : DO NOT USE
	[21]	R/W	0x0	keyscan_fifo_data_filter_en	Enable to filter data; 0x0 : Disable 0x1: Enable
	[20:12]	R/W	0x0	keyscan_fifo_filter_data	Data to be filtered; 0x0 : Disable 0x1: Enable
	[9:5]	R/W	0x1a	keyscan_fifo_th_level	FIFO_threshold interrupt; FIFO threshold to send interrupt
	[4]	R/W	0x0	keyscan_fifo_th_int_en	FIFO_threshold interrupt enable; 0x0 : Disable 0x1: Enable
	[3]	R/W	0x0	keyscan_fifo_or_int_en	FIFO_OVER_READ_INT. Read RX FIFO when RX FIFO empty; 0x0 : Disable 0x1: Enable
	[2]	R/W	0x0	keyscan_scan_finish_int_en	0x0 : Disable scan finish interrupt 0x1: Enables scan finsh interrupt
	[1]	R/W	0x0	keyscan_fifo_notempty_int_en	0x0 : Disable FIFO int interrupt 0x1: Enable FIFO int interrupt
	[0]	R/W	0x1	keyscan_all_release_int_en	0x0 : Disable Release int interrupt 0x1: Enable Release int interrupt
<b>COLCR</b>					
0x0C	[27:8]	R/W	0	keyscan_col_sel	The control register to define which column is used 0x0 : No key column is selected 0x1: Key column 0 is selected 0x2 : Key column 1 is selected 0x3 : Key column 0 and column 1 are selected 0x4 : Key column 2 is selected ... 0xfffffe : Key column 1 to column 19 are selected 0xfffffff: Key column 0 to column 19 are selected

Offset	Bit	Access	INI	Symbol	Description
	[4:0]	R/W	0	keyscan_col_num	The control register to define how many key column to use Ex : reg_col_num = 0x0, only use one key column reg_col_num = 0x1, use two key columns reg_col_num = 0x13, use column 0 ~ column 19
<b>ROWCR</b>					
0x10	[19:16]	R/W	0	keyscan_row_num	The control register to define how many key row to use Ex : reg_row_num = 0x0, only use one key row reg_row_num = 0x1, use two key rows reg_row_num = 0xb, use row0 ~ row11
	[11:0]	R/W	0	keyscan_row_sel	The control register to define which row is used 0x0 : No key row is selected 0x1: Key row 0 is selected 0x2 : Key row 1 is selected 0x3 : Key row 0 and row 1 are selected 0x4 : Key row 2 is selected ... 0xffff: Key row 0 to row 11 are selected
<b>FIFODATA</b>					
0x14	[15:0]	R	0	keyscan_fifo_entry	[4:0] column index [8:5] row index Other: reserved
<b>INTMASK</b>					
0x18	[4]	R/W	0	keyscan_fifo_th_int_mask	FIFO_threshold interrupt; 0x1: Mask interrupt
	[3]	R/W	0	keyscan_fifo_or_int_mask	FIFO_OVER_READ interrupt 0x1: Mask interrupt
	[2]	R/W	0	keyscan_scan_finish_int_mask	Scan finish Interrupt mask signal 0x1: Mask interrupt
	[1]	R/W	0	keyscan_fifo_notempty_int_mask	FIFO Interrupt mask signal 0x1: Mask interrupt
	[0]	R/W	0	keyscan_all_release_int_mask	Release Interrupt mask signal 0x1: Mask interrupt
<b>INTCLR</b>					
0x1C	[8]	W1C	-	keyscan_fifo_limit_st_clr	Clear FIFO limit status Write 1 to clear
	[7]	W1C	-	keyscan_fifo_datafilter_st_clr	Clear FIFO filter status Write 1 to clear
	[6]	W1C	-	keyscan_fifo_clr	Clear FIFO data Write 1 to clear

Offset	Bit	Access	INI	Symbol	Description
0x20	[5]	W1C	-	keyscan_fifo_ov_st_clr	Clear overflow status flag Write 1 to clear
	[4]	W1C	-	keyscan_fifo_th_int_clr	FIFO_threshold interrupt; Write 1 to clear
	[3]	W1C	-	keyscan_fifo_or_int_clr	RX_FIFO_READ_FAIL_INT Write 1 to clear
0x21	[2]	W1C	-	keyscan_scan_finish_int_clr	Interrupt clear signal for scan finish int Write 1 to clear
	[1]	W1C	-	keyscan_fifo_notempty_int_clr	Interrupt clear signal for fifo int Write 1 to clear
	[0]	W1C	-	keyscan_all_release_int_clr	Interrupt clear signal for release int Write 1 to clear
<b>STATUS</b>					
0x20	[20]	R	0	keyscan_fifo_limit_status	0x1: Overflow FIFO limit in one scan
	[19]	R	0	keyscan_fifo_th_int_status	FIFO_threshold interrupt; 0x0: Interrupt inactive 0x1: Interrupt active
	[18]	R	0	keyscan_fifo_or_int_status	RX_FIFO_READ_FAIL_INT MASK 0x0: Interrupt inactive 0x1: Interrupt active
	[17]	R	0	keyscan_scan_finish_int_status	Scan finish interrupt status 0x0: Interrupt inactive 0x1: Interrupt active
	[16]	R	0	keyscan_fifo_notempty_int_status	FIFO interrupt status 0x0: Interrupt inactive 0x1: Interrupt active
	[15]	R	0	keyscan_all_release_int_status	Release interrupt status 0x0: Interrupt inactive 0x1: Interrupt active
	[9:4]	R	0	keyscan_fifo_data_level	FIFO offset 0x0 : No data in FIFO 0x1: One Data in FIFO ... 0x1A : 26 data in FIFO
	[3]	R	0	keyscan_fifo_datafilter_status	FIFO filter status 0x0 : Data discard not occur 0x1: Data discard occurred
	[2]	R	0	keyscan_fifo_ov_status	The flag to indicate FIFO is overflow 0x1: Overflow occurred 0x0 : No Overflow occurred
	[1]	R	0	keyscan_fifo_full	The flag to indicate FIFO is full 0x1: FIFO is full 0x0 : FIFO is not full

Offset	Bit	Access	INI	Symbol	Description
	[0]	R	0	keyscan_fifo_empty	The flag to indicate FIFO is empty 0x1: FIFO is empty 0x0 : FIFO is not empty

## 9.18. PWM Interface

The RTL8763BO supports up to six PWM signals. (\* when applied to different user scenarios, more timers will be occupied, e.g. RWS, push button, AUX-IN detection and buzzer...etc.)

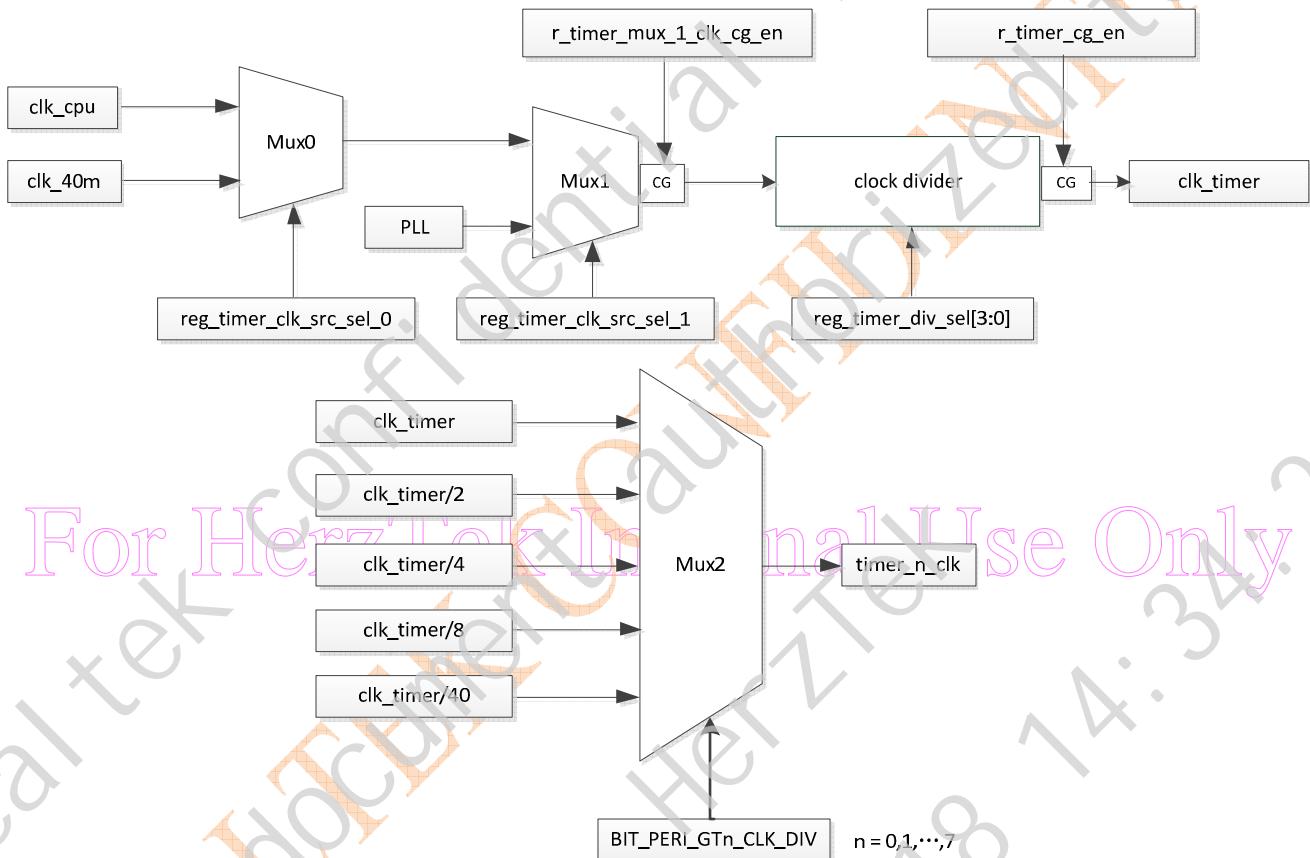


Figure 41. PWM Interface

### PWM Output Setting

The PWM module is controlled by register [ControlReg] [3].

When [ControlReg] [3] = 1, PWM is enabled and the PWM waveform is derived by controlling [LoadCount] and [LoadCount2] registers and deciding the level high and level low time interval:

$$\text{PWM level high timer} = (\text{TimerNLoadCount2} + 1) * \text{timer\_N\_clk clock period}$$

$$\text{PWM level low timer} = (\text{TimerNLoadCount} + 1) * \text{timer\_N\_clk clock period}$$

After the PWM timer is enabled, the register [LoadCount]和[LoadCount2] is loaded periodically. PWM outputs low level during the time interval before LoadCount is decreased to zero; PWM outputs high level during the time interval before LoadCount2 is decreased to zero.

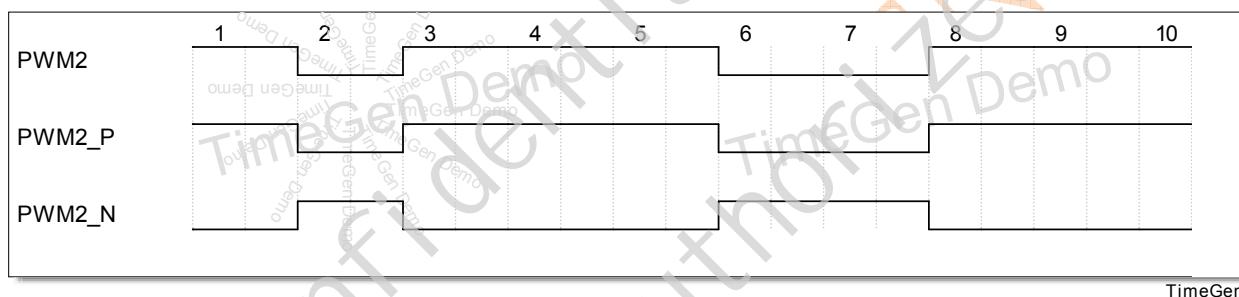
When [ControlReg] [3] = 0, PWM is disabled, the timer toggle still outputs; the output high and low timer is the same, e.g. (LoadCount + 1) \* timer\_N\_clk clock period.

### PWM Complementary Output Setting

Only Timer2 and timer3 support PWM complementary output mode.

Taking timer2 as an example, by setting register [PWM\_CR2][12] and [PWM\_CR3][12] to enable PWM complementary output and dead zone setting.

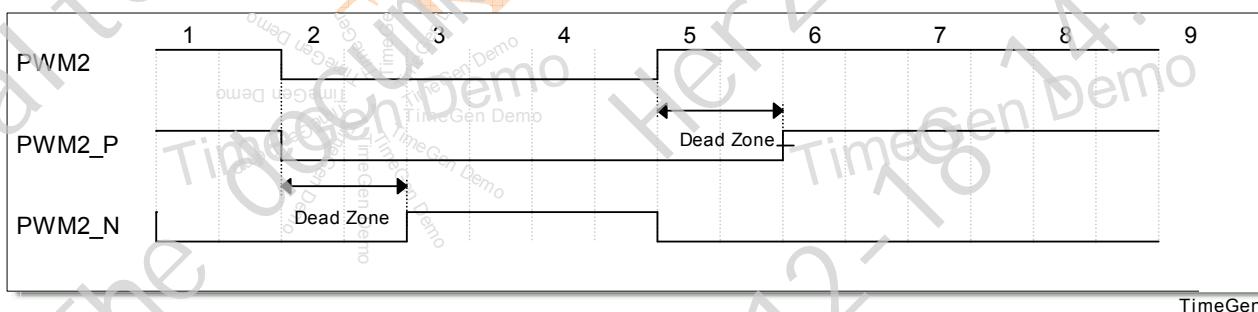
When complementary output mode is enabled but not set in the dead zone, PWM\_2P will be the same as PWM2, while PWM2\_N will be the reverse of PWM2.



**Figure 42. Complementary Output Mode Enabled But Not Set in the Dead Zone**

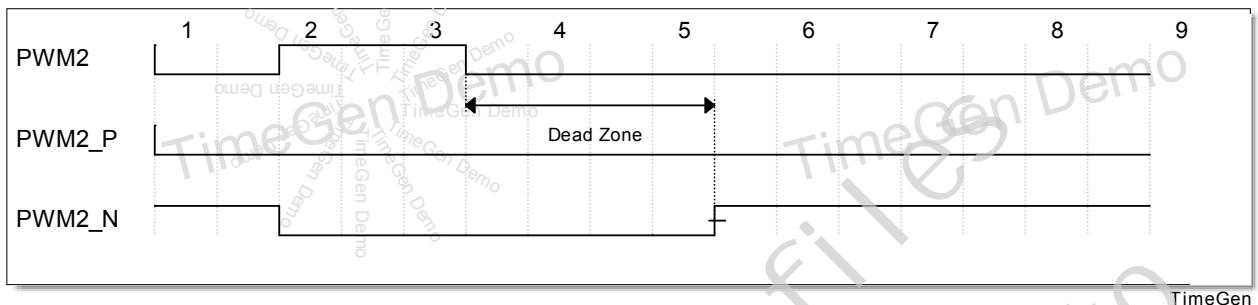
The maximum setting of the dead zone is 256/32000 or 256/32768 according to the source of the low power clock (internal or external 32K clock source).

When the dead zone is set, the level high output of PWM2\_P and PWM2\_N contain a time delay



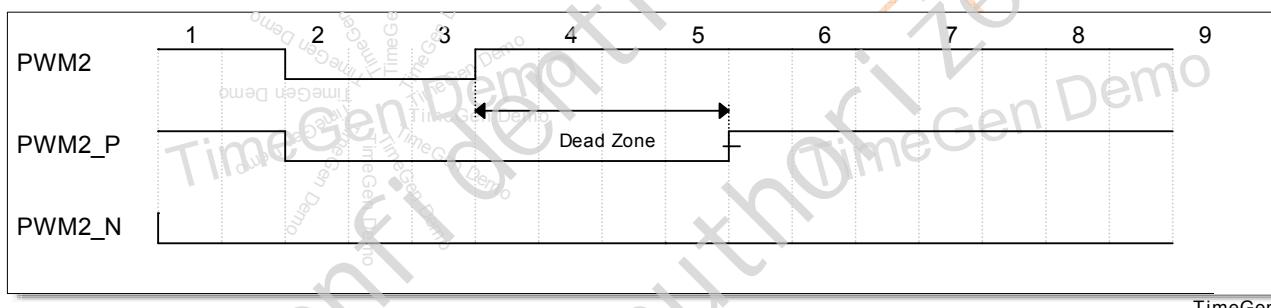
**Figure 43. Maximum Setting of Dead Zone**

When the dead zone is longer than the PWM high level timer, PWM\_P will always be low.



**Figure 44. Dead Zone Is Longer Than PWM High Level Timer**

When the dead zone is longer than the PWM low level timer, PWM\_N will always be low.



**Figure 45. Dead Zone Is Longer Than PWM Low Level Timer**

**Table 20. Hardware Timer (Base Address: 0x4000\_2000)**

Address Range (Base +)	Function
0x00 to 0x10	Reserved
0x14 to 0x24	Reserved
0x28 to 0x38	Timer 2 Registers
0x3c to 0x4c	Timer 3 Registers
0x50 to 0x60	Timer 4 Registers
0x64 to 0x74	Timer 5 Registers
0x78 to 0x88	Timer 6 Registers
0x8c to 0x9c	Timer 7 Registers
0xb0 to 0xcc	TimerNLoadCount2 Registers

**Table 21. Hardware Timer (Base Address: 0x4000\_2000)**

Offset	Bit	Access	INI	Symbol	Description
<b>TimerN Load Count Register</b>					
for N = 2, 0x28 for N = 3, 0x3C for N = 4, 0x50 for N = 5, 0x64 for N = 6, 0x78 for N = 7, 0x8C	[31:0]	R/W	0	TimerNLoadCount	Value to be loaded into TimerN. This is the value from which counting commences.
<b>TimerN Load2 Count Register</b>					
for N = 2, 0xb8 for N = 3, 0xbC for N = 4, 0xC0 for N = 5, 0xC4 for N = 6, 0xC8 for N = 7, 0xCC	[31:0]	R/W	0	TimerNLoadCount2	Value to be loaded into TimerN when timer_N_toggle output changes from 0 to 1. This value determines the width of the HIGH period of the timer_N_toggle output.
<b>TimerN Current Value Register</b>					
for N = 2, 0x2C for N = 3, 0x40 for N = 4, 0x54 for N = 5, 0x68 for N = 6, 0x7C for N = 7, 0x90	[31:0]	R	0	TimerNCurrentValue	Current Value of TimerN
<b>TimerN Control Register</b>					
for N = 2, 0x30 for N = 3, 0x44 for N = 4, 0x58 for N = 5, 0x6C for N = 6, 0x80 for N = 7, 0x94	[3]	R/W	0	TIMER_PWM	Pulse Width Modulation of timer_N_toggle output. 0: Disabled 1: Enabled
	[2]	R/W	0	Timer Interrupt Mask	Timer interrupt mask for TimerN 0: Not masked 1: Masked
	[1]	R/W	0	Timer Mode	Timer mode for TimerN 0: Free-running mode 1: User-defined count mode
	[0]	R/W	0	Timer Enable	Timer enable bit for TimerN 0: Disable 1: Enable
<b>TimerN End-of-Interrupt Register</b>					
for N = 2, 0x34 for N = 3, 0x48 for N = 4, 0x5C for N = 5, 0x70 for N = 6, 0x84 for N = 7, 0x98	[0]	R	-	TimerNEOI	Reading from this register returns all zeroes and clears the interrupt from TimerN.

Offset	Bit	Access	INI	Symbol	Description
<b>TimerN Interrupt Status Register</b>					
for N = 2, 0x38 for N = 3, 0x4C for N = 4, 0x60 for N = 5, 0x74 for N = 6, 0x88 for N = 7, 0x9C	[0]	R	0	TimerNIntStatus	Contains the interrupt status for TimerN.
<b>Timers Interrupt Status Register</b>					
0xa0	[7:2]	R	0	TimersIntStatus	Contains the interrupt status of all timers. 0: Not active after masking 1: Active after masking
	[1:0]	R	-	Reserved	-
<b>Timers End-of-Interrupt Register</b>					
0xa4	[7:2]	R	-	TimersEOI	Reading this register returns all zeroes (0) and clears all active interrupts.
	[1:0]	R	-	Reserved	-
<b>Timers Clock Divider Register 1 (REG_PERI_GTIMER_CLK_SRC)</b>					
0x4000035C	[8:6]	R/W	0	BIT_PERI_GT7_CLK_DIV	GTIMER7 clock divider 0x0-0x11: Div by 1 0x100: Div by 2 0x101: Div by 4 0x110: Div by 8 0x111: Div by40
	[5:3]	R/W	0	BIT_PERI_GT6_CLK_DIV	GTIMER6 clock divider 0x0-0x11: Div by 1 0x100: Div by 2 0x101: Div by 4 0x110: Div by 8 0x111: Div by40
	[2:0]	R/W	0	BIT_PERI_GT5_CLK_DIV	GTIMER5 clock divider 0x0-0x11: Div by 1 0x100: Div by 2 0x101: Div by 4 0x110: Div by 8 0x111: Div by40
<b>Timers Clock Divider Register 2 (REG_PERI_GTIMER_CLK_SRC)</b>					
0x40000360	[30:28]	R/W	0	BIT_PERI_GT4_CLK_DIV	GTIMER4 clock divider 0x0-0x11: Div by 1 0x100: Div by 2 0x101: Div by 4 0x110: Div by 8 0x111: Div by40
	[27:25]	R/W	0	BIT_PERI_G3_CLK_DIV	GTIMER3 clock divider 0x0-0x11: Div by 1 0x100: Div by 2 0x101: Div by 4 0x110: Div by 8 0x111: Div by40

Offset	Bit	Access	INI	Symbol	Description
0x40000364	[24:22]	R/W	0	BIT_PERI_GT2_CLK_DIV	GTIMER2 clock divider 0x0-0x11: Div by 1 0x100: Div by 2 0x101: Div by 4 0x110: Div by 8 0x111: Div by 40
	[21:19]	R/W	-	Reserved	-
	[18:16]	R/W	-	Reserved	-
<b>PWM2_CR</b>					
0x40000364	[12]	R/W	0	-	Dead zone enable (enable to use pwn p/n) 1: Enable 0: Disable
	[10]	R/W	0	-	pwm_p mergence stop state
	[9]	R/W	0	-	pwm_n mergence stop state
	[8]	R/W	0	-	-
	[7:0]	R/W	0	-	Dead Zone Size; Dead Zone Time=(Dead Zone Size) * (32768 or 32000) Dead Zone Size should not be 0
<b>PWM3_CR</b>					
0x40000368	[12]	R/W	0	-	Dead zone enable (enable to use pwn p/n) 0: Disable 1: Enable
	[10]	R/W	0	-	pwm_p mergence stop state
	[9]	R/W	0	-	pwm_n mergence stop state
	[8]	R/W	0	-	Emergency stop 1:Stop output
	[7:0]	R/W	0	-	Dead Zone Size; Dead Zone Time=(Dead Zone Size) * (32768 or 32000) Dead Zone Size should not be 0

## 9.19. IR RC

Table 22. IR RC (Base Address: 0x40003000)

Offset	Bit	Access	INI	Symbol	Description
<b>CLK_DIV</b>					
0x00	[15:4]	-	-	Reserved	-
	[11:0]	R/W	0	IR_CLK_DIV	IR_CLK = IO_CLK/(1+IR_CLK_DIV) TX mode: Divide number to generate Irda modulation frequency RX mode: waveform sample clock
<b>TX_CONFIG</b>					
0x04	[31]	R/W	0	IR_MODE_SEL	0:TX MODE 1:RX MODE
	[30]	R/W	0	IR_TX_START	0:FSM stop at idle state 1:FSM RUN
	[27:16]	R/W	0	IR_TX_DUTY_NUM	Duty cycle setting for modulation frequency EX : for 1/3 duty cycle, IR_DUTY_NUM = (IR_DIV_NUM+1)/3 -1
	[12]	R/W	0	IR_TX_INVERSE	0: Not inverse waveform 1: Inverse waveform
	[11:8]	R/W	0	IR_TX_FIFO_LEVEL_TH	TX FIFO interrupt threshold when TX FIFO depth= < threshold value, trigger interrupt
	[3]	R/W	0	IR_TX_FIFO_LEVEL_IN_T_MASK	TX FIFO Level Interrupt 0: Unmask 1: Mask
	[2]	R/W	0	IR_TX_FIFO_EMPTY_IN_T_MASK	TX FIFO Empty Interrupt 0: Unmask 1: Mask
	[1]	R/W	0	IR_TX_FIFO_LEVEL_IN_T_EN	TX FIFO Level Interrupt when TX FIFO offset= < threshold value, trigger interrupt 0: Disable 1: Enable
	[0]	R/W	0	IR_TX_FIFO_EMPTY_IN_T_EN	TX FIFO Empty Interrupt 0: Disable 1: Enable
<b>TX_SR</b>					
0x08	[13]	R	1	IR_TX_FIFO_EMPTY	0: Not empty 1: Empty
	[12]	R	0	IR_TX_FIFO_FULL	0: Not full 1: Full
	[11:8]	R	0	IR_TX_FIFO_OFFSET	Tx fifo offset
	[4]	R	0	IR_TX_STATUS	0: Idle 1: Run

Offset	Bit	Access	INI	Symbol	Description
0x10	[1]	R	0	IR_TX_FIFO_LEVEL_INT_EN	When TX FIFO offset= < threshold value, trigger interrupt 0: Interrupt inactive 1: Interrupt active
	[0]	R	0	IR_TX_FIFO_EMPTY_INT_EN	TX FIFO Empty Interrupt 0: Interrupt inactive 1: Interrupt active
<b>TX_INT_CLR</b>					
0x10	[2]	W	-	IR_TX_FIFO_LEVEL_INT_CLR	When TX FIFO offset= < threshold value, trigger interrupt Write 1 to clear
	[1]	W	-	IR_TX_FIFO_EMPTY_INT_CLR	TX FIFO Empty Interrupt Write 1 to clear
	[0]	W	-	IR_TX_FIFO_CLR	Write 1 to clear TX FIFO
<b>IR_TX_FIFO</b>					
0x14	[31]	W	-	IR_TX_DATA_TYPE	0: Active carrier 1: Inactive carrier
	[30]	W	-	IR_TX_DATA_END_FLAG	0: Normal packet 1: Last packet
	[29:0]	W	-	IR_TX_DATA_TIME	Length Real active time = length * IR_TX_CLK_Period FIFO width 16bits FIFO depth 16
<b>RX_CONFIG</b>					
0x18	[28]	R/W	0	IR_RX_START	0: FSM stop at idle state 1: FSM RUN
	[27]	R/W	1	IR_RX_START_MODE	0: Manual mode, IR_RX_MAN_START control 1: auto mode,Trigger mode control
	[26]	R/W	0	IR_RX_MAN_START	If IR_RX_TRIGGER_MODE =0 write 1= Start check waveform
	[25:24]	R/W	0	IR_RX_TRIGGER_MODE	00: High-> low trigger 01: Low-> high trigger
	[23:21]	-	-	Reserved	-
	[17]	R/W	0	IR_RX_CNT THR INT MASK	RX count threshold interrupt 0: Unmask 1: Mask
	[16]	R/W	0	IR_RX_FIFO_OF_INT_MASK	IR_RX_FIFO overflow 0: Unmask 1: Mask
	[15]	R/W	0	IR_RX_CNT_OF_INT_MASK	IR_RX counter overflow 0: Unmask 1: Mask
	[14]	R/W	0	IR_RX_FIFO_LEVEL_INT_MASK	RX FIFO Level Interrupt when RX FIFO offser= > threshold value, trigger interrupt 0: Unmask 1: Mask

Offset	Bit	Access	INI	Symbol	Description
0x1C	[13]	R/W	0	IR_RX_FIFO_FULL_INT_MASK	RX FIFO Full Interrupt 0: Unmask 1: Mask
	[12]	-	-	Reserved	-
	[11:8]	R/W	0	IR_RX_FIFO_LEVEL_TH	RX FIFO interrupt threshold when RX FIFO depth >= threshold value, trigger interrupt
	[4]	R/W	0	IR_RX_CNT THR INT_EN	RX count threshold interrupt 0: Disable 1: Enable
	[3]	R/W	0	IR_RX_FIFO_OF_INT_EN	IR_RX_FIFO overflow 0: Disable 1: Enable
	[2]	R/W	0	IR_RX_CNT_OF_INT_EN	IR_RX counter overflow 0: Disable 1: Enable
	[1]	R/W	0	IR_RX_FIFO_LEVEL_INT_EN	RX FIFO Level Interrupt when RX FIFO offset > threshold value, trigger 0: Disable 1: Enable
	[0]	R/W	0	IR_RX_FIFO_FULL_INT_EN	RX FIFO Full Interrupt 0: Disable 1: Enable
	<b>RX_SR</b>				
0x1C	[17]	R	1	IR_RX_FIFO_EMPTY	0: Not empty 1: Empty
	[16]	R	0	IR_RX_FIFO_FULL	0: Not full 1: Full
	[12:8]	R	0	IR_RX_FIFO_OFFSET	Tx fifo offset
	[5]	R	0	IR_RX_STATE	0: Idle 1: Run
	[4]	R	0	IR_RX_CNT THR INT_STATUS	RX count threshold interrupt 0: Interrupt inactive 1: Interrupt active
	[3]	R	0	IR_RX_FIFO_OF_INT_STATUS	RX FIFO overflow interrupt 0: Interrupt inactive 1: Interrupt active
	[2]	R	0	IR_RX_CNT_OF_INT_STATUS	RX counter overflow interrupt 0: Interrupt inactive 1: Interrupt active
	[1]	R	0	IR_RX_FIFO_LEVEL_INT_STATUS	RX FIFO Level Interrupt 0: Interrupt inactive 1: Interrupt active
	[0]	R	0	IR_RX_FIFO_FULL_INT_STATUS	RX FIFO Full Interrupt 0: Interrupt inactive 1: Interrupt active

Offset	Bit	Access	INI	Symbol	Description
<b>RX_INT_CLR</b>					
0x20	[5]	W	-	IR_RX_FIFO_CLR	Write 1 to clear RX FIFO
	[4]	W	-	IR_RX_CNT_THR_INT_CLR	RX count threshold interrupt Write 1 to clear
	[3]	W	-	IR_RX_FIFO_OF_INT_CLR	RX FIFO overflow interrupt Write 1 to clear
	[2]	W	-	IR_RX_CNT_OF_INT_CLR	RX counter overflow interrupt Write 1 to clear
	[1]	W	-	IR_RX_FIFO_LEVEL_INT_CLR	RX FIFO Level Interrupt Write 1 to clear
	[0]	W	-	IR_RX_FIFO_FULL_INT_CLR	RX FIFO Full Interrupt Write 1 to clear
<b>RX_CNT_INT_SEL</b>					
0x24	[31]	R/W	0	IR_RX_CNT THR_TRIGGER_LV	Trigger Level: 0: low level couner >= threshlod trigger interrupt 1: high level couner >= threshlod trigger interrupt
	[30:0]	R/W	0	IR_RX_CNT THR	31bit threshold
<b>RX_FIFO</b>					
0x28	[31]	R	0	IR_RX_DATA_TYPE	0:High 1:Low
	[30:0]	R	0	IR_RX_DATA_TIME	Counter FIFO Depth 16

For HerzTek Internal Use Only.

## 9.20. Memory Management

The memory management unit manages the data buffer between the MCU and DSP.

- System RAM: 160KB MCU RAM and 16KB cache RAM
- DSP RAM: 240KB DSP RAM
- ROM: 768KB ROM
- Serial FLASH support: The RTL8763BO supports internal 16Mbit serial FLASH for IC to storage MCU/DSP customized code, UI, DSP parameter, voice prompt and ROM code fix setting

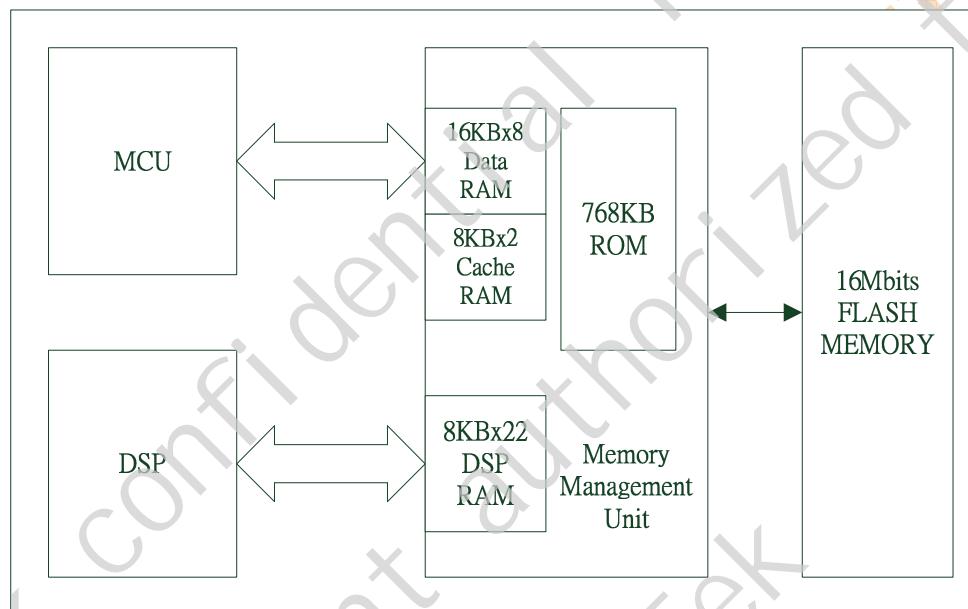


Figure 46. Memory Management

## 9.21. Power Management Unit - Switch Mode Regulator

The RTL8763BO supports dual switch mode regulator with planned external components. The inductor can be as small as 2.2 $\mu$ H with capacitor 2.2 $\mu$ F, which is ideal to design into small PCB applications, for example, wearable devices, earbud headsets, RWS headsets...etc.

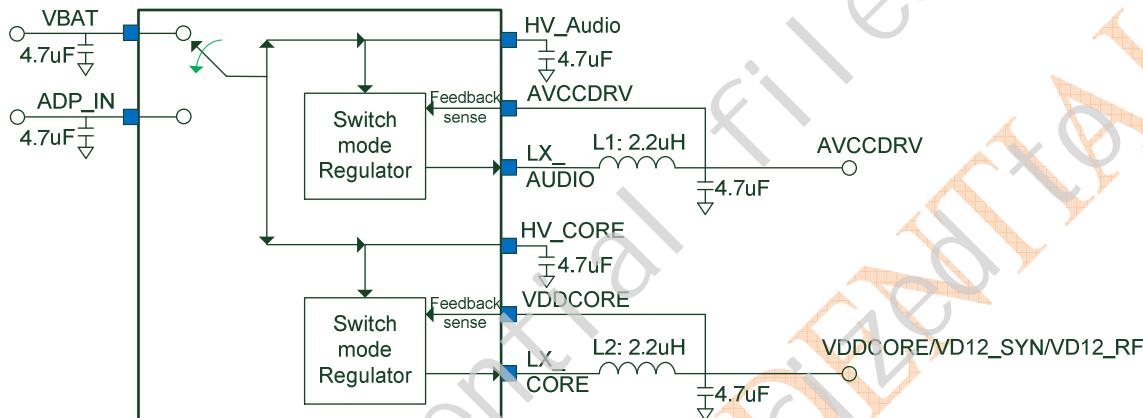


Figure 47. Power Management Unit - Switch Mode Regulator

The 2.2 $\mu$ H inductor is recommended to be a wire-wound inductor. This has a small DCR (around 0.5 $\Omega$ ) for good switching efficiency and good saturation current to guarantee the inductance is enough under normal operation.

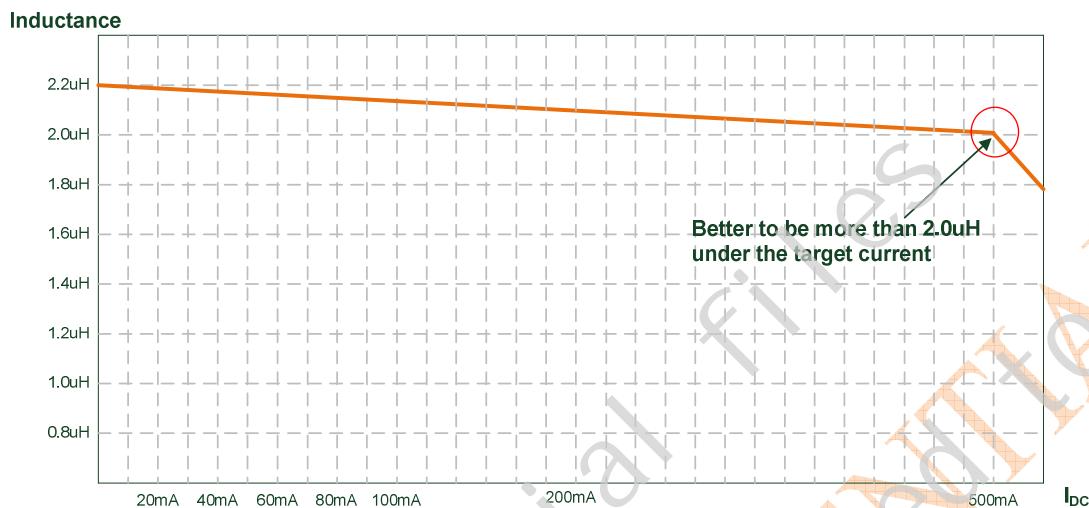
For both L1 and L2, the suggested specification is:

- IDC > 500mA
- DCR < 0.6 $\Omega$
- Wire-wound type

IDC is defined as saturation current, which is further defined as a current that will cause the inductance to be 20% degraded. This is quite different from the Irms or rated current, generally defined in inductor specifications as a current that causes an increase in inductor temperature of 20°C, e.g. 20°C → 40°C. The Irms number or rated current defined in the inductor datasheet may not be the logical buck inductor selection; so always ask the inductor vendor to provide the IDC current vs. inductance curve. The following figure shows an example.

Table 23. Inductor Selection

Manufacturer	Part	Value ( $\mu$ H)	DCR (m $\Omega$ )	I <sub>SAT</sub> (mA)	Dimension (mm <sup>3</sup> )
ZENITHTEK	ZADK-252012SB-2R2M	2.2	93	1800	2.5 x 2 x 1.2
ZENITHTEK	ZWP-0603-2R2K	2.2	560	600	1.2 x 1.8 x 1
TAIYO	NRH3010T2R2MNV	2.2	83	1300	3 x 3 x 1



**Figure 48. Inductor Selection**

- The capacitor 4.7 $\mu$ F specification should be X5R or above in order to ensure the ripple of the buck output power is small for good RF and audio characteristics
- The specification of the capacitor 4.7 $\mu$ F at VBAT and ADP\_IN should be X5R or above
- The routing trace of LX\_AUDIO and LX\_CORE on PCB should be short, and as wide as possible. The 2.2 $\mu$ H inductor and 4.7 $\mu$ F capacitor should be close to the chip

## Power Management Unit - Low Drop Linear Regulator

The RTL8763BO supports the low drop linear regulators listed below:

### LDO AUX1

Output with one capacitor 1 $\mu$ F; suggested to be X5R or above.

### LDO AUX1 LQ

Shares the same pin as LDO AUX1.

### LDO AUX2

Output with one capacitor 1 $\mu$ F; suggested to be X5R or above.

### MICBIAS LDO

No need to add an output capacitor. The output is adjustable according to the MEMs MIC specification.

### LDO VPA33

Output with one capacitor 1 $\mu$ F; suggested to be X5R or above.

The switch mode regulator can be programmed as a low drop linear regulator to eliminate the 2.2 $\mu$ H inductor if current consumption is not a concern.

## 9.22. Battery Charger

The RTL8763BO supports an integrated charger for Li-Ion battery application.

The supported charger current can be programmed in the UI tool; maximum is 400mA with thermal protection.

**Table 24. Charger Mode Definition**

Charger Mode	Battery Voltage	Charger Current	Note
Trickle charger mode	BAT < 3V	0.1C	Charger current is defined by customers via the UI tool.-
Constant Current Mode (CC Mode)	$3.0V \leq BAT \leq 4.2V$ or 4.35V	Customer defined; 400mA max.	Charger current is defined by customers via the UI tool. Customers should pay attention to the charger current setting with regard to their battery pack.
Constant Voltage Mode (CV Mode)	BAT = 4.2V or 4.35V	Controlled by MCU, the charger current slowly degrades from CC mode and stops at 0.1C	The CV mode voltage can be defined with the UI tool. Customers should set the CV mode voltage according to the Li-Ion battery specification. Do not set over specification.
Re-Charge Mode	BAT $\leq 4.0V$	-	-

### Trickle Charger Mode

If the battery voltage is below 3V, the charger will charge the battery with a low current of 0.1C (configurable). If the battery voltage does not rise up to 3.0V before time out, the charger will be in error and stop.

### Constant Current Mode

If the battery voltage is over 3.0V, the charger will be in constant current mode until battery voltage reaches 4.2V.

The constant current is defined in the UI tool by customer product definition.

### Constant Voltage Mode

If the battery voltage reaches 4.2V or 4.35V, the charger will go into constant voltage mode and the charge current will start to drop until reaching 0.1C (configurable). Note that the stop current can be defined in the UI tool by customer.

## Re-Charge Mode

If the battery charge process is completed, the charger will stop charging the battery. If the adapter is not removed and battery voltage drops over a period of time, the charger will re-start the charging process with a 0.25C charge current.

*\*\* Realtek verified the battery charger on Realtek EVB and branded Li-Ion batteries. Realtek confirm that the charger design is suitable based on this environment. The result may be changed due to different PCB layout, schematics design, rBOM, and battery package; customers should verify the battery charger function themselves in each design to assure the charger design correct for the application.*

## Charge Curve

The figure below is a battery voltage vs. charger current curve across different charger modes.

The Li-Ion battery charger in the RTL8763BO is very flexible for customers using various Li-Ion batteries. It supports both 4.2V and 4.35V Li-Ion battery packs. The charge to full voltage can be programmed in the UI tool by the customer.

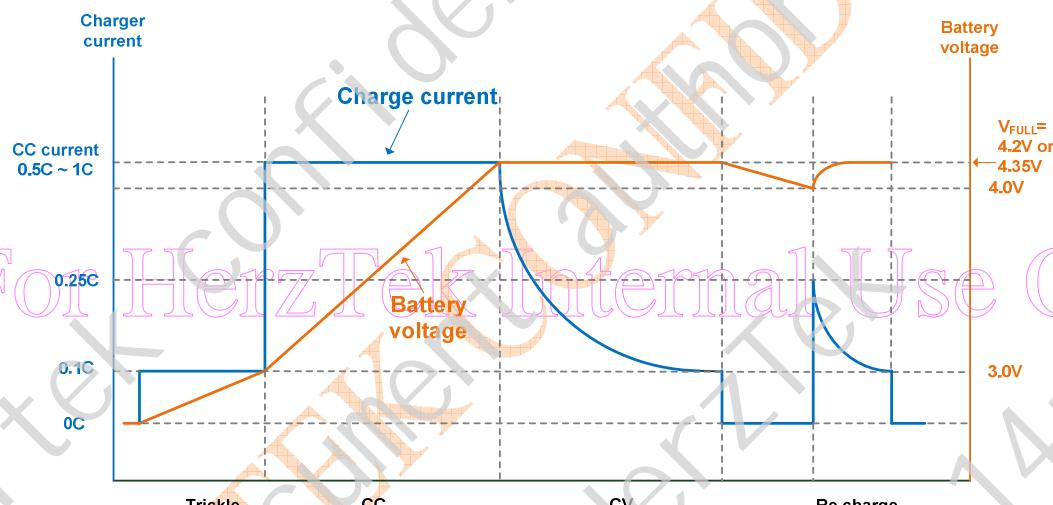


Figure 49. Battery Voltage vs. Charger Current Curve

## Battery Charger Protection Scheme

The RTL8763BO monitors the safety of the charger process and integrates several protection schemes. If the battery is damaged or ageing after a long time of operation, the RTL8763BO will implement the following protection:

- If the battery voltage does not rise to the target voltage in a defined time period, the battery will be judged as a dead battery and the charger will time out and then disable itself.
- Chip thermal detection will be implemented if the chip temperature rises up continuously and over the defined threshold. In such cases the charger current will be decreased or stopped.
- Watchdog protection; the system will be reset if the system hangs.

- Ambient detection design will monitor the battery temperature with an external thermistor close or attached to the battery pack.

*\*\* Realtek verified the battery charger on Realtek EVB and branded Li-Ion batteries. Realtek confirm that the charger design is suitable based on this environment. The result may be changed due to different PCB layout, schematics design, rBOM, and battery package; customers should verify the battery charger function themselves in each design to assure the charger design correct for the application.*

### Ambient Detection for Battery Charge Protection

The RTL8763BO supports an excellent, high precision ambient detection algorithm design with the reference circuit below and with a specified external thermistor located in the battery pack. With this specified thermistor (QVL: Murata, part number: NCP18WB473D03RB or NCP18WB473F10RB), a detection temperature of 0~5°C and 40~45°C can be achieved within +/-2°C difference. When in charger mode, if the reading temperature of the battery pack is out of (0~45°C) range, the charger will stop until the temperature is back to this range again. The stop and re-start temperature can be programmed with the UI tool.

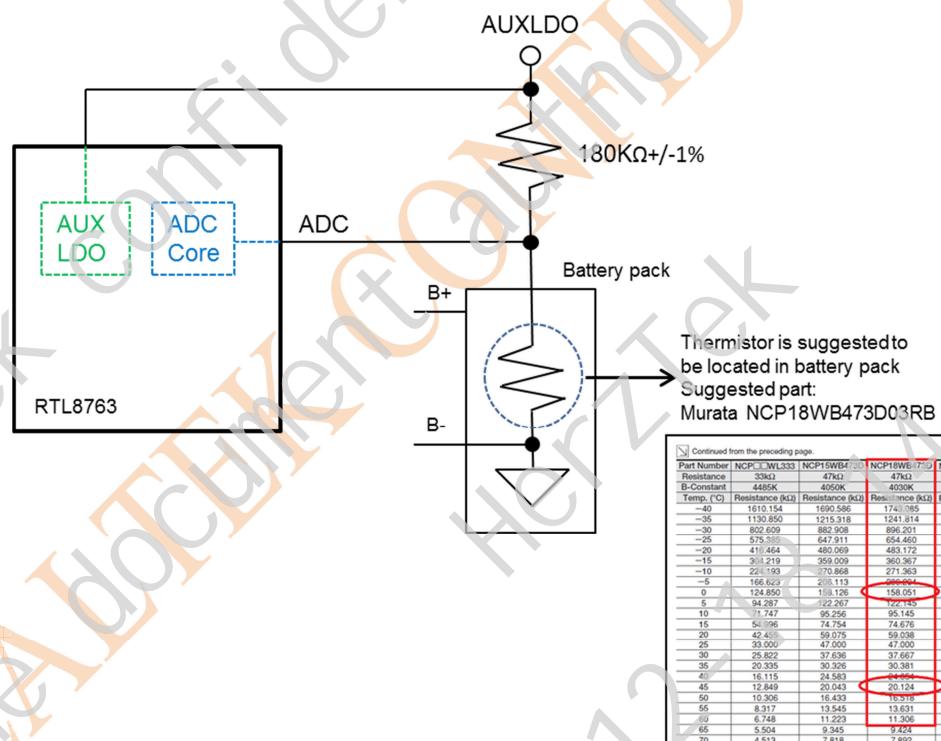


Figure 50. Ambient Detection for Battery Charge Protection

## 9.22.1. PMU Protection Scheme

### OVP

OVP (Over Voltage Protection) is used to protect the battery charger. The RTL8763BO continuously monitors the battery voltage. If an over voltage condition occurs, the charger will stop immediately. The OVP threshold is configurable in the UI tool.

### OCP

OCP (Over Current Protection) is used to protect the PMU in case of an over current condition occurs. It limits the regulator output to protect the PMU from burning out.

### UVP

UVP (Under Voltage Protection) is used to protect the system from operating under a low voltage condition. The RTL8763BO supports both SW UVP and HW UVP. If the battery voltage is below the lower band of the operating threshold, the system will be in hibernation mode first, and the PMU will force a stop of the output, or force a reset if the voltage continues to drop below the brown out or black out threshold.

- SW UVP: Configurable in the UI tool. If the battery voltage is below the pre-defined threshold, FW will turn off the system and hibernate
- HW UVP: The RTL8763BO supports hardware UVP to protect the system from operating under an un-defined voltage. There are two thresholds, brown out and black out. The UVP hardware protection scheme will be triggered when a low voltage condition occurs. The UVP states will be resolved only when the voltage has recovered from the  $V_{LOW} + V_{threshold}$

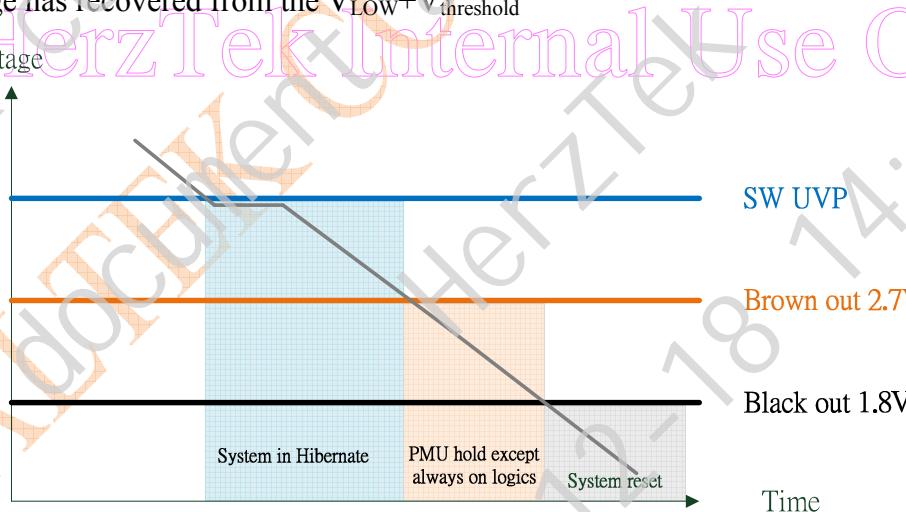


Figure 51. PMU Protection Scheme

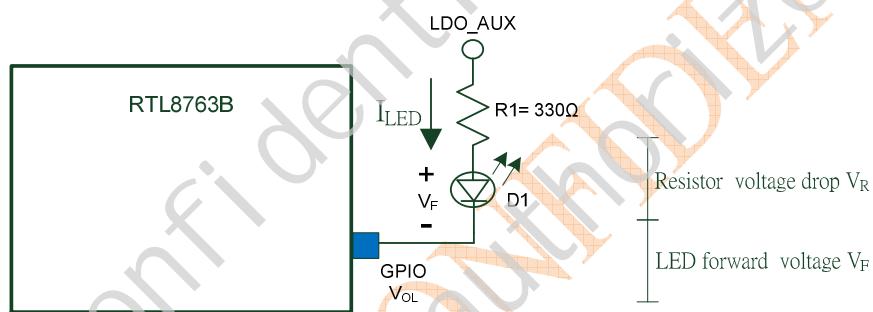
## LED

The RTL8763BO supports dynamic GPIO assignment to drive the LED for status indication. It offers flexibility to assign the GPIO at the best pin out location to ease PCB trace routing constrictions.

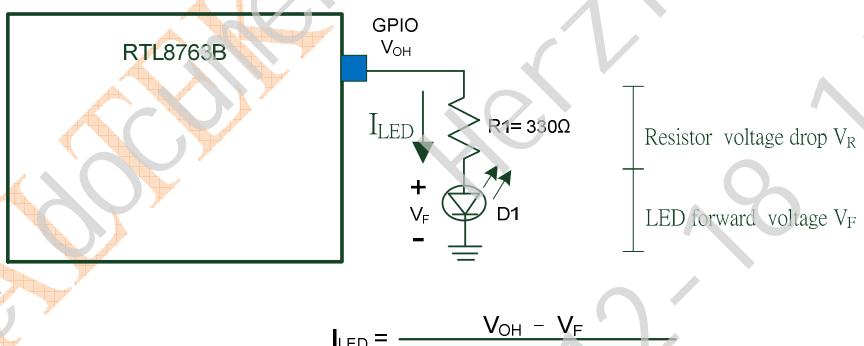
The method of LED indication can be selected in the UI tool and programmed into FLASH memory in the mass production process. The LED can still be active in deep sleep mode without the need for MCU control.

**Table 25. LED**

Parameter	Min.	Typ.	Max.	Unit
Driving Capacity	-	-	12	mA
GPIO VOH	1.8	-	3.6	V
GPIO VOL	-	0.2	-	-



$$I_{LED} = \frac{LDO\_AUX - V_{OL} - V_F}{R1}$$



$$I_{LED} = \frac{V_{OH} - V_F}{R1}$$

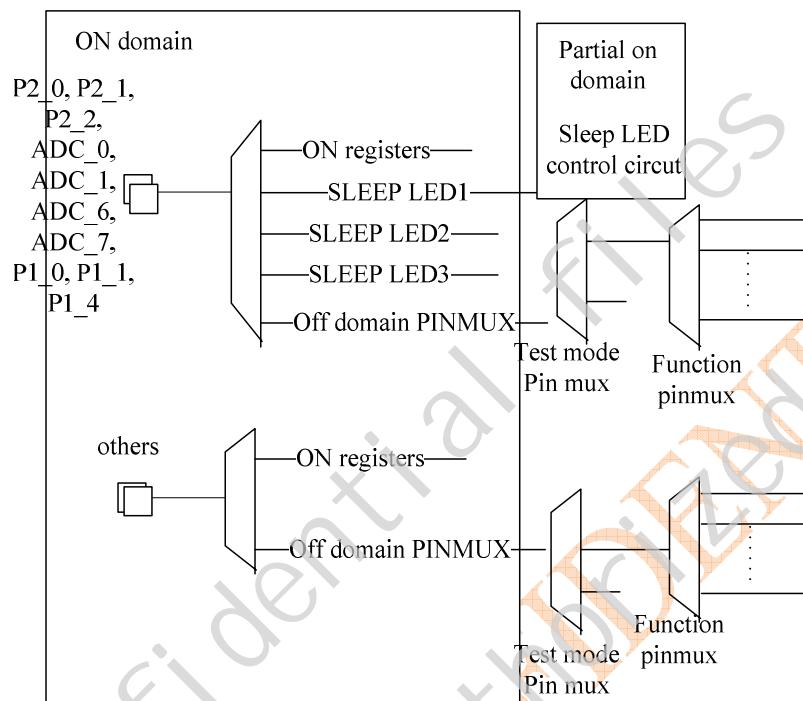
**Figure 52. LED**

Where  $V_F$  is defined in the LED specification,  $V_{OL}$  is defined as the GPIO drive low level, typically 0.2V.  $V_{OH}$  depends on the LDO\_AUX output level. If  $LDO\_AUX=1.8V$ , then  $V_{OH}=1.8V$ . If  $LDO\_AUX=3.3V$ , then  $V_{OH}=3.3V$ .

$R1=330\Omega$  for LED drive with 4mA with  $LDO\_AUX=3.3V$ .

$R1$  can be adjusted according to the LED brightness needed.

## I/O Mux



**Figure 53. I/O Mux**

The table below shows a PIN MUX available list. Each function in the table can be directed to the selected GPIO in the UI tool. These parameters can be set and programmed into the IC.

**Table 26. PIN MUX Availability List**

0	IDEL	2 5	qdec_phase_a_z	5 0	SPI0_CLK (master only)	7 5	KEY_COL_17	1 0 0	SDI (CODEC - slave)	1 2 5	ADC DAT (SPORT0)
1	HCI_UART_TX	2 6	qdec_phase_b_z	5 1	SPI0_MO (master only)	7 6	KEY_COL_18	1 0 1	SDO (CODEC - slave)	1 2 6	DAC DAT (SPORT0)
2	HCI_UART_RX	2 7	LOG0_UART_TX	5 2	SPI0_MI (master only)	7 7	KEY_COL_19	1 0 2	LRC_I (PCM)	1 2 7	MCLK
8	I2C1_DA_T	3 3	IRDA_TX	5 8	KEY_COL_0	8 3	KEY_ROW_5	1 0 8	BT_COEX_I_2	-	-
9	PWM0_P	3 4	IRDA_RX	5 9	KEY_COL_1	8 4	KEY_ROW_6	1 0 9	BT_COEX_I_3	-	-
10	PWM0_N	3 5	DATA_UART_TX	6 0	KEY_COL_2	8 5	KEY_ROW_7	1 1 0	BT_COEX_O_0	-	-
11	PWM1_P	3 6	DATA_UART_RX	6 1	KEY_COL_3	8 6	KEY_ROW_8	1 1 1	BT_COEX_O_1	-	-

1 2	PWM1_N	3 7	DATA_UART_CTS	6 2	KEY_COL_4	8 7	KEY_ROW_9	1 1 2	BT_COEX_O_2	-	-
1 3	PWM0	3 8	DATA_UART_RTS	6 3	KEY_COL_5	8 8	KEY_ROW_10	1 1 3	BT_COEX_O_3	-	-
1 4	PWM1	3 9	SPI1_SS_N_0 (master only)	6 4	KEY_COL_6	8 9	KEY_ROW_11	1 1 4	PTA_I2C_CLK (slave only)	-	-
1 5	PWM2	4 0	SPI1_SS_N_1 (master only)	6 5	KEY_COL_7	9 0	DWGPI0	1 1 5	PTA_I2C_DAT (slave only)	-	-
1 6	PWM3	4 1	SPI1_SS_N_2 (master only)	6 6	KEY_COL_8	9 1	LRC (SPORT1)	1 1 6	PTA_I2C_INT_O UT	-	-
1 7	PWM4	4 2	SPI1_CLK (master only)	6 7	KEY_COL_9	9 2	BCLK (SPORT1)	1 1 7	DSP_GPIO_OUT	-	-
1 8	PWM5	4 3	SPI1_MO (master only)	6 8	KEY_COL_10	9 3	ADCDAT (SPORT1)	1 1 8	DSP_JTCK	-	-
1 9	PWM6	4 4	SPI1_MI (master only)	6 9	KEY_COL_11	9 4	DACDAT (SPORT1)	1 1 9	DSP_JTDI		-
2 0	PWM7	4 5	SPI0_SS_N_0 (slave)	7 0	KEY_COL_12	9 5	SPDIF_TX	1 2 0	DSP_JTDO		-
2 1	qdec_phas e_a_x	4 6	SPI0_CLK (slave)	7 1	KEY_COL_13	9 6	DMIC1_CLK	1 2 1	DSP_JTMS		-
2 2	qdec_phas e_b_x	4 7	SPI0_SO (slave)	7 2	KEY_COL_14	9 7	DMIC1_DAT	1 2 2	DSP_JTRST		-
2 3	qdec_phas e_a_y	4 8	SPI0_SI (slave)	7 3	KEY_COL_15	9 8	LRC_I (CODEC - slave)	1 2 3	LRC (SPORT0)		-
2 4	qdec_phas e_b_y	4 9	SPI0_SS_N_0 (master only)	7 4	KEY_COL_16	9 9	BCLK_I (CODEC - slave)	1 2 4	BCLK (SPORT0)		-

## 9.23. Reference Circuits

### 9.23.1. RTL8763BO Reference Circuits

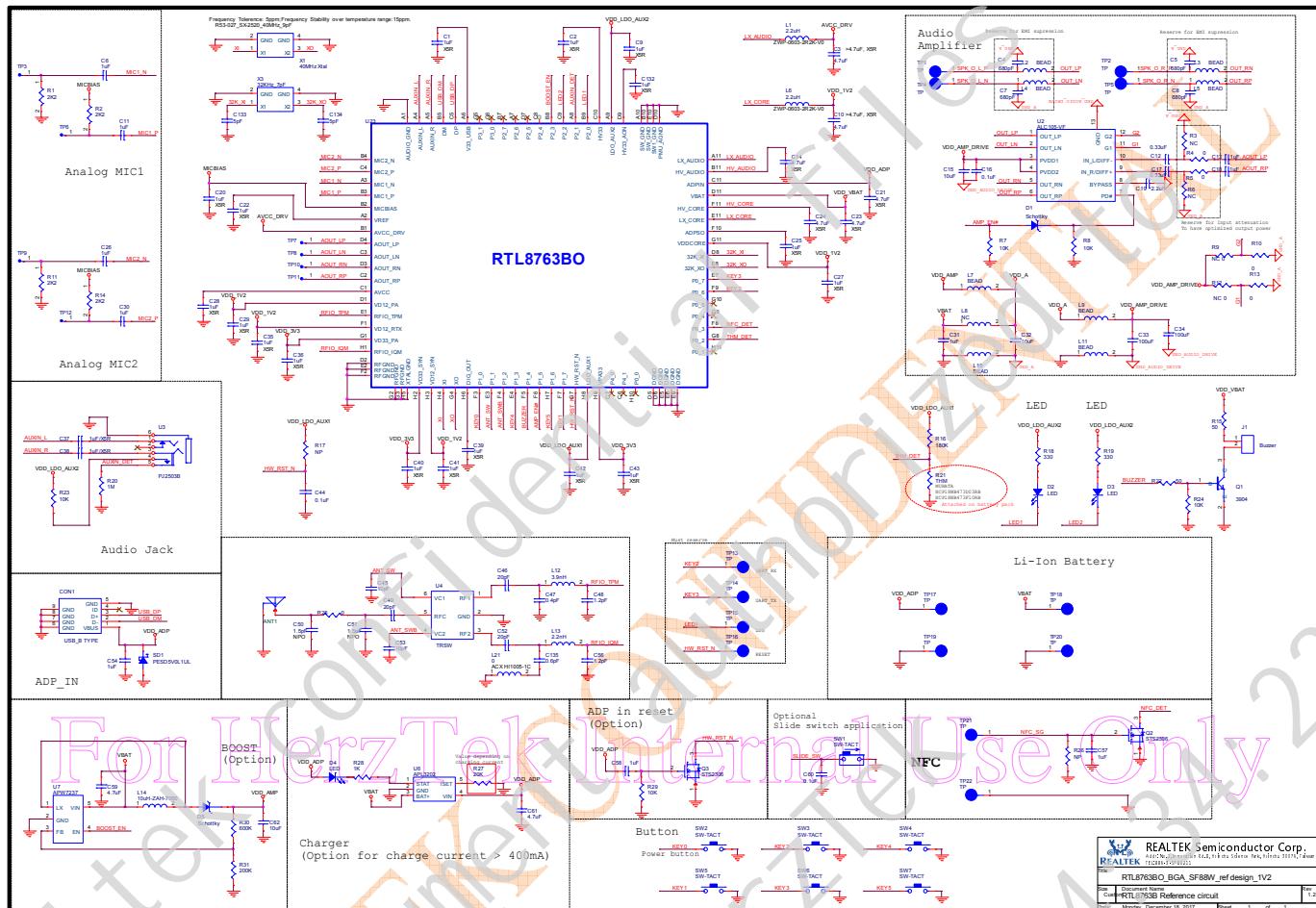


Figure 54. RTL8763BO Reference Circuits

## 10. Electrical Characteristics

### 10.1. Absolute Maximum Ratings

Table 27. Absolute Maximum Ratings

Item	Min.	Typical	Max.	Unit
Storage Temperature	-40	-	+105	°C
<b>Power Management Unit</b>	<b>Min.</b>	<b>Typical</b>	<b>Max.</b>	<b>Unit</b>
VDD_CORE	VDDCORE	-	1.32	V
Synthesizer control	VD12_SYNC	-	1.32	V
RF transceiver control	VD12_RTX	-	1.32	V
Codec	AVCC @ 1.8V mode	-	2.1	V
	AVCC @ 2.8V mode	-	2.9	V
Headphone driver	AVCC_DRV @ 1.8V mode	-	2.1	V
	AVCC_DRV @ 2.8V mode	-	2.9	V
VDDIO1/ADC Power	VDD_AUX1	-	3.6	V
VDDIO2	VDD_AUX2	-	3.6	V
BAT IN	VBAT	-	4.5	V
ADAPTER IN	ADP_IN (DC)	-	7	V

### 10.2. Recommended Operating Conditions

Table 28. Recommended Operating Conditions

Item	Min.	Typical	Max.	Unit
Operating Temperature	-40	25	+85	°C
<b>Power Management Unit</b>	<b>Min.</b>	<b>Typical</b>	<b>Max.</b>	<b>Unit</b>
VDD_CORE	VDDCORE	1.14	1.1	1.26
Synthesizer control	VD12_SYNC	1.14	1.2	1.26
RF transceiver control	VD12_RTX	1.14	1.2	1.26
Codec	AVCC @ 1.8V mode	1.7	1.8	1.98
	AVCC @ 2.8V mode	2.6	2.7	2.8
Headphone driver	AVCC_DRV @ 1.8V mode	1.85	1.9	2.1
	AVCC_DRV @ 2.8V mode	2.7	2.8	2.9
VDDIO1/ADC Power	VDD_AUX1	1.8	-	3.6
VDDIO2	VDD_AUX2	2.8	-	3.6
BAT IN	VBAT	2.8	-	4.35
ADAPTER IN	ADP_IN (DC)	4.5	-	6.5

### 10.3. Power Management Unit; Switch Mode Regulator for Audio Core and Audio Drive Stage

**Table 29. Power Management Unit; Switch Mode Regulator for Audio Core and Audio Drive Stage**

Item	Min.	Typ.	Max.	Unit
Input voltage	2.8	-	5	V
Output voltage	1.8	-	2.8	V
Inductor inductance	-	2.2	-	µH
Inductor specification, saturation current	-	500	-	mA
Inductor specification, DCR	-	0.1	0.6	Ω
Input capacitor	-	4.7	-	µF
Output capacitor	-	4.7	-	µF

(\*I) +/-20%@500mA

### 10.4. Power Management Unit; Switch Mode Regulator for Digital Core, RF, and Synthesizer

**Table 30. Power Management Unit; Switch Mode Regulator for Digital Core, RF, and Synthesizer**

Item	Min.	Typ.	Max.	Unit
Input voltage	2.8	-	5	V
Output voltage	-	1.2	-	V
Inductor inductance	-	2.2	-	µH
Inductor specification, saturation current	-	500	-	mA
Inductor specification, DCR	-	0.1	0.6	Ω
Input capacitor	-	4.7	-	µF
Output capacitor	-	4.7	-	µF

### 10.5. Power Management Unit; Low Drop Linear Regulator

**Table 31. Power Management Unit; Low Drop Linear Regulator**

#### LDO AUX1

Item	Min.	Typ.	Max.	Unit
Input voltage	2.8	-	5	V
Output voltage	1.8	-	3.6	V
Output current	-	150(*1)	-	mA
Quiescent current	-	30	-	µA

**LDO AUX1 L<sub>O</sub>**

Item	Min.	Typ.	Max.	Unit
Input voltage	2.8	-	5	V
Output voltage	1.8	-	3.6	V
Output current	-	3(*2)	-	mA

**LDO AUX2**

Item	Min.	Typ.	Max.	Unit
Input voltage	2.8	-	5	V
Output voltage	2.8	-	3.6	V
Output current	-	150(*3)	-	mA
Quiescent current	-	30	-	μA

**PALDO**

Item	Min.	Typ.	Max.	Unit
Input voltage	2.8	-	5	V
Output voltage	2.8	3.3	-	V
Output current	-	150(*4)	-	mA
Quiescent current	-	30	-	μA

(\*1) (\*3) For external loading use, the maximum is 100mA.

(\*2) For external loading use, the maximum is 3mA

(\*4) Not for external use

## 10.6. Digital I/O

**Table 32. Digital I/O voltage**

Item	Min.	Typ.	Max.	Unit
Input low voltage	-0.4	-	0.4	V
Input high voltage	0.7 X VDDIO	-	VDDIO+0.4	V
Output low voltage (VDDIO=1.8V)	-	-	0.2	V
Output high voltage (VDDIO=1.8V)	VDDIO-0.2	-	-	V
Output low voltage (VDDIO=3V)	-	-	0.4	V
Output high voltage (VDDIO=3V)	VDDIO-0.4	-	-	V

VDDIO is LDO\_AUX1 or LDO\_AUX2, GPIO power domain, check the pin description.

## 10.7. Power Management Unit; Battery Charger

**Table 33. Power Management Unit; Battery Charger**

Item	Min.	Typ.	Max.	Unit
ADP_IN input voltage	4.5	5	6.5	V
Charge current, ADP_IN >= 5V	-	-	400	mA
Charge current, 4.5V < ADP_IN < 5V	-	-	200	mA
Trickle charge current	5	-	-	mA(*1)

VBAT in Trickle charge mode	0.5	-	3.0	V
VBAT in constant current mode	3.0	-	4.35(*1)	V, max programmable
VBAT in constant voltage mode	-	4.2	4.35(*2)	V, max programmable
Battery charge full, stop current	2mA	0.1C	-	C(*3)
Re-charge threshold	-	4.0	-	V(*4)

(\*1) Adjustable by UI, the max is defined by Li-Ion battery

(\*2) Adjustable by UI, the max is defined by Li-Ion battery

(\*3) 1C= Li-Ion battery full capacity

(\*4) UI configurable

## 10.8. Audio Codec DAC (If not specially marked, the test is with AVcc = 2.8V)

Table 34. Audio Codec DAC (If not specially marked, the test is with AVDD= 2.8V)

	Conditions		Min	Typ.	Max	Unit
Over-sampling rate ( f )	-	-	-	128	-	fs
Operating Temperature	-	-	-40	25	85	°C
Resolution	-	-	-	24	-	Bits
Output Sample Rate, F <sub>sample</sub>	8,16,32,44.1,48,88.2,96kHz	-	8	-	96	kHz
Signal to Noise Ratio (SNR @cap-less mode)	f <sub>in</sub> =1kHz B/W=20~20kHz A-weighted THD+N < 0.02% 0dBFS signal Load=100KΩ	AV <sub>CC</sub> =1.80V  AV <sub>CC</sub> =2.80V	-	98  102	-	dBA
Signal to Noise Ratio (SNR @single-end mode)	f <sub>in</sub> =1kHz B/W=20~20kHz A-weighted THD+N < 0.02% 0dBFS signal Load=100KΩ	AV <sub>CC</sub> =1.80V  AV <sub>CC</sub> =2.80V	-	98  102	-	dBA
Dynamic range	24-bit mode  16-bit mode	AV <sub>CC</sub> =1.80V  AV <sub>CC</sub> =2.80V  AV <sub>CC</sub> =1.80V  AV <sub>CC</sub> =2.80V	- - - -	97 101 96 96	- - - -	dB
Digital Gain		-65.625	-	0	-	dB
Digital Gain Resolution		-	0.375	-	-	dB
Analog Gain @headphone stage		-9		0	-	dB
Analog Gain Step		-	3	-	-	dB
Maximum Output Power	16Ω load  32Ω load	AV <sub>CC</sub> =1.80V  AV <sub>CC</sub> =2.80V  AV <sub>CC</sub> =1.80V	- - -	16 40 8	- - -	mW

	Conditions	Min	Typ.	Max	Unit
	AV <sub>CC</sub> =2.80V	-	20	-	
Allowed Load	Resistive	-	16	O.C.	Ω
	Capacitive	1500	-	-	pF
THD+N @single-end mode, 2.8V or 1.8V, 0dBFS input	100KΩ load	-	0.02	-	%
	16Ω load	-	0.04	-	
Signal to Noise Ratio (SNR @ earphone load)	16Ω load, 0dBFS input relative to digital silence	-	96	-	dB
Crosstalk between channels	L vs. R, measured at -10dBFS@1kHz input, single-ended output, 2.8V@16ohm	-	-95	-	dB
	L vs. R, measured at -10dBFS@1kHz input, differential output, 2.8V@16ohm	-	-98	-	dB
	L vs. R, measured at -10dBFS@1kHz input, cap-less output, 2.8V@16ohm	-	-54	-	dB
Analog supply voltage (AV <sub>CC</sub> )	(1) For earphone, AV <sub>CC</sub> = 1.80V (2) For earphone/speakers, AV <sub>CC</sub> = 2.80V	1.80	2.8	3.0	V

## 10.9. Audio Codec ADC (If not specially marked, the test is with AV<sub>CC</sub>= 2.8V)

Table 35. Audio Codec ADC (If not specially marked, the test is with V<sub>CC</sub>= 2.8V)

	Conditions	Min	Typ.	Max	Unit
Operating Temperature	-	-40	25	85	°C
Resolution	-		24		Bits
Input sample rate, f <sub>sample</sub>	8,16,32,44.1,48, 88.2, 96kHz Note: Better to have 88.2, 96kHz	8		96	kHz
Signal to Noise Ratio (SNR @Line-in mode)	f <sub>in</sub> =1kHz B/W=20~20kHz A-weighted THD+N < 0.1% 800mV <sub>RMS</sub> input (AV <sub>CC</sub> =2.8V)	-	97	-	dBA

	Conditions		Min	Typ.	Max	Unit
Signal to Noise Ratio (SNR @Line-in mode)	$f_{in}=1\text{kHz}$ B/W=20~20kHz A-weighted $\text{THD+N} < 0.1\%$ 800mV <sub>RMS</sub> input (AV <sub>CC</sub> =1.8V)		-	96	-	dBA
Signal to Noise Ratio (SNR @MIC mode)	$f_{in}=1\text{kHz}$ B/W=20~20kHz A-weighted $\text{THD+N} < 0.5\%$ 8mVRMS input 40dB gain (AV <sub>CC</sub> =2.8V)	8kHz, 16kHz	-	70	-	dBA
Dynamic range	AV <sub>CC</sub> =1.80V		-	95	-	dB
	AV <sub>CC</sub> =2.80V		-	95	-	
Digital Gain	-		-17.625		30	dB
Digital Gain Resolution	-		-	0.375		dB
MIC Boost Gain	0/20/30/40dB		0	20	40	dB
MIC Input full-scale at maximum gain (differential)	Gain=40dB		-	5.65*AVDD	-	mV <sub>RMS</sub>
MIC Input full-scale at minimum gain (differential)	Gain=0dB		-	0.8*AVDD	-	V <sub>PP</sub>
3dB bandwidth	-		20	-	-	kHz
Microphone mode input impedance	Input impedance		-	6	10	KΩ
	Input capacitance		-	20	-	pF
THD+N (microphone input) @30mV <sub>RMS</sub> input, 20dB gain	-		-	0.03	-	%
THD+N (line input) @-3dBFS	AV <sub>CC</sub> = 1.8 or 2.8V		-	0.02	-	%
ADC channels	-		-	2	-	ch
Line-input full-scale	AV <sub>CC</sub> = 2.8V		-	2.2	-	V <sub>PP</sub>
Line-input full-scale	AV <sub>CC</sub> = 1.8V		-	1.4	-	V <sub>PP</sub>
Line-input input impedance	Input impedance		-	10	-	KΩ
	Input capacitance		-	20	-	pF
Crosstalk between channels	Line-in		-	-98	-	dB
	MIC-IN		-	-98	-	dB

	<b>Conditions</b>	<b>Min</b>	<b>Typ.</b>	<b>Max</b>	<b>Unit</b>
Analog supply voltage ( $AV_{CC}$ )	(1) For BT earphone, $AV_{CC}=1.80V$ (2) For BT earphone/ speakers, $AV_{CC}=2.80V$	1.80	2.8	3.0	V
MIC bias	$AV_{CC}=2.80V$	$AVDD*0.75$	-	$AVDD*0.9$	V
	$AV_{CC}=1.8V$	1.5V	-	-	

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## 11. RF Characteristics

### 11.1. Transmitter BT Classic Basic Data Rate (BDR)

Table 366. Transmitter BT Classic Basic Data Rate (BDR)

Parameter	Min.	Typ.	Max.	Bluetooth Specification
Transmitter Frequency (MHz)	2402	-	2480	2402 ~ 2480, 79CH
Transmitter Power (dBm)	-	10	-	-
Transmitter power control step (dB)	-	4	-	2dB ≤ step size ≤ 8 dB
20dB bandwidth (kHz)	-	900	-	1000kHz
Initial carrier frequency offset <sup>(*)1</sup>	-	±10kHz	-	±75kHz
Frequency drift (kHz)	DH1	-	±10kHz	±25kHz
	DH3	-	±10kHz	±40kHz
	DH5	-	±10kHz	±40kHz
Frequency deviation Δf <sub>avg</sub> (kHz)	-	160	-	140~175kHz
Frequency deviation Δf <sub>2max</sub> (kHz)	115	-	-	≥ 115kHz
f <sub>1avg</sub> /f <sub>2avg</sub>	-	0.88	-	≥ 0.8
Adjacent channel TX power (dBm)	N+2	-	-20	≤ -20dBm
	N-2	-	-20	≤ -20dBm
	N+3	-	-40	≤ -40dBm
	N-3	-	-40	≤ -40dBm

(\*1) Initial carrier offset should be calibrated in MP process in customer side.

Table 377. Harmonic

Parameter	2402MHz	2440MHz	2480MHz	Unit
2 <sup>nd</sup> harmonic typical <sup>(*)3</sup>	-	-50	-	dBm
3 <sup>rd</sup> harmonic typical <sup>(*)3</sup>	-	-50	-	dBm

(\*3) A π-type matching or a Low Pass Filter (LPF) or a Band Pass Filter (BPF) is needed to suppress the 2nd and 3rd harmonic energy, as described in the Realtek design guide.

### 11.2. Transmitter BT Classic Enhanced Data Rate (EDR)

Table 38. Transmitter BT Classic Enhanced Data Rate (EDR)

Parameter	Min.	Typ.	Max.	Bluetooth Specification
Transmitter frequency (MHz)	2402	-	2480	2402 ~ 2480, 79CH
Relative TX power (dB)	-	-1	-	-4 ~ +1
EDR carrier frequency stability (kHz)	-	10	-	-75≤ωi≤75 -75≤(ωi+ωo)≤75
2M EDR modulation accuracy EDR TX=7.5 dBm	RMS DEVM	-	0.2	≤ 0.2
	Peak DEVM	-	0.35	≤ 0.35
	99% DEVM	-	100%	99%DEVM ≤ 0.3
3M EDR modulation accuracy EDR TX=7.5 dBm	RMS DEVM	-	0.13	≤ 0.13
	Peak DEVM	-	0.25	≤ 0.25
	99% DEVM	-	100%	≥ 99%

Parameter		Min.	Typ.	Max.	Bluetooth Specification
EDR differential phase encoding		-	100%	-	$\geq 99\%$
2M EDR in-band spurious emission (dBm)	M-N  = 1	-	-	-26	$P_{TX-26dB}(f) \leq P_{TXref} - 26dB$ for $ M-N  = 1$ (M: Tx Channel, N: Adjacent Channel)
	M-N  = 2	-	-	-20	$P_{TX}(f) \leq -20dBm$ for $ M-N  = 2$ (M: Tx Channel, N: Adjacent Channel)
	M-N  = 3	-	-	-40	$P_{TX}(f) \leq -40dBm$ for $ M-N  \geq 3$ (M: Tx Channel, N: Adjacent Channel)
3M EDR in-band spurious emission (dBm)	M-N  = 1	-	-	-26	$P_{TX-26dB}(f) \leq P_{TXref} - 26dB$ for $ M-N  = 1$ (M: Tx Channel, N: Adjacent Channel)
	M-N  = 2	-	-	-20	$P_{TX}(f) \leq -20dBm$ for $ M-N  = 2$ (M: Tx Channel, N: Adjacent Channel)
	M-N  = 3	-	-	-40	$P_{TX}(f) \leq -40dBm$ for $ M-N  \geq 3$ (M: Tx Channel, N: Adjacent Channel)

### 11.3. Transmitter BT Classic Bluetooth Low Energy (BLE IQM)

Table 39. Transmitter BT Classic Bluetooth Low Energy (BLE IQM)

Parameter		Min.	Typ.	Max.	Bluetooth Specification
Transmitter frequency (MHz)		2402	-	2480	2402 ~ 2480, 40CH
Transmitter Power (dBm)		-	10	-	-
In-band emission (dBm)	M-N  = 2	-	-	-20	$PTX \leq -20 dBm$ for $(f_{TX} \pm 2 MHz)$
	M-N  $\geq 3$	-	-	-30	$PTX \leq -30 dBm$ for $(f_{TX} \pm [3+n] MHz)$ ; where n=0,1,2...
Carrier frequency offset (kHz) and drift(kHz)	$f_n$ (*1)	-	$\pm 10$	-	$f_{TX} - 150kHz \leq f_n \leq f_{TX} + 150 kHz$
	$ f_0, f_n , n=2,3,4...k$	-	$\pm 15$	-	$ f_0, f_n  \leq 50 kHz$ where n=2,3,4...k
$ f_1, f_0 $ and $ f_n - f_{n-5} $		-	$\pm 15$	-	$ f_1, f_0  \leq 20 kHz$ and $ f_n - f_{n-5}  \leq 20 kHz$
Modulation characteristics $\Delta f_{avg}$ (kHz)		-	250	-	225~275kHz
Frequency deviation 99.9% of $\Delta f_{max} \geq 185kHz$		-	100%	-	$\geq 99.9\%$
$f_{1avg}/f_{2avg}$		-	0.88	-	$\geq 0.8$

(\*1) Initial carrier offset should be calibrated in the MP process at the customer side.

## 11.4. Receiver BT Classic Basic Data Rate (BDR)

Table 40. Receiver BT Classic Basic Data Rate (BDR)

Parameter	Min.	Typ.	Max.	Bluetooth Specification
Sensitivity, DH1 (dBm)	-94.5	-	-	$\leq -70\text{dBm}$ , BER $\leq 0.1\%$
Sensitivity, DH3/DH5 (dBm)	-94.5	-	-	$\leq -70\text{dBm}$ , BER $\leq 0.1\%$
C/I carrier over Interference (dB)	Co-channel	-	10	$C/I_{\text{co-channel}} (\text{dB}) \leq 11\text{dB}$
	Adjacent 1MHz	-	-13	$C/I_{1\text{MHz}} \leq 0\text{dB}$
	Adjacent 2MHz	-	-43	$C/I_{2\text{MHz}} \leq -30\text{dB}$
	Adjacent $\geq 3\text{MHz}$	-	-45	$C/I_{3\text{MHz}} \leq -40\text{dB}$
	Image interference	-	-22	$C/I_{\text{Image}} \leq -9\text{dB}$
	Adjacent (1MHz) interference to in-band mirror frequency	-	-29	$C/I_{\text{Image}+1\text{MHz}} \leq -20\text{dB}$
Blocking (dBm)	30MHz ~ 2000MHz	-10	-	-10
	2000MHz ~ 2400MHz	-27	-	-27
	2500MHz ~ 3000MHz	-27	-	-27
	3000MHz ~ 12.75GHz	-10	-	-10
Inter-modulation (*1) (*2)	BER @ f1: 2407MHz & f2 = 2412MHz (%)	0		$\leq 0.1$
	Max Intermodulation Level @ f1: 2407MHz & f2 = 2412MHz (dBm)	-30.0		$\geq -39$
	BER @ f1: 2397MHz & f2 = 2392MHz (%)	0		$\leq 0.1$
	Max Intermodulation Level @ f1: 2397MHz & f2 = 2392MHz (dBm)	-30.0		$\geq -39$
	BER @ f1: 2446MHz & f2 = 2451MHz (%)	0		$\leq 0.1$
	Max Intermodulation Level @ f1: 2446MHz & f2 = 2451MHz (dBm)	-30		$\geq -39$
	BER @ f1: 2436MHz & f2 = 2431MHz (%)	0		$\leq 0.1$
	Max Intermodulation Level @ f1: 2436MHz & f2 = 2431MHz (dBm)	-30		$\geq -39$
	BER @ f1: 2485MHz & f2 = 2490MHz (%)	0		$\leq 0.1$
	Max Intermodulation Level @ f1: 2485MHz & f2 = 2490MHz (dBm)	-30		$\geq -39$
	BER @ f1: 2475MHz & f2 = 2470MHz (%)	0		$\leq 0.1$
	Max Intermodulation Level @ f1: 2475MHz & f2 = 2470MHz (dBm)	-30		$\geq -39$
Maximum Input (dBm)		0		BER $\leq 0.1\% @ -20\text{dBm}$

## 11.5. Receiver BT Classic Enhanced Data Rate (EDR)

Table 41. Receiver BT Classic Enhanced Data Rate (EDR)

Parameter	Min.	Typ.	Max.	Bluetooth Specification
Sensitivity, 2-DH5 (dBm)	-94	-	-	$\leq -70\text{dBm}$ , BER $\leq 0.01\%$
Sensitivity, 3-DH5 (dBm)	-87	-	-	$\leq -70\text{dBm}$ , BER $\leq 0.01\%$
EDR BER Floor performance	-	0	-	BER $\leq 0.001\%$
EDR-2M C/I carrier over Interference (dB)	Co-channel	-	10	$C/I_{\text{co-channel}} (\text{dB}) \leq 13\text{dB}$
	Adjacent 1MHz	-	-12	$C/I_{1\text{MHz}} \leq 0\text{dB}$
	Adjacent 2MHz	-	-42	$C/I_{2\text{MHz}} \leq -30\text{dB}$
	Adjacent $\geq 3\text{MHz}$	-	-47	$C/I_{3\text{MHz}} \leq -40\text{dB}$
	Image interference	-	-28	$C/I_{\text{Image}} \leq -7\text{dB}$
	Adjacent (1MHz) interference to in-band mirror frequency	-	-32	$C/I_{\text{Image}\pm 1\text{MHz}} \leq -20\text{dB}$
EDR-3M C/I carrier over Interference (dB)	Co-channel	-	17	$C/I_{\text{co-channel}} (\text{dB}) \leq 21\text{dB}$
	Adjacent 1MHz	-	-5	$C/I_{1\text{MHz}} \leq 5\text{dB}$
	Adjacent 2MHz	-	-36	$C/I_{2\text{MHz}} \leq -25\text{dB}$
	Adjacent $\geq 3\text{MHz}$	-	-44	$C/I_{3\text{MHz}} \leq -33\text{dB}$
	Image interference	-	-23	$C/I_{\text{Image}} \leq 0\text{dB}$
	Adjacent (1MHz) interference to in-band mirror frequency	-	-27	$C/I_{\text{Image}\pm 1\text{MHz}} \leq -13\text{dB}$
Maximum Input (dBm)		0		BER $\leq 0.1\% @ -20\text{dBm}$

## 11.6. Receiver BT Classic Bluetooth Low Energy (BLE) IQM

Table 42. Receiver BT Classic Bluetooth Low Energy (BLE) IQM

Parameter	Min.	Typ.	Max.	Bluetooth Specification
Sensitivity LE 1M	-97	-	-	$\leq -70\text{dBm}$ , PER $\leq 30.8\%$
C/I carrier over Interference (dB)	Co-channel	-	6	$\text{C/I}_{\text{co-channel}} (\text{dB}) \leq 21\text{dB}$
	Adjacent 1MHz	-	-3	$\text{C/I}_{1\text{MHz}} \leq 15\text{dB}$
	Adjacent 2MHz	-	-40	$\text{C/I}_{2\text{MHz}} \leq -17\text{dB}$
	Adjacent $\geq 3\text{MHz}$	-	-50	$\text{C/I}_{3\text{MHz}} \leq -27\text{dB}$
	Image interference	-	-29	$\text{C/I}_{\text{Image}} \leq -9\text{dB}$
	Adjacent (1MHz) interference to in-band mirror frequency	-	-30	$\text{C/I}_{\text{Image} \pm 1\text{MHz}} \leq -15\text{dB}$
Blocking (dBm)	30MHz ~ 2000MHz	-30	-	-30
	2000MHz ~ 2400MHz	-35	-	-35
	2500MHz ~ 3000MHz	-35	-	-35
	3000MHz ~ 12.75GHz	-30	-	-30
Inter-modulation (*1) (*2)	PER @ f1: 2407MHz & f2 = 2412MHz (%)	0		PER $\leq 30.8\%$
	Max Intermodulation Level @ f1: 2407MHz & f2 = 2412MHz (dBm)	-30		$\geq -50$
	PER @ f1: 2397MHz & f2 = 2392MHz (%)	0		PER $\leq 30.8\%$
	Max Intermodulation Level @ f1: 2397MHz & f2 = 2392MHz (dBm)	-30		$\geq -50$
	PER @ f1: 2445MHz & f2 = 2450MHz (%)	0		PER $\leq 30.8\%$
	Max Intermodulation Level @ f1: 2445MHz & f2 = 2450MHz (dBm)	-30		$\geq -50$
	PER @ f1: 2435MHz & f2 = 2430MHz (%)	0		PER $\leq 30.8\%$
	Max Intermodulation Level @ f1: 2437MHz & f2 = 2434MHz (dBm)	-30		$\geq -50$
	PER @ f1: 2485MHz & f2 = 2490MHz (%)	0		PER $\leq 30.8\%$
	Max Intermodulation Level @ f1: 2485MHz & f2 = 2490MHz (dBm)	-30		$\geq -50$
	PER @ f1: 2475MHz & f2 = 2470MHz (%)	0		PER $\leq 30.8\%$
	Max Intermodulation Level @ f1: 2475MHz & f2 = 2470MHz (dBm)	-30		$\geq -50$
Maximum input (dBm)		0		PER $\leq 30.8\% @ -10\text{dBm}$

(\*1)  $f_{\text{channel}} = 2f_1 - f_2$ ,  $|f_2 - f_1| = n * 1\text{ MHz}$ ,  $n = 3, 4$  or  $5$

(\*2) The value of  $n$  (for which the TC is performed) shall be declared by the manufacturer in the IXIT table (See PICS Proforma for Bluetooth low energy RF PHY).

## 11.7. Receiver BT Classic Bluetooth Low Energy (BLE) 2M IQM

**Table 43. Receiver BT Classic Bluetooth Low Energy (BLE) 2M IQM**

Parameter	Min.	Typ.	Max.	Bluetooth Specification
Sensitivity LE 2M	-94	-	-	$\leq -70\text{dBm}$ , PER $\leq 30.8\%$
C/I carrier over Interference (dB)	Co-channel	-	6	$\text{C}/\text{I}_{\text{co-channel}} (\text{dB}) \leq 21\text{dB}$
	Adjacent 2MHz	-	-5	$\text{C}/\text{I}_{2\text{MHz}} \leq 15\text{dB}$
	Adjacent 4MHz	-	-47	$\text{C}/\text{I}_{4\text{MHz}} \leq -17\text{dB}$
	Adjacent $\geq 6\text{MHz}$	-	-51	$\text{C}/\text{I}_{6\text{MHz}} \leq -27\text{dB}$
	Image interference	-	-30	$\text{C}/\text{I}_{\text{Image}} \leq -9\text{dB}$
	Adjacent (2MHz) interference to in-band mirror frequency	-	-27	$\text{C}/\text{I}_{\text{Image} \pm 2\text{MHz}} \leq -15\text{dB}$

## 11.8. Receiver BT Classic Bluetooth Low Energy (BLE) Long Range 500K IQM

**Table 44. Receiver BT Classic Bluetooth Low Energy (BLE) Long Range 500K IQM**

Parameter	Min.	Typ.	Max.	Bluetooth Specification
Sensitivity LE Long Range -500K	-100.5	-	-	$\leq -75\text{dBm}$ , PER $\leq 30.8\%$
C/I carrier over Interference (dB)	Co-channel	-	1.9	$\text{C}/\text{I}_{\text{co-channel}} (\text{dB}) \leq 17\text{dB}$
	Adjacent 1MHz	-	-8	$\text{C}/\text{I}_{1\text{MHz}} \leq 11\text{dB}$
	Adjacent 2MHz	-	-43	$\text{C}/\text{I}_{2\text{MHz}} \leq -21\text{dB}$
	Adjacent $\geq 3\text{MHz}$	-	-54	$\text{C}/\text{I}_{3\text{MHz}} \leq -31\text{dB}$
	Image interference	-	-33	$\text{C}/\text{I}_{\text{Image}} \leq -13\text{dB}$
	Adjacent (1MHz) interference to in-band mirror frequency	-	-33	$\text{C}/\text{I}_{\text{Image} \pm 1\text{MHz}} \leq -19\text{dB}$

## 11.9. Receiver BT Classic Bluetooth Low Energy (BLE) Long Range 125K IQM

**Table 45. Receiver BT Classic Bluetooth Low Energy (BLE) Long Range 125K IQM**

Parameter	Min.	Typ.	Max.	Bluetooth Specification
Sensitivity LE Long Range -125K	-106.5	-	-	$\leq -82\text{dBm}$ , PER $\leq 30.8\%$
C/I carrier over Interference (dB)	Co-channel	-	1.9	$\text{C}/\text{I}_{\text{co-channel}} (\text{dB}) \leq 12\text{dB}$
	Adjacent 1MHz	-	-16	$\text{C}/\text{I}_{1\text{MHz}} \leq 6\text{dB}$
	Adjacent 2MHz	-	-50	$\text{C}/\text{I}_{2\text{MHz}} \leq -26\text{dB}$
	Adjacent $\geq 3\text{MHz}$	-	-60	$\text{C}/\text{I}_{3\text{MHz}} \leq -36\text{dB}$
	Image interference	-	-34	$\text{C}/\text{I}_{\text{Image}} \leq -18\text{dB}$
	Adjacent (1MHz) interference to in-band mirror frequency	-	-38	$\text{C}/\text{I}_{\text{Image} \pm 1\text{MHz}} \leq -24\text{dB}$

## 11.10. Analog ADC Input

Table 466. Analog ADC Input

Parameter	Condition	Min	Typical	Max	Unit
Input impedance	Bypass mode <sup>(*)1)</sup>	-	3M	-	Ω
	Normal mode <sup>(*)2)</sup>	-	100K	-	Ω
Input voltage range	Bypass mode	0	-	1	V
	Normal mode	0	-	3	V
Number of ADC ch.	P0_0 - P0_7 <sup>(*)3)</sup>	-	-	8	ch
Offset	With FT	-	TBD	-	mV
Gain error	With FT	-	TBD	-	%
Internal ref. voltage	-	-	0.5	-	-
Resolution	-	-	12	-	bit
ENOB	-	-	10.3	-	bit

Test condition: VDDIO=3.3V

(\*1) Normal mode: with internal resistor divider

(\*2) Bypass mode: without internal resistor divider

(\*3) The ADC input counts is varied depending on part number

## 11.11. ESD Protection

The table below shows the maximum ESD capability of RTL8763BO.

The ESD protection scheme should be applied during manufacture procedure to avoid unconditional ESD damage.

Table 477. ESD Protection

Parameter	Condition	Min.	Typ.	Max.
Human Body Mode	All pins, test method: JESD22	-	±2KV (all pins)	-
Machine Mode	All pins, test method: JESD22	-	±200V (all pins except XI, XO is rated at 150V)	-
Charged Device Model	All pins, test method: JESD22	-	±400V (all pins)	-
Latch up	All pins, test method: JESD22	-	±200mA (all pins)	-

## 11.12. Power Consumption

VBAT=3.7V, One Headset Test Without Speaker Loading; RF TX= +2dBm, Test With Handset  
APPLE i-Phone7

Table 488. VBAT=3.7V, RTL8763BO One Headset Test Without Speaker Loading; RF TX= +2dBm

Test Condition	Min.	Typ.	Max.	Unit
Power off	-	TBD	-	µA
DLPS mode	-	TBD	-	µA
Standby mode	-	TBD	-	µA
Page mode	-	TBD	-	µA
Page + Inquiry mode	-	TBD	-	µA
A2DP AAC	-	TBD	-	mA
A2DP SBC High quality, bit pool=53	-	TBD	-	mA
A2DP SBC Mid quality, bit pool=35	-	TBD	-	mA
eSCO	-	TBD	-	mA

VBAT=3.7V, RTL8763BO RWS Headset Test Without Speaker Loading; RF TX= +6dBm, Test With Handset  
APPLE i-Phone7 Playing the Master Role, Master Side

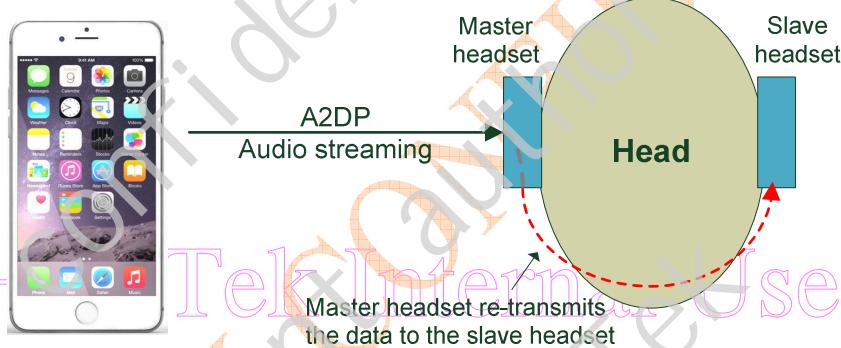
Table 49. VBAT=3.7V, PWS Headset Test Without Speaker Loading; RF TX= +6dBm, Test With Handset  
APPLE i-Phone7 Playing the Master Role, Master Side

Test Condition	Min.	Typ.	Max.	Unit
Power off	-	TBD	-	µA
DLPS mode	-	TBD	-	µA
Standby mode	-	TBD	-	µA
Page mode	-	TBD	-	µA
Page + Inquiry mode	-	TBD	-	µA
A2DP AAC	Master headset	-	TBD	-
	Slave headset	-	TBD	-
eSCO	Master headset	-	TBD	-
	Slave headset	-	TBD	-

VBAT=3.7V, RTL8763BO RWS Headset Test Without Speaker Loading; RF TX= +6dBm, Test With Handset APPLE i-Phone7 Playing the Master Role, Slave Side

**Table 50.** VBAT=3.7V, RTL8763BO RWS Headset Test Without Speaker Loading; RF TX= +6dBm, Test With Handset APPLE i-Phone7 Playing the Master Role, Slave Side

Test Condition	Min.	Typ.	Max.	Unit
Power off	-	TBD	-	µA
DLPS mode		22		µA
Standby mode	-	145	-	µA
Page mode	-	175	-	µA
Page + Inquiry mode	-	310	-	µA
A2DP SBC High quality (bit pool=53)	Master headset	-	11	-
	Slave headset	-	6.8	-
eSCO	Master headset		9.3	-
	Slave headset	-	8.3	-



**Figure 55.** VBAT=3.7V, RTL8763BO RWS Headset Test Without Speaker Loading; RF TX= +6dBm, Test With Handset APPLE i-Phone7 Playing the Master Role, Slave Side

## 12. Mechanical Dimensions

### 12.1. Package Dimensions BGA88

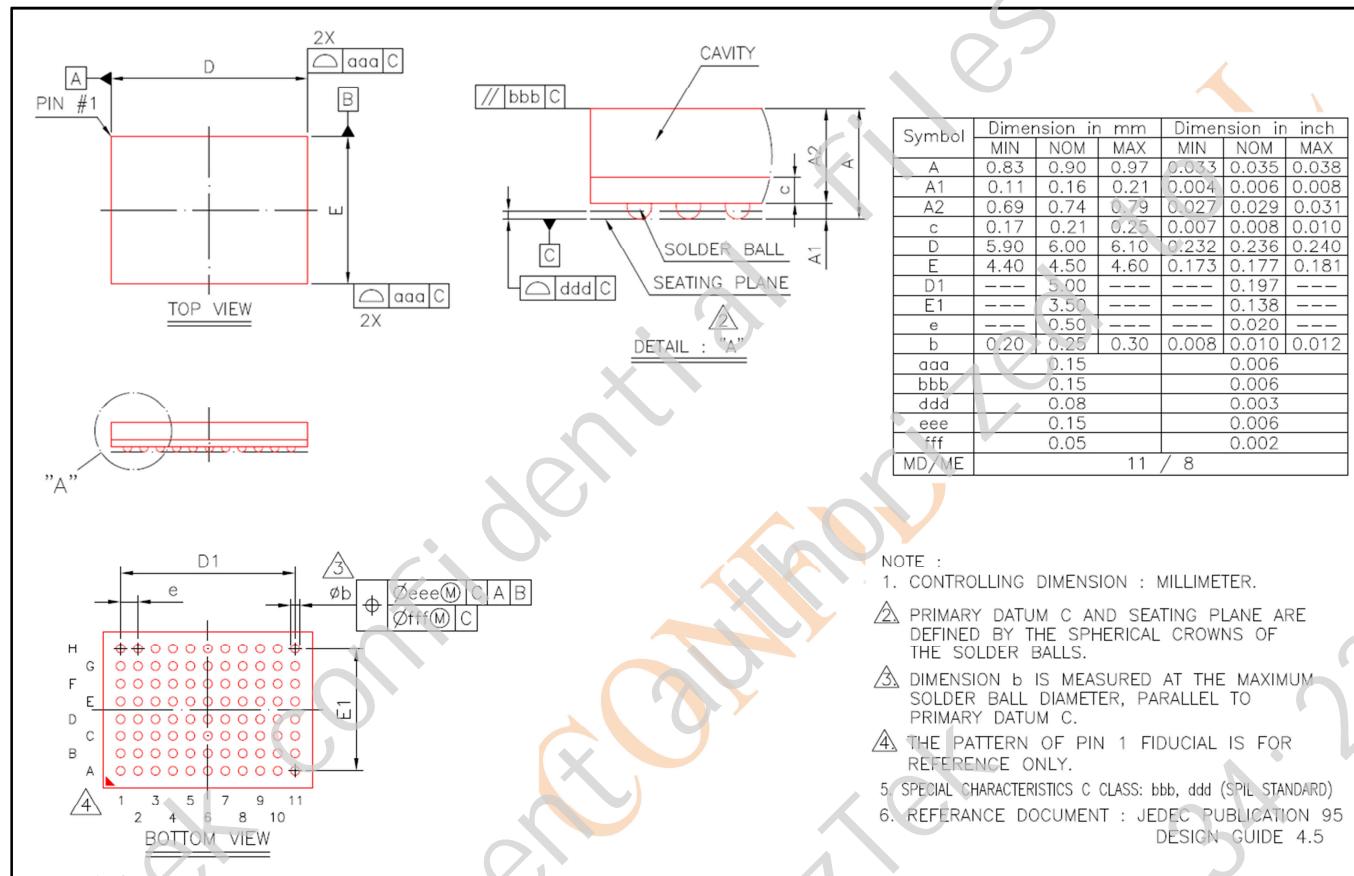


Figure 56. Package Dimensions BGA88

## 12.2. BGA88 Layout Land Pattern Stencil Open

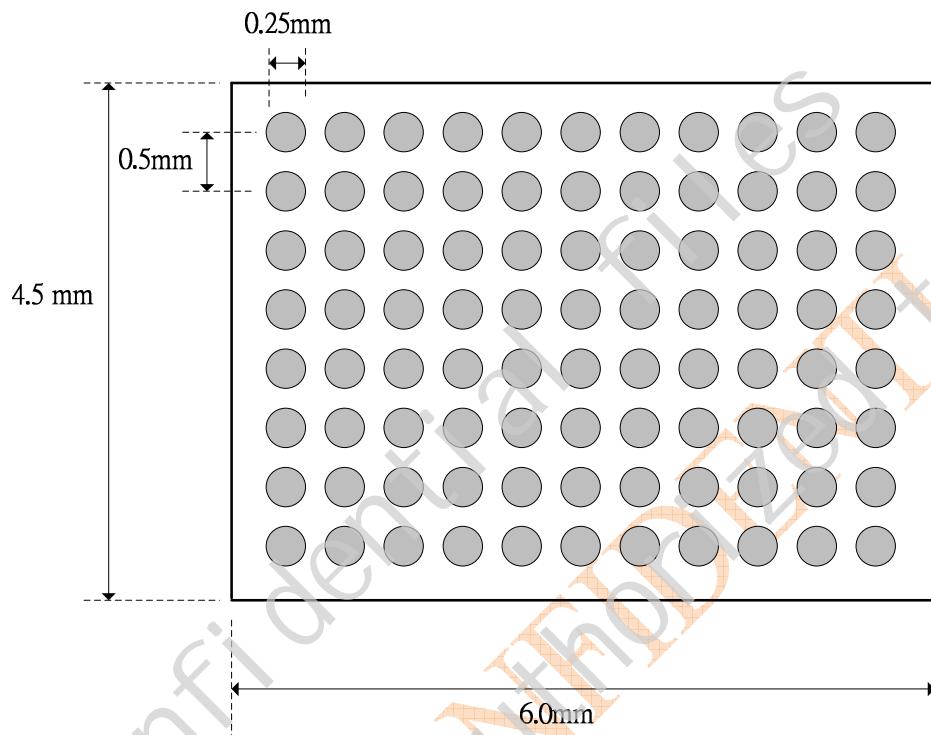


Figure 57. BGA88 Layout Land Pattern Stencil Open

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### 12.3. Suggested Stencil Open for SMT Soldering on EP Pad (Exposed Pad Under the Chip)

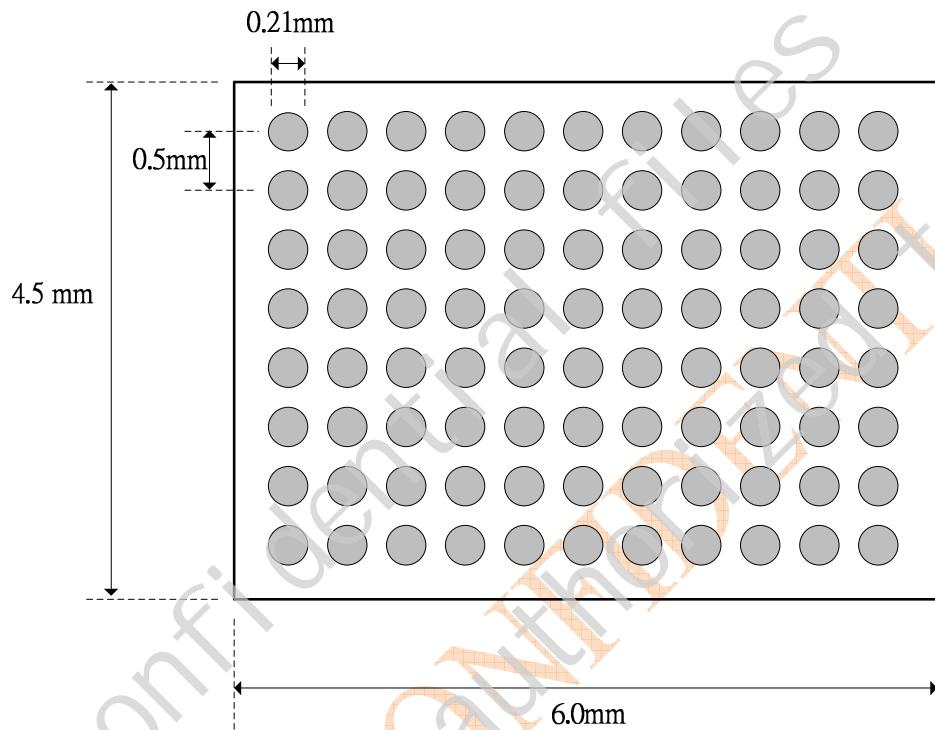


Figure 58. Suggested Stencil Open for SMT Soldering on EP Pad

For HerzTek Configuration Only

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## 12.4. Reflow Profile

Stage <sup>②</sup>	Note <sup>③</sup>	Pb-free assembly <sup>④</sup>
Average ramp-up rate <sup>⑤</sup>	T <sub>L</sub> to T <sub>p</sub> <sup>⑥</sup>	3 °C/ second max. <sup>⑦</sup>
Preheat <sup>⑧</sup>	Temperature min (T <sub>smin</sub> ) <sup>⑨</sup>	150°C <sup>⑩</sup>
	Temperature max (T <sub>smax</sub> ) <sup>⑪</sup>	200°C <sup>⑫</sup>
	Time (t <sub>smin</sub> to t <sub>smax</sub> ) <sup>⑬</sup>	60 – 120 seconds <sup>⑭</sup>
Time maintained above <sup>⑮</sup>	Temperature (T <sub>L</sub> ) <sup>⑯</sup>	217°C <sup>⑰</sup>
	Time (t <sub>L</sub> ) <sup>⑱</sup>	60 – 150 seconds <sup>⑲</sup>
Peak package body temperature (T <sub>p</sub> ) <sup>⑳</sup>		See following table. <sup>㉑</sup> T <sub>p</sub> must not exceed the specified classification temp in following table. <sup>㉒</sup>
Time (t <sub>p</sub> ) within 5°C of the specified classification temperature (T <sub>c</sub> ) <sup>㉓</sup>		30 seconds <sup>㉔</sup>
Ramp-down rate (T <sub>p</sub> to T <sub>L</sub> ) <sup>㉕</sup>		6 °C / seconds max. <sup>㉖</sup>
Time 25°C to peak temperature <sup>㉗</sup>		8 minutes max. <sup>㉘</sup>

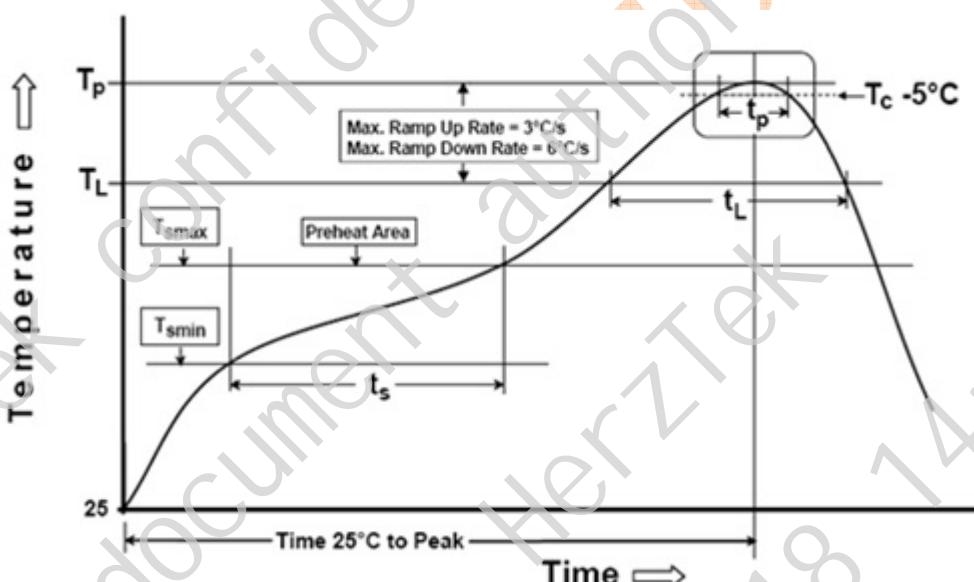


Figure 59. Reflow Profile

## 12.5. Tape and Reel Information

### 12.5.1. Tape Information

TBD

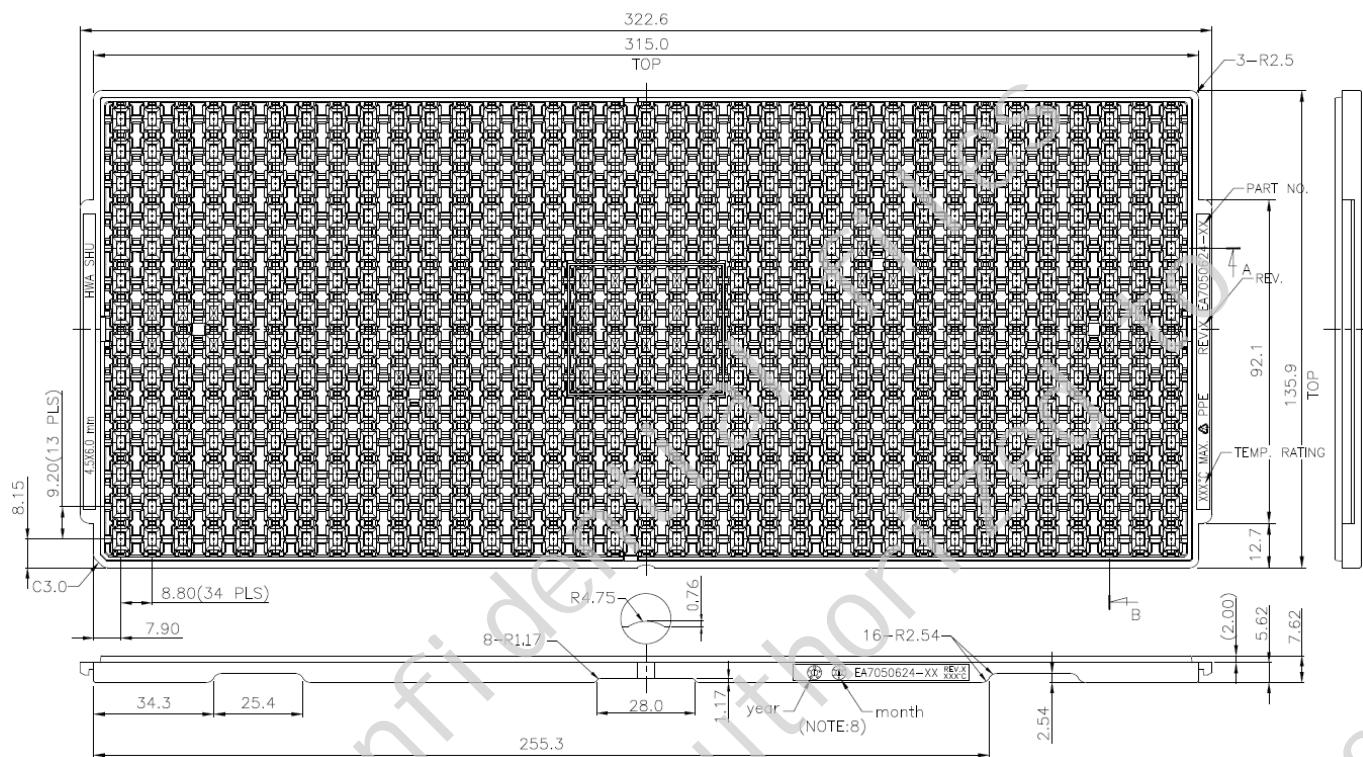
### 12.5.2. Reel Information

TBD

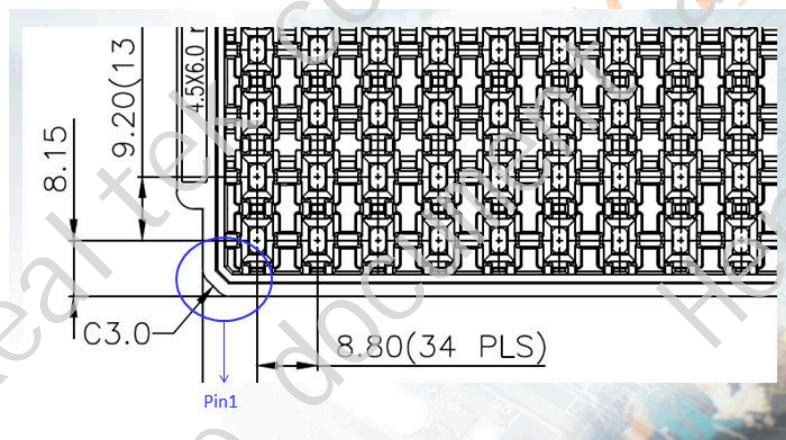
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### 12.5.3. IC Tray Information



The bevel angle of the tray indicates pin1.



### 12.5.4. Storage Conditions

	MIN.	TYP.	MAX.
Storage Temperature	-	-	30°C
Storage Humidity	-	-	60%

## 13. Ordering Information

**Table 51. Ordering Information**

Part Number	Package	Status
RTL8763BO	SF88W, 4.5mm x 6mm Outline; 'Green' Package	-

Note: See page 11 for package identification information.

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