TD 5

Register allocation and final code generation

In the following exercises we are looking for compiler independant optimisations (on the 3-address code). The goal here is to allocate registers with as few "spilled variables" as possible.

5.1 Register Allocation

EXERCISE #1 ▶ **Code production and register allocation**
Consider the expression $E = ((n * (n+1)) + (2 * n)$. We assume that we have:

- The variable n is stored in the stack slot referred as $[n]$ in the load (ld) instruction (unlike the labs, we consider that variable n is stored in memory anyway here).

1. Generate a 3 address-code with temporaries and `ld` instruction to load n. Do it as blindly as possible (no temporary recycling).
2. (Without applying liveness analysis) Draw the liveness intervals. How many registers are sufficient to compute this expression?
3. Draw the interference graph (nodes are variables, edges are liveness conflicts).
4. Color this graph using the algorithm seen in the course (unbounded number of colors).
5. Give a register allocation with $K = 2$ registers, and rewrite code.

EXERCISE #2 ▶ **Adapted from exam 2018**

We consider the following MiniC program:

```
int x,y,z,t;
x=12; y=3+x; z=4+y; t=x-y+z;
```

The 3 address code generation process of Lab 4/5 produces the following code, where $(t,z,y,x) \mapsto (temp\_0, temp\_1, temp\_2, temp\_3)$:

```
1  li temp_4, 12
   mv temp_3, temp_4
   li temp_5, 3
   add temp_6, temp_5, temp_3
   mv temp_2, temp_6
6  li temp_7, 4
   add temp_8, temp_7, temp_2
   mv temp_1, temp_8
   sub temp_9, temp_3, temp_2
   add temp_10, temp_9, temp_1
11 mv temp_0, temp_10
```

1. Fill the array with the result of the liveness analysis. Each star in a line will mean "the temporary is alive

at the entry of this line":

code	temp_1	temp_2	temp_3	temp_4	temp_5	temp_6	temp_7	temp_8	temp_9	temp_10
`li temp_4, 12`										
`mv temp_3, temp_4`										
`li temp_5, 3`										
`add temp_6, temp_5, temp_3`										
`mv temp_2, temp_6`										
`li temp_7, 4`										
`add temp_8, temp_7, temp_2`										
`mv temp_1, temp_8`										
`sub temp_9, temp_3, temp_2`										
`add temp_10, temp_9, temp_1`										
`mv temp_0, temp_10`										

2. Draw the interference graph.

   In the rest of the exercice we will use the following notations: Color 1 is red, and is associated to register t1; Color 2 is blue, and is associated to register t2. If a third color is needed, it will be associated to memory location -8(fp).

3. Color the graph with the heuristic of the course and 2 colors. Do not forget to draw the color stack.

4. What are the variable(s) to spill? Allocate this/these variable in memory without live range splitting (second algorithm of the course) and generate code for the associated instructions.

EXERCISE #3 ► **(If time allows) Register allocation, adapted from Exam, 2016**

We consider (in two columns) the following RISCV code. The tmp_i are temporaries to be allocated (in registers, in memory). For this exercise, we consider that we have two instructions that are capable to directly read/write at memory labels (`ld , sd`).

```
[...]
ld  tmp_1, label1
ld  tmp_2, label2
sub tmp_3, tmp_1, tmp_2
ld  tmp_4, label3
ld  tmp_5, label4
sub tmp_6, tmp_4, tmp_5
add tmp_7, tmp_6, 0
add tmp_8, tmp_3, tmp_7
sd  tmp_8, label5
ret
```

```
;;données/résultats (.dword = 8 bytes)
label1 : .dword 2
label2 : .dword 3
label3 : .dword -1
label4 : .dword 7
label5 : .dword 0
```

1. What is the computed expression? Where will it be stored?

2. Fill the following table with stars: put a star for a given temporary at a given line if and only if it is alive *at the entry of the instruction.* After the last store, all temporaries are supposed to be dead.

code	tmp_1	tmp_2	tmp_3	tmp_4	tmp_5	tmp_6	tmp_7	tmp_8
`ld tmp_1, label1`								
`ld tmp_2, label2`								
`sub tmp_3, tmp_1, tmp_2`								
`ld tmp_4, label3`								
`ld tmp_5, label4`								
`sub tmp_6, tmp_4, tmp_5`								
`add tmp_7, tmp_6, 0`								
`add tmp_8, tmp_3, tmp_7`								
`sd tmp_8, label5`								

3. Draw the interference graph.

4. Color the graph with the algorithm from the course with an infinite number of color (green, blue, red, black , . . . in this order).

5. (We make as it we had only 2 available registers). We decide to spill the tmp_3 register and place it in memory.

   Generate the final code with two registers (t_3, t_4), sp and fp for the stack, $s1, s2, s3$ for the spill management.