**BYOC course**

**Homework exercise #1**

**An example project**

**Part2**

1. **Homework 1 report**

Your homework assignment is made the report detailed in sections 3.1-3.3 and of a zip file of your entire project – as described in section 3.4 below.

1. **Compilation**
   1. Fill up the following table showing the compilation errors you found

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| No. | Compilation error message | filename | Line no. | What was the error | What was the fix |
| 1 | Character 'o' is not in type std\_logic | mux\_2to1.vhd | 23 | ‘o’ wrong type | ‘0’ is the correct |
| 2 | found '0' definitions of operator "=", cannot determine exact overloaded matching definition for "=" | counter\_6bits.vhd | 23 | “1” wrong | ‘1’ correct |
| 3 | Cannot read from 'out' object anodes\_out. Formal port in\_no of mode in cannot be associated with actual port anodes\_out of mode out | p4\_top.vhd | 135-136 | Location of ‘digit\_no’ and ‘anodes\_out’ | Replaced locations |
| 4 | Expression has 4 elements ; formal cntr\_out expects 5; | p4\_top.vhd | 123-124 | (4 downto 0)  And  (6 downto 5)  It’s 7 elements but have only 6 | Changed it to:  (3 downto 0)  And  (5 downto 4) |
| 5 | Choice ('0','1','1','1') is already covered | decoder\_7seg.vhd | 41 | ‘0111’ already covered | Changed in line 41 to ‘0110’ |
| 6 | We shouldn’t use the "sevenseg\_out<7>" LOC= "C17" | P4\_toplevel.ucf | 14 | NET "sevenseg\_out<7>" not found | Delete the definition of DP in line 14 |
| 7 |  |  |  |  |  |
| 8 |  |  |  |  |  |
| 9 |  |  |  |  |  |
| 10 |  |  |  |  |  |
| 11 |  |  |  |  |  |
| 12 |  |  |  |  |  |
| 13 |  |  |  |  |  |
| 14 |  |  |  |  |  |
| 15 |  |  |  |  |  |

1. **Simulation**

Use may use the Xilinx ISIM or the Modelsim student edition simulator.

After running the simulation you should:

* 1. Save the format of signals you want to monitor on the simulator screen
  2. Run the simulation and show the problem you find by printing the screen and attaching it to this doc file.
  3. Fix the problem. Explain the source of the problem, and show simulation of the corrected result.
  4. Use the following format for this:

|  |
| --- |
| Problem description: |
|  |
| Simulation picture before fixing: |
|  |
| Fix description |
| In file decoder\_2to4.vhd, line 22,  ‘1011’ is wrong  Changed it to ‘1101’. |
| Simulation picture after fix: |
|  |

If more than a single fix step was used, duplicate the above format and show the 2nd, 3rd, 4th,… fix as well.

1. **ISE compilation & testing on Nexyxs2 board**

In this stage you are required to keep the BIT files of all of your trials. Call them p4\_v1.bit, p4\_v2.bit, p4\_v3.bit etc. Read again the description of the project in section 1.a of part1 of the report and verify that your design complies with that description (if you want a good grade). Then fill up the following table showing other errors you found in this step.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| No. | Error symptom | filename | Line no. | What was the error | What was the fix |
| 1 | Forwarding of the number after pushing on the button H13 instead of B18 as required | P4\_toplevel.ucf | 21 | Incorrect button used | Definition the correct pushbutton to B18 |
| 2 | Incorrect printing of the numbers on the display | P4\_toplevel.ucf | 1, 12, 13 | Incorrect values of anodes\_out | The correct definition of the anodes\_out values |
| 3 | Number frequency is too large | cd\_divider.vhd | 32 | Incorrect value of cntr(23) that influences on the frequency | Input the right value cntr(24) |
| 4 |  |  |  |  |  |
| 5 |  |  |  |  |  |
| 6 |  |  |  |  |  |
| 7 |  |  |  |  |  |
| 8 |  |  |  |  |  |
| 9 |  |  |  |  |  |

1. **Submission instructions**

You should submit a single zip file called **HW1.zip** including this report and the Simulation and implementation projects. It should have four directories/folders. The first is called **Src**, the 2nd is called **Sim** the third is called **ISE** and the last one is called **Docs**. Those will include:

* **Src** – here you put all of the \*.vhd sources, (including the TB and the ucf files), used for simulation and implementation
* **Sim** – here you should have all of the Simulation project files created by the simulator you used (ISIM or Modelsim)
* **ISE** – here you should have all of the Implementation project files created by Xilinx ISE SW in the laqb
* **Docs** – Here you put your report. The first few lines in the report will have your ID numbers (names are optional). You should submit is in Microsoft Word file format to allow addition of remarks by the grader.

**Enjoy the homework**