Design of Integrated, Low Power, Radio Receivers in BiCMOS Technologies

by

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(ABSTRACT)

Despite increasing levels of integration in modern electronic products, radio receiver designs continue to rely on discrete LC, ceramic, and electro-acoustic devices for the realization of RF and IF bandpass filtering. Although considerable research has been directed at developing suitable switched-capacitor and Gm-C based replacements for these filters, the resulting designs have yet to see substantial commercial application.

A critical problem faced by existing active filter implementations is found to be the power consumption required to simultaneously achieve narrow fractional bandwidths and acceptable dynamic range. This power consumption, which can reach several hundred milliwatts, is incompatible with portable wireless product design. Additional problems include the complexity of tuning control circuits required to achieve small fractional bandwidths, and difficulties in extending filter designs to higher frequencies. These problems are examined in depth, and performace bounds and new implementation techniques are considered.

A detailed study of active filters reveals that their dynamic range limitations are fundamentally the result of regenerative gain associated with the realization of high-Q poles. Thus, some form of energy storage and exchange mechanism is shown to be required to decrease the regeneration needed. This leads to an investigation of on-chip LC filtering. It

is shown that on-chip spiral inductors can be designed to resonate with both intentional and parasitic capacitances, forming stable tuned circuits operating from 100 MHz to over 1 GHz. Although the Q of the inductors employed is typically small ($Q < 10$), negative resistance circuits can be used to increase the effective Q to arbitrarily high values. Hence, very small fractional bandwidths ($< 2\%$) can be obtained. Moreover, even a small inductor Q is shown to provide significant increases in dynamic range over that achievable in fully active filter designs.

Important practical considerations surrounding the implementation of Q-enhanced LC filters in silicon CMOS processes are then investigated, including realizing the necessary on-chip spiral inductors and Q-enhancement circuits, predicting frequency and Q tolerances and temperature stability, and developing real-time frequency and Q tuning mechanisms. These issues are studied in depth and two prototype filters designed to validate theoretical predictions are reported. Performance levels achieved by these prototypes indicate that Q-enhanced filtering offers a viable approach to solving the on-chip bandpass filtering problem. These filters can therefore be expected to play an important role in the development of future integrated receiver products.

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Chapter 1

Introduction

1.1 Scope

The goal of this research is to identify and address problems involved in building complete radios in integrated circuit form. To contain the scope of the effort, the research is focused primarily on *receiver* design in the *VHF to L-band spectrum*, and on *low cost, low power, silicon* IC technologies. The selected frequency spectrum encompasses a wide range of commercially important radio services including FM and television broadcast, pagers, low-earth-orbit navigation and communication satellites, portable and cellular telephones, and the rapidly evolving Personal Communications Services (PCS) industry as a whole.

1.2 Problem Overview

At the present time, various manufacturers offer a wide range of IC building blocks for receiver design, including RF amplifiers, mixers, synthesizers, and IF amplifiers/demodulators. However, completely integrated, high-performance receivers are essentially non-existent. One of the main challenges facing complete integration of receiver hardware has been a lack of suitable on-chip RF and IF filtering. Thus, a major portion of this dissertation is focused on the problem of realizing high performance, integrated bandpass filters. An additional obstacle to full integration is frequency synthesis. Although many "complete" synthesizer IC offerings can be found, a closer examination reveals that the VCO and tuned circuits for

the synthesizer are not included on-chip. This problem is also considered and is shown to be closely related to the realization of bandpass filters.

Issues surrounding receiver integration are addressed in this dissertation from both a systems and a circuits perspective. The problem faced is ultimately a circuits problem, but the degree to which any given circuit approach is successful must be assessed in the larger context of the host receiver system and its intended function and environment. This introduces an additional dimension to the research – a study of system requirements and an assessment of alternative receiver architectures. Indeed, a review of work on integrated receiver design over the past two decades shows that alternative architectures have been extensively applied. These architectures can, to some extent, reduce the need for high-performance RF bandpass filters. However, dynamic range, image rejection, and power consumption considerations make the *total* elimination of RF bandpass filtering impractical in many wireless services. This conclusion, addressed in Chapter 4, is a major reason for the emphasis on integrated RF filtering in this dissertation.

1.3 Dissertation Outline

Chapter 1 provides a statement of scope, an introduction to the problem addressed, and an outline of the structure of the dissertation.

The study of integrated receiver design begins in Chapter 2 with a survey of the state-of-the-art in both research and commercial products. Commercial integrated circuits developed over the past three decades are reviewed and cellular and PCS chip sets currently being introduced are discussed. This material is followed by a comprehensive survey of the literature illustrating the technical approaches taken and the levels of performance achieved by researchers working on integrated filters, integrated synthesizers, and fully integrated receivers. Published work by the author is included in this chapter to provide a continuity

of discussion, and to serve as a preview of more detailed discussions in subsequent chapters.

Having examined current technology and research efforts in Chapter 2, Chapter 3 turns to the issue of receiver system requirements. The purpose of this chapter is to identify the level of technical performance that integrated receiver technology must provide to be commercially viable. The subject of receiver system performance is introduced through an examination of the spectrum environment in which receivers are required to operate. Commercial wireless services which can benefit from low-power, integrated receiver technology are then identified, and system parameters that affect receiver design are summarized for each service. Finally, receiver performance measures including sensitivity, dynamic range, selectivity, and fidelity are quantified, and system level performance requirements are mapped to requirements on integrated filters.

Chapter 4 continues the investigation of system level issues by examining receiver architecture alternatives. A historical overview of receiver development is presented first, showing the origins of the superheterodyne receiver and the implicit assumptions about amplifier and filter technology on which this architecture is based. Variants of the superheterodyne architecture are then investigated in detail, with emphasis on identifying fundamental bounds and practical limits to the performance that can be achieved. Finally an "ideal" low-power receiver architecture is derived, and practical considerations regarding its viability are examined.

Throughout the study of receiver architectures in Chapter 4, the importance of high dynamic range bandpass filtering is illustrated, setting the stage for the study of these filters in subsequent chapters. Chapter 5 thus returns to the investigation of circuit level filter design issues begun in Chapter 2. The major categories of on-chip filter implementation technologies are reviewed and implementation issues are discussed. Although on-chip electro-acoustic filters are found to show some promise, their construction requires fabrication technology that is beyond the scope of this research. Hence, discussion of these filters is left primarily to

the work cited in the references. Within the remaining filter technologies, Gm-C and Q-enhanced LC designs are identified as the most viable for implementation at IF and RF frequencies.

The two main problems with these filters, dynamic range limitations and the need for real-time tuning are then studied in Chapters 6 and 7 respectively. In the discussion of dynamic range, it is demonstrated that Q-enhanced LC filters possess a significant advantage over Gm-C and other fully active filter designs operating at comparable power levels. In the discussion of filter tuning, the sensitivities of filter center frequency and Q to manufacturing tolerances and temperature effects are investigated and the need for real-time tuning is demonstrated. The major control system designs that have been proposed in the literature are then reviewed and a new "orthogonal reference tuning" technique is presented. The concept of "keep-it-simple" (KIS) tuning, wherein minimum complexity and cost are considered important goals, concludes the chapter.

Based on the advantages of Q-enhanced LC filters identified in Chapters 5 - 7, Q-enhanced filter design is selected as the technology of choice. Chapter 8 provides a detailed study of factors affecting the realization of these devices in integrated circuit form. Particular emphasis is placed on the performance of on-chip inductors on which the filters are based, and on the issues of Q enhancement, frequency and Q stability, and higher-order filter design.

Chapter 9 describes the design and performance of two prototype integrated circuits fabricated in the course of this research. These ICs were developed to demonstrate the viability of this new area of filter design, and to validate theoretical performance predictions in earlier chapters. The first IC includes a Q-enhanced, second-order filter which relies on off-chip inductors and varactor tuning diodes. This chip was designed primarily to validate dynamic range predictions and to investigate filter tuning requirements. However, coupled with an on-chip mixer, the device provides the basis for an ultra-high-Q, regenerative, VHF receiver

front-end. Dynamic range performance of this filter, which draws less than 1.5 mA and provides a gain of over 30 dB, is shown to be suitable for demanding applications such as low-earth-orbit satellite receivers. The second IC is a two pole (fourth-order) Q-enhanced filter with on-chip inductors and tuning capability. This filter, which operates at a frequency of 200 MHz and a selectivity Q of 100, is targeted at the first IF section of modern cordless and cellular phones. The filter draws less than 6 mA when operating from a 3 V supply, and consumes less than 3.3 mm^2 of IC area, making it a viable alternative to off-chip electro-acoustic filters currently used in these products.

Having demonstrated the viability of on-chip bandpass filters using Q-enhanced LC technology, Chapter 10 presents a preliminary study of a fully integrated receiver design. The remaining problem of integrating local oscillators is investigated, followed by the development and performance analysis of a receiver architecture suitable for use in future wireless products. Finally, Chapter 11 concludes the dissertation with a summary of results and a list of key research areas for further investigation.

Chapter 2

Background and Literature Review

This chapter surveys reported work in the area of integrated receiver design. The survey is organized into the following main sections:

- Commodity ICs
- Integrated bandpass filters
- Integrated synthesizers
- Integrated receivers

Throughout this chapter, published work by the author is cited together with discussions of work by previous researchers. This is done where appropriate to provide a more complete treatment, and to help introduce work covered in subsequent chapters.

The first section of this chapter presents a sampling of commercially available, integrated circuit receiver building blocks. These blocks include RF amplifiers, mixers, IF and AGC amplifiers, frequency synthesizers, and demodulators – plus devices that incorporate several of these functions in a single chip. Absent from this list are bandpass filters and local oscillator tuned circuits. A look at modern receiver designs in this section shows that these functions are currently implemented off-chip in the form of discrete LC, ceramic, crystal, or surface acoustic wave (SAW) filters and resonators.

Section 2.2 reviews the extensive body of research on integrated filter design conducted over the past three decades. Emphasis is placed on bandpass filters suitable for use in radio receivers. Performance figures of reported designs are tabulated and discussed. The important problems of power consumption, filter tuning, and dynamic range are introduced and the technologies available for implementing on-chip filters in different frequency ranges are considered.

Section 2.3 reviews research into fully integrated frequency synthesizers, with concentration on high quality oscillator designs. Here the most important problems are found to be phase noise and spurious signal levels. VCOs for phase locked loop architectures, as well as direct digital synthesis (DDS) are considered.

Finally, Section 2.4 discusses implementations of partially or fully integrated receivers. In the commercial sector, application specific integrated circuits (ASICs) have been designed for selected markets with varying levels of integration. Reported designs for broadcast receivers and pagers are reviewed. In these radio services, consumer demand is sufficiently high to justify designing for a fixed frequency band and information bandwidth. Thus, on-chip bandpass filtering becomes practical from an economic viewpoint. However, we find that for technical reasons these ASIC designs depart from the classical superheterodyne receiver architecture in order to avoid or minimize the demand for RF and IF bandpass filtering. The extensive work on integrated bandpass filtering discussed in Section 2.2 is thus seen to have found limited use in commercial impementations. The reasons and possible solutions to this technology transfer problem will be looked at in depth throughout this dissertation.

2.1 Commercial Integrated Circuits

One approach to assessing the state of the art in receiver integration is to conduct a study of commercial wireless products and the IC components from which they are built. Such a study gives an indication of what is feasible with current manufacturing technology, subject to business and market constraints. In this section, we present an overview of commercial IC devices offered at the time of this writing (1Q95), with emphasis on those ICs applicable to the design of high volume products, including radio and television broadcast receivers, pagers, portable and cellular telephones, and the evolving PCS digital wireless market.

Commercial ICs can be divided into two broad classifications:

- Commodity ICs
- Application Specific ICs (ASICs)

This section looks exclusively at commodity ICs, defined here as devices offered for sale by IC manufacturers to manufacturers of wireless products and systems. These ICs are usually intended for wide market penetration, and consequently often adopt a "building block" approach to system design. Information on these devices is widely available in data books and in trade journal advertisements and new product announcements.

In contrast to commodity ICs, ASICs are devices targeted at a single application and as such, may allow a higher level of integration. Information on ACICs is more difficult to find, but is often available in research papers. These devices will be covered in Section 2.4 where integrated receiver research is reviewed.

2.1.1 Receiver Building Blocks

A summary of commodity ICs introduced over the past three decades is presented in Table 2.1.

Beginning in the late 1960s and early 1970s, IC technology had advanced sufficiently that relatively large sections of products such as televisions could be economically integrated onto a single chip. Receiver ICs, including the MC1350 IF amp, CA3089 IF subsystem, CA3065 sound circuit, and MC1310 FM stereo demodulator represented the first steps toward reducing the part count, size, and cost of these products.

By the late 1970s and early 1980s, so-called "single-chip" broadcast receiver ICs such as the National Semiconductor LM1868 were being produced. The LM1868 provides all the active circuitry necessary for an AM receiver, plus most of the active circuits needed for an FM receiver. However, the RF amplifier, local oscillator (LO), and mixer for the FM receiver section must be implemented with off-chip discrete transistors – providing higher gain and better noise figure performance than that obtainable with on-chip devices at the time the IC was introduced. Beyond these discrete transistors and their bias circuitry, additional off-chip components required include bandpass filters, LO tank circuits, the FM demodulator phase shift network, and various coupling and bypass capacitors.

Toward the middle of the 1980s, significant new markets began to open up largely due to growth in use of personal pagers and in portable and cellular telephones. The Signetics NE/SA615 FM IF subsystem, targeted at these markets, represents a modern derivative of the earlier generation CA3089 IF subsystem. Although the RF amplifier, tuned circuits, and filters remained off-chip in this device, the NE/SA615 integrated numerous functions including a low noise mixer with capability extending to 500 MHz, a local oscillator transistor, an IF amplifier/limiter, a quadrature detector, muting, and a high dynamic range received signal strength indicator (RSSI). In addition, the operating voltage and current

Table 2.1: Building Block ICs for Radio Receivers.

Manufacturer	**Part #**	Function	Applications	Features
Motorola	MC1350	IF Amp	Television, general purpose	90 MHz bandwidth, AGC with 60 dB range, 50 dB gain at 45 MHz, 12V
RCA	CA3065	Sound Circuit	Television	4.5 MHz subcarrier IF amp/limiter, detector, audio amp, and volume control, 12V
RCA/Harris	CA3089	FM IF	FM broadcast, FM 2-way, general purpose	10.7 MHz IF amp/limiter, detector, signal level detector, audio amp, muting/squelch, AFC amp, 8.5 - 16V
Motorola	MC1310	Stereo Demod	FM Broadcast	Baseband L-R subcarrier demodulation, L/R audio matrixing, stereo indicator, 8 - 14V
Signetics	NE/SA615	FM IF	VHF/UHF receivers, cellular IF, general purpose	500 MHz downconversion mixer, local oscillator, IF amp/limiter, quadrature detector, muting, and RSSI. 500 MHz mixer RF bandwidth with 5 dB NF at 45 MHz and 18 dB gain, 25 MHz IF bandwidth with 102 dB gain, 90 dB RSSI range, 4.5 - 8V
National Semiconductor	LM1868	AM/FM Receiver	AM/FM broadcast	AM: RF/AGC amp, mixer, LO, IF amp, detector; FM: IF amp/limiter, quadrature detector, muting, meter drive; audio preamp and power amp, 3 - 15V
Motorola	MC3363	VHF FM Receiver	49 MHz portable phone, pagers, VHF radios	Dual conversion receiver including 450 MHz RF amplifier transistor, first mixer and LO with tuning diode, second mixer and LO, IF amp/limiter, quadrature detector, muting, FSK comparator, RSSI, 2 - 7V at 3.6mA excluding RF transistor
Motorola	MC4044	Phase/Frequency Detector	PLL synthesizers	Linear phase/frequency detector, lock detection, charge pump, 5V
Plessey	SP4653	Prescaler	PLL synthesizers	1.1 GHz divide-by-256, 10 mV input sensitivity, 5V
Motorola	MC44802	PLL Synthesizer	Television tuners	1.3 GHz divide-by-8 prescaler, programmable 15-bit divider, programmable reference divider, crystal reference oscillator, tristate phase/frequency detector, tuner bankswitching drivers, serial programming, 5V, 60mA
National Semiconductor	LMX1501A	PLL Synthesizer	Cellular/PCS	1.1 GHz synthesizer similar to above, but with dual-modulus prescaler, 2.7 - 5.5V, 6mA
Harris	HSP45102	DDS Synthesizer	Frequency hopped PCS	40 MHz clock, up to 20 MHz output with 0.009 Hz resolution, 5V, 99mA

consumption of the device were lower than that of the CA3089, reflecting growing market demand for smaller and lighter weight portable equipment.

One of the highest levels of integration in commodity ICs available today is represented by the Motorola MC3363 VHF FM receiver introduced around 1990. Shown in a 49 MHz portable phone application circuit in Figure 2.1, this device is similar in many respects to the NE/SA615, but adds several key components including an RF amplifier transistor, an additional mixer, a varactor tuning diode, and a data slicer (comparator) for FSK bit decisions. However, in common with all other commodity ICs, preselection/image filtering, channel select filtering, quadrature detection phase shifter, and tuned circuits for the local oscillators must still be implemented off-chip with discrete components.

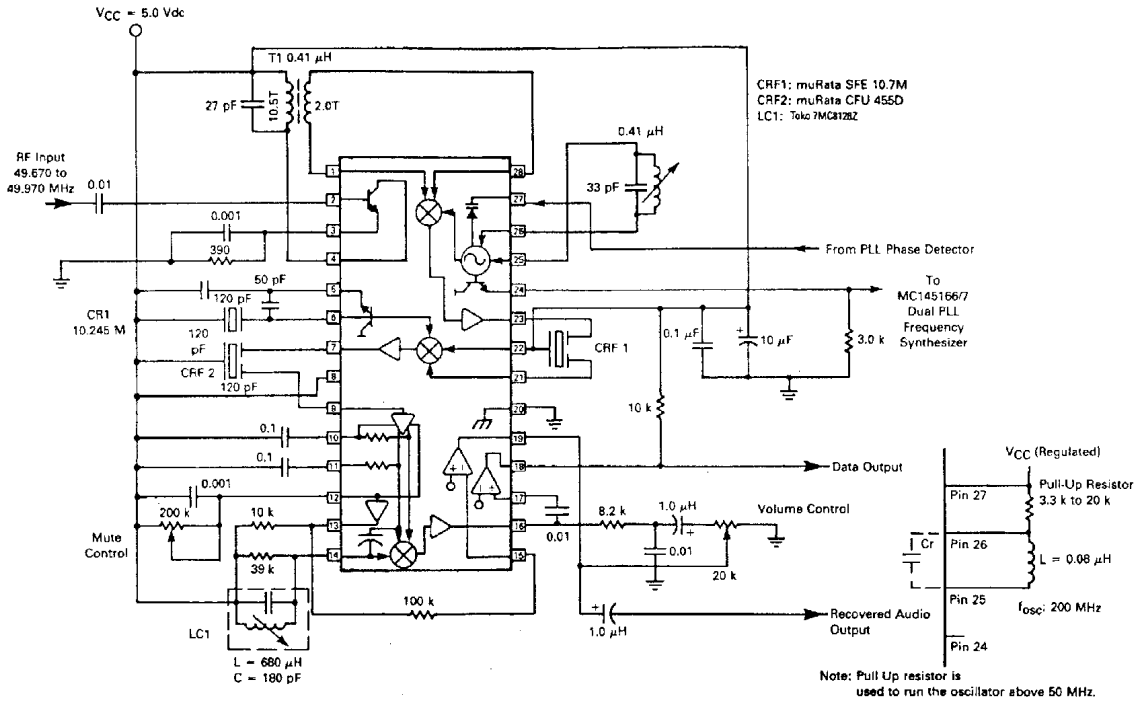

Figure 2.1: MC3363 Based 49 MHz Portable Phone. Copyright of Motorola. Used by permission.

The lower half of Table 2.1 lists several ICs used in the tuning function of radio receivers.

In early receivers, this tuning was provided by manually tuned variable capacitors, or for the case of television receivers, by mechanical switching of inductors. Today, most receivers (except very low cost AM/FM broadcast units) rely on digitally programmed frequency synthesizers. Modern tuners offer crystal controlled frequency stability, free from adjustment, plus enhanced ease of use and additional features including search/scan.

The first frequency synthesizers were constructed from a set of phase locked loop (PLL) building blocks such as the Plessey SP4653 prescaler and Motorola MC4044 phase detector, together with suitable TTL or CMOS programmable dividers. In modern receivers, these functions have been integrated into "single-chip" PLL synthesizer ICs such as the Motorola MC44802 for television tuners and the National Semiconductor LMX1501A for cellular radios. These devices offer most functions needed for designing a digitally tuned LO controlled by keyboard entry or a receiver's microprocessor. However, like the receiver ICs discussed previously, the tuned circuits required for the PLL's VCO remain off-chip.

An interesting alternative to PLL synthesizers is offered by the relatively new direct digital synthesis (DDS) ICs. An example device is listed at the end of Table 2.1. DDS devices do not require tuned circuits (except for a crystal reference) and would therefore appear to bypass the need for on-chip VCOs in integrated receivers. Unfortunately however, the output frequencies of DDS devices are comparatively low and must be multiplied or mixed up to VHF through L-band for use as a receiver's first LO, usually involving the use of auxiliary PLL synthesizers and tuned circuits. In addition, current devices are relatively expensive ($20 or more) and consume substantial power (e.g. > 100 mW).

2.1.2 Cellular Telephone Design Example

Modern hand-held cellular telephones represent one of the most sophisticated and challenging areas of wireless circuit design today. Hence, it is worthwhile studying the architecture and level of integration currently being achieved in these products. This section overviews

the design of a 1991 vintage cellular phone marketed by the Radio Shack^{TM} division of the Tandy Corporation in the United States.[1] The phone operates in the North American Advanced Mobile Phone System (AMPS) service at 800 MHz, providing synthesized tuning of 832, 30 kHz wide channels. Frequency division duplex is employed with a 45 MHz split between transmit and receive subbands. Voice modulation is analog FM with ± 12 kHz deviation, and control data are sent using 20 k baud Manchester encoded FSK. The phone is approximately 7 x 2.2 x 1.4 inches in size and sold for around $430 (without service activation) in 1994. It contains two PC boards, each measuring 6.8 x 2 inches. One board performs the analog RF/IF functions, while the other provides microprocessor control, user interface, and baseband audio processing. The phone is powered by six NiCad batteries delivering a nominal voltage of 7.2V and a current capacity of 700 mAh. Performance specifications for this phone are summarized in Table 2.2 [34], and a block diagram of the RF/IF board is shown in Figure 2.2.

The RF/IF PC board connects the phone's antenna to a duplexer formed by two ceramic bandpass filters, one centered on the receive subband and one on the transmit subband. Following the duplexer, receive signals are amplified by a discrete transistor LNA and fed through a second ceramic filter to achieve the required image frequency rejection levels. The first down conversion is provided by a double balanced passive mixer, converting the received signal to a 45 MHz IF where it is then amplified by a second discrete transistor LNA and filtered by a 4-pole (8th order) ladder filter composed of two cascaded monolithic crystal filters (MCFs). This filter narrows the receive bandwidth sufficiently to enable the second IF to be implemented at a comparatively low 455 kHz. A Signetics SA615 is employed to provide the second down conversion mixer, 455 kHz IF amplification, limiting, quadrature detection, and signal strength monitoring. An off-chip 44.45 MHz crystal provides the local oscillator tank circuit and an off-chip 455 kHz ceramic BPF is used for final channel selection. Baseband audio is delivered to the adjacent PC board for FSK data decisions

[1] Radio Shack is a registered trademark of the Tandy Corporation.

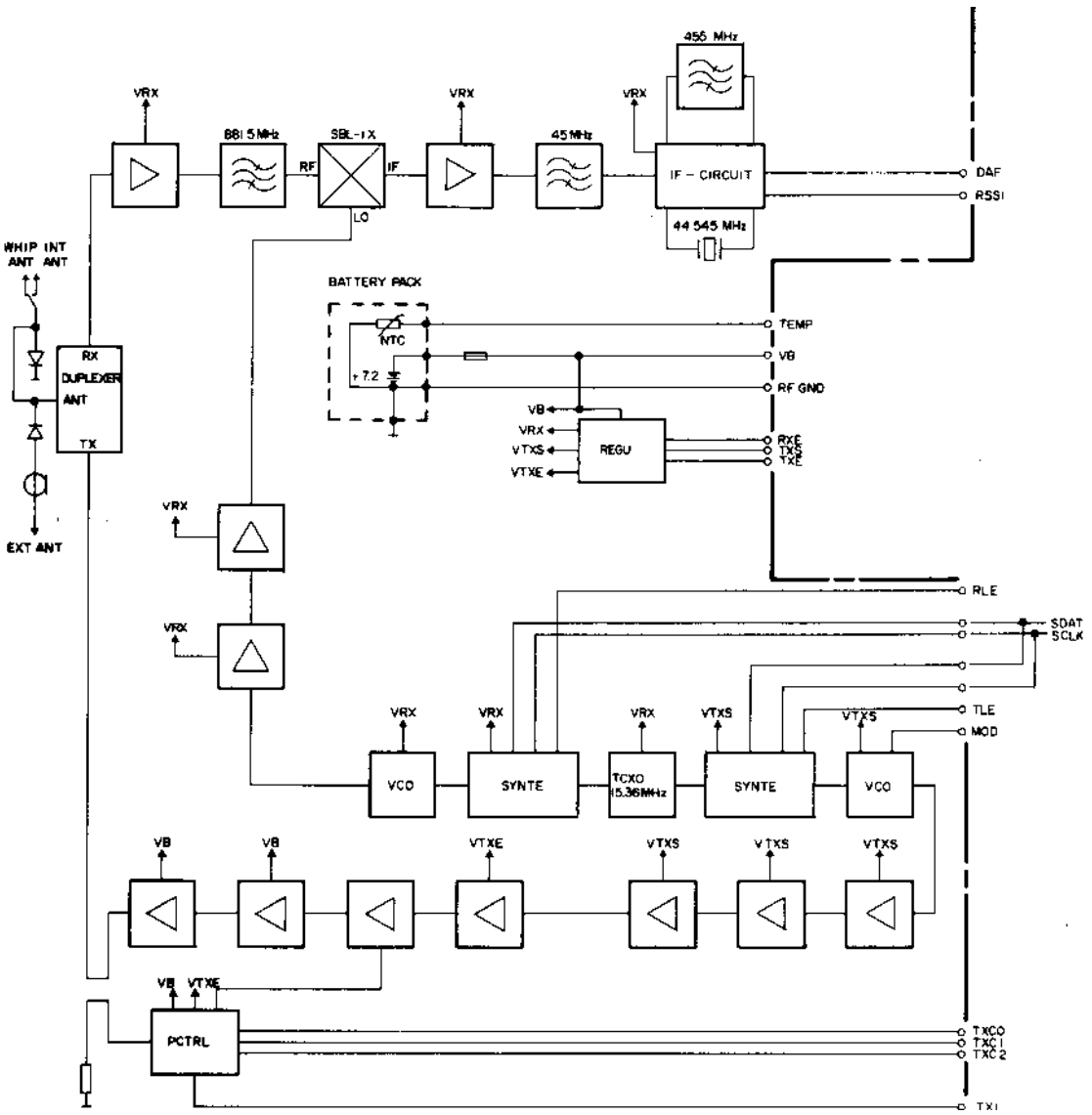

Figure 2.2: Cellular Phone Block Diagram. Copyright 1991 Tandy Corporation. Reprinted by written permission, from [34].

Table 2.2: Specifications for 1991 Cellular Phone.

Parameter	Value
Batteries	7.2 V nominal @ 700 mAh
Minimum Voltage	6.5 V
Current Consumption Receive Transmit	 50 mA (360 mW) 550 mA (4 W)
Temperature	-30^o to + 65^o C
Number of Channels	832
Frequency Stability	$\pm$ 2.5 ppm
FM Deviation	$\pm$ 12 kHz
Sensitivity	-116 dBm (12 dB SINAD)
RSSI Dynamic Range	$>$ 60 dB
Selectivity Adjacent channel Alternate channel	 $>$ 16 dB $>$ 65 dB
Image Rejection	$>$ 60 dB
Receiver Intermodulation	$<$ -26 dB

and voice band filtering and amplification.

Tuning is performed on the RF/IF board using two MB1502 synthesizer ICs (one for the transmit frequency and one for the receive frequency), with discrete component loop filters, VCOs, and buffer amplifiers. The FM transmit signal is formed by phase modulating the transmitter synthesizer VCO, and then amplifying the signal with a series of seven discrete transistors. The final two transistors operate in class C and harmonic suppression is provided by microstrip impedance matching networks and by the transmit portion of the antenna duplexer.

In all, the RF/IF circuit board contains 4 ICs and 344 discrete components - representing a relatively low level of integration. Thus, the phone's small size is due primarily to the use of fine geometry PC board construction (10 mil traces), and of low profile surface mount components.

2.1.3 Cellular/PCS Front End, Power Amplifier, and Transverter ICs

In the years since the cellular phone in the previous section was designed, several new ICs have become available, enabling further size and weight reductions in newer products. These ICs, summarized in Table 2.3, provide integrated solutions to the design of receiver front ends (LNAs and mixers), transmitter power amplifiers and, in the case of newer time division duplex (TDD) services such as DECT, transmit/receive (T/R) switching.

The products listed in Table 2.3 span both the existing cellular phone frequencies and the newly allocated spectra from 900 MHz to 2.4 GHz. Several products, such as the NEC UPC2757T downconverter and Siemens CMY90 front end ICs offer broadband operation across this full spectrum, but at the cost of requiring external matching networks. Most newer products are targeted at particular spectrum segments (e.g 900 MHz, 1.8 GHz, or 2.4 GHz) and provide on-chip 50 Ohm impedance matching for reduced external part count.

Table 2.3: Cellular/PCS Front Ends and Transverters.

Manufacturer	Part #	Function	Technology	Features
NEC	UPC2757T	Downconverter	Silicon	0.1 - 2 GHz mixer with 10 - 300 MHz IF, local oscillator, IF amp, 13 dB gain, 3V, 5.6mA
Siemens	CMY90	Front End	GaAs	0.4 - 3 GHz LNA, mixer, IF amp, 4.5 dB NF with 15 dB gain at 900 MHz, 3V, 2.5mA
Triquint	TQ9203J	Front End	GaAs	0.8 - 1 GHz, 2 LNAs with switch for antenna diversity, mixer with 45 - 200 MHz IF, 2.7 dB NF with 20 dB gain, -10 dBm IIP3, 5V, 10.5mA
Motorola	Ref: [44]	Front End	GaAs	0.7 - 0.9 GHz, RF amp, mixer, IF amp, 50 Ohm matching at RF, LO ports, 3.6V, 2.7mA
Philips	SA620	Front End	Silicon	1.2 GHz, LNA, mixer, VCO, gain switching, 14.5/-4.5 dB gain with -18/+1.5 dBm IIP3, 50 Ohm RF port, 2.7 - 5.5V, 10mA
Motorola	MRFIC2401	Front End	GaAs	2.0 - 2.8 GHz, LNA, mixer, 3dB NF with 21 dB gain, -15 dBm IIP3, 50 Ohm RF/LO ports, 5V, 10mA
AT&T	Ref: [41]	Transverter	GaAs	2.4 GHz RF to 915 MHz IF half-duplex conversion, T/R switch, LNA, mixer, and LPF in receive path; mixer, amp with power control/detect, harmonic suppression filtering, T/R switch in transmit path; shared VCO with on-chip tank circuit – excluding varcap; 0.25W output; $\pm$ 5V

Impedance matching is provided by on-chip LC networks incorporating spiral inductors. A typical example described in [46], employs an L-type network to convert 600 Ohms to 50 Ohms with a loaded Q of 1.7. This low-Q circuit provides good matching across the desired band, but introduces a bandpass response restricting the IC to the targeted spectrum segment (the 900 MHz ISM band in the case of this IC). On the plus side, the bandpass response can be helpful in reducing transmitter harmonic and spurious outputs, and in receivers it provides attenuation to out-of-band signals. However the Q is not sufficient in any of the devices to serve as preselection/image filters and off-chip filters are still required. This fact is clearly illustrated in the next section when modern "chip sets" for cellular and PCS wireless products are reviewed.

2.1.4 Cellular/PCS Chip Sets

The state of the art in cellular and PCS RF integration is illustrated by chip set offerings currently being introduced. These chip sets are targeted at emerging digital wireless markets such as Digital European Cordless Telecommunications (DECT), Groupe Special Mobile (GSM) and its 1.8 GHz derivative (DCS1800), North American Digital Cellular (NADC) IS-54, and Code Division Multiple Access (CDMA) systems such as IS-95. Table 2.4 summarizes ICs targeted at the analog portion (both transmitter and receiver) of products in these markets, while Table 2.5 summarizes some of the baseband processing chips becoming available.

The National Semiconductor DECT chip set illustrated in Figure 2.3 is representative of the level of integration being achieved [28]. The chip set includes the LMX2215/16 receiver LNA and downconversion mixer, the LMX2240 IF amplifier/limiter/detector/RSSI, the LMX2410 baseband data processor, and the LMX2320 synthesizer IC and is expected to sell for under $30 in quantity.

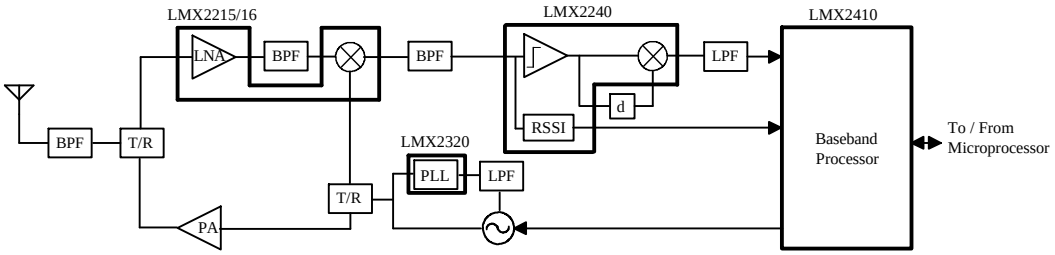

Figure 2.3: National Semiconductor DECT Chip Set. After Eccles [28].

An alternative chip set targeted at DECT but not yet commercially available is shown in Figure 2.4 [39]. This chip set, developed by Hewlett Packard and MOSAIC Microsystems adopts a different tranceiver architecture and partitioning of functions, but represents a similar level of integration. Although the T/R switch, LNA, and PA are not part of the set, these functions are available from other manufacturers as seen in the previous section.

Table 2.4: Cellular/PCS RF Chip Sets.

Manufacturer	Application	Technology	Partitioning
Philips	FM Cellular	Silicon	SA620 – Front end (LNA, mixer, VCO) SA615 – IF (mixer, amp/limiter, detector, RSSI) SA7025DK – Synthesizer (prescaler, dividers, phase detector)
National Semiconductor	DECT	Silicon	LMX2215/16 – Front end (LNA, mixer) LMX2240 – IF (amp/limiter, detector, RSSI) LMX2320 – Synthesizer (prescaler, dividers, phase detector) LMX2410 – Baseband processor (demod comparator with threshold D/A, RSSI A/D, digital FIR gaussian filter and D/A for transmit data)
HP & MOSAIC Microsystems	DECT	Silicon	Transverter (T/R mixers, VCO, frequency doubler, prescaler) IF (LO, mixer, IF amp/limiter, detector, RSSI, data detector)
Philips	GSM/DCS1800	Silicon	SA1620 – Transverter (LNAs and mixer with 60 dB gain control in receive path; IF level control, SSB mixer, and PA driver in transmit path) SA1638 – IF (I/Q mixers for transmit and receive, fixed frequency synthesizer with quadrature LO output) UMA1019 – Synthesizer (prescaler, dividers, phase detector)
RF Micro Devices	CDMA/FM Cellular	GaAs	RF9906 – Front End (LNA, mixer, IF amp) RF9907 – Receive IF (IF amp with 90 dB AGC range) RF9909 – Transmit IF (IF amp with 84 dB gain adjust) RF9908 – Up Converter (Mixer, buffer amps)
Qualcomm		Silicon	BBE – Mod/demod (Fixed frequency synthesizer with VCO, mixers for I/Q modulation/demodulation, D/As and A/Ds)

Table 2.5: Cellular/PCS Baseband Chip Sets.

Manufacturer	Application	Partitioning
Philips	GSM/DCS1800	PCD5072 – ADCs for I/Q detection, DSP, audio D/A and amp for receive; DSP, GMSK modulator, I/Q A/Ds for transmit; AGC and AFC D/As PCF5083 – Speech coding/decoding, channel coding/decoding, encryption/decryption, burst buffering, TDMA timing
Qualcomm	CDMA/FM Cellular	MSM2 – CDMA and FM demods, viterbi decoder, voice coding, data interleaving/deinterleaving — – Audio A/D and D/As
Texas Instruments	NADC (IS-54)	TCM4300 – Data demodulation, timing, and power management TMS320IS54B – Voice and channel coding/decoding TVL320AC3X – Audio A/D and D/As and amplifiers

In addition, the CMOS synthesizer shown in Figure 2.4 is readily available elsewhere.

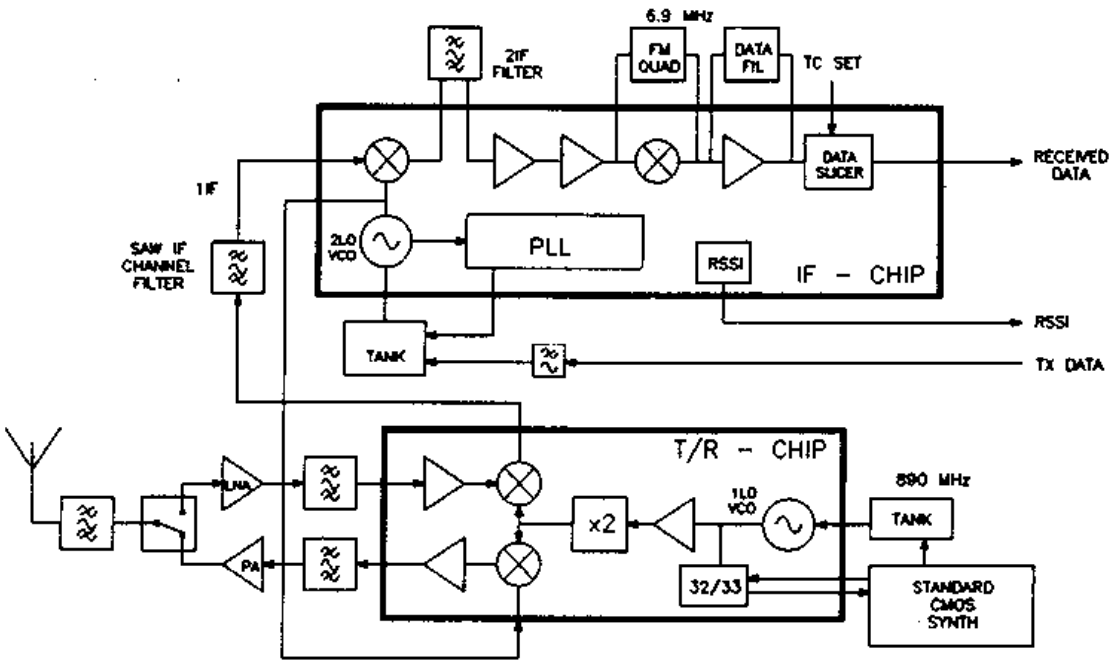

Figure 2.4: HP and MOSAIC Microsystems DECT Chip Set. Copyright 1993 IEEE. Reprinted with permission, from [39].

From these examples, we note that the following functions must still be implemented off-chip to form a complete tranceiver product:

- Bandpass filters for RF preselection/image filtering
- Bandpass filters for channel selection at first and second IFs
- Tank circuits for first and second LOs
- Quadrature detection phase shift network
- Lowpass data filters

Examination of chip sets for other cellular and PCS markets listed in Table 2.4 and of

associated tranceiver designs [25] [38] [31], yields the same conclusions – as of 1995, virtually all analog portions of a tranceiver are available in a small number of ICs, with the exception of high frequency filters and tank circuits.

2.1.5 Discussion

Given current market pressures to reduce the size and cost of wireless products, it is reasonable to ask why these key components have so far not been integrated with the remainder of the receiver functions. For wireless commodity ICs, the reasons may be either economically or technically based.

From an economic viewpoint, including filters and tuned circuits on-chip can have a negative effect on the breadth of the market that a commodity IC can penetrate. For example, if a front-end chip targeted at the cellular market is restricted to the US band of 869 - 894 MHz by an on-chip preselection/image filter, that chip becomes unsuitable for use in other markets such as Europe where GSM cellular is implemented at 935 - 960 MHz. The commodity IC manufacturer is then forced to weigh the costs associated with producing multiple versions of the chip against the benefits of higher integration – smaller end product size, plus capture of a portion of the filter vendor's market.

However, for other cases, such as IF filters in broadcast receivers, where the operating frequency and bandwidth are standardized, we would expect integration to be fully warranted from an IC manufacturer's perspective. Yet, broadcast receiver commodity ICs still rely on off-chip ceramic IF filters purchased from separate vendors. In this case it appears clear that technical reasons must be at least partly involved. These technical considerations are investigated in the following sections where research into on-chip bandpass filters and oscillators is reviewed.

2.2 Integrated Bandpass Filter Research

Research into bandpass filters for radio applications dates to the very beginning of electrical engineering. Research on *integrated* RF bandpass filters however, is comparatively recent, with work beginning around the 1960's [59] [79]. In this section we attempt to organize this area of research into a coherent picture and to assess why these filters have so far seen little or no commercial applications. We begin with a look at the competition – off-chip ceramic, crystal, SAW, and LC filters. Following this, we look at on-chip filtering alternatives including:

- Digital filters,
- Analog passive filters (including electro-acoustic and LC types),
- Analog active filters (including switched-capacitor, and Gm-C), and
- Q-enhanced LC filters.

The important topics of filter tuning and dynamic range are also considered.

2.2.1 Filter Performance Benchmarks

In order for an integrated bandpass filter to see commercial application, it must be both technically and economically competitive with the discrete filters which it is to replace. Table 2.6 lists performance data for some discrete ceramic, crystal, SAW, and LC filters available today. These filters span the range of IF and RF frequencies from 262 kHz to 914 MHz. All of the filters listed except three (the 881 and 914 MHz filters) are intended for use as channel select filters at standardized IF frequencies. The 881 and 914 MHz filters are RF preselect/image filters intended for use at the front end of cellular and cordless phones.

Table 2.6: Discrete Filter Performance Benchmarks.

Part #	Type	Application	Freq	Bandwidth	Shape Factor	IL	Price
TOKO HCFM8-262B	Ceramic	AM Broadcast IF	262 kHz	6 kHz (2.3%)	-16 dB @ ± 9 kHz	6 dB	$1
TOKO CFMR-455B	Ceramic	AM Broadcast IF	455 kHz	6 kHz (1.3%)	-16 dB @ ± 9 kHz	6 dB	$1
MuRata SFP450F	Ceramic	Pager IF	450 kHz	6 kHz (1.3%)	-40 dB @ ± 12.5 kHz	6 dB	–
MuRata SFE4.5MBF	Ceramic	Television Sound IF	4.5 MHz	120 kHz (2.7%)	-20 dB @ ± 270 kHz	6 dB	–
MuRata SFE10.7MS2-Z	Ceramic	FM Broadcast IF	10.7 MHz	230 kHz (2.1%)	-20 dB @ ± 290 kHz	6 dB	$0.30
ECS ECS-10.7-15B	MCF	Cellular Phone IF	10.7 MHz	25 kHz (0.2%)	-40 dB @ ± 25 kHz	2.5 dB	$3
Siemens B4535	SAW	DECT IF	110 MHz	1.1 MHz (1%)	-20 dB @ ± 1.5 MHz	–	$3
MuRata LFC30-01B0881B025	LC	Cellular RF	881 MHz	25 MHz (2.8%)	-20 dB @ ± 78 MHz	3.5 dB	–
Toko 6DFA-881E-11	Dielectric	Cellular RF	881 MHz	25 MHz (2.8%)	-20 dB @ ± 78 MHz	1.8 dB	–
Toko 6DFA-914A-14	Dielectric	Cordless Phone RF	914 MHz	1 MHz (0.1%)	-24 dB @ ± 45 MHz	2.2 dB	–

Some general conclusions that can be drawn from this table include:

- Fractional bandwidths are small (1% to 3%, with 0.1% possible),
- Shape factors are moderate (16 to 20 dB attenuation at 2 to 3 times the nominal bandwidth), but can be higher for cascaded designs such as the SFP450F,
- Insertion loss is moderate (1.5 to 6 dB)
- Cost is low ($0.30 to $3) when purchased in high quantities

The small fractional bandwidth of these filters minimizes the number of IFs required in a receiver, which helps to minimize overall receiver cost. The moderate shape factors provide acceptable selectivity for some applications, although two of these filters will frequently be used in cascade to achieve a better alternate channel selectivity. (Note however that *adjacent* channel selectivity may still be relatively low as seen in the specifications for the

cellular phone in Table 2.2.) The relatively low insertion loss of these filters minimizes the amount of RF/IF amplification required preceding the filter, thereby improving the receiver's noise figure and intermodulation dynamic range. Finally, the cost of the filters helps to explain their nearly universal use in consumer products. This cost also hints at one reason integrated filters have not yet replaced these discrete devices. At $1 per filter, only a very small fraction of chip area can be used by an on-chip filter if it is to be cost competitive.

2.3 On-Chip Filter Alternatives

A wide range of technologies exists through which filters may conceivably be implemented on-chip. These technologies, ranging from digital signal processors (DSP) to active analog designs and electro-acoustic implementations, are summarized in Figure 2.5 and examined in the following sections.

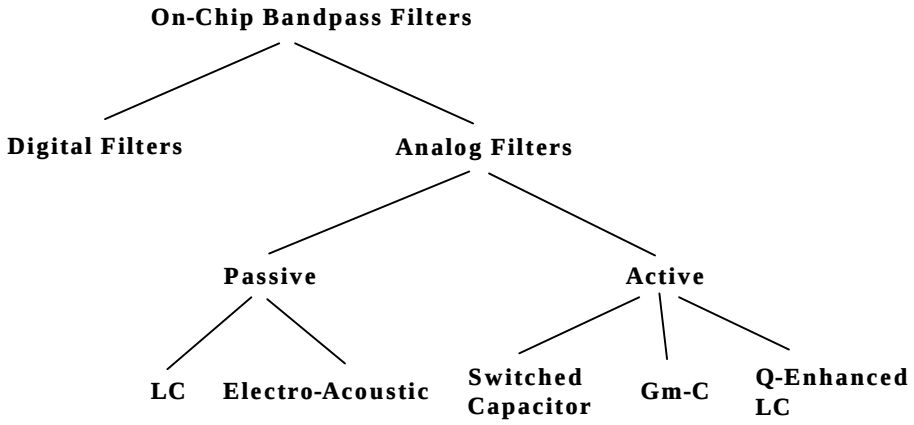

Figure 2.5: On-Chip Bandpass Filter Alternatives.

2.3.1 Digital Filters

In theory, DSP could be used to implement any of the filters shown in Table 2.6. In practice, however, current technology rules out this possibility for all but perhaps the lowest frequency (< 1 MHz) devices. Practical problems with the DSP filtering approach include:

- the need for analog anti-aliasing filters,
- chip area requirements,
- electromagnetic compatibility with low level analog signals,
- requirements for a high resolution, high speed analog to digital converter (ADC), and
- power consumption at high frequencies.

If we neglect all of these problems except the last, we still find that the DSP solution is generally unsuitable for all but the lowest frequency applications. For integrated receiver designs within the scope of this dissertation, low power consumption is a requirement. Based on data in Tables 2.1, 2.3, and 2.4, we conclude that any solution drawing more than a few milliamps will not be greeted favorably by designers of portable equipment.

In a DSP solution, the two major power consumers will be the ADC and the DSP computational circuitry, both of which increase consumption with frequency of operation. Vittoz [182] has developed bounds on the power consumption of DSP circuitry (excluding the ADC) for lowpass filters as a function of dynamic range requirements. For a 1 um, 3V digital process and 60 - 80 dB dynamic range (corresponding to 10 - 13 bit resolution), he computes a power consumption on the order of 1 nJ per pole, per Hz of corner frequency. To apply these results to bandpass filters, we must use the center frequency of the filter. As an example, a 10 MHz, fourth-order IF filter requires $(1nJ/pole)(4poles)(10^7Hz) = 40$ mW. In a 3 V process, this corresponds to 13 mA. Cascading two such filters for improved

alternate channel rejection raises the figure to 26 mA at 10 MHz. Hence, even without considering power consumption of the ADC, the need for an anti-alias filter, electromagnetic compatibility with small signals, or chip area requirements, the DSP solution is not suitable at frequencies of 10 MHz and above.

While it can be argued that power consumption will decrease for DSP circuits as smaller geometries become available, these improvements will be gradual and will not change the general conclusions reached here in the near future [182]. Therefore, in the remainder of this dissertation we will exclude digital solutions and look exclusively at the remaining analog circuit options in Figure 2.5.

2.3.2 Analog Passive Filters

Within certain constraints, it is possible to implement completely passive on-chip filters. As shown in Figure 2.5, the two basic technologies are the same as those used to realize the most popular off-chip filter types – LC filters and electroacoustic filters. Both types have been realized in silicon IC processes [167] [60] [131], although with performance well below that currently possible off-chip.

Passive LC Filters

On-chip capacitors can be fabricated in one or more forms in all IC processes. On-chip inductors can also be fabricated through the use of planar spiral geometries formed in one or more of the process' metal layers. Such inductors are employed routinely in the design of GaAs monolithic microwave integrated circuits (MMICs) operating at several GHz. More recently, spiral inductors have begun to see commercial application in silicon processes at lower frequencies, where they are employed in on-chip impedance matching networks [46]. Their use in filter design at frequecies below 2 GHz has been investigated by Nguyen and

Meyer [131] for lowpass filters, and by Chang, Abidi, and Gaitan [122] for bandpass filters. Negus, et. al. [46] has also reported their use in silicon for both bandpass filtering and impedance matching functions.

A significant problem with all on-chip LC filters realized to date is low Q, as illustrated in Table 2.7.[2] In silicon processes operating at 2 GHz and below, the quality factor of on-chip spiral inductors is generally 10 or less [131] [77], while in-circuit Q can be significantly lower. For matching networks or lowpass filter design, these quality factors are often acceptable – provided the impedance ratio or filter order is sufficiently low. However, for bandpass filters intended for use in superheterodyne receivers, they are far too low to achieve the desired fractional bandwidths. An in-circuit Q of 5 implies a bandwidth of 20% – nearly an order of magnitude away from than that offered by the discrete filters seen previously in Table 2.6.

Table 2.7: On-Chip Spiral Inductors in Silicon Processes.

Ref	Inductance	Resonance	In-circuit Q	Turns	Dimension
[131]	1.9 nH	9.7 GHz	8 @ 4.1 GHz	4	115 um
[131]	9.7 nH	2.5 GHz	3 @ 900 MHz	9	230 um
[122]	100 nH	800 MHz	1.3 @ 400 MHz	20	440 um
[122]	100 nH	3 GHz*	3 @ 800 MHz*	20	440 um

Reasons for low spiral inductor quality factors are discussed in Chapter 8 together with possibilities for process modifications that could be used to provide some improvements. However, improvements sufficient to realize narrow bandwidth passive LC filters are unlikely because of the substantial process modifications needed. Realization of on-chip, high-Q, LC bandpass filters therefore requires the addition of active circuitry to compensate for coil losses [57]. These techniques are considered in Section 2.3.3 below and in Chapters 5 - 9 later in this dissertation.

[2]The performance of inductors marked with an asterisk (*) has been enhanced by removal of the underlying substrate using a post-fabrication etch.

Passive Electro-Acoustic Filters

A handfull of researchers have investigated the possibility of implementing electro-acoustic filters on-chip as shown in Table 2.8 [60] [167] [158] [163] [165]. Such filters have been integrated with active circuitry in silicon IC processes, but require process additions/modifications. To date, these filters have also required relatively large chip areas. Both of these factors are likely to limit their ability to compete with low cost off-chip designs. Nevertheless, their performance is reasonably good and they offer the advantage of being completely passive – consuming no power and yielding excellent dynamic range. These performance features may allow them to compete in some applications in the future, if and when their fabrication reaches a suitable level of maturity.

Table 2.8: On-Chip Electro-Acoustic RF Bandpass Filters.

Ref	Year	Type	Freq	Bandwidth	IL	Size
[163]	1990	BAW	1.1 GHz	30 MHz (3%)	1.1 dB	58 mm^2
[159]	1992	BAW	1.8 GHz	180 MHz (10%)	3.6 dB	–
[165]	1989	SAW	283 MHz	18.7 MHz (6.6%)	–	≈10 mm^2
[165]	1989	SAW	283 MHz	500 kHz (0.18%)	–	≈10 mm^2
[167]	1989	SAW	160 MHz	180 kHz (0.1%)	–	10 mm^2

Like their discrete counterparts, on-chip electro-acoustic filters can be divided into two major subcategories:

- Bulk acoustic wave, and
- Surface acoustic wave devices.

Bulk acoustic wave (BAW) devices are usually referred to in the literature as either thin film resonators (TFRs) or film bulk acoustic resonators (FBARs) to emphasize their construction and crystal resonator-like behavior. In [163], a FBAR filter operating at 1.1 GHz

is described. This filter was constructed in four layers consisting of a sputtered SiO2 base for support and temperature compensation, followed by a 0.25 um layer of oriented gold onto which a piezoelectric layer of ZnO was sputtered. The final layer consisted of evaporated aluminum, with a 0.2 to 0.5 um thickness. The fabrication procedure is stated to be compatible with the fabrication of active devices, although this was not demonstrated in the reported examples. The filter consisted of two resonators together with shunt inductors to resonate out the FBARs' parallel plate capacitances. The resulting 2-pole response showed very low insertion loss (1.1 dB) and a 3% fractional bandwidth. Such a device could be used as a front end preselect/image filter for cellular or PCS receivers. The techniques are reported to be suitable for use from 1 to 5 GHz. However, for a 1 GHz filter, the chip size is relatively large ($58mm^2$) – primarily due to the use of the on-chip spiral inductors.

A more complex stacked crystal filter (SCF) construction, not requiring spiral inductors has also been reported [159]. This device yielded a 10% fractional bandwidth, one pole response at 1.8 GHz. To the author's knowledge, no MCF structures have yet been implemented, although their possibility has been considered [158].

On-chip surface acoustic wave (SAW) filters have been reported in [60], [167], and [165]. These devices were constructed together with RF active circuitry in a modified BIFET process. As shown in Table 2.8, on-chip SAW filters include both wideband transversal designs (6.6% fractional bandwidth), and narrowband resonators (0.2% fractional bandwidth). These filters, operating at 283 MHz were fabricated using a ZnO piezoelectric deposited on top of aluminum interdigital transducers, resting on a field oxide SiO2 base. The surface acoustic wave propagates at the boundary of the SiO2 and ZnO and shows good performance, provided the thickness of the SiO2 and ZnO are selected properly [165]. For example, the dynamic range for a SAW delay line constructed in this form was found to be approximately 130 dB. The additional SAW filter entries in Table 2.8 listed as operating at 160 MHz are preliminary extrapolations of this work targeted at use in an up-conversion FM broadcast receiver [167]. The size of these filters ($21mm^2$ and $9mm^2$) is significant, but

not impractical.

Based on these reported results and projections, integrated electro-acoustic filters appear to offer good performance in moderate chip areas and could become practical as RF and IF filters in PCS receivers with further development. However, due to lack of access to suitable fabrication facilities, this option is not pursued in this dissertation. The interested reader is referred to the references for more information.

2.3.3 Analog Active Filters

The vast majority of research in on-chip filtering has dealt with the design of active filters – a mature subject on which hundreds of papers have been published and numerous textbooks have been written. Here we will concentrate on a subset of this work – the design of integrated bandpass filters targeted at radio receiver applications. As we will see, dynamic range, a significant area of concern in all active filter applications, is particularly troublesome in high-Q bandpass designs. In addition, fabrication tolerances and temperature drift also present significant technical challenges.

Implementation approaches for active filters can be grouped into three main categories, which are considered in the following subsections:

- Switched-capacitor filters,
- Continuous-time Gm-C filters, and
- Q-enhanced LC filters.

Switched-Capacitor Filters

At low frequencies (below about 10 MHz), switched-capacitor (SC) designs can provide precision filtering in the face of wide fabrication tolerances. By simulating a resistor's current-voltage relationship with charge sharing via capacitors and FET switches, "RC" time constants become dependent on capacitor ratios and clock rates alone. Since capacitor ratios can be held to tolerances as tight as 0.1% to 0.5% on a chip [91], very accurate responses can be achieved. The primary disadvantages of SC implementations are the need for fast settling amplifiers, and the need for anti-alias filtering at the input and reconstructive smoothing at the output. The former limits the frequency range over which the SC filter can operate, while the latter adds complexity and requires some degree of oversampling, beyond the Nyquist rate.

Some examples of reported SC bandpass filter implementations targeted at radio receiver design are shown in Table 2.9. The 260 kHz filter in [56] is a good example of early work in this area. This 3-pole (6th order) bandpass filter provides a fractional bandwidth of 2.5%, a dynamic range of 70 dB, and a power dissipation of 70 mW. With a 4 MHz clock, anti-aliasing can be provided with a simple low order, lowpass filter.

The remaining implementations listed in Table 2.9 illustrate both the possibilities and the practical problems of implementing SC filters at higher frequencies. These filters show reduced dynamic range, higher power dissipation, or both. Moreover, except for the GaAs implementation, the clock to center frequency ratio has been lowered to approximately 4:1 in order to reduce amplifier settling time problems, requiring more aggressive anti-alias filtering. The GaAs 20 MHz filter achieves a respectable dynamic range (for its bandwidth) and good clock to center frequency ratio, but its power consumption is unsuitable for a portable radio receiver application. In addition, at 8.6 mm^2 chip area for a 1-pole (2 nd order) design, its cost may also be a problem.

Table 2.9: Switched-Capacitor RF Bandpass Filters.

Ref	Year	Freq	Bandwidth	Order	Power	DR	Process	Size	Voltage
[56]	1983	260 kHz	6.5 kHz (2.5%)	6th	70 mW	70 dB	4 um CMOS	–	$\pm 5V$
[85]	1986	3.1 MHz	56 kHz (1.8%)	6th	45 mW	51 dB	1.75 um CMOS	$2mm^2$	$5V$
[86]	1988	10.7 MHz	430 kHz (4%)	6th	500 mW	42 dB	2.25 um CMOS	$2mm^2$	$10V$
[61]	1991	20 MHz	1.25 MHz (6.3%)	2nd	440 mW	65 dB	0.5 um GaAs	$8.6mm^2$	–

Continuous-Time Gm-C Filters

The problems associated with implementing SC filters at frequencies of several MHz or higher have led researchers to the design of continuous-time (CT) active filters. While CT filters actually predate SC filter design, implementation of CT filters in completely monolithic form is comparatively new.

One significant difference between discrete active filter design and the design of on-chip active filters can be seen in the building blocks employed. In discrete designs, these building blocks usually include resistors, capacitors, and operational amplifiers. The resulting filters are referred to as RC active filters. In the design of most modern integrated CT filters, suitable resistors are often not available, and MOSFETs biased in the resistive region are often used in their place. The resulting filters are then referred to as MOSFET-C filters [91]. In addition, the desire to operate at high frequencies and with smaller chip areas often rules out the use of operational amplifiers. Simpler active filters with fewer internal nodes and associated parasitic poles can be created using transconductance amplifiers, implemented with a small number of FETs. These Gm or operational transconductance amplifiers (OTAs) can be used to form gain stages and integrators. The names given to the resulting filter designs include Gm-C filters [94], OTA-C filters [94], transconductance-C filters [75], and transconductance - amplifier - capacitor (TAC) filters [68]. For uniformity and simplicity, we shall refer to all of these as Gm-C filters in this dissertation.

Today the dicipline of on-chip Gm-C filter design is well established. Several excellent review articles have appeared on the subject in leading journals [81] [91] [94], as well as books [63] [72] [84] and collections of reprint articles [93]. Nevertheless, commercial applications of Gm-C filters to date have been limited primarily to lowpass filters. An example is the AD896 from Analog Devices, designed for use in read channels of disk drives. The only potential applications of bandpass designs known to the author include a 5.5 MHz filter with a 5% fractional bandwidth designed at Philips as part of a television chroma, luminance, and sound separator IC [71], and a 55 kHz, 10% fractional bandwidth design used at Sony in an AM receiver [48]. However, it is not clear from the available literature if these filters have made it into marketed products.

Possible reasons for this limited commercialization of integrated bandpass filters can be seen by examining Table 2.10. This table summarizes the performance of bandpass filters reported from 1968 to 1994 that have been targeted at receiver design. Conclusions that can be drawn from these data include:

- Fractional bandwidths of many implementations are often excessive (up to 20%),
- Power dissipations are often high (100 mW or above),
- Chip area consumption is moderate to high ($4mm^2$ or above), and
- Dynamic range is low to moderate (40 to 70 dB).

Further research overviewed in the section on dynamic range below reveals that all of these problems are related. In fact, there are fundamental limitations to the dynamic range that can be achieved for a given power consumpation and filter fractional bandwidth. In the opinion of the author, these dynamic range limitations are perhaps the single most important reason why these filters have so far not seen significant commercial use.

Another significant problem with on-chip CT filters is frequency and Q accuracy. Achieving

Table 2.10: Continuous-Time Gm-C RF Bandpass Filters.

Ref	Year	Freq	Bandwidth	Order	Power	DR	Process	Size	Voltage
[79]	1968	650 kHz	13 kHz (2%)	2nd	100 mW*	65 dB	Bipolar	–	$+12, -6V$
[71]	1980	5.5 MHz	280 kHz (5%)	2nd	–	–	Bipolar	$\ll 11mm^2$	$12V$
[64]	1984	500 kHz	96 kHz (19%)	6th	55 mW	60 dB	6 um CMOS	$4mm^2$	$10V$
[55]	1986	10.7 MHz	2 MHz (19%)	6th	650 mW	60 dB	Bipolar	$16mm^2$	$\pm 5V$
[65]	1987	455 kHz	7 kHz (1.5%)	8th	–	40 dB	–	–	$5V$
[75]	1988	4 MHz	800 kHz (20%)	8th	900 mW	75 dB*	3 um CMOS	$23mm^2$	$\pm 5V$
[98]	1989	12.5 MHz	250 kHz (2%)	4th	360 mW	60 dB	3 um CMOS	$7.8mm^2$	$\pm 6V$
[66]	1989	10.7 MHz	1.1 MHz (10%)	4th	80 mW	50 dB	Bipolar	$4mm^2$	$6V$
[66]	1989	40 MHz	3.2 MHz (8%)	4th	80 mW	49 dB	Bipolar	$2mm^2$	$6V$
[68]	1989	95 MHz	8 MHz (8%)	2nd	–	–	3 um CMOS	–	–
[78]	1990	1.0 MHz	300 kHz (30%)	6th	25 mW	45 dB	1.75 um CMOS	$4mm^2$	$5V$
[69]	1990	200 kHz	20 kHz (10%)	18th	1.2 mW	54 dB	3 um CMOS	$2.5mm^2$	$4V$
[83]	1992	10.7 MHz	300 kHz (3%)	4th	220 mW	68 dB	1.5 um CMOS	$6mm^2$	$\pm 2.5V$
[54]	1994	455 kHz	27 kHz (6%)	18th	33 mW	64 dB	1.2 um CMOS	$17mm^2$	$5V$

full integration requires tightly controlled or trimmed on-chip resistor and capacitor tolerances together with precision temperature compensation. The alternative is to employ some form of on-chip tuning mechanism. The former adds considerably to the cost of design and fabrication, and is practical only at relatively large fractional bandwidths The latter adds complexity to the design, but has nevertheless become a necessary part of the on-chip Gm-C filter design dicipline [106]. In the subsections below, these two problems are investigated in greater depth.

Tuning Techniques Tuning of an on-chip Gm-C filter's frequency and Q is required due to fabrication tolerances and temperature drift of capacitances and transistor gains. To compensate for these factors, all of the filter implementations in Table 2.10 which have included tuning circuits on-chip employ some variant of a technique originally introduced by Tan and Gray [89]. This technique is now known as master/slave tuning [106].

In the simplest implementations of the master/slave technique, the "master" is an on-chip tunable oscillator whose component values are related by known ratios to those used in the "slave", which is the filter being tuned. Both master and slave receive the same tuning control voltages and/or currents so that changes in the master's frequency and Q are tracked by the slave. The desired filter tuning is then effected by phase locking the master oscillator to a known reference frequency supplied to the chip from an external source. In a radio receiver, such a reference might be available in the form of either a master local oscillator for frequency synthesis, or a clock for the control microprocessor.

With proper design, matching and tracking for both capacitors and transistor gains in Gm-C filters can be held to as tight as 0.1% to 0.5% [91], which is adaquate for realizing selectivity Q values as high as 50-100 and pole frequencies as accurate as about 1%. This implies a practical lower limit to bandpass filter fractional bandwidths of about 2% – a conclusion supported by filter realizations listed in Table 2.10.

If smaller fractional bandwidths are desired, some form of "self-tuning" technique is needed. A handfull of researchers have addressed this problem, offering control systems with varying degrees of complexity and performance. In 1981, Tsividis [108] proposed a technique involving switching between two filters, allowing the filter used in the signal processing to be periodically taken off-line and retuned. Tuning off-line can be relatively easy and can provide arbitrary precision. For example, for a second-order filter, a sinusoid at the filter's center frequency can be fed to the filter. The amplitude and phase of the sinusoid at the filter output can then be used to sense and adjust the filter's Q and center frequency respectively. Later, Brooks and VanPeteghem [100] introduced an approach that allows the filter involved in the signal processing path to be tuned without interruption. Their Correlated Tuning Loop (CTL) technique performs a narrowband autocorrelation on the filter's input signal and a narrowband cross correlation between the filter's input and output signals to derive tuning control signals. More recently, Kozma, Johns, and Sedra [103] [104] presented a tuning technique based on adaptive filtering and described an approach incorporating two

filters which could allow tuning the filter used in the signal processing path without interruption. In this approach, filter A continuously processes the input signal while filter B is first tuned with a known reference as descibed above, and then connected to the input signal so that its output can serve as a reference for adjusting filter A. With this arrangement, filter B could be periodically tuned as in [108], and no interruption of the signal processing by filter A is needed.

In a paper by the author [105], a technique called orthogonal reference tuning (ORT) was developed and prototyped. In this approach, a known reference signal is employed and is present in the filter passband together with the RF/IF signal being processed. This is permissible provided the reference signal can be made orthogonal, or nearly orthogonal, to the processed signal so that the two can be separated at the filter output. This is shown to be possible for certain types of modulation, including wideband FM and digital signaling such as BPSK and spread spectrum. The details of this technique are presented in Chapter 7 later in this dissertation.

It is interesting to note that to date none of these approaches have been implemented on-chip. This fact is most likely due partly to their complexity, and partly to the inherent dynamic range limitations of high-Q filters for which they are most applicable. These dynamic range limitations are investigated in some depth in the following section.

Dynamic Range Limitations Dynamic range (DR) is an important performance parameter in radio receiver design. For receivers incorporating active filters, the DR of the filter employed will upper bound the receiver DR and is therefore of paramount importance in the filter's design.

Dynamic range is typically defined as the maximum output signal power P_{sat} prior to some level of gain compression and/or signal distortion, divided by the integrated output noise power P_N in the bandwidth of interest B. In filter design, the filter noise bandwidth is

often used, which for high order filters is approximately equal to the filter's nominal (e.g. 3 dB) bandwidth. Thus,

$$DR = \frac{P_{sat}}{P_N} = \frac{V_{sat}^2}{V_N^2} \tag{2.1}$$

where V_{sat} and V_N are the saturation and integrated noise voltages measured at the filter output.

All filters, whether active or passive possess a finite DR. For example, in a passive electro-acoustic filter, P_N is determined by thermal noise, and can be computed by

$$P_N = kTB \tag{2.2}$$

where k is Boltzmann's constant, and T is the physical temperature in Kelvin (e.g. K = 290). The limit on maximum signal power is determined by non-linearities in stress and strain relationships in the piezoelectric material, and although it may be very large, it is still finite. As an example, the DR of an on-chip SAW delay line is given in [167] as 130 dB. This figure is considerably higher than the *instantaneous* DR of many receivers.[3] Hence, the issue of DR in passive filters is often ignored.

In active filters however, DR limitations can be much more severe. One obvious limitation is that imposed by saturation of the active circuits employed. For most filters, the maximum output signal power will be some fraction of the total power consumed by the circuit. A less obvious, but equally important factor in active filters is an increase in the noise floor over that given in (2.2) due to shot and thermal noise in the devices used, and the amplification

[3]In receivers such as televisions, where linear modulation is used, the overall DR may be 100 dB or higher due to the use of AGC, but the instantaneous DR is usually less. For FM receivers where limiting is employed, the circuits prior to the channel select filter must still be linear and their DR is usually below 100 dB.

of this noise in certain areas of the circuit.

In a 1983 paper on SC filters, Choi [56] made the observation that noise in high-Q SC filters is greater than that of low-Q filters due to the inherent gains associated with the filter resonators. However, no quantitative treatment was given. Khorramabadi [64] quantified this effect for the case of continuous-time filters, giving the following expression for the noise at the output of a 6th order Gm-C ladder filter

$$V_N^2 = \frac{3kTQ}{C_{intg}} \tag{2.3}$$

where Q is the filter's selectivity Q and C_{intg} is the capacitance associated with the integrators used. Applying the definition of DR in (2.1), the DR *of this filter* becomes

$$DR = \frac{V_{sat}^2 C_{intg}}{3kTQ} \tag{2.4}$$

in which the dependence of DR on Q is clearly evident.

The issue of *fundamental* limits on DR for arbitrary Gm-C filter designs was investigated in detail by Groenewold [115] [116]. In a 1992 paper, he showed that for a high-Q biquad, the optimum DR that can be achieved is given by

$$DR_{opt} = \frac{V_{sat}^2 C_{total}}{4kTFQ} \tag{2.5}$$

where C_{total} is the total capacitance in the filter's integrators, and F is a noise factor term ($F > 1$) used to account for possible excess noise contributions by non-ideal devices. In the same paper, an approximate upper bound on optimum DR for a general high-Q BPF was derived as

$$DR_{opt} \leq \frac{V_{sat}^2 C_{total}}{2\pi kTFQ} \tag{2.6}$$

a result in general agreement with that predicted by Khorramabadi for a particular 6th order filter. Similar relationships for the dependence of DR on filter Q for high-Q designs have also been published by Abidi [110].

The results published by Groenewold have been extended by the author in [119] to show the dependence of DR on filter power consumption P_{diss} and filter bandwidth B – parameters more appropriate to system level receiver design studies. Under these constraints, it was shown that the optimum DR is inversely proportional to the *square* of the filter Q

$$DR_{opt} = \frac{\eta P_{diss}}{4\pi kTFBQ^2} \tag{2.7}$$

where η is an efficiency factor relating the power consumed by the filter to the maximum output signal power. In the same paper, the DR of several hypothetical low power Gm-C filters were compared to DR measurements reported for commercial radio receivers. From these comparisons it was concluded that Q values up to approximately 100 in Gm-C bandpass filters can theoretically yield acceptable DR at acceptable power consumption, if an efficiency of 0.1 and a noise factor of 2 can be achieved. This result is studied in detail in Chapters 5 and 6. A comparison of this result with DR figures listed in Table 2.10 on a normalized, per Hz basis suggests that efficiencies and/or noise figures of realizations to date are about one order of magnitude worse than this, indicating where some room for improvement might be found.

A detailed study of Groenewold's work reveals that the mechanism responsible for limiting DR in high-Q bandpass filters is essentially the regenerative gain associated with the realization of high-Q complex poles – exactly the reason cited by Choi [56] for SC filters. This implies that the only way to improve DR performance in an active filter (for a fixed power

consumption and bandwidth) is to decrease the regenerative gain. In turn, this suggests a need for resonance circuits which possess energy storage and exchange mechanisms (see Chapters 5 and 6).

This line of reasoning by the author led to an exploration of the dynamic range of Q-enhanced LC filters. In [119] it was shown that a 2nd order bandpass LC filter whose Q has been increased by active negative resistance circuitry does indeed provide marked improvements in DR over Gm-C filters. The DR for such a filter is found to be:

$$DR_{opt} = \frac{\eta P_{diss}}{4\pi kTFBQ^2} Q_o^2 \tag{2.8}$$

where Q_o is the base Q of the LC circuit prior to Q enhancement. Thus, even though the Q of on-chip inductors may be limited to 10 or less, an on-chip Q-enhanced LC filter should be able to realize small fractional bandwidths while providing a 20 dB improvement in DR over an Gm-C realization. Alternatively, for a given DR, the Q-enhanced filter with a coil Q of 10 requires *two orders of magnitude less power* than a Gm-C filter operating at similar efficiency. This feature is one of the primary reasons for the emphasis on Q-enhanced filtering in this dissertation.

Q-Enhanced LC Filters

Q-enhanced (QE) LC filtering is an emerging research area on which few papers have so far been published [57] [76] [119]. One possible realization of an Q-enhanced LC filter which has been used by the author is illustrated in Figure 2.6

In this realization, a MOSFET differential input amplifier Q1A, Q1B provides current drive to an LC tank circuit composed of L1A, L1B, and C1. Stray capacitances CSA and CSB represent both the inductor turn-to-substrate capacitance as well as transistor gate and

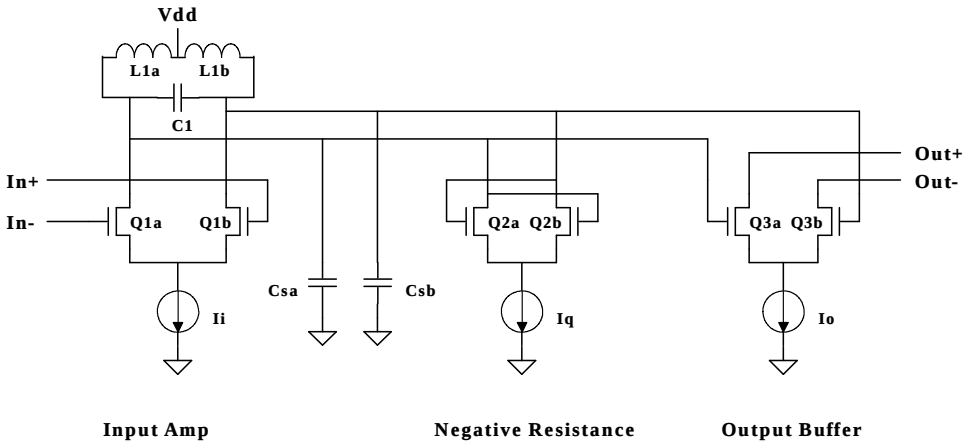

Figure 2.6: Q-enhanced LC Bandpass Filter.

drain loading, modifying the tank circuit's resonance frequency. By itself, the resulting modified tank circuit's differential impedance seen between the drains of Q1A and Q1B has low Q due largely to the spiral inductor series resistance losses. These losses, combined with smaller losses from the tank circuit capacitances, can be represented (near the resonant frequency) by a suitable valued resistance in parallel with C1. The negative resistance circuit composed of cross-coupled differential amplifier Q2A, Q2B cancels most of this resistance, producing a Q-enhanced resonance. This circuit is tuned by varying the tail current Iq to effect a desired Q. Finally, output buffer Q3A, Q3B serves to isolate the filter load from the tank circuit and provide a lower impedance drive capability.

While the concept of increasing the Q of a tank circuit dates to the early days of radio design in the form of regenerative receivers [2] [20], the use of this technique for high-order, precision filtering has so far received little attention. One possible explanation for this is the applicable frequency range of on-chip inductors. According to [77], this range is limited to about 1 GHz and above. In fact, work by the author indicates that this is a soft limit which depends on fabrication process characteristics, and on what constitutes acceptable

Q for a coil – factors considered in depth in Chapters 6 - 8. With the advent of new frequency spectrum allocations at 900 MHz, 1.8 GHz, and 2.4 GHz for cellular and PCS, there is now increased motivation for exploring this area of active filter design. Such designs could function either as RF preselection/image filters or as IF channel selection filters in cellular/PCS receivers.

The earliest reference to Q-enhanced bandpass filtering in the 1 - 2 GHz range known to the author is a paper by Duncan, et. al. in 1993 [57]. This work described a "series mode" compensation of inductor losses to raise the Q of 5 nH inductors from 5 to 20 at 1.6 GHz. Automatic frequency or Q tuning was not addressed, and only simulated results were reported. In [93], a "parallel mode" approach was descibed in which an active negative resistance circuit was placed in parallel with the inductance as in Figure 2.6. Later [77], results were reported for a frequency scaled, board-level prototype using the parallel mode approach. An approach to frequency tuning without requiring a varicap diode was also discussed [76] [77].

Q-enhanced LC filters possess a number of attractive features besides the dynamic range advantage discussed in the previous section. For example, they should exhibit lower sensitivity to active components [57], which can make Q tuning easier. In addition, stray capacitances such as CSA and CSB in Figure 2.6 which present significant problems in Gm-C filter design [65] are easily tuned out in Q-enhanced filters by adjusting the value of the inductors or the resonanting capacitance C1. These issues are explored more fully in Chapters 5 and 8.

2.3.4 Summary of Alternatives

The options discussed in the preceding sections for implementing on-chip, low power, RF bandpass filters are summarized in Table 2.11.

Digital filters operating at acceptable power levels have been shown to be viable only at

Table 2.11: Summary of On-Chip RF Bandpass Filter Alternatives.

Filter Type	Advantages	Disadvantages	Frequency	Applications
Digital	Precision, dynamic range, programmability	Power consumption, chip area, aliasing, ADC requirements, external clock requirement	< 10 MHz	Low IF filtering, baseband filtering and signal processing.
Passive LC	Dynamic range, stability	Quality factor, chip area	> 100 MHz	Power amp harmonic suppression, low Q RF preselection
Electro acoustic	Dynamic range, stability	Process modifications, chip area	> 100 MHz	RF preselection, IF filtering
Switched capacitor	Precision	Dynamic range at high Q, aliasing, external clock requirement	< 10 MHz	Low frequency, moderate Q IF filtering, baseband filtering
Gm-C	Frequency of operation	Dynamic range at high Q, tuning requirement	< 100 MHz	Moderate Q IF filtering, baseband filtering
Q-enhanced LC	Dynamic range, stability	chip area, tuning requirement	> 100 MHz	RF preselection, IF filtering

relatively low frequecies, limiting their application to low IF and baseband processing.

Passive LC circuits are limited to operating at *high* frequencies due to the size of on-chip inductors, and to the design of low Q, large fractional bandwidth filters due to inductor losses. Nevertheless, passive LC circuits are used routinely in GaAs ICs and are beginning to be applied in silicon ICs both as impedance matching networks and as harmonic suppression filters in power amplifiers.

On-chip electro-acoustic filters, either in the form of bulk acoustic wave (BAW) or surface acoustic wave (SAW) devices, offer potentially good performance for high frequency applications with both moderate (e.g 10%) and narrow ($< 1\%$) fractional bandwidths. Economic acceptance of these devices will hinge on the availability of modified fabrication facilities and on what constitutes acceptable chip areas.

Switched-capacitor (SC) filters, which are used extensively in baseband signal processing applications, have also been demonstrated at IF frequencies. Their frequency range is limited to less than about 10 MHz in low cost silicon processes. Moreover, high-Q filters are fundamentally limited in dynamic range – a property shared with continuous-time active

filters. For low power applications, this limits SC filter realizations to moderate fractional bandwidths with pole Qs of 50 to 100.

Continuous-time on-chip active filters designed for high frequency operation employ Gm-C architectures rather than the more traditional operational amplifier based designs used in discrete RC filters. This allows them to work at higher frequencies than SC filters. Although most reported designs have been implemented at or below about 10 MHz, operation to 95 MHz has been demonstrated, and finer geometry processes could double or quadruple this range in the future. However, in common with SC designs, fundamental dynamic range problems will limit their application to moderate fractional bandwidths (pole Qs of 50 to 100) in low power designs.

Finally, for frequencies above 100 MHz, Q-enhanced LC filtering offers a potentially good alternative to electro-acoustic filtering – without the need for fabrication process modifications. Dynamic range of Q-enhanced LC filters is improved over that of SC and Gm-C designs by a factor of Q_o^2, where Q_o is the Q of the LC resonator employed before Q enhancement. Commercial viability of this new area of research will depend on the dynamic range values achieved in practice, on the development of suitable methods for frequency and Q tuning, and on chip area requirements of the inductors employed.

2.4 Integrated Synthesizers

In Section 2.1.1 we saw that frequency synthesizer ICs as well as receiver ICs with which they were designed to operate both lacked one key component – on-chip tuned circuits. In this section we examine some of the technical reasons why complete synthesizers, including oscillator resonant circuits, are not currently implemented on-chip. A brief look at the direct digital synthesis alternative to traditional PLL synthesizers is also included.

2.4.1 On-Chip Local Oscillators and VCOs

The reasons for oscillator resonant circuits remaining off-chip have much in common with the problems associated with on-chip filtering. From an economic viewpoint, restricting an IC to a particular frequency range limits its market size, just as on-chip filters would. Nevertheless, just as for filters, there are several markets which are large enough to warrant fixed frequency band products, with broadcast radio and television as well as cellular and PCS among them. Thus the reasons for their limited use must be largely technical.

A look at commercial offerings shows that various forms of integrated oscillators have been available for many years. For example, ring oscillators and Gm-C oscillators such as those employed in master/slave tuning of Gm-C filters can be easily built. These circuits can be made tunable, and can operate at frequencies up to at least several hundred MHz [141] [96], satisfying two important requirements for use in tuners. A third requirement however, that of spectral purity, is more problematic.

In radio receivers, phase noise and spurious outputs of local oscillators can often be critical to receiver performance [147]. Phase noise and spurious outputs can be a limiting factor in receiver dynamic range, as well as a contributor to poor signal to noise ratios and bit error rates of demodulated signals. In addition, spurious outputs can result in spurious signals being received which are not actually present in the environment.

One additional technical problem in implementing on-chip oscillators is on-chip signal coupling. Placing oscillator circuits on-chip with a digital synthesizer IC can be expected to produce substantial spurious outputs due to the presence of high frequency harmonics of digital switching waveforms. This problem may be solvable however, by careful choice of frequencies and divider ratios. An alternative is to partition the system design into one digital IC and one analog IC, physically separating the digital synthesizer circuits from the analog oscillator. However, even if this is done, the problem of oscillator phase noise

remains.

Oscillator Phase Noise

Theoretical formulas for predicting oscillator phase noise were developed by Leeson and Robins in the early 1960s [142] [147]. For an LC based oscillator, Robins has derived the ratio of the one-sided phase noise power N_{op} in a 1 Hz bandwidth to the oscillator output power P_{osc} as a function of frequency offset Δf from the nominal oscillator frequency f_o as

$$\frac{N_{op}}{P_{osc}} = \frac{kTF}{8Q^2P_{osc}}(\frac{f_o}{\Delta f})^2 \tag{2.9}$$

where k is Boltzmann's constant, T is temperature in Kelvin, F is a noise factor of the oscillator active circuits, and Q is the loaded quality factor of the LC resonant circuit. This formula is derived by treating the oscillator as a linear filter with sufficient Q enhancement that it amplifies the thermal noise to the desired output power level of the oscillator. $\frac{1}{f}$ noise of active devices is not included in the derivation, so that (2.9) applies only at large frequency offsets. The linear assumption, which can be achieved with a detector and AGC circuit if necessary, is a relatively good one for high quality oscillators. This simple formula provides significant insight into the spectral purity problem and shows fundamental limits to achieving good phase noise performance. Good phase noise requires a large resonant circuit Q, with performance improving as Q^2 – exactly the same behavior noted for Q-enhanced LC filters.

Since (2.9) was derived for LC oscillators, it is not directly applicable to active circuits without inductors. We may expect nevertheless that the phase noise of inductorless oscillators would be on the order of that predicted by (2.9) for the case of $Q = 1$. This expectation is supported by the following result for the phase noise of a Gm-C based oscillator published, but not derived, in [149]:

$$N_{op} = kTR(1 + A + 2Q)(\frac{\omega_o}{\Delta\omega})^2 \tag{2.10}$$

In (2.10), Q is now defined as X_c/R – a figure of merit for the active inductor and capacitor employed. X_c is the tank circuit capacitive reactance, R is the series resistance of the tank circuit, and A is a noise factor term which is taken to be 1 for an ideal OTA.

The value of N_{op} in (2.10) is strictly increasing with R and is minimum for $R = 0$, corresponding to use of an ideal active inductor, and lossless capacitor. Under this condition, we can rewrite (2.10) in the form of (2.9) to allow a comparison:

$$\frac{N_{op}}{P_{osc}} = \frac{2kT}{P_{osc}}(\frac{f_o}{\Delta f})^2 \tag{2.11}$$

This result supports our earlier conclusions. The phase noise of oscillators using active inductors is significantly and fundamentally inferior to that of LC oscillators – just as the dynamic range of Gm-C filters was found to be inferior to that of Q-enhanced LC filters. The important issue of what level of phase noise is acceptable will be considered in detail in Chapter 10. The answer to this question will be found to depend on the radio system in which the oscillator is employed.

2.4.2 Reported Implementations

Table 2.12 summarizes some of the work in on-chip oscillators reported to date and the phase noise performance obtained.

In [96], Voorman, et. al. report an oscillator constructed with a Gm-C architecture operating at 215 MHz, which is converted to 430 MHz using an on-chip frequency doubler. Although few details are given, a spectrum analyzer display shows a phase noise at 100 kHz offset of approximately -90 dBc/Hz.

Table 2.12: Reported Work in On-Chip Oscillators.

Reference	Type	f_o	Q	Power	Phase Noise
[96]	Gm-C	430 MHz	-	-	-90 dBc @ 100 kHz
[144]	LC	1.8 GHz	5*	70 mW @ 5 V	-67 dBc @ 20 kHz -88 dBc @ 100 kHz
[149]	LC	1.1 GHz	21	1 mW @ 1 V	-75 dBc @ 10 kHz
[150]	TFR	300 MHz	-	-	-110 dBc @ 1 kHz

In 1992, Nguyen [144] et. al. describe the design of an integrated LC-based VCO operating at 1.8 GHz and possessing a 5% tuning range. As an alternative to the use of varactors for tuning, a cross-coupled, dual tank circuit Colpitts configuration is used. The inductors employed are square spirals with outer dimensions of approximately 200 um. One has 9 turns, giving approximately 7 nH inductance, while the other has 7 turns, giving 5 nH of inductance. The circuit operated at 5V and consumed 70 mW of power. The measured phase noise is -67 dBc at 20 kHz offset and -88 dBc at 100 kHz offset.

As an alternative to on-chip spiral inductors which are known to be low in Q, Steyaert and Craninckx [149] investigated the use of bondwires to create inductors. A 1.1 GHz oscillator was constructed which consumed 1 mW of power from a supply as low as 1 V. Even at this reduced power, the phase noise is improved over Nguyen's result, thanks to the higher inductor Q.

In [150] and [151], Burns, et. al. report results for an oscillator at 300 MHz based on a thin film bulk acoustic wave resonator. These resonators provide Qs in the range of 1000 or above, which accounts for the significant improvement in phase noise over other work listed in the table. A phase noise of -110 dBc/Hz was reported at an offset of only 1 kHz.

To put all of these results into some perspective, they are shown plotted together with the phase noise of a cellular phone VCO in Figure 2.7. The curve for the cellular phone VCO is taken from the National Semiconductor LMX1501A synthesizer data sheet and represents

a highly optimized discrete VCO design. To provide a meaningful comparison, all phase noise values plotted in Figure 2.7 have been normalized to a 1 GHz operating frequency according to the frequency scaling behavior predicted in (2.9) and 2.11.

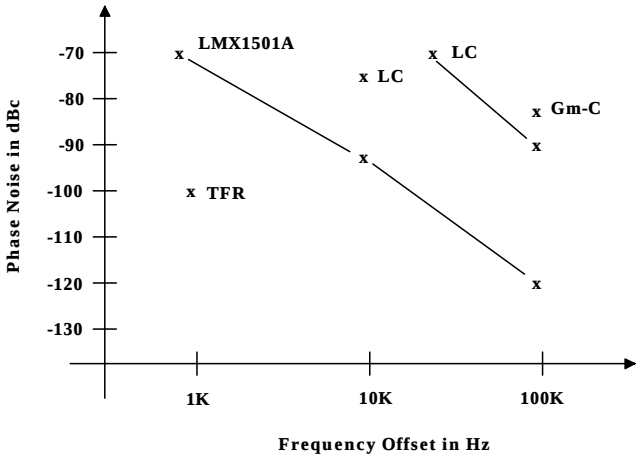

Figure 2.7: Phase Noise Comparison of On-Chip Oscillators.

Finally, we note that there appears to be at least one example of an on-chip synthesizer being produced in a commercial chip. In [29], a product announcement for an RF IC for a global positioning system (GPS) receiver shows a block diagram with an on-chip oscillator together with PLL synthesizer divider circuits. However, no description of, or technical information on, the oscillator was provided.

2.4.3 Direct Digital Synthesis

One possible alternative to use of on-chip VCOs is direct digital synthesis (DDS) technology [143] [33]. Direct digital synthesis has several attractive features including:

- Phase noise is equivalent or better than that of the crystal reference clock signal used,

- Frequency resolution can be very small ($\ll$ 1 Hz), and
- Switching time is nearly instantaneous.

The biggest problems facing these devices are power consumption, spurious frequency generation, and chip area. As an example, a DDS operating at a 150 MHz clock rate has been reported in [145]. Built in a 1.25 um CMOS process, it consumes approximately 1 W of power and 25 mm^2 of chip area. Spurious levels are -67 dBc when using an external 12 bit digital to analog converter (DAC). A more recent, lower power DDS has been reported in [140]. Implemented in a 1 um CMOS process, it includes an on-chip 10 bit DAC, dissipates 40 mW at 40 MHz clock frequency, and consumes approximately 15 mm^2 of chip real estate.

Perhaps the biggest problem with DDS devices in radio receiver applications is their relatively low frequency of operation. The synthesized sinusoid of a DDS is limited to less than half of the clock rate by the Nyquist criterion. This requires that the synthesized signal either be frequency multiplied to the desired final local oscillator operating frequency (e.g. 1 GHz), or that it be mixed with an auxiliary oscillator. Frequency multiplication by a factor N results in an increase in both phase noise and spurious levels by $20log(N)$ [147] [143], resulting in poor performance for large N. The other alternative, frequency mixing, requires a high purity oscillator operating near the desired final frequency together with an image rejection mixer, a bandpass filter, or both. Thus, the generation of the desired LO signal may actually be complicated by the use of the DDS in comparison with a simpler VCO and PLL synthesizer approach. The advantages of DDS are primarily found only when fine frequency resolution and/or fast tuning is required.

2.5 Integrated Receivers

In Section 2.1, we looked at commodity ICs targeted at radio design and discovered that despite high levels of integration in many devices and names such as "single-chip receiver"

coined by their manufacturers, two key components – bandpass filters and LO tuned circuits – were not included. In this section, we investigate research and development efforts directed toward *complete* integration of receivers from antenna input to baseband (audio or digital) output. A summary of this work is provided in Table 2.13 and discussed below.

Table 2.13: Reported Work in Integrated Receivers.

Ref	Application	Architecture	Sensitivity	Selectivity	Size	Voltage	Current
[85]	Narrowband FM	Dual Conversion Superhet	5 mV	31 dB	7.7 mm^2	5 V	20 mA
[167]	FM Broadcast	Up Conversion Superhet	1 uV	–	$> 9mm^2$	–	–
[43]	FM Broadcast	Low IF w/ Modulation Compression	1 uV	35 dB	4.5 mm^2	3-18 V	8 mA
[48]	AM/FM Broadcast	Low IF w/ Image Reject Mixer	1 uV	40 dB	12 mm^2	0.9-4.5 V	16 mA
[51]	Paging	Zero IF	–	–	5 mm^2	1.8 V	2.5 mA
[52]	Paging	Zero IF	-126 dBm	70 dB	18 mm^2	2-3.5 V	2.7 mA

2.5.1 Classical Superheterodyne Architectures

Reported work on integration of classical superheterodyne receivers is limited, and to date no complete single-chip designs have been realized in hardware. In Section 2.2, we postulated that the availability of suitable bandpass filters is largely to blame for this – a conclusion supported by work reported in [42], [50], and [167] which is reviewed below.

Downconversion Designs

In 1986, Song, et. al. [50] employed two switched-capacitor bandpass filters in the design of a CMOS dual conversion superheterodyne narrowband RF "receiver". The design consisted of an RF down conversion mixer followed by a 3 MHz first IF bandpass filter with a 6th order response and a bandwidth of 55 kHz. Continuous-time anti-alias filters are included at input and output ports of this filter. A second mixer downconverts the first IF filter

output to a 72 kHz second IF where a 6th order switched capacitor bandpass filter narrows the channel bandwidth to 24 kHz.

Demodulation of narrowband FM is provided on-chip through the digital equivalent of a one-shot FM detector. Following demodulation, a 3.75 kHz switched capacitor, 7th order lowpass filter is used to smooth the output signal. A single reference clock together with appropriate dividers provides all clocking for the SC filters as well as the LO signal for the second mixer. The RF front end and first mixer LO are not included on-chip. Aside from these omissions, the largest problems with this design are the basic receiver architecture and the performance achieved.

According to the authors, the low first IF (3 MHz) was selected to avoid problems with available on-chip bandpass filters which are difficult to implement at higher frequency (especially for SC designs), and are limited in Q. Although the chip was stated as being targeted at use with RF inputs in the range of 50 - 100 MHz, this low IF would make this difficult in some applications. If operated at 50 MHz, a 4th order preselect filter with a 1% fractional bandwidth would be required to provide adaquet image rejection. At 100 MHz, the fractional bandwidth needed would be 0.5%. Moreover, if the service band of interest exceeds 500 kHz, this filter would need either a higher order response to provide sharper rolloff, or would have to be tunable.

In addition to these problems, the 1.8% distortion achieved is somewhat high and the 31 dB alternate channel selectivity is probably too low to be practical - especially when competing with other receivers which routinely achieve figures of 40 - 70 dB or higher.

Upconversion Designs

One approach to dealing with the image problems of superheterodyne receivers is to use an up-conversion architecture in which the first IF is higher in frequency than the desired RF

signals. In an up conversion design, requirements on RF preselection/image filtering are relaxed substantially, although other requirements become more severe. For example, the up-conversion is usually followed by a down conversion to a low second IF for amplification and detection. The ratio of the first to second IF frequencies may be as high as 100, requiring a very narrow first IF filter implemented as a ceramic or SAW design. However, this narrow filter can now be implemented at a single frequency (assuming receiver tuning is done using the first mixer LO), regardless of how wide the service band of interest is.

These features together with the problems of implementing on-chip high-Q active bandpass filters led researchers at Delft University to explore the possibility of building up conversion receivers with on-chip SAW filtering [167] [120] [165] [42]. In [167], P. T. M. van Zeijl et. al. explored the feasibility of an integrated up conversion FM broadcast receiver with a first IF at 160 MHz. The integration of RF front-end circuitry (amplifiers and mixers) together with SAW filters was demonstrated, although a filter with the required bandwidth was not realized in this effort. In addition, other required circuits such as the synthesizer, second IF, and demodulator were omitted. General conclusions drawn from this work include:

- Integration of active circuits with SAW filters is viable if "minor" fabrication process modifications are made,
- filter area is relatively large and a resonator filter design should be used to meet the very narrow fractional bandwidth required (0.1% in this case),
- dynamic range performance is excellent, with both the electrical circuits and a SAW delay line exhibiting over 100 dB in a bandwidth of 180 kHz,
- the image frequency at 400 MHz can be attenuated by 50 dB using a simple antenna matching network / filter circuit, and
- SAW filter frequency tolerance and temperature sensitivity are potential problems (300 ppm accuracy and 3 ppm / ^{o}K temperature stability required).

Related work by Eikenbroek [42] and van der Plas [49] explored the feasibility of an up conversion receiver for AM broadcast and shortwave (150 kHz - 30 MHz) using on-chip SAW filtering. Recognizing the frequency accuracy and stability problems of the necessarily narrowband SAW filters, they investigated the use of a selective AM detector, rather than the use of narrowband active filtering at a 2nd IF. No selectivity figures were reported for the proposed detector, but concerns were raised about its required complexity.

2.5.2 Ultra-Low IF Architectures

For other researchers, problems with implementing suitable on-chip bandpass filters led to departures from the classical superheterodyne receiver. An excellent review of this work is provided by Abidi in [40].

One of the earliest such departures was reported by Kasperkovitz [43] at Philips Research Laboratories. In this work, an FM broadcast receiver was designed and implemented using an ultra low IF frequency of 70 kHz. This choice places the image frequency in the gap halfway between the desired station and the adjacent channel. Distortion problems resulting from large deviations ($\Delta f > 70kHz$) were avoided by employing AFC feedback to compress the peak modulation deviations to $\pm$ 15 kHz. Selectivity prior to demodulation is provided by a 4th order continuous-time filter with a cutoff of 100 kHz. This filter gives 38 dB of attenuation to an adjacent channel signal displaced 300 kHz away (European FM). Adjacent channel selectivity, although not quoted, should be in the neighorhood of 35 dB after capture ratio is subtracted from the 38 dB attenuation. Sensitivity of the receiver was quoted at approximately 1 uV.

The Philips receiver, which was marketed as the TDA 7000, was perhaps the first IC to qualify as a true "radio-on-a-chip". External components were limited primarily to the antenna, manually tuned tank circuit, batteries, and speaker power amplifier. However, the performance was rather limited as seen by figures quoted in Table 2.13. In fact, the

device data sheet provides little information in the form of specifications beyond sensitivity and maximum signal level. Adjacent and alternate channel selectivity and intermodulation dynamic range figures are not given – possibly indicating that the device performs poorly in these areas.

Approximately a decade later, work at SONY on developing a single-chip AM/FM stereo receiver resulted in a non-traditional architecture similar in many ways to that of the Philips receiver. The SONY receiver is a dual conversion superheterodyne with a 30 MHz first IF and an ultra-low second IF. Images from the first down conversion are attenuated by a low complexity off-chip antenna matching/filter network. Interestingly, no bandpass filtering is provided at the 30 MHz first IF. Instead, this IF is used solely to simplify the implementation of an image-rejection (IR) second mixer which downconverts to 150 kHz for FM and to 55 kHz for AM. An off-chip adjustment for mixer balance allows the IR mixer to attenuate images by approximately 40 dB.

As in the Philips design, final channel selectivity is provided in FM mode by an on-chip high order lowpass filter. In AM, selectivity is provided by an on-chip 55 kHz, 6th order, continuous time bandpass filter with a Q of 10. Overall receiver performance is improved over that of the earlier Philips design as seen in Table 2.13, although at the price of higher current consumption, larger chip area, and increased off-chip component count. Selectivity and image rejection are nevertheless quite low relative to more traditional superheterodyne receiver designs implemented with off-chip ceramic filters.

2.5.3 Direct Conversion Architectures

In addition to these designs for FM broadcast, single-chip receiver ICs have been implemented for the radio paging market [51] [52]. Here too, alternatives to traditional superheterodyne architectures have been adopted in order to avoid on-chip bandpass filters. In [51], Vance describes a zero IF (direct conversion) architecture which is ideally suited to the

narrowband FSK modulation used in pagers. The method employs in-phase and quadrature phase (I and Q channel) mixers to generate two baseband waveforms. On-chip lowpass filters follow the mixers to provide channel selectivity, after which the signals in each channel are amplified, limited, and fed to a flip flop detector.

The flip flop detector represents a perfect solution to the demodulation of FSK signals in a direct conversion receiver. The flip flop is clocked by the square wave output from the I channel limiter and latches the value of the Q channel limiter output on each I channel rising edge. Because of the quadrature downconversion and the binary FSK signal, the Q channel output is either 90 degrees leading or lagging from the I channel, depending on the FSK bit polarity. Thus the data latched will either be zeros or ones, depending on the modulation bit.

Details of the circuit implementation and performance measurements are not given by Vance, but a similar design by Wilson, et. al. [52] reported in 1991 gives some indication of the level of integration and performance achievable. Their design, shown in Figure 2.8, employs a ferrite core loop antenna resonated with an off-chip tunable capacitor. This tuned antenna is connected to an RF amplifier. An LC tuned circuit load employed with the RF amplifier as well as the 90 degree phase splitter required for I/Q mixing are implemented off-chip. The RF amplifier active circuits together with all remaining circuitry (except for the crystal resonator for the LO) are implemented on-chip.

Lowpass filters consisting of a third-order Sallen-Key stage followed by a 7th order gyrator-capacitor stage provide channel selectivity, and also account for approximately half of the 18 mm^2 chip area. The filter cutoff frequency is one-time tuned by an external resistor which controls bias currents and transistor gains. As seen in Table 2.13, this high order on-chip filtering results in good adjacent channel selectivity, although at the expense of substantial chip real-estate. The receiver also achieves a respectable blocking dynamic range (BDR) of 82 dB at 1 MHz offset, while operating at 2.7 mA from a 2 V supply. However, it must be

noted that the pager IC employs the equivalent of 4th order preselection filtering (tuned antenna plus tuned load RF amplifier) implemented *off-chip* which may be responsible for part of its BDR achievement.

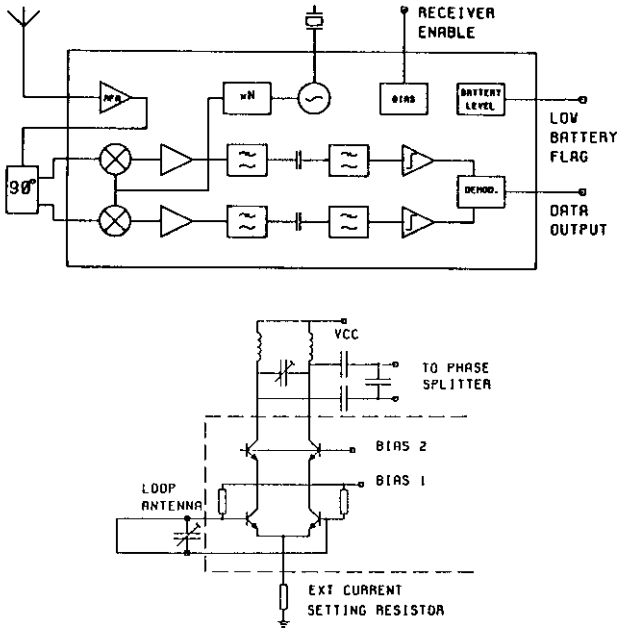

Figure 2.8: Single-Chip Paging Receiver. Copyright 1991 IEEE. Reprinted by permission, from [52].

As a final example of work in highly integrated receivers, we mention the on-going Wireless Tranceiver Project at the University of California at Los Angeles [40]. In this project, the UCLA team is designing and implementing a two chip, direct conversion, frequency hopped, FSK tranceiver for use in the 900 MHz ISM band. At the time of this writing, little performance information is available outside of that reported for individual components such as the DDS and RF amplifier chips referred to earlier in this chapter [122] [140].

Chapter 3

System Requirements

Commercial acceptance of integrated radio receivers will depend, to a large degree, on the performance that can be achieved. Thus, before studying circuit level approaches to integration, it is important to understand the system level performance requirements that must be met. In this chapter, identification of performance requirements begins with a brief study of the radio frequency spectrum in which modern receivers are required to operate. An overview of important commercial wireless services that could benefit from integrated receiver technology is then provided. Finally, the critical performance measures that most directly affect the design of integrated receiver hardware are examined.

In Chapter 2, RF and IF bandpass filters were found to be the primary components hindering complete integration of radio receivers. Thus, discussion of receiver performance will be heavily weighted toward requirements that have a significant bearing on filter design. Throughout this chapter, a superheterodyne architecture will be assumed. This selection is reasonable since nearly all present day receivers use some variant of the superheterodyne approach, and because performance measures applicable to superheterodyne receivers are shared to a large degree by alternative receiver designs. The issue of alternative receiver architectures and their impact on filter design will be examined in detail in Chapter 4.

3.1 The Spectrum Environment

The useful radio frequency spectrum extends from ultra low frequencies in the neighborhood of 10 KHz to millimeter wave frequencies of 30 GHz and above. Within this spectrum, a large number of radio services exist, ranging from maritime, mobile, aeronautical, and satellite communications, to radio and television broadcast. Recently, commercial interest has focused on the use of VHF to L-band frequencies to provide personal, low power, point-to-point communications. Applications for this technology include radio paging, portable and cellular telephones, and a wide range of future personal communications services such as wireless local area networks.

These new systems reside in regions of spectrum previously allocated for other uses, and must cooperate with a variety of existing services, as illustrated in Figure 3.1. This problem is complicated by the fact that portable radio receivers typically employ omni-directional antennas and are therefore susceptable to signals arriving from any source emitting radio energy in their direction.

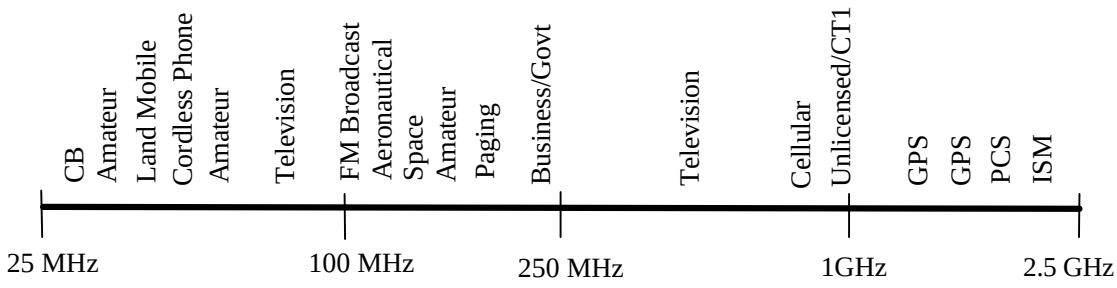

Figure 3.1: Frequency assignments in the VHF to L-band spectrum.

To illustrate some of the specific challenges involved in modern receiver design, Figure 3.2 shows a spectrum plot of signals present in the 80 - 180 MHz frequency band. This view was taken using a spectrum analyzer connected to a 12 inch dipole antenna at approximately

20 foot elevation in rural Blacksburg, Virginia. Signal densities in many metro areas are as much as an order of magnitude higher.

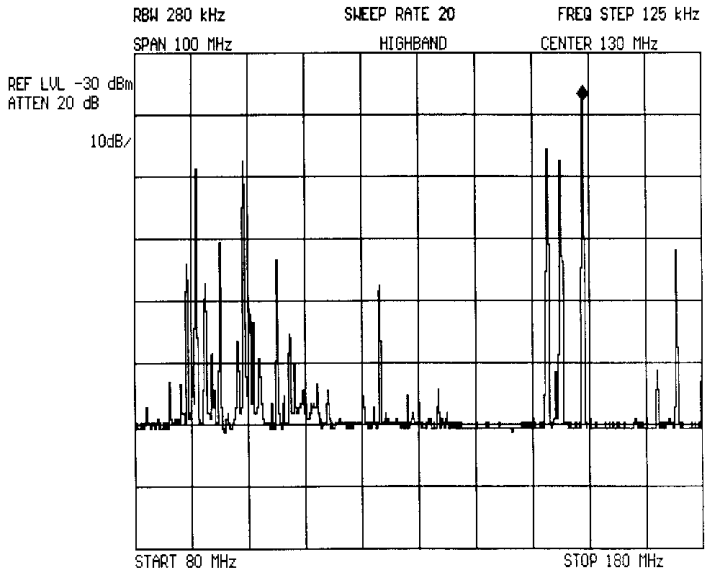

Figure 3.2: Radio frequency environment from 80 MHz to 180 MHz.

The cluster of signals to the left of center in Figure 3.2 is the FM broadcast band. Within this band, stations geographically close to the receiver appear at substantially higher amplitudes than those farther away. In the spectrum plot shown, signal level variations of 40 dB can be seen, whereas in some cases, variations of 80 dB or higher must be accommodated by the receiver hardware. In addition, up to 100 stations may exist at any one time within the FM broadcast service, each 200 KHz wide, and separated from other signals by as little as 200 KHz.[1] The same receiver must therefore select, amplify, and demodulate the desired signal in the presence of a wide range of interfering stations on nearby frequencies.

Finally, interference from neighboring services must be considered. This problem is best

[1]Where possible the Federal Communications Commission attempts to allocate station frequency assignments at 400 KHz intervals or greater to minimize adjacent channel interference problems. However, in large metro areas, stations can often be found spaced by the minimum 200 KHz interval.

illustrated by referring to the right side of Figure 3.2. The large signals in this portion of the spectrum are from pager service transmitters located approximately two miles from the receiver site. Frequencies just 15 MHz below these signals (at about 140 MHz) are allocated to other services, including weak signal satellite applications [9]. Signals in these services may originate from low-earth-orbit (LEO) satellites, and enter terrestrial handheld receivers at levels as low as -120 dBm (far below the spectrum analyzer's noise floor seen in Figure 3.2). This level is over 80 dB below that of the paging service signals located just 15 MHz away.

3.2 Commercial Wireless Services

In addition to challenges presented by the radio spectrum environment, receiver designs must take into account a wide range of system design parameters including operating frequency, signal bandwidth, and modulation type. These parameters can have a significant impact on the design of integrated receivers and are therefore reviewed in this section.

A sampling of wireless services within the VHF through L-band spectrum which can benefit from integrated, low power receiver technology is illustrated in Table 3.1. The first column in this table shows the type of service, while the remaining columns show the system parameters that define the physical layer of the communication link. The listed parameters are those that most directly affect requirements for integrated receiver and filter designs.

Column two indicates the frequency at which front-end preselect and image filters would be required to operate. The range of frequencies shown also defines the required preselect filter bandwidth, which varies from 1% to 20% of the RF center frequency depending on the service in question.[2] In cases where two ranges are shown, one range is for the base

[2]Preselect filters wider than the service band can be used, but will result in potential problems with out-of-band service interference. Preselect filters narrower than the service band are also possible, but must track the local oscillator as the receiver is tuned. This issue is investigated in Section 3 and in Chapter 4.

Table 3.1: Example wireless services and system parameters

Service	Band	Channel BW	Modulation	Duplex Method	Multiplex Method
Broadcast					
FM	88 - 108 MHz	200 KHz	FM w/DSB subcarrier	None	N/A
AM	0.54 - 1.7 MHz	10 KHz	AM	None	N/A
Land Mobile					
Public Safety	150 - 174 MHz	12.5 - 25 KHz	NBFM	TDD (Simplex)	FDM
Public Safety	450 - 512 MHz	12.5 - 25 KHz	NBFM	TDD (Simplex)	FDM
Paging					
POCSAG	150 - 174 MHz	12.5 - 25 KHz	FSK	None	FDM/TDM
Cordless Phone					
CT1	46.61 - 47 MHz 49.67 - 50.00 MHz	$<$ 20 KHz	FM	FDD	FDMA
CT1/900	900 - 928 MHz	Various	Spread Spectrum	Various	CDMA/FDMA
CT2	864.1 - 868.1 MHz	100 KHz	GMSK	TDD	FDMA
CT3/DCT900	864.1 - 868.1 MHz	1 MHz	MSK	TDD	FDMA/TDMA
Cellular Phone					
AMPS	869 - 894 MHz 825 - 849 MHz	30 KHz	FM	FDD	FDMA
IS54	869 - 894 MHz 825 - 849 MHz	30 KHz	DQPSK	FDD	FDMA/TDMA
IS95	869 - 894 MHz 825 - 849 MHz	$\leq$1.7 MHz	Spread Spectrum	FDD	CDMA
PDC/JDC	810 - 826 MHz 940 - 956 MHz	25 KHz	DQPSK	FDD	FDMA/TDMA
GSM	890 - 915 MHz 935 - 960 MHz	200 KHz	GMSK	FDD	FDMA/TDMA
DCS1800	1710 - 1785 MHz 1805 - 1880 MHz	200 KHz	GMSK	FDD	FDMA/TDMA
PCS					
DECT	1882 - 1897 MHz	1.728 MHz	GMSK	TDD	FDMA/TDMA
PHP/PHS	1895 - 1918 MHz	300 KHz	DQPSK	TDD	FDMA/TDMA
Satellite					
ORBcomm	137 - 138 MHz	$\leq$9 KHz	PSK	TDD	FDMA/TDMA

to portable link, while the other is for the portable to base link. These systems employ full duplex (simultaneous transmission and reception), and typically must share a single antenna between the receiver and the transmitter through the use of duplex filters.

The third column provides a rough indication of the bandwidth that the final IF filter in the receiver is required to have. In addition, this parameter, combined with the RF frequency gives an indication of the accuracy required in the receiver's local oscillator. For example, systems such as AMPS cellular have very stringent requirements on frequency accuracy due to the use of a 30 KHz bandwidth when operating at an RF frequency of 900 MHz, whereas systems such as DECT and IS95 have more relaxed requirements due to the use of bandwidths in the MHz range.

The fourth column specifies the modulation method used. Besides determining the demodulator type, this feature influences the manner in which signal level variations are handled. For example, AM and DQPSK may require automatic gain control (AGC), whereas FM, FSK, and MSK/GMSK modulations can be decoded with a simpler limiting IF amplifier receiver design.

Column five specifies the duplex method used. In a frequency-division duplex (FDD) system, a duplex filter is needed to simultaneously use the antenna for transmit and receive. This is an important issue for integration of radio hardware since duplex filters must handle substantial tranmitted power and therefore may not permit the use of active filter technology. The alternative time-division duplex (TDD) approach requires only an RF switch, and therefore is more integration friendly.

Finally, column six specifies the multiplex method used. This aspect of the system architecture has important implications for filter tuning approaches discussed in Chapter 7. Systems which employ some form of time division multiplexing (TDM) may allow filters to be taken off-line during timeslots that are not of interest to the receiver, allowing simplified tuning approaches to be developed.

3.3 Receiver Performance

The fundamental tasks a receiver is required to perform include:

- selection of a desired signal from a potentially dense spectral environment;
- amplification of the signal to a level suitable for demodulation; and
- demodulation of the signal to recover the transmitted information.

The ability of the receiver to carry out these tasks is typically quantified through a set of performance measures which fall into the following general categories:

- Sensitivity;
- Dynamic Range;
- Selectivity; and
- Fidelity.

These performance measures are examined in depth in the following sections and will play a central role in the assessment of proposed techniques for integrated receiver design throughout this dissertation.

3.3.1 Sensitivity

The sensitivity of a receiver is a measure of its ability to amplify and demodulate weak signals. Sensitivity is often expressed in terms of the minimum signal level at the antenna which produces some acceptable level of fidelity in the demodulator output. This measure of

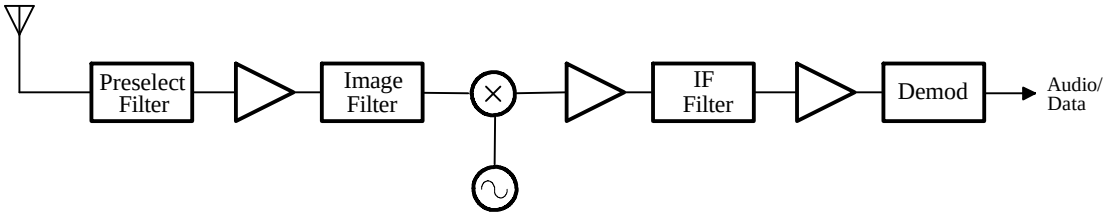

Figure 3.3: Superheterodyne receiver architecture.

sensitivity depends on the particular signaling method and demodulator design employed, as well as on the receiver's RF and IF circuits. This dissertation, however, is primarily concerned with the development of techniques for integrating filters, since circuits for amplifiers and demodulators are well established. Hence, a measure of sensitivity independent of the signaling method and receiver demodulator implementation is more appropriate. For this reason, receiver noise figure will be the primary measure of sensitivity used.

The noise figure F of an arbitrary system can be defined as:

$$F = \frac{S_i/N_i}{S_o/N_o} \tag{3.1}$$

where S and N represent signal and noise powers and the subscripts i and o represent the input and output of the system in question. For radio receivers, these locations are typically defined as the antenna port and the demodulator input, respectively.

The importance of noise figure in the design of integrated bandpass filters can be understood by referring to the receiver shown previously in Figure 3.3. In theory, it may be possible to replace the preselect filter, low noise amplifier (LNA), and image filter in this design with a single fully integrated active filter. If such a replacement is made however, the noise figure

of the filter must compare favorably with the circuit blocks it replaces to avoid degrading the overall receiver sensitivity. For typical receivers with omni-directional antennas, this places a requirement of 3 to 15 dB on the filter implementation, depending on the system in which the receiver is used.

For the case of integrated IF filters, the noise figure requirements are relaxed. Here, the impact of the filter's noise figure on that of the overall receiver is reduced by the gain in the receiver's front-end. To quantify this statement, recall that the overall receiver noise figure F can be related to the noise figure of individual portions of the receiver by [172]:

$$F = F_1 + \frac{F_2 - 1}{G_1} \tag{3.2}$$

where F_1 and G_1 represent the noise figure and gain of the front-end receiver circuits preceding the IF filter, respectively, and F_2 is the noise figure of the filter itself. Thus, given a noise figure for the front-end and a maximum acceptable noise figure for the overall receiver, the maximum allowed noise figure for the filter can be found from the relation:

$$F_2 = \left(\frac{F}{F_1} - 1\right) G_1 F_1 + 1 \tag{3.3}$$

For a typical receiver design, the gain G_1 used is based on tradeoffs between noise figure and dynamic range performance, and lies in the range of 10 to 10,000 (10 to 40 dB). Assuming that the allowed degradation in receiver noise figure from the filter is 3 dB ($\frac{F}{F_1} = 2$), then the above expression can be simplified to:

$$F_2 \approx G_1 F_1 \tag{3.4}$$

Expressed in dB, this equation states that the noise figure of the filter should be the sum of the receiver's front-end gain and noise figure. Thus, for a receiver with a 3 dB front-end

noise figure, a 30 dB front-end gain, and an overall noise figure target of 6 dB for the receiver as a whole, the noise figure of the filter should be 33 dB.

While a lower noise figure in the filter will decrease the impact on the receiver as a whole, care must be taken to avoid lowering the filter's already limited dynamic range. For example, analysis of Equation (3.3) indicates that the degradation in the above example can be lowered to 1 dB by cutting the filter noise figure to 27 dB. However, this will cause a loss of 6 dB to the effective dynamic range of the filter.

3.3.2 Dynamic Range

In Section 3.1, it was shown that receivers may be required to cope with signal level variations of up to 80 dB or more in some applications. The lowest signal level that can be received is determined by the thermal noise floor in the environment together with the receiver's noise figure, while the highest signal allowed is a function of saturation and distortion effects in the receiver's active circuits. In a traditional receiver, this overall dynamic range is limited by the performance of amplifiers and/or mixers. In a receiver employing active bandpass filters, the filters' dynamic range may become the limiting factor.

In the published literature, the dynamic range of active filters is generally quoted as a simple ratio of maximum in-band signal level to the total in-band filter noise. In receiver design, however, several different definitions of dynamic range exist, and the most important dynamic range measures are those that deal with interfering signals *outside* the signal passband. Thus, a more complete specification of filter dynamic range performance is needed.

In the subsections which follow, each of the three main definitions of receiver dynamic range (total, blocking, and spurious-free) are reviewed, and the implications of these performance parameters for the design of integrated bandpass filters are discussed. Detailed relationships between the definitions presented below and the classic definition of filter dynamic range

will be undertaken in Chapter 6.

Total Dynamic Range

The total dynamic range of a receiver DR_{tot} may be defined (in dB) as

$$DR_{tot} \equiv P_{max} - P_{min} \tag{3.5}$$

where P_{max} is the power above which unacceptable distortion in the demodulated signal occurs, and P_{min} is the minimum usable input signal power for satisfactory reception. Typical values of DR_{tot} found in modern receivers range from 40 dB to well over 80 dB depending on the type of radio service in which the receiver is used, and on the power consumption and cost of the receiver hardware.

The value of DR_{tot} *required* in a receiver depends primarily on how close the receiver is allowed to come to the transmitter and on how large the effective radiated power is at the transmitter site. For FM broadcast receivers, the ratio of maximum to minimum power encountered can reach 100 dB or more under worst case conditions, while for satellite ground station receivers, values as low as 20 dB may be found. The value quoted for the FM broadcast case is based on receiver design data published in references [43] and [48], while the value for satellite reception is easily derived from the carrier to noise ratios required at the demodulator input (e.g. 13 dB) added to a typical link margin of 7 dB [179].

For the important case of cellular telephone receivers, extensive studies of signal levels versus distance from base station transmitters have been performed, and dynamic range requirements can be derived directly from propagation and transmitter power considerations. The following analysis is based on information in reference [11] and illustrates some of the factors involved.

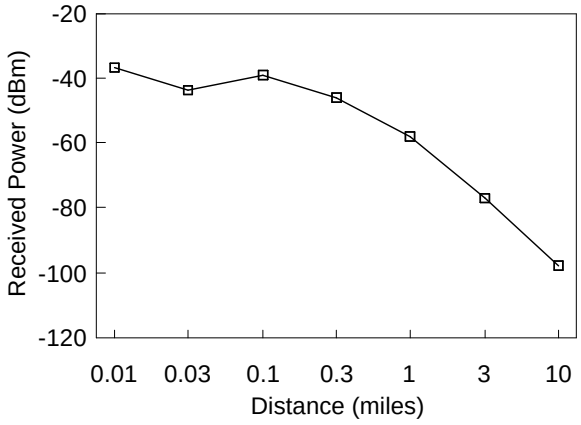

Figure 3.4: Received signal levels versus distance from transmitter.

Figure 3.4 shows a typical cellular radio system signal level profile plotted for transmitter to receiver separations R of 0.01 miles (53 ft) to 10 miles. This plot was constructed based on a transmitter antenna with a directivity gain $G_t = 4$ (6 dB), mounted at a height of 30 m (100 ft), and driven with a power level (per user) of $P_t = 10$ watts. Based on this power and directivity, the power density P in the region between 0.1 and 1 miles can be estimated as [11]:

$$P \approx \frac{P_t G_t}{4\pi R^{2.4}} \tag{3.6}$$

and the received power P_r can then be found from:

$$P_r = P A_e \approx P \frac{\lambda^2}{4\pi} \tag{3.7}$$

where A_e is the effective aperture of the receiving antenna, λ is the free-space wavelength at the operating frequency, and a propagation constant of 24 dB per decade (close to that of free-space) has been assumed. At larger distances from the transmitter (i.e. $>$ 1 mile), the signal falls at a faster rate of approximately 40 dB per decade due to ground reflection

and shadowing considerations, while at very close distances (< 0.1 miles), the signal falls below the 24 dB per decade asymptote predicted by Equations (3.6) and (3.7) due to large elevation angles which place the angle to the receiver outside the main lobe of the transmit antenna [11]. Finally, given the overall signal level variation of 60 dB seen in this plot, a total dynamic range requirement of approximately 90 dB can be derived by adding a variance of 20 dB to account for multipath fading, and a bias of 10 dB to provide an adequate carrier-to-noise level at the receiver's demodulator input.

In order to translate these requirements to requirements on active filters used within a receiver, additional factors must be taken into account. For example, in systems employing modulation such as AM or PSK, automatic gain control (AGC) amplifiers are often used within the receiver to normalize the signal level presented to the demodulator circuits. Since the AGC is typically placed before the IF channel selection filters, the total dynamic range requirement on an active IF filter can be significantly smaller than that of the overall receiver. Similar considerations also apply to the RF preselect filter when switchable attenuators are used at the antenna input port.

For example, an IF filter with a 50 dB total dynamic range can be used in a receiver system with a 60 dB AGC and still meet a total dynamic range requirement exceeding 100 dB. Meeting a more relaxed 80 dB requirement can be achieved with a single 30 dB step attenuator placed at any location ahead of the filter, while meeting the total dynamic range requirement in the satellite receiver would require no AGC or attenuator at all.

Blocking Dynamic Range

The most difficult dynamic range requirements in any receiver design are those which deal not with signal variations in the desired signal, but rather with the reception of a weak desired signal in the presence of one or more large interfering signals *outside* the desired signal channel. Such signals may reside in other channels of the service band, or in other

portions of the radio spectrum.

Under the condition that the desired signal is weak (e.g. near the noise floor), the full sensitivity, and hence, the full gain of the receiver may be required. Thus, AGC and attenuator circuits, if present, are not active and large interfering signals will be amplified to very high levels, resulting in saturation of circuits and reduction of receiver gain. If the gain is reduced to the point that the desired signal is no longer received, the signal is said to be "blocked". Thus, the blocking dynamic range (BDR) of a receiver can be estimated[3] (in dB) as:

$$BDR \approx P_{1dB} - P_{min} \tag{3.8}$$

where P_{1dB} is the power of an interfering signal at the antenna that results in 1 dB gain compression and P_{min} is the minimum usable signal power defined earlier.

The BDR value *required* in a receiver depends on the environment in which the receiver operates, and ideally can be found based on considerations similar to those discussed in the preceding section. However, the problem is complicated here by the presence of a large and variable number of potential interferers, and the existence and physical proximity of transmitters in other service bands which may be difficult to fully characterize. Thus, an alternative method of establishing requirements is preferable.

One useful method is to benchmark the performance of existing receivers. In fact, the allocation of frequencies and the design of wireless services are typically based on this approach [4] [7] [14]. An alternative approach is to study the theoretical and practical limits to performance through an analysis of receiver design techniques. Both of these

[3]This approximation assumes that noise measured at the system output is not subject to compression. An exact analysis of the densitization problem requires a detailed characterization of circuit non-linearities, noise mixing processes, and the system in which the circuits are used [176]. However, the given expression is approximately valid for many situations and produces acceptable results for this discussion.

methods are considered in the following discussion.

The BDR of a receiver is a function of several parameters, including:

- the 1 dB compression point and noise figure of individual active circuits preceding the IF channel select filter,
- the gain distribution preceding the IF channel select filter, and
- the frequency offset of the interfering signal causing blocking.

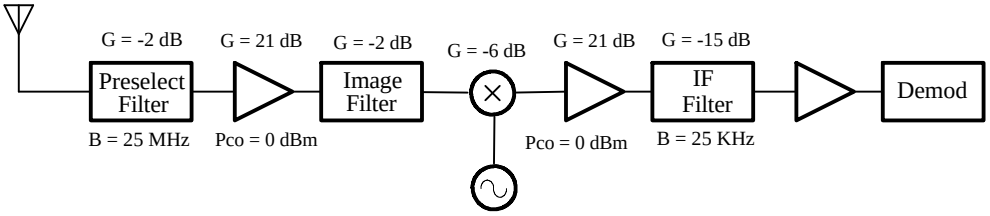

Figure 3.5: Representative receiver hardware design.

To observe the effects of these parameters on dynamic range performance, consider the low-power receiver design shown in Figure 3.5, in which two amplifiers, two passive filters, and one passive mixer precede the IF channel select filter. Each amplifier is assumed to have a compression point referred to its output P_{co} of 0 dBm, and a power gain of 21 dB. The compression point for the receiver as a whole can then be found from the IF amplifier output compression point minus the net gain preceding it, giving:

$$P_{1_{dB}} = P_{co} - G \tag{3.9}$$

or -32 dBm. To find the blocking dynamic range from Equation (3.9), the receiver noise floor P_{min} must also be known. This power may be found (in dBm) from the relation:

$$P_{min} = 10log(kT_aB) + NF + C/N_{min} + 30 \tag{3.10}$$

where k is Boltzmann's constant, T_a is the antenna noise temperature, B is the signal or IF bandwidth, NF is the receiver noise figure, and C/N_{min} is the minimum required carrier to noise ratio needed at the demodulator input. (The final factor of 30 dB converts the power in dBW to dBm.) Assuming an antenna noise temperature of 290 K, a bandwidth of 30 KHz, a noise figure of 6 dB, and a minimum carrier to noise ratio of 10 dB, P_{min} found from Equation (3.10) is -113 dBm. Hence, the blocking dynamic range for this receiver is $BDR \approx -32 - (-113) = 81$ dB.

This value of BDR will hold for any interfering signal within the 20 MHz passband defined by the preselect and image filters, since the receiver amplifies and translates all signals within this bandwidth to IF. Outside this service band, BDR will generally be higher due to attenuation of interfering signals by preselect and image filters.

The in-band BDR of this design can be improved either through an increase in the IF amplifier compression point, or by lowering the gain ahead of the IF filter. However, both options come at a price. Raising P_{co} of the amplifiers employed will generally require a circuit design which consumes more power, and therefore may be an unacceptable option for portable receiver operation. Alternatively, lowering the gain will increase the receiver's noise figure, with diminishing returns on dynamic range performance, and possibly unacceptable lowering of the receiver's sensitivity. Thus, the art of receiver design includes trade-offs between noise figure and dynamic range performance. Moreover, these observations demonstrate that there are practical as well as theoretical upper bounds on the dynamic range that can be achieved within a receiver design at a given power consumption and a specified bandwidth.

To validate these statements, Table 3.2 shows the measured dynamic range of three representative commercial receivers [52] [118] [111]. Since the bandwidth of the receivers affects the value of P_{min}, and hence BDR, dynamic range values are shown normalized to a constant 25 KHz bandwidth in the third column. The BDR performance of the paging receiver is in good agreement with the example receiver calculation above. In the other two cases, BDR is larger due to the higher power consumptions typically used in mobile and base station receiver designs. Amplifiers and mixers in these radios often operate at power consumptions as high as 1 W, making output compression points up to +20 dBm possible. In addition, the higher cost and larger size of these units may permit the use of lower loss filters and hence, lower front-end gain.

Table 3.2: Example BDR performance.

Receiver Type	BDR / BW	BDR in 25 KHz BW
VHF Pager	$\leq$ 82 dB / 20 KHz	$\leq$ 83 dB
VHF Mobile	108 dB / 2.4 KHz	98 dB
HF Base	115 dB / 2.4 KHz	105 dB

The implications of this discussion for the design of integrated receivers and active filters are significant. Receiver BDR performance is seen to be dependent on power consumption, bandwidth, and gain of circuits preceding the IF filter. Similarly, in Chapter 2, the dynamic range of active filters was found to depend on power consumption, bandwidth, and filter Q. Thus, active filters may offer acceptable dynamic range performance in receiver applications despite their inherent dynamic range limitations if the filter Q is limited to moderate values. These factors will be examined in detail in Chapter 6 after expressions for the dynamic range of active filters have been derived.

BDR at Frequency Offsets In classic superheterodyne receiver architectures, BDR is relatively constant for any interfering signals within the service band, but increases for

out-of-band signals due to the attenuation offered by the receiver's preselect filter. For integrated active filters, however, BDR may or may not be constant with frequency. In fact, it will be shown in Chapter 6 that the BDR of appropriately designed filters increases at a rate of 6 dB per octave outside the filter passband. In general, this may be less than the improvement offered by passive filters, which may use a multipole design.

Thus, a receiver with an integrated active preselect filter may not be able to meet the performance of existing receivers and it becomes necessary to investigate how much BDR is actually required. This is a complex issue since it depends on the entire RF spectrum the receiver will encounter during use. Factors such as how close the receiver may come to transmitter installations in other services, what effective aperture and impedance level the receiver's antenna presents at the interfering signal's operating frequency, and what the active preselect filter's input impedance is at this frequency will all play a role in making this decision, and should be carefully assessed before committing to a fully integrated preselect filter design.

Spurious-Free Dynamic Range

In addition to the blocking problems discussed in the preceding section, strong interfering signals may generate spurious signals within the receiver's front-end circuits. These signals, which are products of non-linear intermodulation distortion in active circuits, may interfere with the reception of a desired signal in certain situations. A measure of the receiver's immunity to this problem is the receiver's spurious-free dynamic range (SFDR) discussed in this section.

Nonlinearities responsible for spurious signal generation within a receiver are the same as those responsible for blocking. However, since the mechanism involved is more complex than that of simple gain compression, some review of concepts and notation is needed before proceeding further.

To understand the production of spurious signals within a receiver, consider a system h (such as a small signal amplifier) with input x_i and output x_o as illustrated in Figure 3.6. For simplicity, we will assume that h is memoryless, so that the time dependence of x_i and x_o may be ignored in determining the system's nonlinear behavior. For notational convenience, we will further assume that DC bias in the input is removed.

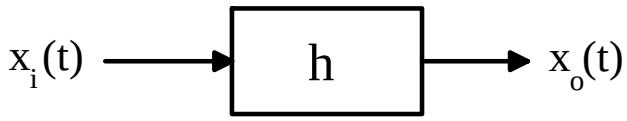

Figure 3.6: Simple nonlinear system model.

If the input x_i to this system is sufficiently small, then a simple Taylor series may be used to provide an approximation of x_o of the following form:

$$x_o \approx h(0) + \frac{\partial h}{\partial x_i} x_i + \frac{1}{2!} \frac{\partial^2 h}{\partial x_i^2} x_i^2 + \frac{1}{3!} \frac{\partial^3 h}{\partial x_i^3} x_i^3 + ... \tag{3.11}$$

or

$$x_o \approx a_0 + a_1 x_i + a_2 x_i^2 + a_3 x_i^3 + ... \tag{3.12}$$

Intermodulation distortion is produced when two or more signals at different frequencies are present at the system input. Following established convention, consider the case of two sinusoidal signals, at frequencies ω_1 and ω_2, where ω_1 and ω_2 are "closely spaced". That is, where $|\omega_1 - \omega_2| \ll |\omega_1 + \omega_2|$, and:

$$x_i(t) = V_1 cos(\omega_1 t) + V_2 cos(\omega_2 t) \tag{3.13}$$

Inserting Equation (3.13) into Equation (3.12), expanding, and collecting terms, $x_o(t)$ may then be written in the form:

$$\begin{aligned} x_o(t) &= a_0 + a_2\left(\frac{V_1^2}{2} + \frac{V_2^2}{2}\right) \\ &\quad + \left[a_1 V_1 + a_3\left(\frac{3V_1^3}{4} + \frac{2V_1^2 V_2}{4}\right)\right] cos(\omega_1 t) + \left[a_1 V_2 + a_3\left(\frac{3V_2^3}{4} + \frac{2V_2^2 V_1}{4}\right)\right] cos(\omega_2 t) \\ &\quad + a_3\left(\frac{V_1^2 V_2}{4} cos((2\omega_1 - \omega_2)t) + \frac{V_2^2 V_1}{4} cos((2\omega_2 - \omega_1)t)\right) \\ &\quad + ... \end{aligned} \tag{3.14}$$

The first two terms of this result comprise the DC output of the system plus a DC offset which depends on the second-order (quadratic) non-linearity and the input signal amplitudes. In general, this DC shift is unimportant and can be ignored. The next two terms contain the desired output plus additional responses that account for the gain compression. This gain compression behavior is responsible for determining the blocking dynamic range. Finally, the last term contains the intermodulation products of interest in the following discussion. Additional terms such as harmonics of the input frequencies are also produced, but are not shown since they can be easily removed by filtering.

The importance of the intermodulation products can be understood by assuming that ω_1 and ω_2 are frequencies located one and two channel spacings above the frequency ω_o to which the receiver in Figure 3.7 is tuned.[4] Under this condition, the intermodulation product frequency $(2\omega_1 - \omega_2)$ falls exactly at ω_o. Thus, two strong interferers at ω_1 and ω_2 passing through the receiver's amplifier and mixer circuits produce a spurious signal that falls within the receiver's passband and cannot be removed by any form of filtering. If the spurious product is of sufficient amplitude, it may dominate the desired signal and prevent

[4]This choice of frequencies is far from unique. Many other channel spacings will produce the effects described, especially when more than two signals are considered.

successful reception. Alternatively, if no desired signal is currently present, the spurious product may be falsely interpreted by the receiver as a valid signal. Whether or not either of these conditions occur will depend on the amplitudes V_1 and V_2 of the interferers and on the nonlinearity term a_3.

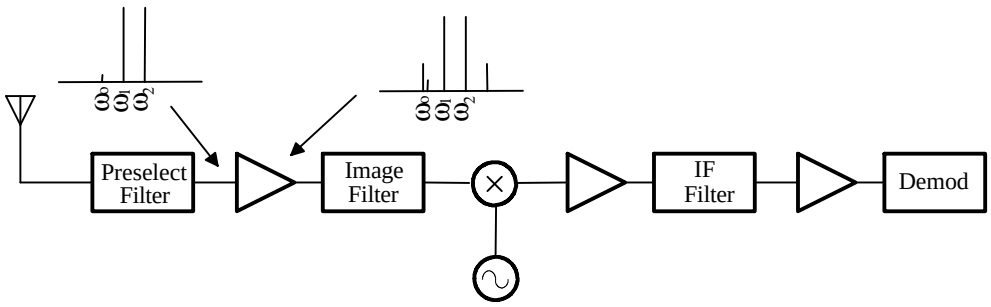

Figure 3.7: Intermodulation products within a receiver front-end.

For simplicity, assume that $V_1 = V_2 = V_i$. Then, the amplitudes of each of the expected outputs at ω_1 and ω_2 from the interferers due to the gain coefficient a_1 of the system (ignoring gain compression effects) is:

$$V_{o_1} = a_1 V_i \tag{3.15}$$

and the amplitudes of the intermodulation product resulting from the a_3 term in the nonlinearity expansion is of the form:

$$V_{o_3} = a_3 \frac{V_i^3}{4} \tag{3.16}$$

If the input and output impedances of the circuit are specified, these relationships can be written more simply in terms of power in dB as:

$$P_{o_1} = P_i + G \tag{3.17}$$

and

$$P_{o_3} = 3P_i + constant \tag{3.18}$$

where P_i is the input power, G is the small signal power gain, and P_{o_1} and P_{o_3} are the output power of the first-order (expected) and third-order (spurious) signals, respectively. These expressions are plotted in Figure 3.8 together with the effects of gain compression and higher-order terms of the series expansion not considered above. This figure provides a convenient illustration of the important performance parameters related to receiver dynamic range, including [112]:

G	The small signal amplifier gain
P_{c_i}	The gain compression point referred to the input
P_{c_o}	The gain compression point referred to the output
IIP_3	The third-order intercept point referred to the input
OIP_3	The third-order intercept point referred to the output
MDS	The minimum discernible signal, (noise floor referred to the input), and
P_{i3}	The input power at which intermodulation products rise above the noise floor.

If the circuit noise floor (in some specified bandwidth) is known, both the blocking dynamic range and the spurious-free dynamic range can be found in terms of these parameters through relatively straightforward graphical constructions.

In Figure 3.8, the noise floor referred to the output is represented by the upper border of

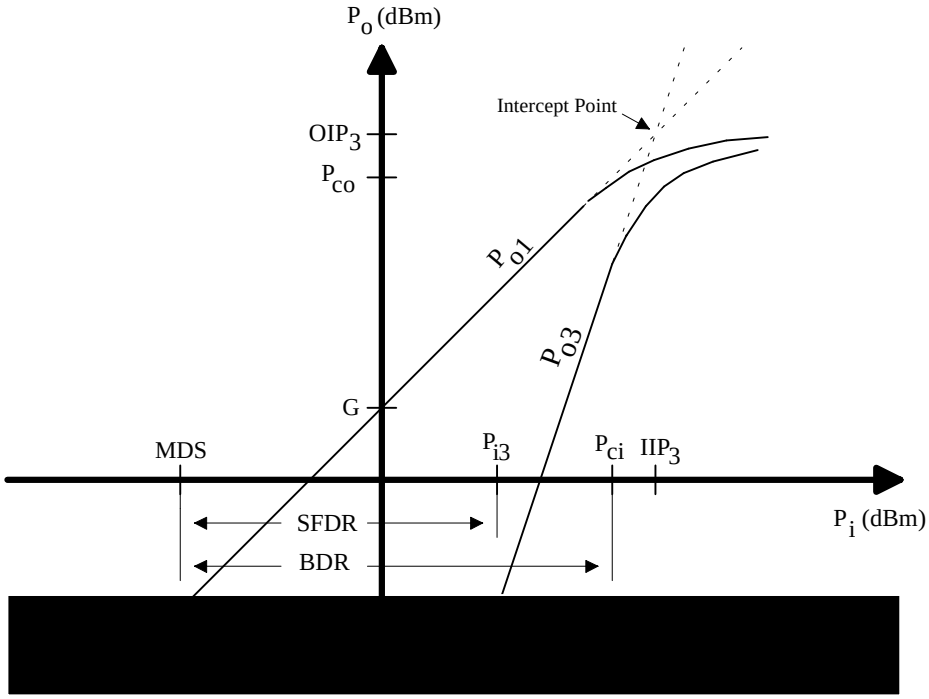

Figure 3.8: Graphical determination of dynamic range.

the shaded region. The MDS or noise floor referred to the input is then found as the input power at which the P_{o1} curve hits the noise floor, and the blocking dynamic range can be found as the distance between this point and the 1 dB compression point P_{ci} as shown below the x axis, giving:

$$BDR = P_{c_i} - MDS \tag{3.19}$$

The spurious free dynamic range (SFDR) is defined as the input power P_{i3} above which third-order intermodulation products rise above the noise floor, divided by the MDS. Expressed in dB, the SFDR is of the form:

$$SFDR = P_{i_3} - MDS \tag{3.20}$$

The power P_{i_3} can be found in terms of the third-order input intercept point IIP_3 and MDS through simple geometric considerations. Based on the slopes shown in Figure 3.8, for the P_{o_1} and P_{o_3} curves, P_{i_3} is given by:

$$P_{i_3} = IIP_3 - \frac{1}{3}(IIP_3 - MDS) \tag{3.21}$$

Combining this result with equation (3.20), the following expression for SFDR results.

$$SFDR = \frac{2}{3}(IIP_3 - MDS) \tag{3.22}$$

Thus, from equations (3.19) and (3.22), both the BDR and SFDR figures of merit can be found, provided the 1 dB compression point and third-order intercept points are known. These quantities are often specified by manufacturers or measured for new designs. In

[119], it is suggested that these two points may also be found in terms of each other. This conclusion is based on empirical evidence showing that IIP_3 and P_{c_i} can be related by:

$$IIP_3 = P_{c_i} + \Delta \tag{3.23}$$

where Δ lies in the range of 5 to 15 dB, depending on details of circuit implementation. In [176], Meyer and Wong have subsequently noted that a Δ value of 9 dB can be derived directly from Equation (3.14) if the Taylor series expansion is truncated after the cubic term. Combining Equations (3.19), (3.22), and (3.23), and using $\Delta = 9$ dB, yields:

$$SFDR \approx \frac{2}{3}(BDR + 9) \tag{3.24}$$

Based on Equation (3.24), all of the conclusions concerning BDR performance of receivers arrived at in the preceding section are seen to apply to SFDR performance as well. In particular:

- There are upper bounds on the spurious-free dynamic range that a receiver can achieve. As in the case of BDR, these limits depend on the power consumption of the active circuits employed and on the gain preceding the IF channel select filter.
- Increasing the receiver's SFDR performance requires either an increase in amplifier compression points, which requires higher power consumption, or a reduction in gain, which sacrifices the overall noise figure, raising the receiver's noise floor together with the the input compression point and produces diminishing results.
- The SFDR of a superheterodyne receiver is relatively constant within the passband defined by the preselect filter, and increases outside this passband by an amount determined by the attenuation characteristic of upstream filters.

SFDR requirements for signals which fall within the preselect filter's passband can be established either through an analysis of receiver hardware, or through benchmark measurements in commercial receivers. For the case of the receiver design shown previously in Figure 3.5, for which a BDR estimate of 81 dB was found, Equation (3.24) yields a SFDR of 60 dB. This value agrees well with values assumed by studies such as those used in the Federal Aviation Administration's software model used to allocate operating frequencies [14].

As an additional validation of the theory, measured results cited in [113] [114] are given in Table 3.3. These data values, taken from Amateur Radio receivers operating in the 144 - 148 MHz service band, are for FM receivers operating with a bandwidth of 12.5 KHz. Values shown in the table have been normalized to a 25 KHz bandwidth by subtracting 2 dB from the reported values.

Table 3.3: Example SFDR performance.

Receiver Type	In-Band SFDR	SFDR at 10 MHz Offset
Mobile	67 dB	84 dB
Mobile	68 dB	94 dB
Mobile	71 dB	85 dB
Handheld	58 dB	76 dB
Handheld	60 dB	83 dB
Handheld	64 dB	74 dB

As in the case of BDR measurements, mobile receivers, which consume higher powers than handheld units, generally provide the highest performance. For handheld units, the SFDR typically falls in the range of 60 - 65 dB (for 25 KHz bandwidth), validating the general conclusions above.

Out-of-band SFDR measurements are also shown in the table for a 10 MHz offset from the center of the service band giving an indication of the level of performance that may be acceptable. These values were measured with the receiver tuned to 146 MHz and interferers placed at 156 MHz and 166 MHz to simulate the effects of large adjacent service band paging

signals. As expected, the values are higher than the in-band measurements. However, the improvement shown is suggestive of only a 1-pole to 2-pole roll-off in the receiver's preselect filter. Hence, the concerns raised in the preceding section relative to using active filters in preselect applications may not represent a serious problem.

3.3.3 Selectivity

The selectivity of a receiver is a measure of its ability to amplify and demodulate signals at a desired frequency while rejecting signals at other frequencies in the environment. While the blocking and intermodulation characteristics of receivers discussed in the previous section can limit the selectivity obtainable, selectivity is primarily a function of IF channel select filter design.

For the classic superheterodyne architecture, which provides the basis for most modern receiver designs, primary measures of receiver selectivity include:

- adjacent/alternate channel selectivity;
- image rejection; and
- spurious response rejection.

Adjacent and Alternate Channel Selectivity

To determine channel selectivity requirements of a receiver, the distinction between adjacent and alternate channels must first be understood. The term "adjacent channel selectivity" is often used in the literature to refer to any channel in the receiver's service band which is near the channel being received. In this dissertation, however, a more precise definition will be assumed in which an adjacent channel is either the channel immediately above or

immediately below the one to which the receiver is tuned. The term "alternate channel" will then be used to refer to signals either *two* channels above or below the channel tuned. Channels at larger distances will not be specifically referenced.

For practical as well as economic reasons, radio system designers often specify that two signals in the same geographic area may not reside in adjacent channels. This system constraint, which has been adopted by broadcast services and by first generation cellular services, relaxes performance demands on both receiver IF filtering and on transmitter spectral purity. An alternative approach that achieves the same result is to constrain the signal bandwidth to some fraction of the channel spacing so that "guard bands" occur on either side of the transmitted signal. In systems employing this method of spectrum management, signals within the same geographic area may be assigned to adjacent channels, but the spectrum utilization remains comparable to that above due to decreased usage of the channel bandwidth. A third option is to rely on the fact that the spectral energy in a transmitted signal employing certain types of modulation and program material is statistically concentrated at the channel center, so that guard bands are implicitly present. In the discussions below, this third case will be treated as equivalent to the second in which guard bands are explicitly defined.

These issues are illustrated in Figure 3.9 in which the attenuation of an IF channel select filter versus frequency offset from the filter center is plotted. For the case where guard bands are not used, the filter bandwidth is generally equal to the channel spacing as shown by the lower attenuation curve. Assuming a Butterworth-type filter rolloff[5], the mean attenuation of this filter and hence the approximate receiver selectivity at adjacent and alternate channels is:

[5]The rolloff of other all-pole filter types commonly used in receivers is similar. Somewhat higher attenuations can be obtained in Chebyshev designs or in filters employing zeros to produce elliptic responses. However, the phase and group delay characteristics of these filters often prevent their use in receiver IF applications.

$$ATTN_{AdjCh} = 6N \quad dB \tag{3.25}$$

$$ATTN_{AltCh} = 12N \quad dB \tag{3.26}$$

where N is the number of filter poles.[6]

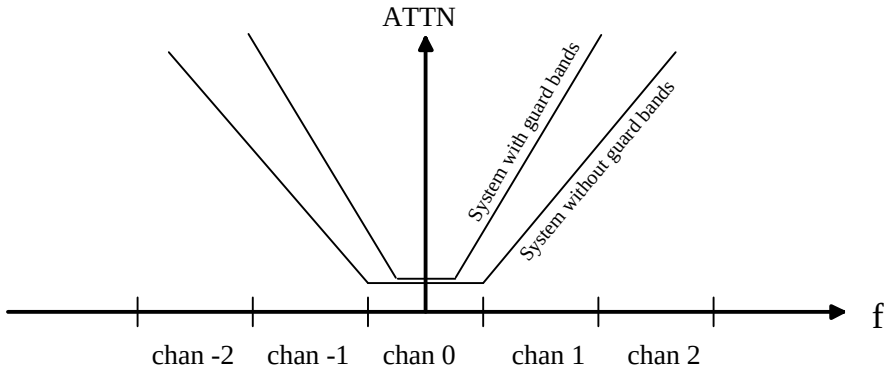

Figure 3.9: IF channel select filter attenuation versus frequency.

Equation (3.25) implies that a selectivity of 50 dB to adjacent channel signals would require a filter with at least 8 poles. In fact, significantly more than 8 poles would be needed if the adjacent channel signal energy is evenly spread across the channel bandwidth. In contrast, 50 dB *alternate* channel selectivity requires a filter with a more realistic complement of 4 to 5 poles.

For the case where guard bands are present in the system architecture (either explicitly or implicitly), the IF filter bandwidth can be reduced as illustrated. This allows good selectivity in adjacent channels to be achieved with a similar number of poles as that in the case without guard bands above.

[6]Following established convention for bandpass filter designs, an N-pole filter is defined here as one of order 2N. That is, the number of poles refers to the order of an equivalent lowpass prototype filter from which the bandpass filter can be derived.

Requirements for the number of poles used in receivers incorporating on-chip IF channel select filters can be determined through the considerations discussed above if specifications for adjacent or alternate channel selectivity are given. For example, the AMPS cellular phone discussed in Chapter 2 lists specifications of > 16 dB adjacent channel selectivity and > 65 dB alternate channel selectivity, implying a requirement of 5 to 6 poles. Alternatively, filter requirements may be determined directly by examining the hardware design of existing products. Examples of filter complements for several radio receiver designs are summarized in Table 3.4 indicating that 4 pole filtering is acceptable in many applications, while 6 pole designs may be found in more expensive products and in more demanding applications.

Table 3.4: Example IF filter complements.

Receiver Type	Filter Poles
Portable FM Broadcast	2 - 4
Hi-Fi FM Broadcast	4 - 6
Cordless Phone	4
DECT	3 - 4 (SAW)
FM Cellular	6

Image Rejection

The image rejection of a receiver is the attenuation offered by the receiver's preselect and image filters to signals residing at the image frequency f_{im}. The frequency f_{im} is a function of the IF frequency f_{IF} used, and can be found from:

$$f_{im} = f_{RF} \pm 2f_{IF} \tag{3.27}$$

depending on whether the LO operates above or below the RF frequency.

The image rejection offered by a preselect filter in a given receiver design can be found

by examining Figure 3.10. The attenuation curve of a preselect filter with bandwidth B is shown under conditions where the receiver is tuned to the center of the filter passband and to the band edge. The former case is applicable to tracking preselect filters, whereas the latter yields worst-case image rejection for the more common case of receivers with fixed-tuned preselect designs.

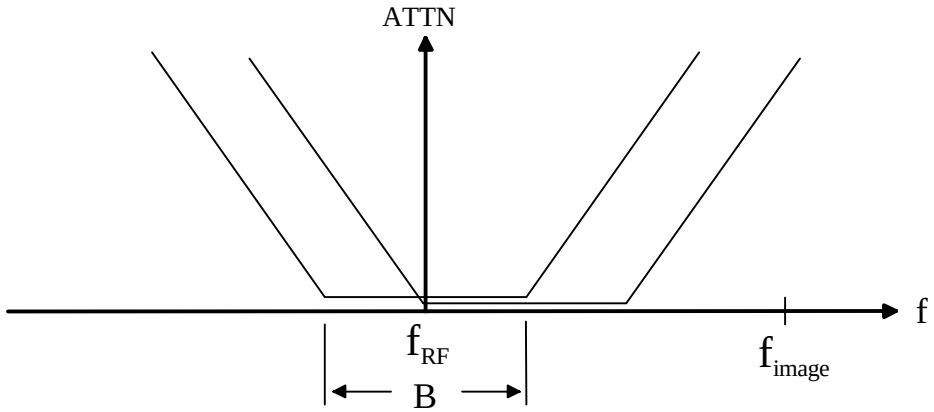

Figure 3.10: Preselect filter attenuation versus frequency.

From these attenuation curves, the image rejection offered by an N-pole filter design to a signal at the image frequency can be found from:[7]

$$ATTN \approx 6Nlog_2\left(\frac{2f_{IF}}{B/2}\right) \tag{3.28}$$

This equation can be used to determine the preselect filter order and IF frequency required to yield a specified requirement. For example, an AMPS analog cellular phone requires $B = 25$ MHz in a fixed-tuned preselect receiver architecture. Using the typical choice of a 45 MHz IF, the number of poles required to provide 60 dB worst case image rejection is 4. Alternatively, for a DECT phone operating with $B = 20$ MHz and $f_{IF} = 110$ MHz, a 60 dB image rejection can be achieved with only 3 poles. Finally, a manually tuned, low-cost FM broadcast receiver typically employs an IF of 10.7 MHz and a tracking preselect filter

[7]The attenuation for the fixed-tuned filter with the receiver tuned to the band edge will be slightly less, but the given equation is sufficiently accurate for this discussion provided that $f_IF \approx 2B$ or greater.

with $B = 2$ MHz. Assuming a somewhat relaxed image rejection requirement of 50 dB, the number of poles required in this design is 2.

The level of image rejection *required* in any given receiver will depend on the location of the image frequencies in the RF spectrum, and on the expected proximity of the receiver to transmitters operating on those frequencies. These issues must be carefully considered when choosing IF and LO frequencies during the receiver design process. For example, an image rejection requirement of 50 dB or less for the FM broadcast receiver discussed above may be permissible since the image frequency with a low-side injection LO design falls into the Aviation band at 110 - 130 MHz. Outside of the immediate vicinity of major airports, these frequencies tend to be sparsely populated and contain only low power signals.

Spurious Response

In early receiver designs, mixer circuits often created frequency conversions other than those desired, leading to spurious responses on a wide range of possible frequencies. This problem is less severe in modern receiver implementations due to the use of improved mixer technology and IF frequencies which are either well below or well above that of the RF signal. However, spurious response problems can still arise in multiple-conversion receiver architectures.[8]

In multiple-conversion designs, images resulting from conversion from one IF to the next create spurious responses, which typically fall at frequencies within the receiver's own service band. Hence, the spurious response attenuation requirements are of the same order of magnitude as those for alternate channel rejection (e.g. ≥ 60 dB).

As an example, consider the AMPS cellular phone discussed in Chapter 2, in which a dual

[8]Spurious responses may also arise when complex synthesizer designs are used for tuning. Only the problems associated with filters are covered here.

conversion architecture was employed with a first IF at 45 MHz and a second IF at 455 KHz. The mixer used in the down conversion from 45 MHz to 455 KHz will produce an image at frequencies either 910 KHz above or below the desired signal, and the extent to which this response is attenuated will depend on the bandwidth and order of the first IF filter.

The filter order required to meet a given spurious specification depends on the ratio of the second IF frequency f_{2IF} to the first IF filter bandwidth B_{1IF}, in a manner similar to that for the preselect filter considered earlier.

$$ATTN_{spur} \approx 6Nlog_2\left(\frac{2f_{2IF}}{B_{1IF}/2}\right) \tag{3.29}$$

The actual number of filter poles needed for an early IF filter depends heavily on tradeoffs made in the overall receiver architecture. This issue will be considered in more depth in Chapter 4. However, as an example calculation, consider a receiver in which a first IF filter bandwidth of 2% (selectivity Q of 50) is used. Assume further that the second IF frequency is 10% of the first IF frequency to allow the selectivity Q of the final channel selection filter to be decreased by a factor of 10 relative to a single-conversion design. Then, to provide 60 dB of spurious response rejection, Equation (3.29) shows that the first IF filter requires N = 3 poles.

3.3.4 Fidelity

Discussions of selectivity in the previous section have addressed filter requirements needed to achieve certain levels of stopband rejection. However, no requirements have yet been determined for filter *in-band* response. In this final section, in-band response characteristics are briefly considered and related to the issue of receiver fidelity.

Fidelity is a measure of a receiver's ability to accurately demodulate the information contained in the desired radio signal. In an analog FM receiver, fidelity may be measured in terms of the total harmonic distortion present in the recovered audio waveform, while in a digital system, fidelity is typically expressed in terms of symbol or bit error rate. These factors depend on both the filtering used, and the demodulator design employed.

Assuming the demodulator is ideal, the receiver's fidelity can be related to the IF channel select filter's in-band response.[9] A perfect filter would provide a flat amplitude response and a linear phase over the signal bandwidth producing only scaling and delay. Real filters however, possess neither of these characteristics and an assessment of amplitude and phase deviations on fidelity is needed. Using appropriate analysis techniques, the effects of various nonideal amplitude and phase response features can be determined, and the results can then be used to specify filter performance based on fidelity requirements. This analysis is complex and outside the scope of this discussion. A simpler alternative approach to determining filter requirements is thus desired. As in the case of dynamic range, benchmarks relative to existing receiver designs can serve this purpose.

In Chapter 2, the most common filter type used in receiver channel select filtering is the MCF design. These filters are members of a broad class of recursive filters with similar response characteristics known as coupled-resonators. Thus, any filter with in-band responses matching or approximating that of a coupled-resonator design should prove acceptable.

In some newer PCS products operating at higher frequencies and larger bandwidths, surface acoustic wave filters may be used. A survey of manufacturer data shows that the response of these filters varies considerably depending on the type of SAW construction (transversal or resonator), and on the filter cost. However, despite their potential for highly linear phase, many of these filters exhibit responses that are similar to those of simple recursive Butter-

[9]The effect of preselect and image reject filters is generally negligible because the gain and phase variations over the signal bandwidth are minimal.

worth forms. Thus, replacements for these filters should provide acceptable performance provided their amplitude and phase responses are at least as good as that of Butterworth designs.

Chapter 4

Alternative Receiver Architectures

In the last chapter, a superheterodyne receiver architecture was assumed in discussing system and filter requirements. Although this choice is generally reasonable, it contains an implicit assumption that receiver channel selectivity is best achieved with fixed-tuned, high-order, bandpass filters operating at relatively low frequencies. In light of the difficulties in integrating bandpass filters identified in Chapter 2 and changes in RF device technology which occur over time, this assumption may no longer be valid. Indeed, there is renewed interest today in alternative receiver designs which can decrease, or if possible, eliminate the need for on-chip bandpass filters altogether. These architectural alternatives are the subject of this chapter.

The study of alternative receiver architectures begins with an overview of early receiver designs, providing an important historical context. Next, the superheterodyne architecture and its many variations are examined in detail. One of these variations, the design of superheterodyne receivers with ultra-low IFs, then leads to the concept of direct conversion receivers in which received signals are converted directly to baseband and all channel selection filtering is done with lowpass filters. Finally, an "ideal" receiver architecture is proposed in which channel selection filters are moved to the receiver's front-end to provide good performance with minimum possible power consumption.

4.1 Early Receiver Architectures

The earliest radio receiver architecture was developed by H.R. Hertz in 1887 [24]. Hertz's receiver was designed purely as a means to validate the existence of radio waves predicted by Maxwell 23 years earlier. The receiver operated at a frequency of 31 MHz and consisted of a simple loop of wire broken by a microscopic gap. This arrangement produced a weak spark when radio energy was created in Hertz's laboratory through the use of a powerful spark gap transmitter.

Commercial development of radio receivers began approximately 10 years later in 1896 when Marconi demonstrated reception of signals over distances of up to 9 miles. Marconi's system used a spark gap transmitter similar to Hertz's, and a receiver consisting of a battery, coherer, and bell. These "demodulator" circuits were connected directly to an antenna constructed with two metal plates, one fixed to a tree and one buried in the ground.

The concept of tuned radio receivers using LC circuits was developed at about the same time by Sir Oliver Lodge, and patented in 1897. Later in 1899, Marconi patented similar technology, giving the Marconi Wireless Telegraph and Signal Company a near monopoly on radio design, and setting the stage for rapid progress in subsequent years.

4.1.1 Tuned RF Receivers

Lodge's, Marconi's, and Hertz's earlier receivers can all be classified as "Tuned-RF" architectures in which selectivity and detection are provided by circuits operating at the same frequency as the transmitted signal. The general concept is illustrated in Figure 4.1.

With the invention of the triode vacuum tube by de Forest, and the development of radio telephony (AM voice transmission) by Fessenden and Alexandersen at the turn of the century, more sophisticated tuned-RF receivers emerged to handle an increasingly congested

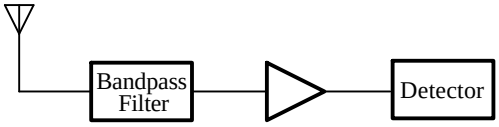

Figure 4.1: Tuned RF receiver architecture.

RF spectrum [24]. These receivers used amplifiers and cascaded stages of tuned circuits (essentially high order filters) to provide both improved sensitivity and increased selectivity. Thus, within only a few years, tuned-RF receivers reached a relatively high level of sophistication as illustrated in the design of Figure 4.2 which was patented in 1913.

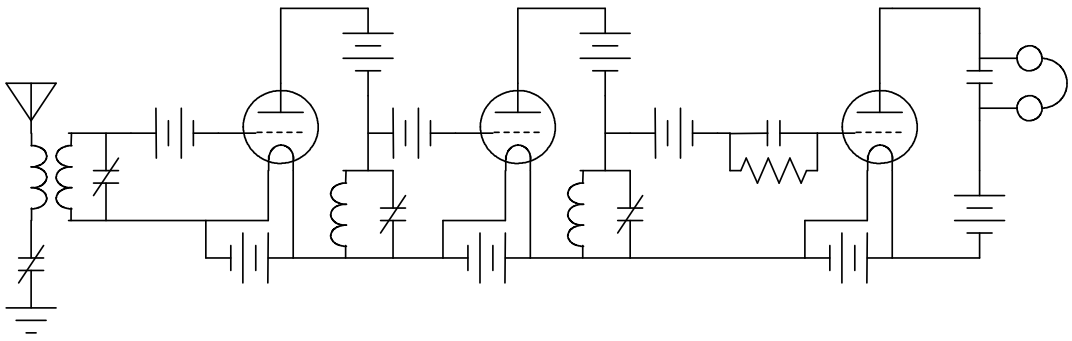

Figure 4.2: Early tuned-RF receiver circuit. [British patent no. 147,147]

Nevertheless, tuned-RF receivers required a fair amount of patience and skill to manually adjust the filtering circuits used. This fact, combined with the cost of using three or more

tubes and the difficulties of extending the designs to higher frequencies, motivated the development of a variety of alternative approaches discussed in the following sections.

4.1.2 Regenerative Receivers

At about the same time that multi-stage tuned-RF receivers were being built, de Forest, von Strauss, Meissner, and others discovered that coupling between the plate coils and grid coils of a tuned amplifier could result in the phenomonon of "reaction" or regeneration [24]. This effect provided a wealth of benefits including an increase in amplification, a reduction in the number of tubes needed within the receiver, and high selectivity without the need for multiple, independently tuned circuits. A block diagram of a regenerative receiver is shown in Figure 4.3 in which the simplicity of the design is readily apparent.

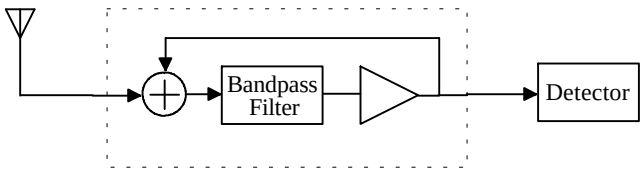

Figure 4.3: Regenerative receiver architecture.

Although the effects of regeneration were not well understood at the time, they may be derived quite easily using modern feedback theory. To quantify these effects, assume that the filter shown in Figure 4.3 is a basic second-order bandpass design with transfer function $H(s)$ given by the relation:

$$H(s) = \frac{s\frac{\omega_o}{Q}}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2} \tag{4.1}$$

where ω_o is the center frequency and Q is the quality factor. With the numerator shown,

the midband gain of $H(s)$ is 1.0, while the 3 dB bandwidth B (in Hz) is related to the Q through the well known expression:

$$B = \frac{2\pi\omega_o}{Q} \tag{4.2}$$

If the amplifier in Figure 4.3 has a gain of A ($A < 1$), then from feedback theory, the closed loop gain $H_{CL}(s)$ of the regenerative circuit in the dashed box is of the form:

$$H_{CL}(s) = \frac{AH(s)}{1 - AH(s)} \tag{4.3}$$

Substituting Equation (4.1) into Equation (4.3) then yields:

$$H_{CL}(s) = \frac{s\frac{\omega_o}{Q}A}{s^2 + s\frac{\omega_o}{Q}(1 - A) + \omega_o^2} \tag{4.4}$$

for which the midband gain, effective Q, and bandwidth are:

$$|H_{CL}(\omega_o)| = \frac{A}{1 - A} \tag{4.5}$$

$$Q_{CL} = \frac{Q}{1 - A} \tag{4.6}$$

$$B_{CL} = \frac{2\pi\omega_o}{Q_{CL}} = B(1 - A) \tag{4.7}$$

As an example, assuming $A = 0.99$, the gain is increased by a factor of 100 (40 dB), the Q is multiplied by 100, and the bandwidth is reduced by 100.

Despite these useful effects, regenerative receivers have a number of limitations. One serious limitation is the need for critical manual adjustment during use to achieve precisely the value of A desired. If the regeneration is advanced too far, the receiver will break into oscillation and reception of the desired signal will be lost.

Although oscillation represented a problem for regenerative receivers intended for AM reception, it was recognized by de Forest and others as a means of producing sine waves electronically, and was exploited to create heterodyne detectors for receiving continuous-wave (CW) telegraph signals. A more elegant solution to the reception of these signals however, was invented by Round [24]. Round showed that if a regenerative amplifier was operated at exactly the point of entering oscillation, it could function simultaneously as a regenerative amplifier, heterodyning oscillator, and audio detector. This special case of regenerative receiver design known as an "oscillating detector" was popular for many years, especially within the amateur community because of its excellent performance and low cost.

4.1.3 Super-Regenerative Receivers

Regenerative receivers were manufactured until at least the 1960's because of their ability to minimize the number of active devices used, and hence to minimize cost. However, their reliance on critical manual adjustment of the regeneration control was a major drawback to their design. In an early attempt to address this problem, Bolitho and Armstrong developed the super-regenerative architecture shown in Figure 4.4 in 1919 and 1922, respectively [24].

The principle of super-regenerative design was to employ regeneration with a feedback gain of slightly greater than one. Although this assured that oscillations would build up, a "quenching" circuit was used to periodically damp the oscillations as shown. With this setup, the presence of an input signal caused oscillations to build up at a rate that increased with increasing signal amplitude. Hence, the average magnitude of oscillation energy provided an indication of both the presence and strength of the received signal.

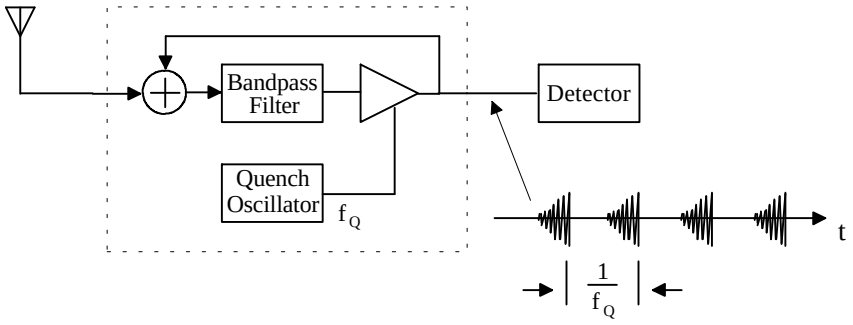

Figure 4.4: Super-regenerative receiver architecture.

Super-regeneration may be viewed as a simple, yet somewhat crude (by today's standards) method of automatically controlling the regeneration setting, thereby eliminating the need for manual adjustment. However, while the need for manual control is eliminated, the super-regenerative architecture retains many other limitations of the basic regenerative concept including:

- Bandpass filtering is limited to a single-pole rolloff;
- Oscillations which occur at the received frequency radiate through the antenna, interfering with other receivers;
- Selectivity decreases for large input signals due to limited dynamic range; and
- Bandwidth is dependent on gain and therefore not matched to the signal being received.

These problems were overlooked in early regenerative and super-regenerative receivers because of the cost benefits afforded by reductions in the number of active devices required. However, with the advent of integrated circuits, this advantage disappeared, and the superheterodyne receiver became the architecture of choice in virtually all receiver designs.

4.2 Superheterodyne Receivers

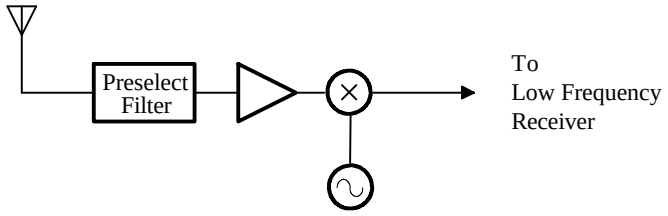

Figure 4.5: Armstrong's original superheterodyne receiver.

The concept of heterodyning an incoming signal to convert it to a lower frequency was developed by Armstrong and others in 1918. Armstrong's original design, shown in Figure 4.5, was intended to allow low frequency radiotelephone receivers to be adapted for use at newer HF frequencies being used in Europe. However, it was quickly recognized that the basic approach offered many additional benefits, including:

- The low-frequency receiver (typically a high quality tuned-RF design) could be adjusted once, and thereafter all tuning could be done by varying the heterodyne oscillator.
- Amplification could be provided primarily at a lower frequency where high gains were easier to achieve.
- Amplification was split between two frequencies, so that the risk of unwanted regenerative feedback could be reduced.
- Narrow, high-order filtering was more easily achieved in the low frequency receiver than at the actual incoming RF frequency being received.

Eventually, the separate tuned-RF receiver was replaced by the dedicated IF section of the modern superheterodyne design, in which pre-tuned fixed-frequency filters are employed. The result became the well-known architecture used today with high quality channel-select filtering and no adjustments aside from volume and tuning controls.

4.2.1 Modern Single Conversion Implementations

The essential components of a modern single conversion superheterodyne receiver architecture are shown in Figure 4.6 and briefly reviewed in the following paragraphs.

In the superheterodyne design of Figure 4.6, the preselect filter serves both to attenuate signals outside the service band and to provide partial rejection of the image frequency created by the heterodyning process. This filter must have low insertion loss to minimize degradation of the receiver's noise figure.[1]

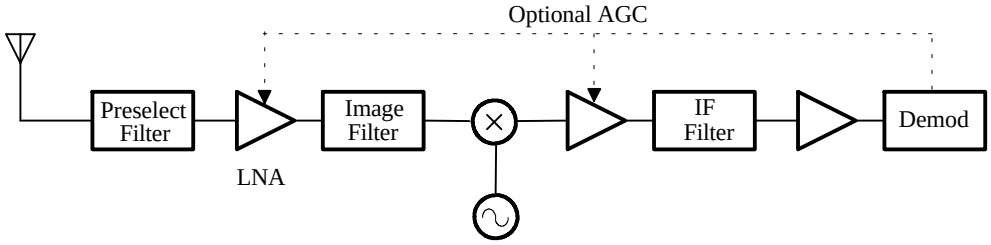

Figure 4.6: Modern superheterodyne receiver.

After preselection, a low noise amplifier (LNA) provides moderate gain to overcome losses in passive circuits up to the input of the first IF amplifier. This gain is needed to provide

[1] In some designs (such as satellite receivers with directional dish antennas), this filter may be placed after the LNA to achieve the best possible noise performance. However, in most terrestrial receiver applications, this option is unacceptable since it leaves the LNA exposed to all signals throughout the RF spectrum.

good noise figure performance, but must be minimized to avoid degrading dynamic range as discussed in Chapter 3.

Following the LNA, an image filter is provided. The purpose of this filter is two-fold. First, it supplements out-of-band attenuation provided by the preselect filter, further increasing image rejection performance and improving BDR and SFDR performance relative to out-of-band interferers. Its primary purpose however is to improve noise figure performance by attenuating noise at the image frequency generated in the LNA and translated to IF in the mixing process.

Next, the mixer and LO convert the signal to the selected IF frequency where additional moderate levels of gain may be provided. Thereafter, the IF channel select filter passes only the signal being received. IF amplification can then be used as needed to increase the signal to an amplitude that can be conveniently processed by demodulator circuits to recover the transmitted information. In analog FM and digital FSK systems, the post-filter IF amplifier subsystem is typically designed to provide very high gains, intentionally forcing the amplifiers into amplitude limiting. Intermodulation products are (ideally) no longer important at this stage in the receiver since all interfering signals have been attenuated by the IF channel select filter. In other designs intended for use with AM and digital phase modulation, automatic gain control is usually employed so that amplitude information is retained and minimal phase distortion occurs.

4.2.2 Multiple Conversion Implementations

The design of superheterodyne receivers involves many trade-offs including selection of IF and LO frequencies to meet image rejection and spurious response objectives, and to minimize the complexity of required bandpass filter components. If the service band of interest is sufficiently narrow relative to the band center frequency, then the single conversion design described in the preceding section can be implemented without requiring an excessive

number of filter poles. However, if the service band is wide, either a tracking preselect filter or a multiple conversion design may be needed.

The tracking design illustrated in Figure 4.7 employs preselection and image filters with bandwidths smaller than the width of the service band of interest. Hence, the number of poles required to achieve a given image rejection performance can be reduced while still converting the signal to a frequency sufficiently low to avoid an excessively narrow IF filter fractional bandwidth. The price paid in this case is the need for a narrow bandwidth, *tunable* filter, and associated tracking between the filter and the local oscillator.

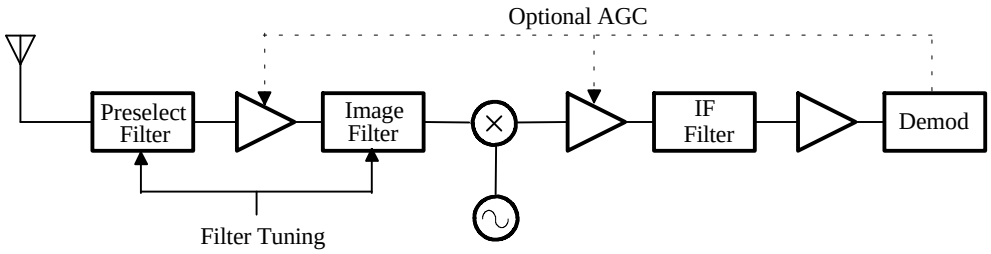

Figure 4.7: Single conversion superheterodyne with tracking preselect.

The alternative multiple conversion design shown in Figure 4.8 converts the incoming signal first to an IF at a relatively high frequency, and then to a lower second IF. This approach minimizes the number of poles needed in the preselect/image filters and allows narrow channel bandwidths to be handled with lower Q filter designs. The price paid in this design is additional circuitry, and the associated power consumption needed to maintain good dynamic range performance in all active devices ahead of the final channel select filter.

The tracking preselect design has historically been difficult to implement due to problems in realizing high quality tunable RF filters. However, in considering receiver integration using active filters, this architecture may prove to be desirable. Integrated active filters necessarily include tuning to address manufacturing tolerances and temperature drift, and

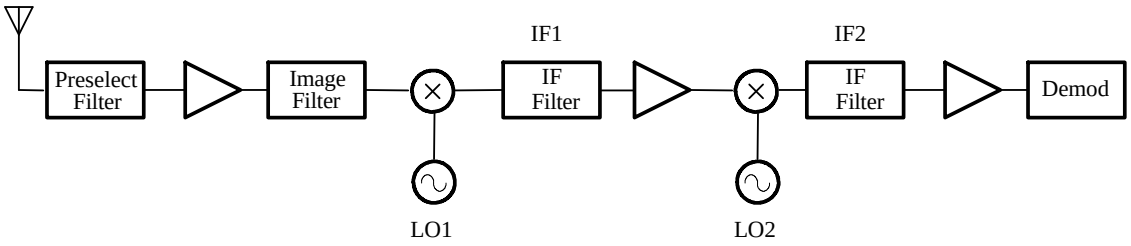

Figure 4.8: Multiple conversion superheterodyne.

this tuning can be used to advantage in this application. Nevertheless, the degree to which the filter can be narrowed will depend on the resulting Q values needed. This issue is considered in Chapter 6, where relationships between Q and dynamic range are derived in detail.

Integration of a multiple conversion design is also a potentially attractive alternative when faced with the quality factor limitations of on-chip active filters. In this case, the increased first LO frequency and the low second IF frequency simultaneously decrease the Q and number of poles needed in both the preselect and channel select filters. However, the need for an additional local oscillator and the additional power consumed must be carefully considered.

4.2.3 Up Conversion Implementations

Historically, one of the main goals of the superheterodyne architecture was to convert the incoming RF signal to the lowest frequency possible, allowing use of less expensive amplification and filtering components. However, with the development of semiconductors operating at several hundred MHz and above, and of quartz and surface acoustic wave filters with fractional bandwidths well under 1%, new architectural options have become

available. Around the late 1970's and early 1980's, these options began to be exploited heavily in the form of up-conversion receiver designs.

For very wide service bands (e.g. 0.1 to 30 MHz), achieving good image rejection with down conversion superheterodyne designs requires elaborate tracking filters and band switching mechanisms. Image rejection requirements can be met more easily however, if the incoming signal is first upconverted to an IF frequency *above* the desired RF frequency as shown in Figure 4.9. Here, both the LO frequency and the IF frequency are relatively high, placing the image frequency well above the highest frequency in the service band. Hence, preselect and image filters can be implemented with simpler *lowpass* filter designs.

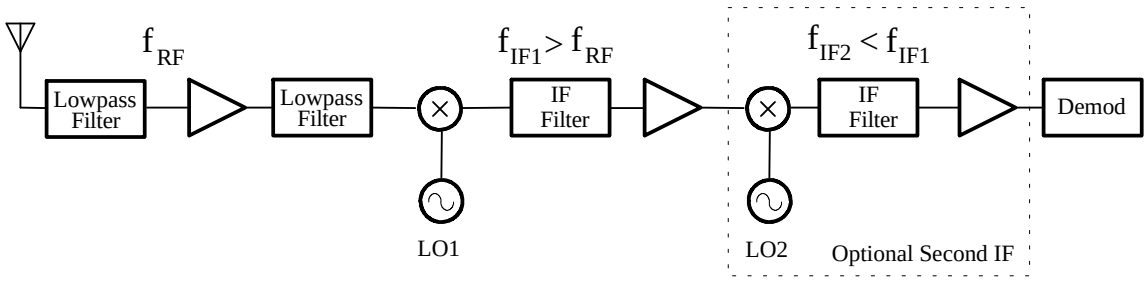

Figure 4.9: Up-conversion supetheterodyne.

Up-conversion architectures are especially useful in applications such as AM and FM broadcast receivers where the service band is broad and the RF frequency is "low" relative to the performance of active devices. However, one of the drawbacks of this architecture is the need for narrow IF filter fractional bandwidths if full channel selectivity is desired at the up-converted frequency, or if subsequent down conversion to a low frequency is desired. In receiver designs with discrete filters, quartz and surface acoustic wave (SAW) filters are often required, leading to increased product cost.

Work on partially and fully integrated AM/FM broadcast receivers has been done at Delft University of Technology in conjunction with Philips Laboratories [45] [47] [53]. In [45]

and [47], a partially integrated solution for the AM portion of a car radio is described in which a 10.7 MHz IF is adopted and an off-chip crystal MCF is used to provide the small fractional bandwidth needed. In [53], the design of an up conversion FM broadcast receiver is described and the use of an *on-chip* SAW filter operating at 160 MHz is investigated. To achieve acceptable channel selectivity at the 160 MHz IF, the IF filter in this application requires a selectivity Q of 800 (160 MHz / 200 KHz), leading the investigators to conclude that a coupled resonator SAW design with physical length of at least 6 mm was required. In addition, the temperature stability needed to maintain the filter centered on the IF frequency was cited as a significant problem to be solved.

Integrated active LC filters could also serve as a first IF in up-conversion designs. However, the Q values needed are generally beyond those that can be realized with adequate dynamic range, so that one or more subsequent down conversions would be required. Thus, this architecture does not appear to offer a good solution to the receiver integration problem.

4.2.4 Designs with Ultra-Low IFs

Problems with image responses can be reduced in some special situations without actually attenuating the image frequency at all. The key to achieving this result is to carefully select the RF to LO frequency relationship so that the image frequency falls within an unused portion of the RF spectrum. This concept led to the development of the ultra-low IF integrated receiver technology described briefly in Chapter 2 and detailed below.

The ultra-low IF architecture is illustrated in Figure 4.10, where the RF frequency f_{RF} is related to the LO frequency f_{LO} through the channel bandwidth B:

$$f_{LO} = f_{RF} + KB \tag{4.8}$$

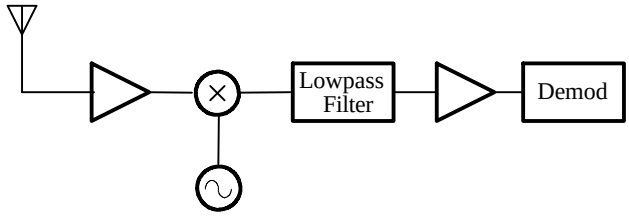

Figure 4.10: Ultra-low IF superheterodyne.

Assuming that the constant K is selected as $K = \frac{1}{2}$, the RF signal will be down converted to an IF frequency of $f_{IF} = \frac{B}{2}$, and channel selectivity can be provided with a lowpass filter with cutoff frequency $f_c = B$. Assuming also that operating frequencies in the system are assigned so that adjacent channel signals are not occupied, the image response, which falls at the center of the adjacent channel, will contain no energy and will not interfere with reception of the desired signal. This basic approach can also be used in systems in which the adjacent channel is occupied, provided that guard bands are present. For example, if guard bands account for half of the channel bandwidth, then $K = \frac{1}{4}$ could be used, and the lowpass filter would be designed with a cutoff frequency of $f_c = \frac{B}{2}$. This basic approach was pioneered at Philips in the early 1980's for use in constructing a fully integrated FM broadcast receiver in which no bandpass filters were required [43].

The performance of the ultra-low IF receiver architecture rests on the degree to which the image frequency is occupied. In turn, this issue depends heavily on system level design considerations and on the ability of transmitters to avoid contaminating neighboring regions of the frequency spectrum. One additional problem is the resulting demand placed on the lowpass filters needed for final channel selection. A careful study of the imaging problem shows that the number of poles required in the lowpass filter is more than twice that needed in an equivalent traditional receiver using bandpass filters with the same final selectivity.

This feature results from the fact that signals in alternate channels are converted into the region of baseband spectrum immediately above the bandwidth defined by the lowpass filter.

4.2.5 Designs with Image Rejection Mixers

Demands on filter requirements can also be reduced through the use of image rejection mixers such as shown in Figure 4.11. In this approach, the use of quadrature mixing attenuates the signal at the image frequency. With precise 90^o phase shifts, a theoretically infinite attenuation results, whereas in practice, the performance is limited to about 30 to 40 dB depending on whether or not trimming is used [48].

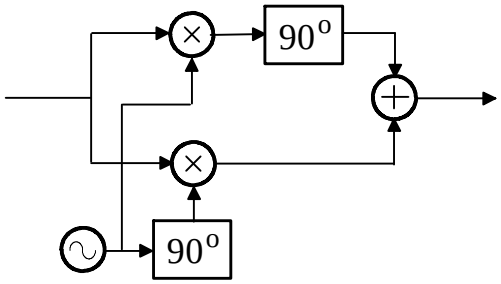

Figure 4.11: Image rejection mixer.

Nevertheless, 30 to 40 dB of attenuation can significantly decrease the number of poles needed in bandpass filters when converting the signal to a subsequent IF stage. For example, if an image rejection of 60 dB is required in the receiver, and 30 dB is provided by the mixer, then the required number of poles in the filter is reduced by half.

Drawbacks of the image rejection approach include difficulties in achieving the necessary phase shift accuracies, and the extra power consumption involved in the use of two mixers. In addition, if an image reject mixer is considered for use at the receiver's front-end, special

consideration must be given to the dynamic range issues discussed in Chapter 3. Use of a reduced number of poles in the RF preselection filter will decrease the attenuation of out-of-band signals at large frequency offsets, lowering the blocking and intermodulation dynamic range performance relative to signals at these frequencies. However, the benchmark receiver performance measurements shown in Table 3.3 suggest that this problem may not be significant provided that one to two poles of preselection filtering is retained.

4.2.6 Designs with Selective Demodulators

A final technique that can be applied to minimize the need for on-chip bandpass filtering in superheterodyne receivers is the implementation of selective demodulators. In theory, it may be possible to reduce the requirements on channel select IF filters while obtaining good receiver selectivity if the demodulator itself is designed to be sensitive to signals only within the desired signal's bandwidth. This concept was studied by Nauta [45], and later by van der Plas [49] at Delft with mixed results. Their work addressed the subject of synchronous detection in AM receivers using the demodulator shown in Figure 4.12.

In this design, a narrow bandwidth PLL recovers the carrier of the AM signal in the presence of one or more interfering signals on adjacent frequencies. The recovered carrier is then mixed with the IF signal to translate the AM spectrum to baseband. A lowpass filter provides the necessary channel selectivity by eliminating adjacent channel interferers which have been translated by the mixer to frequencies above the desired signal's audio bandwidth. Through careful design of PLL and AGC circuits, van der Plas achieved a 50 dB selectivity using this approach. However, he cites difficulties including the need for precision receiver tuning to prevent false PLL lockup, and a relatively large amount of circuitry for carrier regeneration.

Similar techniques can be developed for other modulation types. For example, with digital phase modulated systems, demodulation often involves carrier regeneration and translation

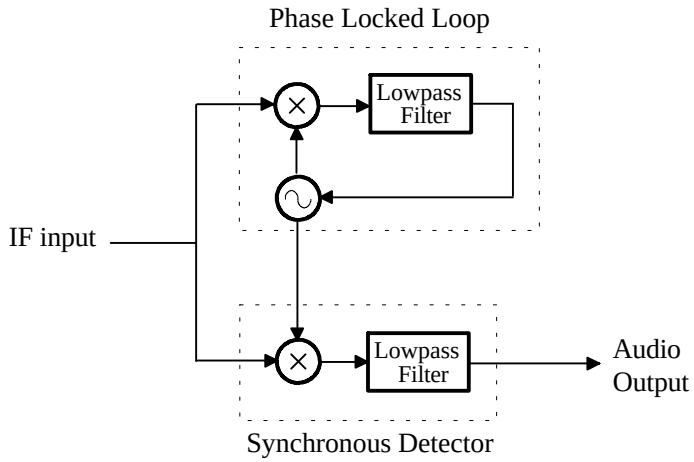

Figure 4.12: Selective AM demodulator.

directly to baseband. Lowpass filters can then be used to remove interferers as before. However, as in van der Plas' work, the implementation of carrier recovery circuits capable of discriminating against large amplitude interfering signals presents significant challenges.

In the case of frequency modulated systems, the three demodulator types commonly used in traditional receivers include frequency discriminators, one-shot multivibrators, and PLLs, none of which is well suited to selective demodulation. A fourth type, however, shows considerable promise for the special case of digital FM systems. The essential concept is equivalent to the use of the direct conversion receiver architecture described in the next section. The interested reader is referred to the references for additional details [52] [51] [40].

4.3 Direct Conversion Receivers

Of all the alternative architectures developed to date, the direct conversion or "zero-IF" design shown in Figure 4.13 offers the most promise for eliminating on-chip bandpass filters

while simultaneously retaining high performance operation.

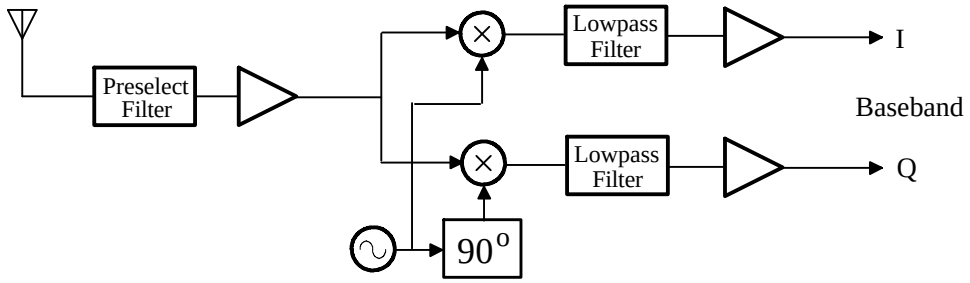

Figure 4.13: Direct conversion receiver architecture.

In a direct conversion architecture, the received signal is passed through a preselect filter whose sole responsibility is to improve dynamic range performance by rejecting potentially large out-of-band interferers. The portion of the spectrum passed by the preselect filter is then amplified and mixed with a local oscillator equal to the frequency of the desired signal. This converts the signal directly to baseband where final channel select filtering is performed with integration-friendly, lowpass filter designs.

Since the center of the "IF" is at zero frequency, no image response is produced, and no image filtering is required. Signals above and below the desired signal frequency are translated into baseband frequencies above that of the desired signal, and are removed by lowpass filtering. The concept of direct conversion thus shares many of the features of selective demodulators dicussed in the preceding section. Indeed, the direct conversion receiver architecture can be viewed as a selective demodulator operating directly at the RF frequency.

The integration-friendly features of the direct conversion design have led several researchers to embrace this architecture as a foundation on which to build fully integrated receiver designs [52] [40]. However, before these receivers can achieve widespread acceptance, several

important practical problems must be addressed.

First, reception of signals in which transmitted information is carried in both sidebands (or equivalently in both dimensions of a sinusoidal basis vector) requires the implementation of in-phase/quadrature (I/Q) channel conversion as shown. The problem of maintaining a precision 90^o phase shift over the range of LO frequencies to which the receiver is tuned is complicated by the fact that the circuits must operate directly at the RF frequency.

Second, the transmitted information may be difficult to extract once it has been separated into I and Q parts. This is especially true for analog FM, but may not be a serious problem for newer digital modulation types.

Third, LO to RF port isolation of the mixers must be carefully considered to prevent radiation and interference to nearby receivers operating at the same frequency. This problem is reduced through the use of an LNA placed between the antenna and mixers. However, operation at very high frequencies (900 MHz to 2 GHz) limits the isolation achievable in practice, making this problem a potentially significant concern.

Fourth, DC offsets occur at the I/Q outputs due to LO to RF feedthrough in the mixers. These effects must be removed with highpass filtering, making reception of low frequency baseband information difficult.

Finally, translation of the entire service band to baseband places significant dynamic range requirements on the mixers as well as on the low pass filters employed. This problem is fundamentally the same as that in traditional superheterodyne receivers. Hence, all the tradeoffs between noise figure, dynamic range, and power consumption discussed in Chapter 3 carry over to the direct conversion architecture.

The advantages and disadvantages of direct conversion receiver designs relative to those of receivers based on the traditional superheterodyne architecture must therefore be decided based on practical rather than theoretical issues. To date, the radio hardware industry

has favored the classic superheterodyne as more robust and lower risk in the design of board-level receiver solutions. Whether or not this decision changes within the domain of integrated receiver design will depend on risk and performance tradeoffs associated with solving the problems listed above, versus solving the problems associated with on-chip bandpass filtering addressed in this dissertation.

4.4 Digital Receivers

Periodically, the concept of an "all digital" receiver design is proposed as a solution to analog signal processing limitations and apparent complexity. Thus, it is prudent to consider whether such an approach could minimize or eliminate the requirement for on-chip filtering.

Two simplified block diagrams of digital receivers are shown in Figures 4.14 and 4.15. The receiver in Figure 4.14 is a superheterodyne-like design in which the sampling frequency is above the desired RF frequency and a "digital down-converter" is used to mix the signal to a lower IF, or directly to baseband. The other design shown in Figure 4.15 is a direct-conversion architecture in which the RF is sampled at the frequency of the desired signal using a quadrature approach.

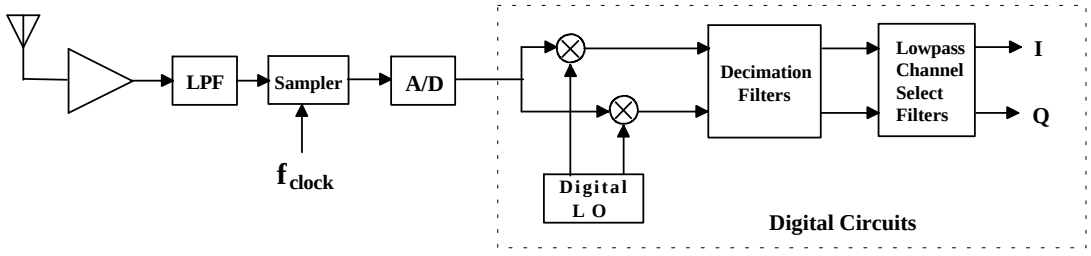

Figure 4.14: Simplified digital receiver architecture.

On the surface, these designs have significant appeal. Assuming for the moment that the RF

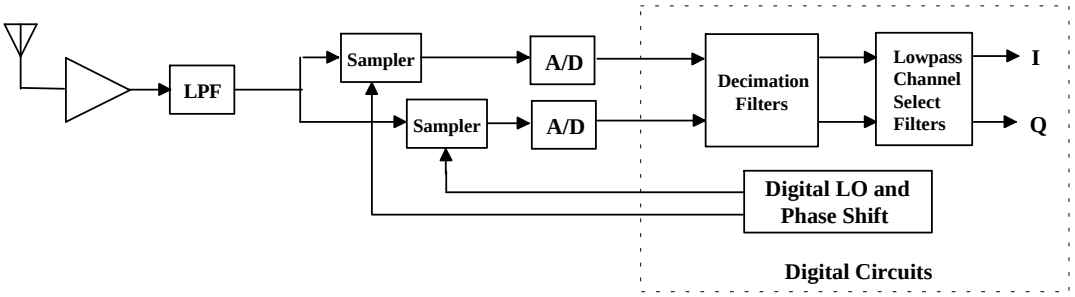

Figure 4.15: Simplified direct-conversion digital receiver architecture.

can be directly sampled, the digital local oscillator can produce high precision quadrature waveforms and the benefits of digital signal processing can be applied to realize channel selection filters with very high selectivity. In addition, adaptive algorithms can be used to combat problems such as multipath distortions in the received signal.

Unfortunately, the assumption that the receiver can sample directly at the RF frequency is fundamentally flawed. In modern cellular and PCS systems, sampling directly at RF entails sampling rates of 900 MHz and above. Further, since the RF front-end is open to the full spectrum environment (no narrowband preselect filtering has yet been assumed), very high dynamic range would be required, implying an analog-to-digital (A/D) converter with 10 bits or more. Attempting to sample to this precision at GHz frequencies is a very difficult task, implying high cost and high power consumptions.[2] Moreover, even if the problems of GHz rate sampling and A/D conversion are put aside, the data rate and word widths alone will be too large to allow processing within acceptable power budgets for portable operation (see Chapter 2 and reference [182]).

In an attempt to circumvent this obvious flaw, most designers have adopted either a conventional receiver front-end, or the use of "sub-sampling" techniques. The former requires all

[2]Even with 10 bits, some form of AGC will generally be required and the spurious-free dynamic range is unlikely to be sufficiently high to handle all the interfering signals present in the environment.

the analog filtering implied by analog receiver designs considered in previous sections, while the latter introduces aliasing which must be eliminated by very narrow preselect filtering prior to sampling.

For example, assume that a sub-sampled, direct-conversion digital receiver architecture is being considered in which the RF frequency is 2 GHz and the sampling frequency is 20 MHz. Such a design will alias any signals spaced by integer multiples of 20 MHz from the desired signal into the baseband processing circuits where they will interfere with, or prevent reception. To solve this problem, a preselect filter with a bandwidth $B \ll 20$ MHz and an attenuation on the order of 60 dB or more would need to be added. To achieve this level of attenuation with a manageable 3-pole bandpass filter design would require a selectivity Q of 500. Thus, rather than simplifying the design of integrated receivers, this approach actually increases the demands on bandpass filter designs.

To reduce the demands on preselection filtering, one might consider increasing the sampling rate. However, at higher rates, the power consumption required in the digital lowpass filters which follow would exceed allowable limits as discussed in Chapter 2. Thus, the use of an analog front-end offers the only viable alternative for low-power, high performance design, and the "digital receiver" concept is more properly seen as a digital demodulator operating at a final, low IF frequency.

4.5 Ideal Low-Power Receivers

Having surveyed existing receiver architectures and assessed their practical problems, one may wish to consider what shape a receiver might assume if only physical laws, rather than technology limitations determined its ultimate performance. In this final section, the design of an *ideal* receiver targeted at future *low-power*, portable, wireless applications is considered. Such a design must provide all the basic receiver functions identified in Chapter

3, including:

- Selecting one signal from a dense spectral environment;
- Amplifying this signal to a level suitable for demodulation; and
- Recovering the transmitted information.

In addition, it should be able to receive signals of any power level (provided they are above the noise floor), and should be immune to the problems of spurious responses created by arbitrarily large interferers.

To avoid violating physical laws in attempting to design such a device, the following assumptions are made:

- The noise figure of passive circuits is equal to their insertion loss.
- The noise figure of active circuits used is greater than or equal to one (0 dB).
- The efficiency of active circuits is less than or equal to one.

As additional constraints, it is assumed that the demodulator used is not frequency selective, and that it requires some amplification of the signal at the antenna. Otherwise the demodulator and the receiver would be the same and the "solution" would be contained in itself.

Based on these assumptions, a little thought shows that the ideal receiver must assume a form similar to that shown in Figure 4.16 in which all selectivity is moved to the RF input. If this were not the case, then large amplitude interferers would reach downstream circuits, causing saturation and intermodulation distortion products resulting in blocking and spurious responses. The only alternative would be to increase the power consumption

of the amplifiers or of the mixer drive circuits to a level at least as high as that of the interferer, which would violate the assumption of low power operation.

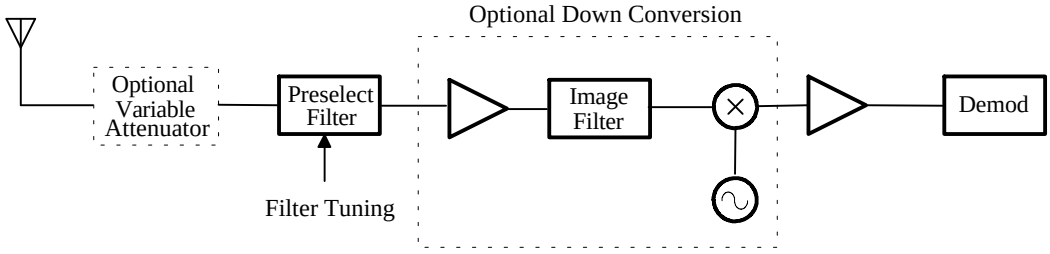

Figure 4.16: Ideal receiver architecture.

With the solution shown, several requirements on the preselect filter must be met:

- It must be high order to attenuate undesired signals.
- It must be tunable so that more than a single station in the service band can be received.
- It must be linear to avoid blocking and spurious responses at high frequencies.
- It must have zero (or negative) insertion loss to avoid degrading the receiver's noise figure performance.

Assuming these requirements are satisfied, downstream circuits can then be implemented with relatively low dynamic range circuits, and very low power. With interfering signals removed by the front-end filter, the dynamic range needed is reduced to that required to establish a specified C/N ratio at the demodulator input. For many modulation types, this can be as low as 15 to 20 dB.

For satellite receivers, where the strength of the desired signal does not vary significantly, the overall receiver dynamic range can be as low as 20 dB, as discussed in Chapter 3. For

terrestrial systems, signal levels at the antenna may vary by as much as 100 dB depending on the distance to the transmitter. However, this range is easily compressed to that of the required C/N for demodulation using suitable attenuators, AGC amplifiers, or limiting mechanisms (for FM modulations). Hence, an ideal receiver designed for these situations could also be implemented with very low dynamic range circuits.

The practicality of such an ideal, low-power receiver is of course open to serious question.[3] Although it is possible to create high quality, tunable, passive filters with narrow bandwidths using technologies such as YIG resonators, such filters are currently too large and too expensive for consumer products. The real value of examining this architecture lies instead, in contrasting it with existing receiver design to illustrate their basic limitations.

In the past, receiver power consumption was a less serious issue than it is today, and traditional superheterodyne receivers served well. With current increases in spectral occupancy and increasing emphasis on reducing power consumption in portable wireless devices, however, low power circuits with good dynamic range have become a necessity. These two conflicting needs can only be addressed through designs which move selectivity closer to the antenna. Hence, while the direct conversion architecture discussed in the previous section shows potential for solving some of the on-chip bandpass filtering problem, a need for bandpass filtering at the front end remains. This conclusion, coupled with the many practical problems associated with realizing the direct conversion receiver architecture, is largely responsible for the emphasis on integrated bandpass filters in the following chapters.

[3]Perhaps the closest consumer market product approximating the ideal receiver design of Figure 4.16 is a fixed-tuned paging receiver produced by Motorola [154] in which a 4-pole crystal filter was used at the RF frequency and the signal was converted directly to a 35 KHz IF for amplification, limiting, and demodulation.

Chapter 5

Integrated Bandpass Filter Design Options

The subject of filter design is a major field of study within the discipline of Electrical Engineering. An exhaustive treatment of bandpass filter design options is therefore well beyond the scope of this dissertation. Fortunately, however, technological constraints imposed by silicon IC processes and by the specialization to low power, high frequency, integrated implementations permits the range of study to be narrowed significantly.

As shown in Chapter 2, digital filtering is not a viable option at center frequencies above about 1 MHz, due to problems of excessive power consumption. This power consumption is determined by device parasitic capacitance and cannot be reduced by alternative filter structures or computational algorithms. Although the development of submicron processes will help in the coming years, the upper limit is unlikely to exceed a few MHz in the immediate future. Thus, the following discussion is restricted to analog methods. This decision narrows implementation alternatives to the general class of linear time invarient (LTI) filters, within which filter implementation options may be grouped, as shown in Table 5.1.

Additional observations made in Chapter 2 rule out the use of switched-capacitor and delay line filters for all but extremely low IF frequencies (e.g. < 1 MHz) when implemented in silicon processes at low power. In this case the main problems are the clock rates and circuit time constants needed to achieve sufficient settling between samples, and the clock noise found in practical realizations. Hence, implementation alternatives for high frequency

Table 5.1: Filter implementation alternatives.

	Continuous-Time	Discrete-Time
Recursive	Active RC, Gm-C, etc. Bulk Acoustic Wave Surface Acoustic Wave	Switched-capacitor
Transversal	Surface Acoustic Wave	CCD delay line

designs are essentially constrained to the continuous-time filter options listed in the first column.

Within the domain of continuous-time filters, designs may be divided into recursive structures and transversal structures. Continuous-time recursive filters have been widely studied and are easily constructed in integrated circuits using active filter design methods. Traditionally, these methods have involved only transistors (or opamps), resistors, and capacitors. Two additional methods are less well known, but also viable options. The first, Q-enhanced LC filters, adds inductors to the list of on-chip elements, extending the capabilities to VHF frequencies and above. The second, electro-acoustic filters, adds piezo-electric components to the list of on-chip elements, raising the possibility of implementing on-chip, bulk and surface acoustic wave devices.

This chapter will concentrate on continuous-time active filter design techniques and recursive filter structures. The subject of electro-acoustic filters is briefly discussed in Section 5.2, but is left mainly to the references for the reasons cited in Chapter 2.

5.1 Continuous-Time Active Filters

In the most general case, continuous-time active filters may be defined through a system of first-order differential equations:

$$\begin{aligned} \frac{d}{dt}X(t) &= AX(t) + Bu(t) \\ y(t) &= CX(t) + du(t) \end{aligned} \tag{5.1}$$

where

X(t)	is an n x 1 state vector
A	is an n x n coefficient matrix
B	is an n x 1 coefficient vector
u(t)	is the system input
y(t)	is the system output,
C	is a 1 x n coefficient vector, and
d	is a scalar.

Taking Laplace transforms and solving for the frequency domain transfer function $H(s)$, yields the familiar ratio of polynomials in s:

$$H(s) \equiv \frac{y(s)}{u(s)} = \frac{a_n s^n + a_{n-1}s^{n-1} + ... + a_o}{b_n s^n + b_{n-1}s^{n-1} + ... + b_o} \tag{5.2}$$

Through suitable choices of coefficients a_i and b_i, desired filter responses can be synthesized. For example, the class of all-pole lowpass responses can be obtained by setting $a_o = 1$ and $a_i = 0$ for $i > 1$, yielding:

$$H_{LP}(s) = \frac{a_o}{b_n s^n + b_{n-1}s^{n-1} + ... + b_o} \tag{5.3}$$

The familiar filter forms such as Butterworth, Chebyshev, and Bessel can then be obtained by proper selection of b_i [187].

To obtain a *bandpass* filter design, a common approach is to begin with Equation (5.3) and then apply the transformation:

$$s \rightarrow \frac{s^2 + \omega_o^2}{Bs} \tag{5.4}$$

where ω_o is the desired center frequency and B is the desired filter bandwidth. This transformation yields a transfer function of the form:

$$H_{BP}(s) = \frac{a'_n s^n}{b'_{2n} s^{2n} + b'_{2n-1} s^{2n-1} + ... + b'_o} \tag{5.5}$$

defining an all-pole bandpass design with filter response characteristics essentially identical to the lowpass prototype, but shifted in frequency and scaled in bandwidth as illustrated in Figure 5.1.

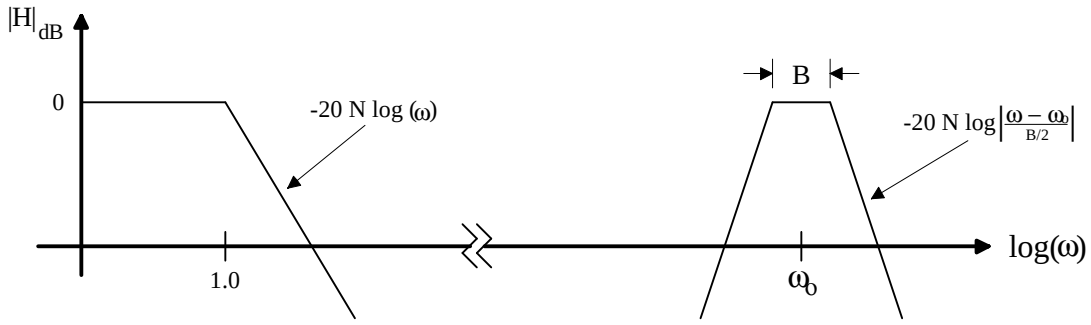

Figure 5.1: Lowpass to bandpass filter transformation.

5.1.1 Bandpass Filter Structures

A practical realization of a filter requires a filter *structure*. This structure can be defined graphically in the form of a signal flow diagram. For example, the structure shown in Figure 5.2 implements the familiar second-order bandpass transfer function:

$$H_{BP}(s) = \frac{s\omega_o}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2} \tag{5.6}$$

with center frequency of ω_o, and quality factor of Q.

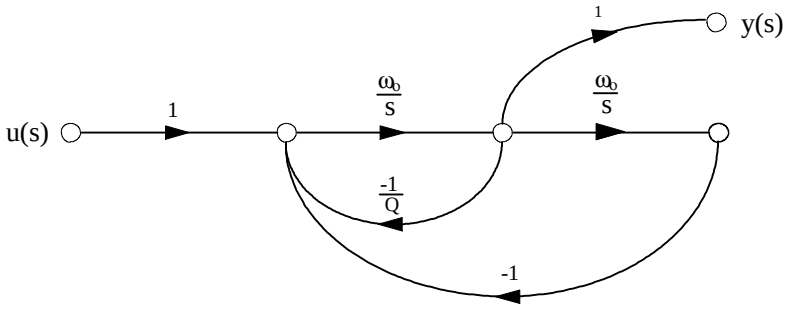

Figure 5.2: Flow diagram representation of filter structure.

A state-space description in the form of Equation (5.1) implies a particular filter structure. However, a desired transfer function expressed in the form of Equation (5.2) has many possible state space representations, and hence, can be realized by more than one structure. The selection of a particular structure must therefore be based on lower-level implementation issues. In active filter design, these issues include sensitivity to component variations, availability of component values, component matching considerations, and filter dynamic range.

Of all possible structures, those that have been found to have the most desirable properties include:

- State Variable
- Cascaded Biquad
- Follow-the-Leader, and

- Multiple Feedback

For the special case of high-Q bandpass active filter design, structures built around second-order resonators of the form expressed in Equation (5.6) have received the most attention [64] [68] [69] [75] [83] [90] [99]. Of these choices, the cascaded biquad structure has been implemented in some realizations [75] [83], and at least one reseacher has considered the follow-the-leader structure [68]. However, the simple coupled-resonator structure shown in Figure 5.3 has generally been preferred because of the following desirable features:

- It can be derived from low sensitivity ladder structures [64].
- It provides good equalization of gains across all nodes at all frequencies within the filter passband, and hence, has good dynamic range performance [68].
- Higher-order filters can be implemented using a set of identical second-order resonator sections [69].

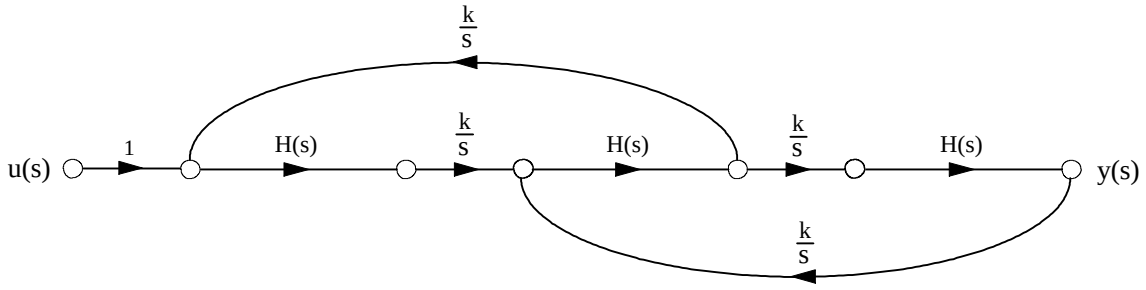

Figure 5.3: Coupled resonator bandpass filter structure.

Of these features, the ability to employ identical resonators represents perhaps the most significant advantage over competing approaches. This property allows a single second-order filter section to be designed and then replicated as needed to create higher-order responses, taking optimum advantage of the matching and temperature tracking features of monolithic IC fabrication processes.

Another important advantage of the coupled-resonator structure is its similarity to existing discrete RF and IF bandpass filter designs. Discrete filters ranging from monolithic crystal filters, to crystal ladders, tuned transformers, helical, dielectric resonator, and interdigital stripline designs are all based on the coupled resonator concept. Hence, they share similar gain and phase response characteristics, allowing on-chip filters to achieve comparable in-band responses simply by providing an equivalent number of resonator sections (equivalent number of poles).

5.1.2 Gm-C Filter Design

Having selected a filter structure, the next step in the design process is to realize a circuit-level implementation. In classic RC active filter design, circuit elements used consist of resistors, capacitors, and operational amplifiers. However, as noted in Chapter 2, the frequency of operation of these designs, as well as that of their on-chip "MOSFET-C" counterparts, is limited by the operational amplifiers employed.

To solve this problem, designers have moved to circuit implementations based on simple transconductance amplifiers such as that shown in Figure 5.4. These amplifiers can be used to perform multiplication by constants through appropriate choices of transistor geometries (W/L ratios), and can be used to implement integrations by loading the outputs with capacitors. Thus, filters based on these techniques are referred to as transconductor amplifier - capacitor (TAC), operational transconductance amplifier - capacitor (OTA-C), or simply transconductor - capacitor (Gm-C) designs.

In practice, transconductors are typically implemented in differential form using some variant of the configuration shown in Figure 5.5. Such differential transconductors have several attractive features including [82] [96]:

- simplification of bias circuit design;

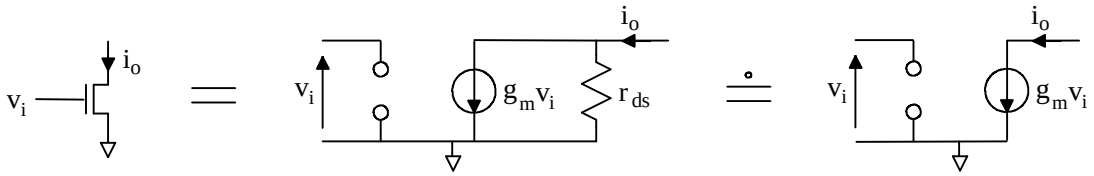

Figure 5.4: Simplified transconductance amplifier.

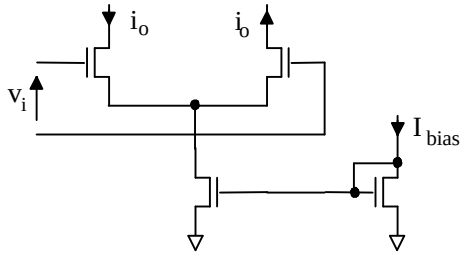

Figure 5.5: Practical differential transconductance amplifier.

- rejection of power supply noise and crosstalk from other circuits present on the same die;
- ability to create both inverted and non-inverted output signals; and
- ability to process signal voltages twice that possible in single-ended circuits with the same fidelity.

Although these features are interesting and important design considerations, they are not essential to the concepts covered in this chapter. Thus, the reader is directed to the cited references for additional low-level implementation details. In the discussions which follow, the simplified, single-ended form of Figure 5.4 will be assumed, with the understanding that similar results can be obtained with fully differential designs.

Using the Gm-C design approach, bandpass resonators can be constructed as shown in Figure 5.6. In this representation, symbols used in [75] have been adopted for the transcon-

ductors, and the ground reference for the transconductors is not explicitly shown.[1] Taking as states the voltages V_{C1} and V_{C2} on capacitors C1 and C2, this circuit can be redrawn in flow diagram form as shown in Figure 5.7, which can be shown to be structurally equivalent to that of Figure 5.2. Thus, if the output is taken to be the voltage V_{C1}, the transfer function is that of a second-order bandpass filter, and the center frequency, Q, and midband gain can be shown to be:

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \tag{5.7}$$

$$Q = \sqrt{\frac{C_1}{C_2}\frac{g_{m1}g_{m2}}{g_{mQ}^2}} \tag{5.8}$$

$$\left|\frac{V_{C1}}{V_i}\right|\Big|_{\omega_o} = \frac{g_{mi}}{g_{mQ}} \tag{5.9}$$

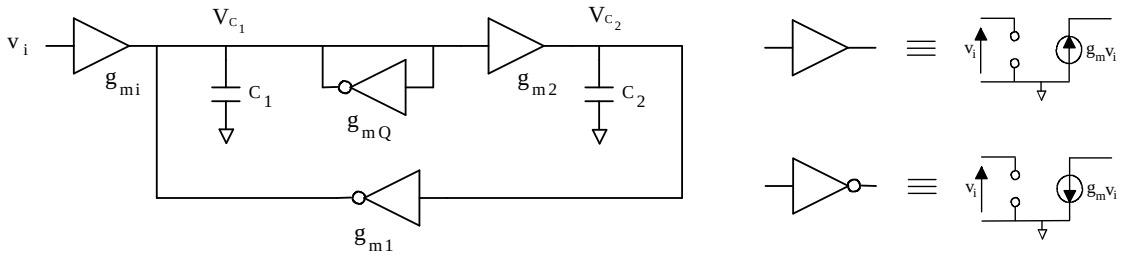

Figure 5.6: Gm-C based bandpass filter.

The degrees of freedom in selecting component values can be reduced by setting $g_{m1} = g_{m2} = g_m$ and $C_1 = C_2 = C$, yielding:

$$\omega_o = \frac{g_m}{C} \tag{5.10}$$

[1]The transconductor g_{m_Q}, which appears to be short circuited, actually draws current from the node common to its input and output, simulating a grounded resistor.

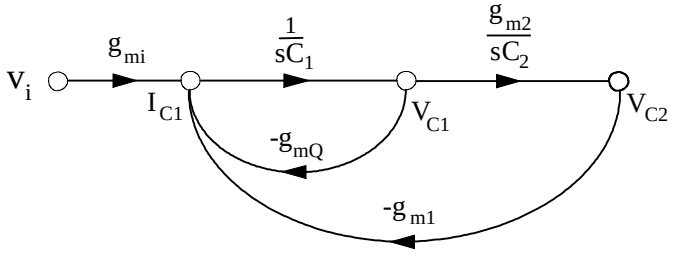

Figure 5.7: Flowgraph of Gm-C based bandpass filter.

$$Q = \frac{g_m}{g_{mQ}} \tag{5.11}$$

$$\left|\frac{V_{C1}}{V_i}\right|\Big|_{\omega_o} = \frac{g_{mi}}{g_{mQ}} \tag{5.12}$$

In addition to giving simpler formulas, this choice yields a circuit in which the gain from the input to each of the capacitor node voltages is equal — a necessary condition for maximizing the dynamic range [115].

An examination of Equations (5.10) - (5.12) produces two important observations related to filter tuning [75]. First, the resonator's center frequency is controlled by a ratio of transconductances and capacitances, which vary independently in IC fabrication processes. Thus, accurate frequencies cannot be realized, and some form of frequency tuning becomes a necessary part of the filter design process. Second, the filter's Q and midband gain are controlled by ratios of transconductances, which can be accurately achieved, making tuning of these parameters theoretically unnecessary. In practice, however, Q tuning may be required in designs operating at very high frequencies, depending on the circuit Q.

The need for Q tuning arises from practical limitations of transconductors such as drain-source conductances and drain/gate capacitances. These problems will be examined in Chapter 7 where tuning control systems designed to correct both frequency and Q errors will be described. A more fundamental problem, however, is that of limited dynamic range.

Qualitatively, dynamic range limitations in active filters arise from the need to recharge the circuit capacitances on each new cycle of the signal being processed. As will be shown in Chapter 6, the circuits used to perform this task consume significant power, and generate substantial noise in the process. These problems can be minimized if energy storage elements can be incorporated in the filter design, a feature offered by the approaches described in the following sections.

RLC Circuit Equivalence

The circuit of Figure 5.5 is equivalent to, and can be replaced by a classic, parallel RLC resonator excited by a current $I_i = g_{m_i} V_i$. To illustrate this fact, the Gm-C circuit is redrawn in Figure 5.8 with the R, L, and C component equivalences indicated. The corresponding RLC circuit is shown in Figure 5.9.

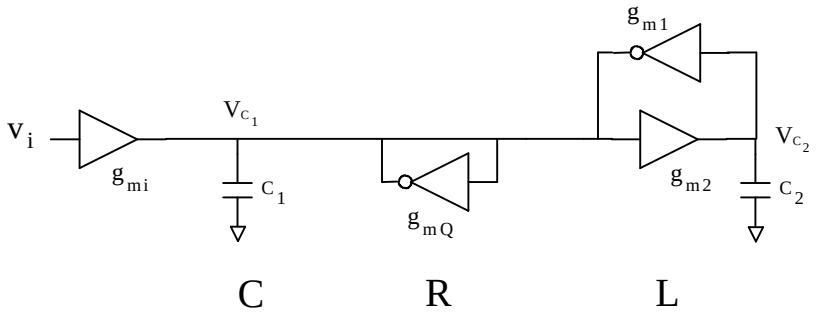

Figure 5.8: RLC equivalents in Gm-C resonator design.

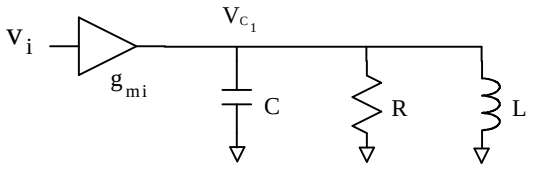

Figure 5.9: RLC resonator equivalent.

The equivalence of R to the g_{mQ} transconductance connected in negative feedback can be

seen by examining the current-voltage relationship of each. A voltage V applied to the transconductor results in a current $I = g_{mQ}V$, yielding an effective resistance of

$$R = \frac{1}{g_{mQ}} \tag{5.13}$$

With a little additional work, it can also be shown that the inductance L is simulated through the capacitively-loaded gyrator consisting of C_2, g_{m1}, and g_{m2}, yielding:

$$L = \frac{C_2}{g_{m1}g_{m2}} \tag{5.14}$$

Alternatively, this equivalence can be seen through a flow graph analysis by redrawing Figure 5.7 as shown in Figure 5.10. In this modified representation, capacitor currents have been shown explicitly, and the right-most node has been labeled I_L to indicate the simulated inductor current. For comparison, the flow graph of the RLC resonator circuit of Figure 5.9 is shown in Figure 5.11. An examination of Figures 5.10 and 5.11 then leads directly to (5.13) and (5.14).

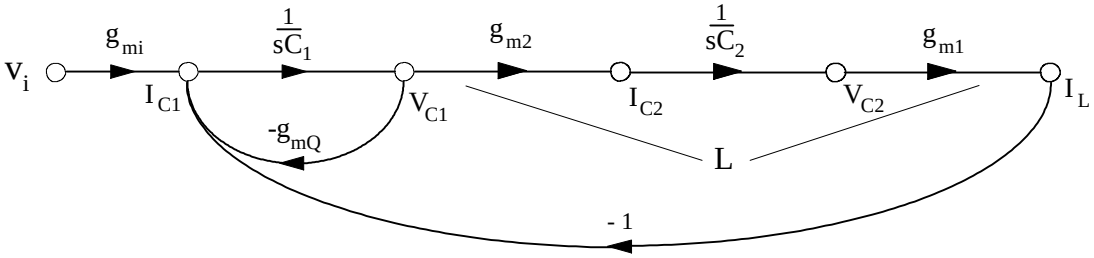

Figure 5.10: Gm-C filter flowgraph with currents and voltages labeled.

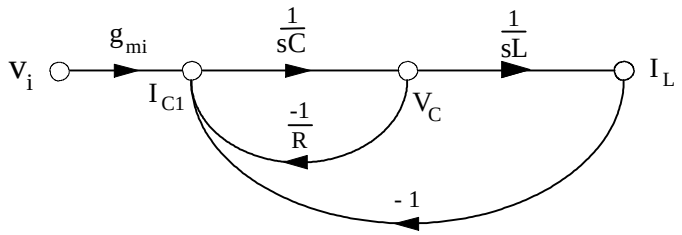

Figure 5.11: Equivalent RLC filter flowgraph.

5.1.3 Q-enhanced LC Filter Design

At frequencies above about 100 MHz, high-Q, Gm-C filters become difficult to implement due to parasitic capacitances in circuit elements and interconnects. In RLC designs, however, these parasitics can be absorbed into the tuned circuits, permitting operation at frequencies approaching the limits of the transistors employed. In addition, RLC designs can theoretically implement bandpass functions without the need for active circuits. However, as noted in Chapter 2, current IC technology limits achievable Q values of on-chip inductors to 10 and below, making integration of purely passive *high-Q* designs impossible.

Nevertheless, integrated RLC filters with $Q > 10$ can be realized if active circuits are admitted into the design process. These active circuits can be used to cancel losses in on-chip inductors, thereby enhancing the effective inductor Q.

To illustrate the fundamentals of the Q-enhanced filter design approach, consider the modified RLC resonator circuit shown in Figure 5.12, and its flowgraph equivalent in Figure 5.13.

Here, a lossy inductor is modeled near the circuit's resonant frequency as an ideal inductor in parallel with a loss resistance R_p. Connected in parallel with R_p is an active negative resistance implemented with a transconductor g_{m_n} arranged in a positive feedback config-

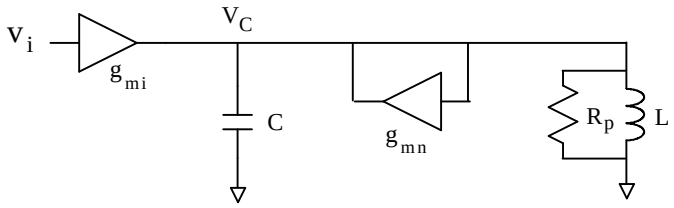

Figure 5.12: Q-enhanced RLC resonator circuit design.

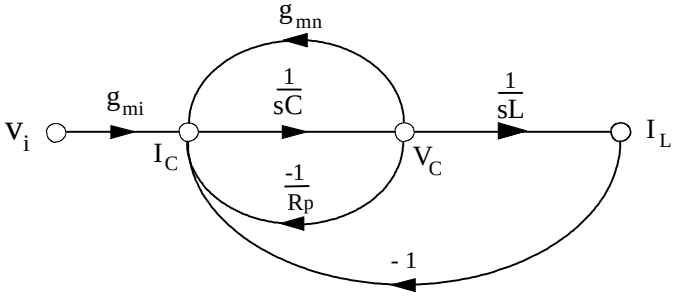

Figure 5.13: Q-enhanced RLC resonator flow diagram.

uration. The parallel combination of R_p and g_{m_n} yields an effective resistance value R_{eff} given by:

$$R_{eff} = R_p || -\frac{1}{g_{m_n}} = \frac{R_p}{1 - g_{m_n} R_p} \tag{5.15}$$

Based on the well-known relationships between inductor quality factor Q_o and the value of R_p, and between the parallel resistance, reactance, and Q of a resonant circuit, the effective Q of this resonator can be found from:

$$Q_{eff} = \frac{1}{1 - g_{m_n} R_p} Q_o \tag{5.16}$$

and can be made arbitrarily large by a suitable choice of g_{m_n}.

With the introduction of the transconductance g_{m_n}, this circuit becomes an active filter, and like the Gm-C design, the transconductor will consume power and add noise to the circuit. However, both the power consumption and the added noise will be significantly less than in the Gm-C case due to the energy storage and exchange that takes place in and between the (lossy) LC resonant circuit elements. These considerations will be addressed in detail in Chapter 6, where quantitative expressions for the DR of both types of filters will be derived and compared.

An additional problem with the Q-enhancement approach is the difficulty of achieving accurate and stable results at large effective Q values. In general, circuit parameters which control Q_o (metal sheet resistance and substrate losses) will be uncorrelated with those determining g_{m_n}, and some form of Q tuning will be necessary. In addition, frequency tuning will typically be required in all but the lowest Q designs due to variations in oxide thicknesses between different fabrication runs. Both of these issues can be addressed through the automatic tuning techniques discussed in Chapter 7, and the detailed circuit design

techniques discussed in Chapters 8 and 9.

5.2 Electro-Acoustic Filters

Before proceeding to a detailed discussion of dynamic range in the following chapter, it should be emphasized that the advantages offered by energy storage and exchange are not unique to LC resonators. These advantages can conceivably be realized by any technology in which these mechanisms exist.

One such technology which has been shown to be compatible with IC design, is the field of electro-acoustics [153] [167] [165]. Through the use of piezo-electric materials added to the fabrication process, devices can be constructed in which an electric field impressed across two capacitive electrodes develops localized stress and strain fields within the material. These fields then exchange energy in the same manner as electric and magnetic fields, leading to propagation of energy away from the source. The source electrodes, or electrodes placed at some other location within the material can then be used to couple acoustic energy back out of the acoustic fields and into the electric circuit. The velocity of propagation through the material is on the order of 3000 m/s, approximately 5 orders of magnitude lower than that of electro-magnetic energy in free space. Thus, filters operating at frequencies of 100 MHz or above can be constructed in areas of a few mm^2 or less, and become compatible with dimensions found in low-cost integrated circuits.

As discussed in Chapter 2, on-chip electro-acoustic filters in the form of both bulk acoustic wave (BAW) and surface acoustic wave (SAW) designs have been studied by various researchers over the past several years, and show considerable promise for use at VHF frequencies and above. Being passive, the resulting designs have significant advantages over both Gm-C and Q-enhanced LC filters in terms of both power consumption and potential dynamic range. To date however, these filters have not reached a suitable level of maturity

for commercialization, and several significant problems remain. Since experimental work in this area requires special fabrication technology not available at the author's institution, these filters will not be addressed further in this dissertation. Developments in the coming years will determine what role, if any, electro-acoustic filtering will play in the design and production of on-chip filters for low-cost commercial wireless products.

Chapter 6

Active Filter Dynamic Range

The dynamic range of an active filter may be defined as in Chapters 2 and 3 as:

$$DR = \frac{P_{max}}{P_{noise}} \tag{6.1}$$

where P_{max} is the maximum allowable signal level and P_{noise} is the noise floor measured in some defined bandwidth. Since P_{max} and P_{noise} must be taken at the same circuit node, an equivalent definition of dynamic range may be written in terms of voltages as:

$$DR = \frac{V_{max}^2}{V_{noise}^2} \tag{6.2}$$

where V_{max} is the maximum allowable signal voltage and V_{noise} is the total RMS noise voltage within the specified bandwidth. For active circuits, both P_{max} and V_{max} are functions of circuit biasing and power consumption and are often known constraints in the design process. Under this condition, DR is determined by the noise introducted by the circuit.

In order to compute either P_{noise} or V_{noise}, noise models for the circuit elements must be available. Models for capacitors, inductors, resistors, and transconductors which will be used in the discussions to follow are shown in Figure 6.1.

Ideal capacitors and inductors do not dissipate energy, and therefore generate no noise. Thus, the noise models for ideal capacitors and inductors are simply the elements themselves

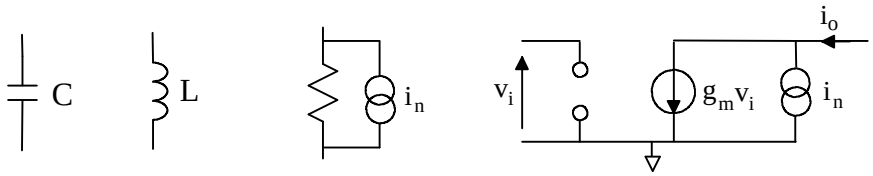

Figure 6.1: Noise models for circuit components.

with no noise sources present. Lossy capacitors and inductors generate noise equal to that of a resistor which gives equivalent energy losses. Thus, if an inductor is modeled as in Figure 5.12 with a parallel loss resistance R_p, the noise of the inductor is simply that of the resistor used to model the losses. For a resistance of value R, the one-sided RMS noise current density is [171] [177]:

$$i_n(f) = \sqrt{4kT\frac{1}{R}} \quad A/\sqrt{Hz} \tag{6.3}$$

where k is Boltzmann's constant, and T is temperature in degrees Kelvin.[1]

Finally, for a transconductor, the RMS noise current density may be approximated as [73]:

$$i_n(f) = \sqrt{4kTFg_m} \tag{6.4}$$

where g_m is the transconductance value and F is a noise figure which typically ranges between 1 and 2, and accounts for variations in the actual transconductor implementation. This model is approximately valid for transconductors created with FET or BJT devices, as well as those using source or emitter degeneration [65].

[1]Since the noise generated by the resistor is uncorrelated with other elements in the circuit, the noise current source is shown without a polarity indication.

Given these models, the noise level at any node or branch in a circuit may be found by computing the noise due to each source independently, and taking the RMS value of the individual contributions. This process will be used in the following sections to find the dynamic range of the Gm-C and Q-enhanced LC resonators discussed in the previous chapter.

6.1 Dynamic Range of Gm-C Filters

The dynamic range of a Gm-C filter may be found by augmenting the flowgraph of Figure 5.10 to show the noise currents injected into the circuit by each transconductor used. The resulting flowgraph is shown in Figure 6.2.

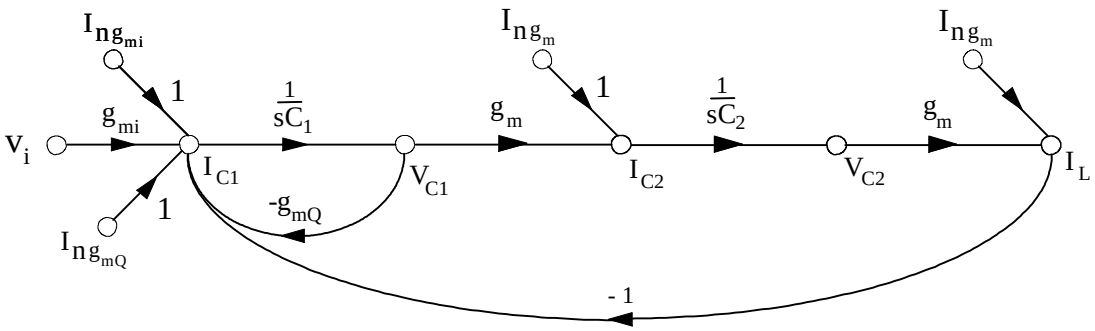

Figure 6.2: Gm-C flowgraph with noise sources included.

To simplify the following discussion, and to maximize the dynamic range [115], both the capacitors C_1 and C_2 and the transconductors g_{m1} and g_{m2} are assumed to be of equal value so that the resonant frequency ω_o, Q, and midband gain are given by Equations (5.10), (5.11), and (5.12), respectively.

The dynamic range of this circuit will be evaluated using Equation (6.2) by examining the signal and noise voltages at the output node V_{C1}. Assuming V_{max} on C1 is known, the dynamic range then depends on V_{noise} at this node alone.

To find V_{noise}, assume that the resonant frequency, Q, and capacitance are specified. Equations (5.10) and (5.11) can then be solved to find g_m and g_{mQ}. Assume also that g_{m_i} is set equal to g_{mQ} to give a midband gain of unity. The actual choice of g_{m_i} does not significantly affect the circuit's dynamic range provided $g_{m_i} \ll g_m$. Under this restriction, the noise produced by transconductor g_{m_i} will be significantly smaller than that produced by transconductor g_m feeding the same node, and may be neglected. Similarly, if Q is large, Equation (5.11) implies that $g_{mQ} \ll g_m$, so that the noise contribution of g_{mQ} may be neglected as well. The noise produced at the output node V_{C1} may then be found based solely on the noise contributions of the transconductors g_m feeding the capacitors.

An analysis of the closed-loop system shown in Figure 6.2 shows that the gain from both noise currents $I_{n_{gm}}$ to the current I_{C1} entering the integrating capacitor is:

$$\frac{I_{C1}}{I_{n_{gm}}} = \frac{s^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \tag{6.5}$$

which has magnitudes of 0, Q, and 1 at frequencies of 0, ω_o, and ∞, respectively. Thus, *at resonance*, both noise currents are amplified by the effective quality factor of the circuit, and when added on a power basis, yield a mean squared noise density at node I_{C1} of:

$$I_n^2(f_o) = 2(4kTFg_m)Q^2 \tag{6.6}$$

To translate this noise current to the noise voltage at the output node V_{C1}, Equation (6.6) is multiplied by the square magnitude of the capacitor's impedance, yielding:

$$V_n^2(f_o) = 2(4kTFg_m)Q^2\left(\frac{1}{\omega_o C}\right)^2 \tag{6.7}$$

Equation (6.6) gives the noise voltage power spectral density (PSD) at the center frequency of the filter only. The *total* mean squared noise voltage at node V_{C1} is found by integrating

the PSD across all frequencies. Since the noise spectrum is shaped by the filter transfer function, the total mean square noise voltage may be found from:

$$V_{noise}^2 = \int_0^\infty V_n^2(f_o)|H(f)|^2 df \tag{6.8}$$

where $H(f)$ is a second-order resonance curve with center frequency f_o, quality factor Q, and midband gain of 1. Since $V_n^2(f_o)$ is a constant with respect to the integration, it can be removed from the integrand. The remaining integral is then the definition of the noise bandwidth B_n of the filter, which for a high-Q second-order resonator is given by the well-known result:

$$B_n = \frac{\pi}{2}\frac{f_o}{Q} \tag{6.9}$$

Combining equations (6.7) – (6.9) with the expression for ω_o given in equation (5.10), then yields:

$$V_{noise}^2 = 2kTF\frac{Q}{C} \tag{6.10}$$

This expression for V_{noise}^2, which is typical of equations found in the literature, shows a scaling of noise by the quality factor of the filter if capacitance is held constant. To complete the evaluation of dynamic range, Equation (6.10) can be combined with Equation (6.2) to give

$$DR = \frac{V_{max}^2 C}{2kTFQ} \tag{6.11}$$

suggesting that dynamic range scales inversely as the filter Q.

6.1.1 Optimum Dynamic Range

Equation (6.11) gives the dynamic range for the particular Gm-C second-order resonator of Figures 5.5. However, it is not clear whether other possible filter structures could achieve a better result. In addition, the dynamic range of higher-order filters has not yet been addressed. These issues were investigated by Groenewold in his Ph.D work at Delft University in 1992 and formed the basis of his disseration [116]. By returning to the general state space description of a linear filter in (5.1), Groenewold showed that the *best possible* dynamic range for a high-Q second-order active filter biquad is given by (6.11).[2] Thus, we can conclude that the filter in Figure 5.6 is in fact an optimal design.

In addition to this result for a high-Q resonator, Groenewold derived the following bound for the dynamic range of higher-order bandpass filters [115]:

$$DR \leq \frac{V_{max}^2 C}{2\pi kTFQ} \tag{6.12}$$

This result, which differs from that in (6.11) only by a small constant, indicates that the optimum dynamic range for a high-order filter is essentially limited to that of a simple resonator design. To understand how such a dynamic range might be achieved in practice, consider the coupled resonator structure of Figure 6.3.

As shown, coupling can be achieved either with capacitors, or with small transconductors whose values are selected to give a voltage gain of approximately 1 from one resonator to the next. In either case, the coupling circuits introduce negligible additional noise into the circuit compared with that of the gyrator transconductors used in the resonator core. Moreover, since the interstage gain is 1, the noise injected into any given resonator from neighboring resonators will be at most equal in magnitude to the noise generated within

[2] Groenwold's result differs from the result here by a factor of 2. This discrepancy arises from differing definitions used for C, which in [115] is defined as the total capacitance of the two integrators combined.

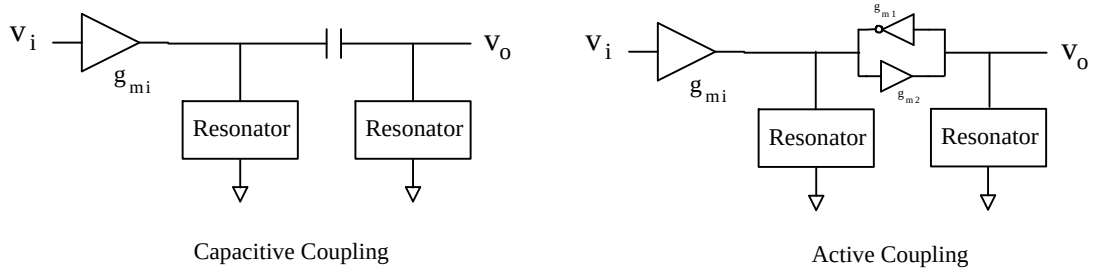

Figure 6.3: Gm-C based coupled resonator filters.

the resonator itself. Thus, the dynamic range of the overall high-order filter is seen to be close to that of the core resonator on which it is built.[3]

6.1.2 Dynamic Range Versus Power Consumption and Bandwidth

Dynamic range expressions such as (6.11) are common in the literature, and have led to the widespread notion that the dynamic range of active bandpass filters is inversely proportional to their quality factor. This conclusion, while correct if C is taken as a constant, is at best misleading. As shown below, dynamic range actually varies inversely as the *square* of the filter Q under conditions of constant power consumption and constant bandwidth.

Fundamentally, all active circuits have a limited dynamic range. Their maximum signal handling capability is limited by their power consumption, while their minimum signal handling capability is limited by thermal and shot noise, and by the bandwidth in which the noise is measured. Yet in (6.11), neither the power consumption nor the filter bandwidth appear explicitly, preventing a direct comparison of filter and system dynamic range performance.

For example, in an amplifier or active mixer circuit used within a radio receiver, the maximum output signal is limited to some fraction η of the DC power P_{DC} consumed, while the

[3]Similar reasoning can also be applied to the cascaded biquad filter structure with similar results.

noise at the output is proportional to the thermal noise kTB, the noise figure F, and the circuit gain G. Thus, the dynamic range may be written in the form:

$$DR = \frac{\eta P_{DC}}{kTBFG} \tag{6.13}$$

In Chapter 3, these concepts were used to illustrate that radio receiver blocking and spurious free dynamic range are fundamentally limited by power consumption and gain of active circuits that precede the IF channel select filters. If the dynamic range of an integrated filter is to be compared with these dynamic range performance measures, Equation (6.11) must be recast in a form similar to that of (6.13).

The effect of power consumption on filter dynamic range was briefly addressed in Groenewold's dissertation, resulting in an expression showing that dynamic range is inversely proportional to the product of center frequency and Q [116].[4]

$$DR \sim \frac{P_{DC}}{f_o Q} \tag{6.14}$$

However, the important issue of bandwidth was ignored. This oversight is easily corrected by replacing the frequency of operation with the product of bandwidth and Q:

$$f_o = BQ \tag{6.15}$$

yielding a result that is inversely proportional to the *square* of the filter Q.

$$DR \sim \frac{P_{DC}}{BQ^2} \tag{6.16}$$

[4]Similar conclusions have been reached by others (c.f. [110] [94]), all leading to the conclusion that DR is inversely proportional to Q.

A full expression for filter dynamic range showing this dependence can be derived using (6.11) together with basic circuit analysis concepts. For the filter of Figure 5.5, the maximum signal current i_{max} that can be delivered to the integrating capacitors is limited by the transconductor's bias current I_{bias}.[5]

$$i_{max} \leq I_{bias} \tag{6.17}$$

Similarly, the maximum signal voltage on the capacitors v_{max} must be less than the supply voltage V_{DC}.

$$v_{max} \leq V_{DC} \tag{6.18}$$

Thus, the product of v_{max} and i_{max} is less than the DC power consumed, as expected:

$$v_{max} i_{max} \leq P_{DC} \tag{6.19}$$

Equation (6.19) can be rewritten as an equality if a suitable efficiency factor η is defined to account for the ratio of v_{max} to V_{DC}, the ratio of i_{max} to I_{bias}, and the ratio of I_{bias} to the total filter current consumption I_{DC}.

$$P_{DC} = \frac{1}{\eta} v_{max} i_{max} \tag{6.20}$$

$$\eta \equiv \frac{v_{max}}{V_{DC}} \frac{i_{max}}{I_{bias}} \frac{I_{bias}}{I_{DC}} \tag{6.21}$$

[5]This assumes class A operation which is typically used in small signal circuit design. However, other modes of operation can be taken into account with a suitable definition for efficiency η.

Finally, for a filter with a given capacitance C, v_{max} and i_{max} are related by the capacitive susceptance $\omega_o C$, giving:

$$i_{max} = v_{max}\omega_o C \tag{6.22}$$

Thus, combining Equations (6.15), (6.20), and (6.22) with Equation (6.11) yields:

$$DR = \frac{\eta P_{DC}}{4\pi kTFBQ^2} \tag{6.23}$$

which can now be compared directly with the performance of the amplifier circuit expressed in (6.13).

The significance of the dynamic range degradation with Q is perhaps best illustrated by a numerical example. Suppose that a filter with a Q of 50 and a bandwidth of 25 KHz is needed in a low power handheld receiver. In Chapter 3, the dynamic range of such a receiver was investigated and found to be on the order of 90 dB.[6] This level of performance was based on amplifiers with output compression points of 0 dBm, implying a power consumption on the order of 20 mW, assuming 10% efficiency.

Using (6.23), the minimum power consumption (per pole) of a Gm-C filter satisfying this dynamic range requirement can now be found. If an efficiency of $\eta = 0.1$ and a noise figure of $F = 2$ are assumed, the minimum power needed is 63 mW per pole. Thus, a 3-pole design would require 189 mW. In practice, obtaining an efficiency of 0.1 in a Gm-C circuit may be difficult due to MOSFET linearity problems. Repeating the calculation with a more realistic value of $\eta = 0.01$, a power consumption of 630 mW per pole, or nearly 2 watts for a 3-pole design is found. Clearly, this is unacceptable in a low power, battery operated receiver design.

[6]The actual result was 81 dB, but included a 10 dB C/N bias not accounted for by (6.23).

6.2 Dynamic Range of Q-Enhanced LC Filters

The dynamic range problems of Gm-C filters can be traced to two primary causes:

- the power required to charge the capacitors in each new cycle, and
- the excess noise generated by transconductors operating at large currents.

In Chapter 5, it was postulated that energy storage and exchange in Q-enhanced filters could help reduce both factors, resulting in substantial improvements in dynamic range performance. In this section, these improvements will be demonstrated quantitatively.

The dynamic range of Q-enhanced LC filters filters could be derived directly using an approach similar to that taken for the Gm-C case, and then compared with (6.23). However, the fundamental mechanisms responsible are better illustrated if the derivation is leveraged off previous results. Thus, in the following analysis, the noise sources present in the flow diagrams of the two circuits will be compared first. This leads to the observation that the noise in the Q-enhanced LC filter is reduced over that of the Gm-C design by a factor of Q_o, where Q_o is the base Q of the passive (un-enhanced) LC resonator on which the filter is built. Then, the currents required in the Q-enhanced LC circuit are examined and shown to be a factor of Q_o less than those in the Gm-C design. Finally, these results are combined to show a total improvement of Q_o^2 when power consumption is held constant.

The Q-enhanced LC resonator flow diagram of Figure 5.13 is redrawn in Figure 6.4 with the noise souces added. Of the three noise sources shown, the source associated with g_{m_i} can be neglected for reasons identical to those stated in the Gm-C filter case. An examination of Equation (5.16) then shows that for $Q \gg Q_o$,

$$g_{m_n} \approx \frac{1}{R_p} \tag{6.24}$$

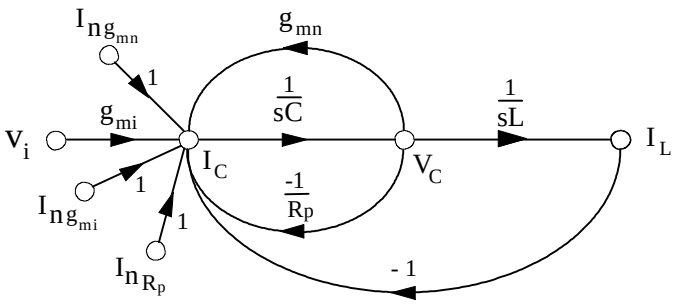

Figure 6.4: Q-enhanced resonator flow diagram with noise sources.

Hence, by (6.3) and (6.4), the noise current power spectral density from the loss resistance and the transconductor are approximately equal and can be estimated as:

$$i^2_{n_{Rp}}(f_o) \approx 4kTg_{m_n} \tag{6.25}$$

$$i^2_{n_{gm}}(f_o) \approx 4kTFg_{m_n} \tag{6.26}$$

As in the Gm-C filter case, these two sources are multiplied by the factor Q to find the noise current entering the capacitor, and when converted to the voltage on the capacitor, yield:

$$v^2_n(f_o) \approx (4kT(F+1)g_{m_n})Q^2\left(\frac{1}{\omega_o C}\right)^2 \tag{6.27}$$

However, in the Q-enhanced LC filter case, g_{m_n} is given by:

$$g_{m_n} \approx \frac{1}{R_p} = \frac{1}{Q_o \frac{1}{\omega_o C}} \tag{6.28}$$

Combining this with (5.10) for the Gm-C filter's resonant frequency ω_o yields

$$g_{m_n} \approx \frac{1}{Q_o} g_m \tag{6.29}$$

where g_m is the Gm-C filter's transconductance value.

Thus, the noise originating from the loss resistance and the negative resistance circuit tranconductance used in the Q-enhanced LC filter is a factor of Q_o less than that from the two transconductances used in the Gm-C filter. The desired result then follows immediately from analogy with (6.11):

$$DR \approx \frac{V_{max}^2 C}{kT(F+1)Q} Q_o \tag{6.30}$$

Dynamic Range Versus Power Consumption and Bandwidth

To complete the comparison of the two filters, an expression in the form of (6.23) must now be derived. In the Gm-C filter, transconductors drive the circuit capacitances directly and must supply all current necessary to charge the capacitors to the designed voltage v_{max}, resulting in the current i_{max} given by (6.22). However, in the Q-enhanced LC filter, the current i_{max} needed from the transconductor is only that required to make up for losses in the inductor. Thus,

$$i_{max} = \frac{v_{max}}{R_p} = \frac{v_{max}}{Q_o \frac{1}{\omega_o C}} = \frac{1}{Q_o} v_{max} \omega_o C \tag{6.31}$$

which is a factor of Q_o less than in (6.22). Thus, the Q-enhanced LC filter achieves a power reduction of Q_o at the same time the dynamic range is improved.

To cast this result in a form that can be compared directly with (6.23), (6.31) can be combined with (6.20) and (6.30) to give:

$$DR \approx \frac{\eta P_{DC}}{2\pi kT(F+1)BQ^2} Q_o^2 \tag{6.32}$$

This is a significant improvement, even for the case of low quality factor inductors. For example, if $Q_o = 5$, the dynamic range improvement (assuming other factors are equal) is over 14 dB. Alternatively, for the same dynamic range as a Gm-C filter, the Q-enhanced LC filter requires over an order of magnitude less power.

Returning to the numerical example used for the Gm-C filter, a 90 dB dynamic range Q-enhanced LC filter with $B = 25$ KHz, $Q = 50$, and $Q_o = 5$ requires only 1.9 mW per pole if $\eta = 0.1$ and $F = 2$ are assumed. Even for the more practical case of $\eta = 0.01$, the power is 19 mW per pole, and is still compatible with the 20 mW per amplifier consumption of the example receiver design.

6.3 Relationship of Filter Dynamic Range to Receiver Dynamic Range

Applications for integrated bandpass filters within radio receivers fall into two major categories: preselect filters, and channel select filters. In the preceding sections, the bandwidth B used in deriving (6.23) and (6.32) was the 3 dB bandwidth of the filter resonator. For channel select filters, this bandwidth can be assumed to be approximately equal to the width of the radio channel, and hence the noise bandwidth seen by the receiver's demodulator. Thus, (6.23) and (6.32) can be used directly to upper bound the instantaneous *in-band* dynamic range of a receiver in which the filter is used.[7] However, for preselect filters, the filter bandwidth is generally wider than the radio channel, and (6.23) and (6.32) require

[7]The term instantaneous is used here to emphasize that the total dynamic range of the receiver can be higher due to the use of AGC or attenuators as discussed in Chapter 3.

modification.

For preselect filters, the noise actually seen by the receiver's demodulator is reduced by the IF channel select filter according to

$$\frac{P_{n_{IF}}}{P_{n_{filt}}} = \frac{B_{n_{IF}}}{B_{n_{filt}}} \tag{6.33}$$

where $P_{n_{IF}}$ is the noise power measured in the IF filter's noise bandwidth $B_{n_{IF}}$, and $P_{n_{filt}}$ is the noise power measured in the preselect filter's noise bandwidth $B_{n_{filt}}$. Thus, the dynamic range measured at the receiver's detector will be a factor of $\frac{B_{n_{filt}}}{B_{n_{IF}}}$ larger than that suggested by (6.23) and (6.32).

Combining (6.33) with the dynamic range expressions in (6.23) and (6.32), and with the resonator noise bandwidth in (6.9) yields the following results for the instantaneous dynamic range of active preselect filters:

$$DR_{Gm-C} \approx \frac{\eta P_{DC}}{8kTFB_{n_{IF}}Q^2} \tag{6.34}$$

$$DR_{QE-LC} \approx \frac{\eta P_{DC}}{4kT(F+1)B_{n_{IF}}Q^2}Q_o^2 \tag{6.35}$$

6.4 Blocking and Spurious Free Dynamic Range

Expressions (6.23), (6.32) and (6.34), (6.35) provide upper bounds on the *instantaneous total* dynamic range of a receiver employing Gm-C and Q-enhanced LC filters. However, as noted in Chapter 3, the total dynamic range of a receiver can be increased through AGC and switchable attenuator circuits, and is therefore not a major concern. The most critical dynamic range measures are, instead, those that determine the receiver's ability to function

relative to out-of-band interferers. Thus, the blocking dynamic range and spurious free dynamic range of the filters are critical performance concerns.

If the efficiency used in evaluating (6.23), (6.32), (6.34), and (6.35) is defined as the ratio of the 1 dB compression signal power to the DC power consumed, then these expressions can be used to estimate the filter's BDR relative to *in-band* signals. The in-band SFDR can then be estimated through (3.24), provided the BDR is properly converted to dB. For preselect filters, these equations will give reasonable bounds on receiver performance relative to signals that fall within the service band. However, for signals which fall outside the service band, or for the case of IF filters where interferers are necessarily outside the passband of the filter, further study is needed.

In the following analysis, assume that the filter in question is a single second-order resonator of the form shown in Figure 5.5 or Figure 5.12, and that the input transconductor g_{m_i} is chosen to provide a voltage gain greater than 1. Under this condition, signal compression will be produced by nonlinearities at the filter's output before being produced in the input transconductor's voltage to current transfer characteristic.

The output compression point will be set by the filter's power consumption, and will be essentially the same for signals inside or outside the filter passband. However, since the gain of the filter is a function of frequency, the *input* compression point will be larger for signals outside the passband than for those within the passband and the effective BDR will be higher than predicted by (6.23), (6.32), (6.34), and (6.35).

These effects may be most easily quantified by adopting the terminology of Chapter 3 in which powers and gains are written in dBm and dB respectively. Let the compression point and the noise floor referred to the input (in dBm) be written as P_{c_i} and MDS, respectively. Then the BDR may be expressed in dB as:

$$BDR = P_{c_i} - MDS \tag{6.36}$$

If the filter has a power gain G in dB, then the output compression point P_{c_o} may be written (in dBm) as

$$P_{c_o} = P_{c_i} + G \tag{6.37}$$

which may be combined with (6.36), to yield:

$$BDR = P_{c_o} - G - MDS \tag{6.38}$$

In this equation, both P_{c_o} and MDS are fixed, but the gain term G varies with frequency f. For signals outside the filter passband, G may be approximated as:

$$G(f) = G_o - 20log\left|\frac{f - f_o}{B/2}\right| \tag{6.39}$$

where G_o is the midband gain, f_o is the center frequency, and B is the 3 dB bandwidth. Inserting (6.39) into (6.38), and combining with (6.36) and (6.37), the BDR may then be written as:

$$BDR(f) = BDR(f_o) + 20log\left|\frac{f - f_o}{B/2}\right| \tag{6.40}$$

Thus, BDR is found to improve with frequency offset as anticipated. For a preselect filter, this improvement occurs only for signals outside the service band. However, for an IF channel select design, the improvement occurs for signals inside the service band and can be significant even at relatively small frequency offsets. For example, evaluation of equation

(6.40) yields 6 and 12 dB increases for the cases of adjacent and alternate channel interferers respectively.

Variations in SFDR with frequency offset can be derived similarly, and are found to be

$$SFDR(f) = SFDR(f_o) + 20log\left|\frac{f - f_o}{B/2}\right| + 2 \tag{6.41}$$

where the additional factor of 2 dB results from the fact that the second tone in the two tone signal used in the SFDR measurement is at a frequency of $2(f - f_o)$, and is therefore attenuated more than the tone at $f - f_o$.

The ultimate dynamic range performance at large offsets is determined by nonlinearities in the input transconductor's voltage to current transfer function and can be very high, even in low power designs. For example, with a MOSFET-based transconductor biased at 1 V above threshold, and a 1 KΩ source impedance, the 1 dB compression point referred to the filter input will be on the order of 1 mW or 0 dBm. If the input signal noise floor is -120 dBm, the ultimate BDR at large signal offsets will approach 120 dB.

Higher-Order Filters

Equations (6.40) and (6.41) were derived for the case of a simple second-order resonator. To extend these results to higher-order filter designs, the structure of the higher-order filter must be considered. The improvement will depend on how the gain from the filter input to each internal node within the filter varies with frequency. The limiting factor will be the node at which saturation first occurs.

For example, Figure 6.5 shows transfer functions from the input of a fourth-order (2-pole) coupled resonator filter to the capacitor node in each of the filter's two resonator sections. The effect of coupling is a broadening of the first resonator's bandwidth and the creation of

the desired two-pole response at the second resonator's output. However, the filter rolloff to the first resonator is still that of a single-pole transfer function. Thus, the equations derived above for the simple resonator remain valid in this higher-order design provided suitable adjustments are made for the bandwidth B.

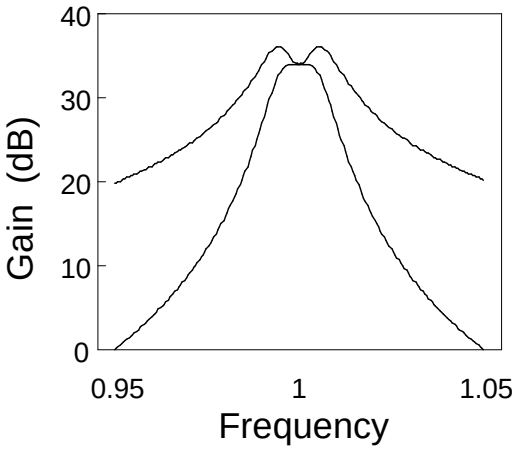

Figure 6.5: Transfer functions to internal nodes in coupled resonator filter.

Although it is possible to design filters in which the response to all internal nodes is N-pole, preliminary analysis of these filter structures suggests that they possess a significantly degraded initial in-band dynamic range. Thus, they would possess an overall inferior dynamic range performance relative to that of the coupled resonator structure assumed here.

6.5 Limitations on Filter Q

The dynamic range of Gm-C filters has been extensively studied in the literature and is described as being inversely proportional to Q. However, as shown in this chapter, the dynamic range of these filters is actually inversely proportional to the *square* of the filter Q when power consumption and bandwidth are held constant.

To understand this result and the limits it places on Q values of active filters used in radio receivers, consider the case of a receiver front-end design such as that shown in Figure 6.6a in which a passive preselect filter is employed. Although the passive filter may have very high dynamic range by itself, downstream active circuits within the receiver will limit the maximum signal levels allowed, and thus the dynamic range of the system as a whole.

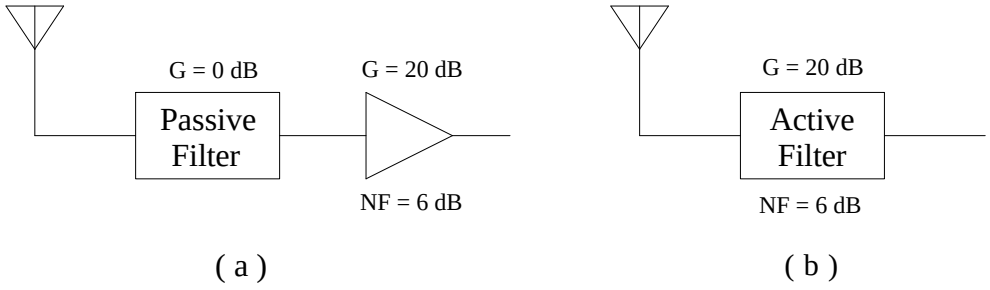

Figure 6.6: Receiver front-ends employing a) passive filter, and b) active filter.

The dynamic range of this system when used in a receiver with a signal or IF bandwidth $B_{n_{IF}}$, can be written in the form:

$$DR = \frac{P_{co}}{kTFGB_{n_{IF}}} \tag{6.42}$$

where P_{co} is the amplifier's output compression point, F and G are the amplifier's noise figure and gain, respectively, and k and T have their usual meanings. For simplicity, the insertion loss of the filter is assumed to be zero.

In general, P_{co} will be limited by the amplifier's power consumption P_{DC} and efficiency η, so that (6.42) may be rewritten as:

$$DR = \frac{\eta P_{DC}}{kTFGB_{n_{IF}}} \tag{6.43}$$

Hence, in this system dynamic range is seen to be independent of filter Q. For example, a system employing a 1 MHz filter centered at 10 MHz ($Q_1 = 10$) will have the same dynamic range as a system employing a 1 MHz filter centered at 100 MHz ($Q_2 = 100$). In an active filter implementation, however, the dynamic range of the 100 MHz filter will be a factor of $(Q_2/Q_1)^2 = 100$ less than that of the 10 MHz filter due to the higher Q needed to obtain the smaller fractional bandwidth.

This degradation comes about because the only way to raise the Q of the active filter without increasing its power consumption is to hold the capacitive reactances constant. Thus, to raise the filter Q, the transconductance g_{m_Q} in the Gm-C filter design must be decreased, or the equivalent parallel resistance in the Q-enhanced LC filters must be increased. In either case, the principal noise sources in the circuit remain constant, but the gain of the filter from the noise sources to the filter output rises, increasing the filter's noise floor and lowering the dynamic range. Thus, degradation in dynamic range can be viewed as the result of increases in regenerative gain needed to realize the desired Q.

However, a moderate amount of gain can be tolerated and is needed in a receiver front-end to maintain good noise performance as discussed in Chapter 3. Thus, filters with $Q > 1$ may be acceptable, despite their inherent dynamic range degradations, if Q is limited to moderate values. In the receiver implementation of Figure 6.6a, the gain that degrades receiver dynamic range is that of the amplifier, whereas in the active filter implementation in Figure 6.6b, the gain is an integral component of the Q enhancement process and can be provided by the filter itself.

The *in-band* dynamic range of these two systems can be compared by taking the ratio of Equations (6.42) and (6.34) with appropriate subscripts added to distinguish the terms in each expression. For the case of a Gm-C active preselect filter, the following expression results:

$$\frac{DR_{passive}}{DR_{Gm-C}} = \frac{\eta_{passive}}{\eta_{Gm-C}} \frac{F_{Gm-C}}{F_{passive}} \frac{P_{DC_{passive}}}{P_{DC_{Gm-C}}} \frac{8Q^2}{G} \tag{6.44}$$

By specifying that the powers for the two systems should be equal, and by making the simplifying assumption that similar efficiencies and noise figures can be achieved in the two cases, (6.44) can then be solved for the maximum allowable filter Q that will prevent in-band dynamic range degradation in the overall receiver system:

$$Q_{max_{Gm-C}} \approx \sqrt{\frac{G}{8}} = 0.35\sqrt{G} \tag{6.45}$$

Repeating this analysis for the case of Q-enhanced LC filters, yields the result:

$$Q_{max_{QE-LC}} \approx \sqrt{\frac{G}{8}} Q_o = 0.35\sqrt{G} Q_o \tag{6.46}$$

To determine numerical values for Q, the gain G must be specified. Depending on system performance requirements and cost factors, typical receiver designs may use gains ranging from 10 dB to 40 dB within the front-end and down-converter circuits preceding the IF filter. Thus, it is instructive to tabulate Q_{max} values for cases with G varying between these values. The results are shown in Table 6.1.

Table 6.1: Approximate upper bounds on active filter Q when used in radio receivers.

System Gain	$Q_{max_{Gm-C}}$	$Q_{max_{QE-LC}}$		
		$Q_o = 2.5$	$Q_o = 5$	$Q_o = 10$
10 dB	1.1	2.8	5.5	11
20 dB	3.5	8.8	18	35
30 dB	11	28	55	110
40 dB	35	88	175	350

In using Table 6.1, it is important to remember that the derivation of (6.45) and (6.46)

assumed similar noise figures and efficiencies could be achieved in the two systems. Moreover, the power consumption of only a single resonator was accounted for, and the case of out-of-band dynamic range performance was not considered. Thus, these results should be used only as a preliminay guide.

Equations similar to (6.45) and (6.46) can be derived for the case of IF filters. However, in this case, higher Q values can be tolerated because the signals causing blocking and intermodulation distortion are necessarily outside the filter passband. The increase in allowable Q will depend on what interference signals are expected. If the system design precludes the existance of large adjacent channel signals, then the worst case interferers will reside in alternate radio channels and an improvement of 6 to 12 dB can be expected depending on the details of the filter design. This can be used to buy an additional factor of 2 to 4 in Q, or to make up for the increased power consumption of a high-order filter design.

Chapter 7

Tuning Techniques for Active Filters

In addition to dynamic range limitations discussed in Chapter 6, continuous-time integrated active filters suffer from significant center frequency and quality factor errors, especially when operating at high Q (e.g. $Q > 10$). These problems generally require the incorporation of some form of frequency and/or Q tuning control system into the filter design.

In this chapter, the major tuning control systems that have been proposed in the literature are reviewed and a new class of techniques referred to as orthogonal reference tuning (ORT) is investigated in detail. In addition, several simplifications of control system designs are proposed. Before proceeding with these discussions, however, some introductory remarks are presented to illustrate the need for tuning control.

7.1 The Need for Filter Tuning

The need for tuning of active, continuous-time filters was introduced briefly in Chapter 5. In the case of a Gm-C design, the filter's center frequency ω_o and quality factor Q were derived in terms of the transconductances and capacitances used, and were found to be:

$$\omega_o = \frac{g_m}{C} \tag{7.1}$$

$$Q = \frac{g_m}{g_{mQ}} \tag{7.2}$$

Since transconductances and capacitances in integrated circuits have large tolerances (typically ±10% or higher [97]), and their deviations are largely uncorrelated, equation (7.1) suggests that initial frequency errors of ±20% or more can be expected. In contrast, matching and tracking of like components on an integrated circuit can be as tight as ±0.1% [175] [97]. Thus, (7.2) suggests that Q accuracies as good as ±0.2% may be feasible. In practice, however, the Q of high frequency Gm-C filters is a more complex function of circuit parameters than suggested by (7.2), and further discussion is needed.

The derivation of (7.2) was based on the assumption that ideal transconductors and integrators can be created. At low frequencies (e.g. < 1 MHz), this assumption is valid since transconductors with very high output resistances can be realized with the cascode design approach illustrated in Figure 7.1. At low frequencies, cascoded transconductors can be loaded with capacitances to form integrators with precise 90^o phase shifts at the filter's natural frequency ω_o. As long as ω_o is sufficiently low relative to that of the parsitic pole ω_p introduced at the internal node between the two transistors, the existence of parasitics can be ignored in the design.

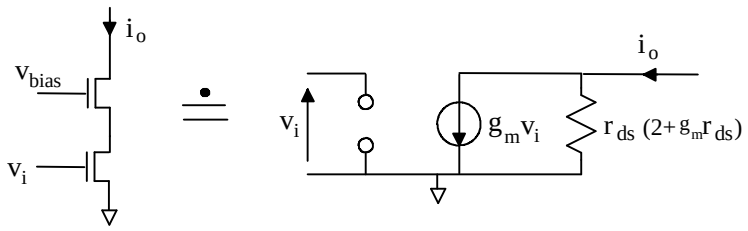

Figure 7.1: Use of cascode design to raise circuit output resistance.

The required separation between ω_o and ω_p, however, is a function of the filter Q. In high Q designs, transfer function distortions and stability problems can occur even when ω_p is several orders of magnitude above ω_o [99]. To see this, consider the modified resonator flow diagram shown in Figure 7.2 in which the effect of the pole at ω_p in each transconductor has been represented by small phase errors added to the nominal -90^o integrator phase.

The effect of the pole can be modeled as a multiplication of the effective transconductor value by:

$$P(s) = \frac{\omega_p}{s + \omega_p} \tag{7.3}$$

and for $\omega_o \ll \omega_p$, the phase error introduced can be approximated at $\omega = \omega_o$ by:

$$\theta = \angle \frac{\omega_p}{j\omega_o + \omega_p} \approx -\frac{\omega_o}{\omega_p} \quad radians \tag{7.4}$$

From the derivation shown in Figure 7.2, the main effect of excess integrator phase is seen to be an enhancement of the resonator Q, and the effective Q may be found in terms of the ratio of ω_o and ω_p as:

$$Q_{eff} = \frac{1}{\frac{1}{Q} + 2\theta} = \frac{Q}{1 - 2\frac{\omega_o}{\omega_p}Q} \tag{7.5}$$

Evaluation of (7.5) shows that a filter with $Q = 100$ will experience a 10% Q increase for $\omega_p = 2000\omega_o$, while for $\omega_p = 200\omega_o$, the same filter would oscillate. These two cases correspond to filters with center frequencies of 1 MHz and 10 MHz implemented in a process with $f_T > 2$ GHz, clearly illustrating the practical problems associated with extending Gm-C bandpass filter designs to higher frequencies.

Various approaches exist, of course, for correcting the Q errors predicted by (7.5). The simplest is to increase the intentional damping term $\frac{1}{Q}$ by increasing the transconductance g_{mQ}, while a more robust approach described in [99] introduces a pole-zero pair to correct effects over a wider frequency range. Both approaches, however, involve the use of circuits which do not match or track the ratio $\frac{\omega_o}{\omega_p}$ accurately enough to avoid the use of post-fabrication Q tuning.

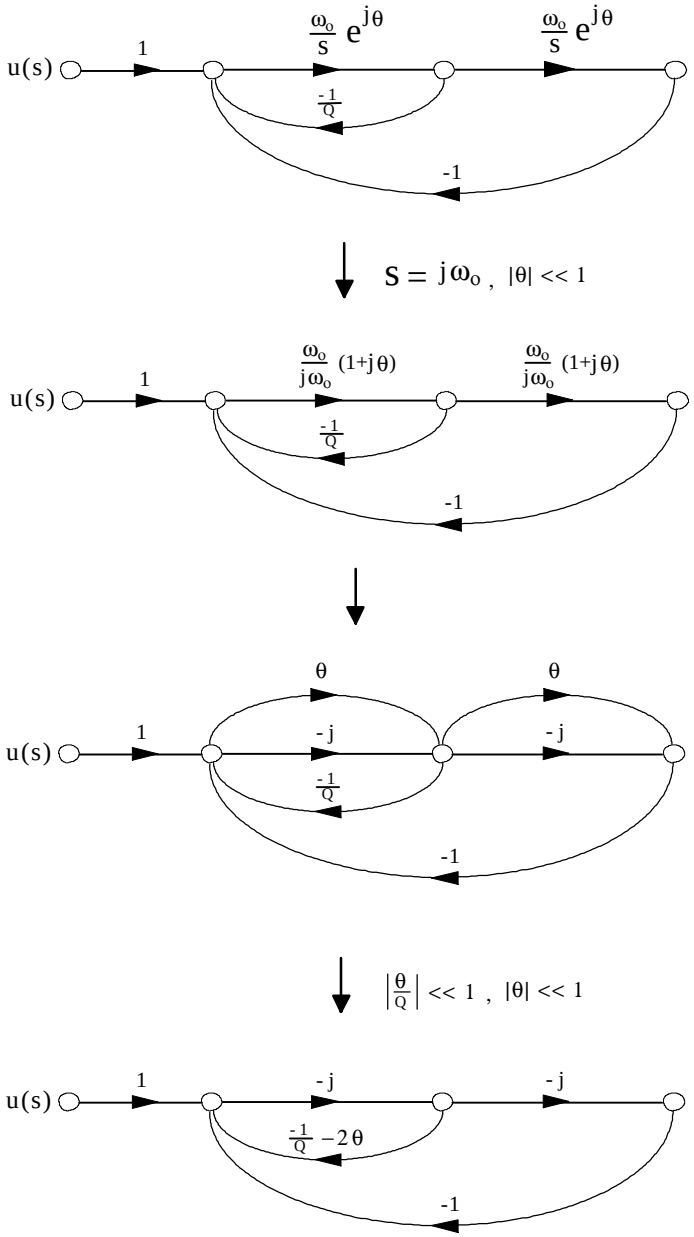

Figure 7.2: Effects of excess integrator phase on resonator design.

One additional option is to avoid the use of the cascade circuit altogether, so that internal nodes and associated parasitic poles are eliminated [68]. Unfortunately, the output resistance of the basic single-transistor transconductor is then too low to realize high-Q filter designs. While intentional excess phase lag could be introduced, or negative resistance circuits could be added to raise the effective Q, the Q tuning problem re-appears in either case. Thus, in general, high frequency, high-Q, Gm-C filters require tuning of both frequency and Q to realize accurate (and stable) responses [75].

The requirement for filter tuning implies the need for circuits that allow frequency and Q to be varied through current or voltage control. This need can be satisfied by a variety of design techniques, but is often addressed through use of current programmable transconductors such as the differential pair shown earlier in Figure 5.5 [64]. By implementing the transconductances g_m and g_{mQ} with these designs, frequency and Q can be independently set as shown in Figure 7.3.

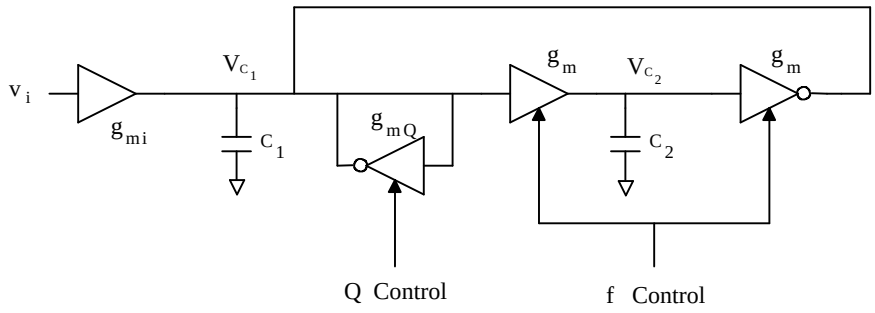

Figure 7.3: Control of frequency and Q in Gm-C resonators.

Similar tuning considerations apply to the case of Q-enhanced LC filter design, although the circuit parameters defining resonant frequency and Q are somewhat different. This subject has not been treated in significant depth in the literature and a full discussion in this dissertation is deferred to the next chapter. However, the essential points are outlined in the paragraphs below.

The resonant frequency ω_o of an ideal Q-enhanced LC resonator is given by the well-known expression:

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{7.6}$$

while the effective Q was found in Chapter 5 to be of the form:

$$Q_{eff} = \frac{1}{1 - g_{m_n} R_p} Q_o \tag{7.7}$$

The inductance L in (7.6) is determined largely by the inductor geometry and can be accurately controlled. However, the capacitance C may vary by $\pm 10\%$ or more, so that frequency deviations of $\geq 5\%$ can be expected. Thus, tuning of frequency becomes a necessity for all but the lowest Q resonator designs.

In the case of quality factor, the need for tuning may be even more pronounced. Parameters that determine g_{m_n} are uncorrelated with those that determine the inductor loss resistance R_p, so that the denominator in (7.7) becomes difficult to control when $g_{m_n} R_p \rightarrow 1$. Thus, at large Q enhancements ($\frac{Q_{eff}}{Q_o} \gg 1$), tuning of Q is required.

The need for tunable frequency and Q circuits in Q-enhanced LC filters can be satisfied though techniques such as those shown in Figure 7.4. Here, the control of filter Q is provided in a manner essentially equivalent to that used in the Gm-C case. However, control of frequency requires some means of varying circuit capacitance or circuit inductance. This requirement can be satisfied with varactor diodes (if supported in the process), or through switchable capacitances. Alternatively, the effective inductance value can be varied through the technique shown in Figure 7.5 [76]. The advantage of this technique is that continuous tuning can be provided without the need for varactor diodes. However, since additional active circuitry and noise is introduced, care must be taken to avoid degrading the filter's

already limited dynamic range.

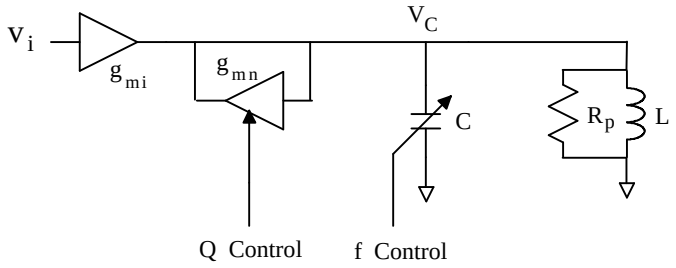

Figure 7.4: Control of frequency and Q in Q-enhanced LC resonators.

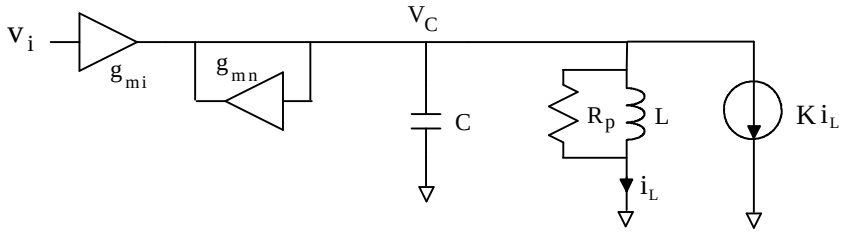

Figure 7.5: Controlling the effective inductance value in Q-enhanced LC resonators.

7.2 Tuning Control Sytem Designs

Having demonstrated the need for filter tuning, this section turns to the question of how to design frequency and Q control systems. Ideally, one-time tuning could be performed using simple trimming techniques following fabrication, and no control system would be required. Unfortunately, cost and technical problems associated with trimming, combined with strong temperature and voltage dependences found in Gm-C and Q-enhanced circuits rule out this option for all but the lowest frequency and lowest Q implementations. Thus,

control system designs are needed in which tuning can be performed while the filter is in use.

Unlike the fundamental dynamic range limitations discussed in the previous chapter, the design of tuning control systems is an engineering problem, which in theory can be solved. In practice, however, control systems proposed in the literature are sometimes complex and may involve substantial amounts of additional circuitry, over and above that required by the filter itself. The issue of complexity is often overlooked, but is an important facet of design, and will play an important part in discussions in the following sections.

7.2.1 Master-Slave Tuning

Master-slave tuning, was the first technique developed for real-time tuning of active continuous-time filters [89], and continues to be the dominant approach used today. In the classic master-slave architecture shown in Figure 7.6, an on-chip oscillator (the master) is implemented using circuits similar to those employed within the filter to be tuned (the slave). Both circuits receive the same frequency control input, which is derived by phase locking the master oscillator to an external reference. Thus, when the master oscillator's frequency is set, the passband of the filter is properly tuned.

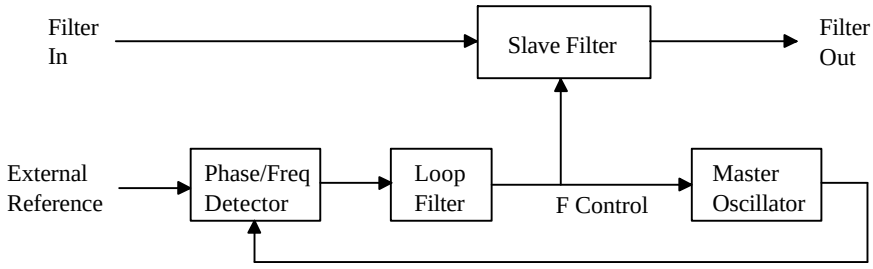

Figure 7.6: Master-slave frequency tuning.

The accuracy of this technique depends on the degree of matching and tracking between master and slave circuits. With careful design, capacitances as well as transconductances can be matched to closer than 1% [97], implying frequency accuracies down to 2% or better.

Although not indicated in Figure 7.6, the master-slave approach can also be used to provide control of filter Q [106]. One approach is to construct the master oscillator in the form of a second-order resonator structurally identical to that used within the filter to be tuned, but with a lower value of g_{mQ} (or g_{m_n}). The value of g_{mQ} (g_{m_n}) for both master and slave are made tunable as shown in Figure 7.3, and share a common Q control input. By adding a control loop to precisely set the amplitude of the master circuit's oscillation, the exact setting for $Q \rightarrow \infty$ is then obtained, and with a fixed offset between master and slave transconductances designed into the filter, a finite and known filter Q is achieved.

Several variations of the master-slave technique have been reported in the literature (c.f. [75] and [83]. However, all implementations share the following essential features:

- Tuning relies on matching and tracking of on-chip components, limiting the frequency accuracies and Q values that can be obtained.
- Substantial additional circuitry is required, adding to chip real-estate usage, power consumption, and cost.
- An external tuning reference signal must be supplied, introducing the need for careful design to minimize reference signal feedthrough, and potentially adding to the cost of the system in which the filter is used.

Although none of these limitations is severe enough to prevent use of the master-slave technique in low to moderate Q filter designs ($Q < 50$), higher Q designs require an alternative approach. These approaches, discussed in the following sections, are designed to eliminate the reliance on component matching, but in some cases can help to reduce or eliminate other limitations of the master-slave approach as well.

7.2.2 Self-Tuning

Self-tuning [108] was the first technique proposed for achieving higher Q values than those possible with the master-slave approach. The essential concept behind this technique is illustrated in Figure 7.7.

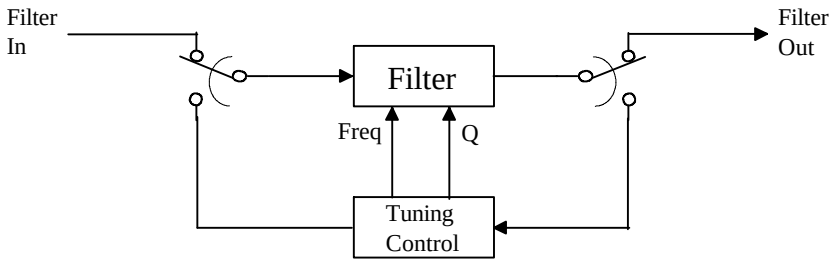

Figure 7.7: Self-tuning technique.

During use, the filter is periodically taken off-line and tuned directly, either by passing a known reference signal through it, or by some other suitable means. Since the filter is directly tuned, no ratios of on-chip components are involved, and the accuracy of tuning is theoretically unlimited. However, in a practical implementation, the following issues must be addressed:

- Processing of the desired signal is interrupted while the filter is being tuned.
- Suitable tuning control circuits must be designed to measure and adjust the filter frequency and Q.
- The filter must show good short-term stability to maintain its frequency and Q settings between tuning updates.

A solution to the first problem was offered by Tsividis in [108]. This solution consisted of switching between two filters, with one performing the desired signal processing task while

the other undergoes tuning updates. Whether or not the resulting transients associated with filter switching are acceptable will depend on the design of the system in which the filter is used.

The second problem, involving the design of the required tuning control circuits was not discussed in the original paper. However, such circuits could be built using a variety of approaches. One possibility is to employ an external reference signal with a frequency equal to that of the desired filter center frequency. Assuming that only a single resonator in the filter is tuned at a time, this signal could be passed through the resonator and its phase and amplitude measured at the resonator's output to determine center frequency and Q errors, respectively. Appropriate control updates could then be applied to force the filter back to the proper frequency and Q values. Details of this approach are presented in the discussion of the orthogonal reference technique later in this chapter.

The third problem, the need for short-term frequency and Q stability to hold the filter parameters constant between tuning updates, will depend on the circuit design. Although this issue is not addressed in the literature, tests conducted by the author and described in [105] show that this requirement can generally be met for filters with Q values up to at least several thousand.

7.2.3 Correlated Tuning Loop

An interesting alternative technique which avoids both the matching and tracking limitations of the master-slave design and the filter switching problems associated with the self-tuning approach is illustrated in Figure 7.8 [100]. This technique, referred to as the Correlated Tuning Loop (CTL), uses the signal being processed to characterize the filter's response. Assuming that this signal contains energy in the neighborhood of the filter center frequency, narrowband in-phase and quadrature samples of this energy can be measured at both the filter input and output with the circuits shown. These measurements can then be

used to determine the phase and amplitude shift introduced by the filter, and to update the filter's frequency and Q settings appropriately.

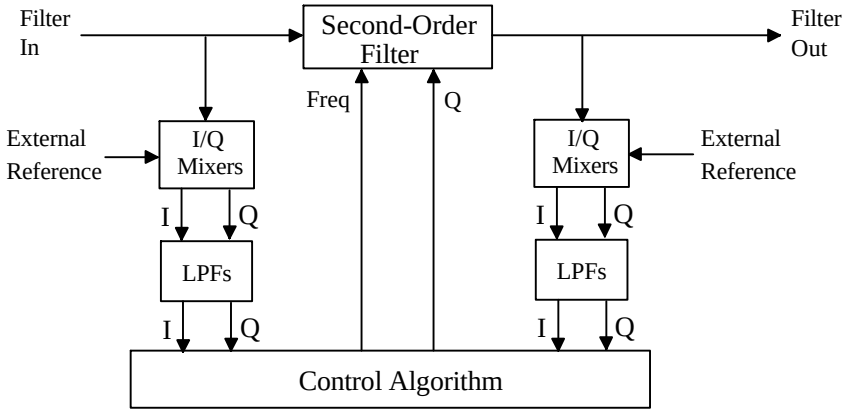

Figure 7.8: Correlated Tuning Loop technique.

Although the CTL technique is theoretically sound, and has been demonstrated in hardware [109], it contains at least three significant limitations:

- It assumes certain spectral properties are always present within the input signal.
- It requires significant extra circuitry (4 mixers plus a quadrature reference).
- It requires measurements to be made directly at the filter *input*.

The last two points are of particular concern in radio receiver applications. Essentially what is required are two auxiliary direct-conversion receivers. Aside for the complexity and power consumption of these circuits, the need for measurements at the input of the filter implies that at least one of these receivers must have very high dynamic range - possibly greater than that of the filter itself. Thus, the practicality of the CTL technique is open to serious question in this application.

7.2.4 Adaptive Filter Tuning

A potentially attractive alternative to the CTL technique which eliminates the need for measurements at the filter's input has been proposed by Kozma, Johns, and Sedra in [103]. This technique uses adaptive filter theory to adjust filter parameters based on comparisons with a known model.

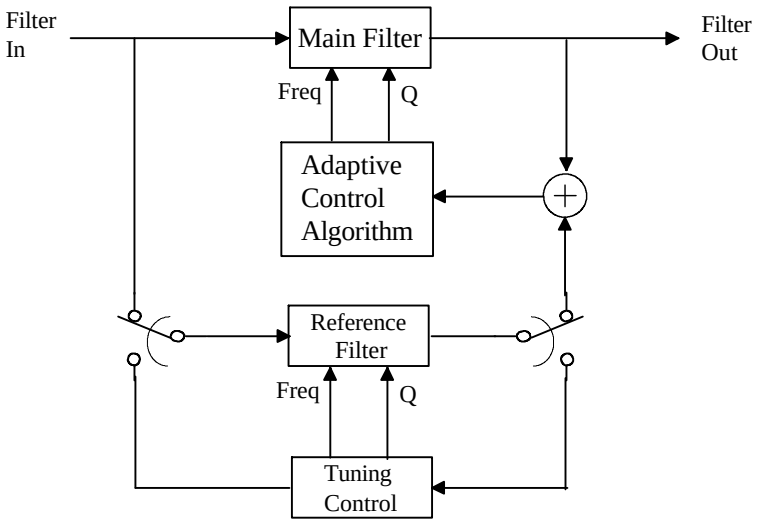

Figure 7.9: Adaptive Filter Tuning.

In the configuration shown in Figure 7.9, the main filter can be tuned directly without interrupting the signal processing task. The reference filter shown is used as a model, and is periodically adjusted using the self-tuning technique described previously. Since the self-tuning technique does not rely on matching, the reference filter can be adjusted to arbitrary accuracy. The adaptive control algorithm then compares the output of this filter with that of the main filter, adjusting the latter to make the two outputs match. Hence, the main filter is tuned to the same level of accuracy achieved by self-tuning of the reference filter while continuously processing the desired signal.

The price paid for this achievement, however, is a relatively high level of complexity, adding to power consumption and cost. In addition, this approach, like the CTL design discussed in the previous section, assumes certain spectral properties are present in the input signal to allow it to be tuned. This latter limitation is removed by the orthogonal reference technique described in the following section.

7.2.5 Orthogonal Reference Tuning

In this section, an alternative approach to tuning high-Q filters is proposed and investigated in detail. The new technique, referred to orthogonal reference tuning (ORT), uses only a single instance of the filter, requires no filter switching, and does not rely on the input signal and its characterization for tuning. Instead, a known reference signal is employed and is present in the filter passband together with the RF/IF signal being processed. This is permissible provided the reference signal can be made orthogonal, or nearly orthogonal, to the processed signal so that the two signals can be separated at the filter output to the degree necessary to meet overall system design goals.

The extent to which orthogonality can be achieved depends on the signal type being processed, and different methods will be appropriate for different applications. For example, with a receiver designed for use with digital biphase shift-keyed (BPSK) modulation [23], essentially complete orthogonality can be achieved using a quadrature phase signal as a tuning reference. Another approach offering complete orthogonality is possible in communication systems employing time division multiple access (TDMA). In TDMA systems, time orthogonality could be achieved by applying the tuning reference signal to the filter during

[1]Portions of this subsection are extracted from the following paper by the author: W. B. Kuhn, A. Elshabini-Riad, and F. W. Stephenson, "A New Tuning Technique for Implementing Very High Q, Continuous-Time, Bandpass Filters in Radio Receiver Applications", IEEE Int. Symp. on Circuits and Systems, 1994, pp 5-257 - 5-260.

time slots which are not of interest to the receiver. In this case, the concept of an orthogonal reference reduces to the self-tuning technique discussed earlier.

A more general approach which achieves approximate orthogonality is illustrated in Figure 7.10. In this design, referred to as spread-spectrum orthogonal reference tuning (SS-ORT), the reference signal is modulated with a direct-sequence spread-spectrum pseudo-random bit sequence (PRBS) [23].

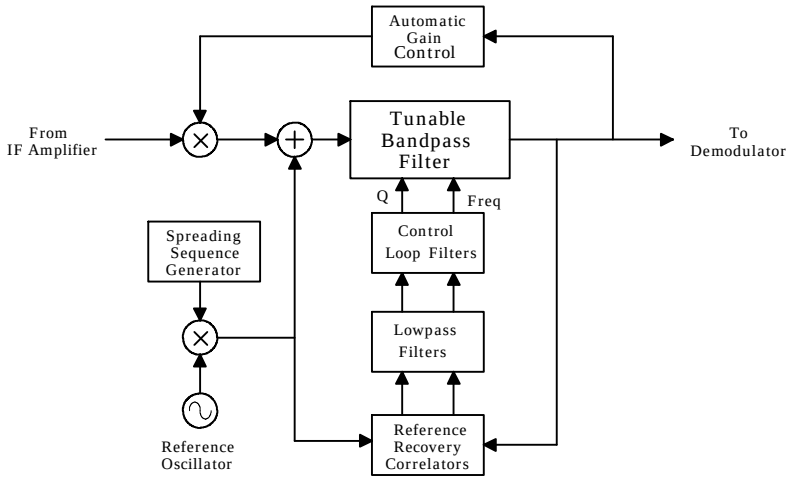

Figure 7.10: SS-ORT Technique Simplified Block Diagram.

The SS-ORT technique is well suited to use with two of the most popular signal formats found in radio receiver applications - wideband frequency modulation (WBFM) and low dimension digital phase modulations such as QPSK. In the following discussion, assume that the filter being tuned is a simple second-order bandpass section. Higher order filters can be implemented as cascade designs with straightforward extensions that tune individual second-order sections.

During operation, the receiver automatic gain control (AGC) shown in Figure 7.10 maintains the desired IF input signal at a constant level as seen by the filter. A reference oscillator at the filter's center frequency is modulated with a PRBS waveform and then summed with this

IF input signal so that both are present in the filter simultaneously. The amplitude of this reference waveform is held to a fraction of the IF signal's amplitude to minimize interference in the demodulation process. This fraction is described by a carrier-to-reference power ratio (C/R) at the filter output, which is maintained at a level of approximately 20 dB.

At the filter output, the reference must be recovered from the combined signal and then used to determine control inputs for adjusting the filter's frequency and Q. Using established methods from the area of spread-spectrum systems, recovery can be achieved by correlating the output of the filter with the reference signal applied at the filter's input, and then lowpass filtering the result. In the process, the higher amplitude IF signal is spread, so that only a fraction of its power passes through the lowpass and control loop filters. If this fraction is sufficiently small, accurate tuning information can be obtained.

Reference Recovery Analysis

A quantitative analysis of the reference recovery problem can be made with the help of Figure 7.11. The input signal to the bandpass filter is a summation of a spread reference waveform $r(t)$ and an IF input signal waveform $c(t)$.

To simplify the analysis, the IF input signal will be represented as a simple sinusoid. The two signals may then be expressed as:

$$r(t) = \sqrt{2R}s(t)cos(2\pi f_o t) \tag{7.8}$$

$$c(t) = \sqrt{2C}cos(2\pi f_o t + \theta_c) \tag{7.9}$$

where R and C represent the signal powers, f_o represents the frequency, $s(t)$ is a pseudo-random sequence waveform with discrete amplitudes of +1 and -1 and bit duration $T_b = \frac{1}{R_b}$, and θ_c is a relative phase angle. These two signals are passed through the second-order

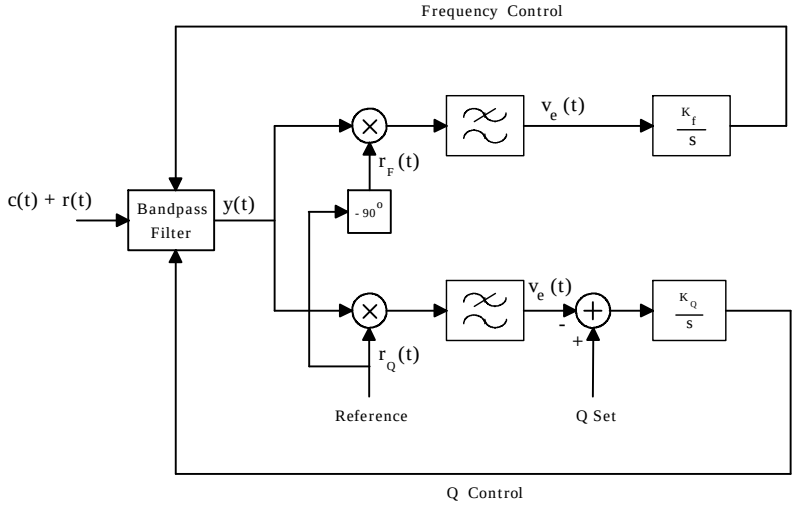

Figure 7.11: SS-ORT Control System.

bandpass filter producing an output that may be approximated by:

$$y(t) = \frac{Q(t)}{Q_o}[\sqrt{2R}s(t)cos(2\pi f_o t + \theta_F(t)) + \sqrt{2C}cos(2\pi f_o t + \theta_c + \theta_F(t))] \tag{7.10}$$

where Q_o is the nominal filter Q, $Q(t)$ is the actual Q at time t, and $\theta_F(t)$ is a phase offset created by an error in the filter center frequency. This approximation is valid for small frequency errors provided the reference signal is narrowband with respect to the filter's 3 dB bandwidth B_o. For a small frequency error of $\Delta F(t)$, $\theta_F(t)$ is calculated from the filter transfer function phase angle as:

$$\theta_F(t) = \frac{d\theta}{dF}\Delta F(t) = \frac{2}{B_o}\Delta F(t) \tag{7.11}$$

As shown in Figure 7.11, the filter output $y(t)$ given in (7.11) is then correlated with scaled and phase-shifted versions of the reference waveform. The response of the control system to disturbances in the filter Q and frequency, and the magnitude of tuning errors introduced

by the presence of the IF input signal $c(t)$ may be determined by correlating $y(t)$ with the reference signals $r_Q(t)$ and $r_F(t)$ for the respective control loops:

$$r_Q(t) = \sqrt{2}s(t)cos(2\pi f_o t) \tag{7.12}$$

$$r_F(t) = \sqrt{2}s(t)sin(2\pi f_o t) \tag{7.13}$$

The result for the frequency control loop is derived below. The Q control loop may be analyzed similarly.

Using superposition, we examine the control system under the influence of the reference signal $r(t)$ first and then add in the effects of $c(t)$. With $c(t)$ set to zero, the output of the correlator in the frequency control loop averaged over any large number of RF cycles by the lowpass filter is found from (7.10), (7.11), and (7.13) as:

$$v_e(t) \approx -\sqrt{R}sin(\theta_F(t)) \approx -\sqrt{R}\frac{2}{B_o}\Delta F(t) \tag{7.14}$$

The resulting control system response may be evaluated with the help of Figure 7.12 in which F_d represents an internal disturbance in the filter frequency, F_c represents the frequency correction applied by the control system, and F_e is the frequency error of the filter (equivalent to $\Delta F(t)$ in (7.14)). The error voltage at the output of the discriminator and the frequency control voltage are represented as v_e and v_c respectively, and K_d, K_f, and K_c are gain values relating the various voltages and frequency quantities, with K_d given by (7.14). The closed-loop response of this system is found to be:

$$H(f) = \frac{F_c(f)}{F_d(f)} = \frac{1}{1 + j\frac{f}{B_{CL}}} \tag{7.15}$$

where B_{CL} is the 3 dB bandwidth of the control loop given by $B_{CL} = \frac{K_d K_f K_c}{2\pi}$

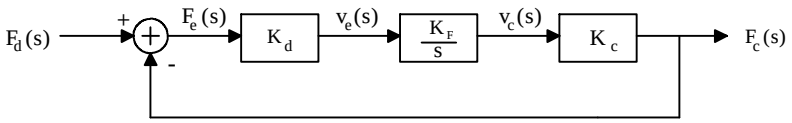

Figure 7.12: Frequency Control Loop Block Diagram.

In general one would like to set B_{CL} in (7.15) as large as possible for best correction of frequency disturbances F_d. However, as shown below, B_{CL} must be kept relatively small to minimize errors in the control system caused by the IF signal $c(t)$ which until now has been ignored in the analysis. These errors will be evaluated first by determining a frequency disturbance value F_d that would produce an output from the discriminator equivalent to that produced by the presence of $c(t)$ in the filter. Equation (7.15) will then be applied to find the resulting frequency correction signal F_c which in this case is a frequency control error produced by $c(t)$.

The worst case (maximum) output from the frequency discriminator is obtained when the second term of $y(t)$ in (7.10) is in phase with the reference signal $r_F(t)$. Under this condition:

$$v_e(t) = \sqrt{C}s(t) \tag{7.16}$$

Using (7.14), the equivalent frequency disturbance is:

$$F_d(t) = -\frac{B_o}{2}\sqrt{\frac{C}{R}}s(t) \tag{7.17}$$

To determine the resulting control system output for this input, the waveform $s(t)$ may be approximated as a stationary random process with power spectral density (PSD):

$$S_{F_d}(f) = \frac{1}{R_b} sinc^2\left(\frac{f}{R_b}\right) \tag{7.18}$$

resulting in a PSD at the control system output equal to:

$$S_{F_c}(f) = \frac{B_o^2}{4R_b}\frac{C}{R} sinc^2\left(\frac{f}{R_b}\right)|H(f)|^2 \tag{7.19}$$

If the cutoff frequency of $H(f)$ is low in comparison with the bit rate R_b of $s(t)$, then the $sinc^2$ term may be approximated as one, and the mean square magnitude of F_c is found to be:

$$\begin{aligned} \overline{F_c^2} &= \int_{-\infty}^{\infty} S_{F_c}(f)df \\ &= \frac{B_o^2}{4R_b}\frac{C}{R}\int_{-\infty}^{\infty}|H(f)|^2 df \end{aligned} \tag{7.20}$$

Recognizing the integral of $|H(f)|^2$ as the noise bandwidth B_N of the control system response, the root mean square (RMS) magnitude of frequency error caused by the presence of the carrier $c(t)$ may then be written:

$$\Delta F_{RMS} = \sqrt{\overline{F_c^2}} = \frac{B_o}{2}\sqrt{\frac{C}{R}\frac{B_N}{R_b}} \tag{7.21}$$

The quantity $\frac{R_b}{B_N}$ is the processing gain G_p of this spread-spectrum system. In terms of this gain, the normalized RMS error of filter frequency tuning may be written as:

$$\frac{\Delta F_{RMS}}{B_o} = \frac{1}{2}\sqrt{\frac{C}{R}\frac{1}{G_{P_F}}} \tag{7.22}$$

The normalized RMS error of the filter Q can be derived similarly and is found to be:

$$\frac{\Delta Q_{RMS}}{Q_o} = \sqrt{\frac{C}{R}\frac{1}{G_{P_Q}}} \tag{7.23}$$

Equations (7.22) and (7.23) can be solved for the required processing gain for a specified RMS variation in frequency and Q. For example, to achieve a 10 percent RMS variation in Q with C/R=20 dB, the required processing gain is 40 dB. This corresponds to a control loop noise bandwidth 10,000 times smaller than the PRBS modulation rate. Clearly, the control loop bandwidth is relatively low, and good short term stability of frequency and Q in the filter is required.

PRBS Modulation Rate

From the preceding discussion, it is clear that the PRBS modulation rate should be selected as large as possible to maximize processing gain and control loop bandwidth. However, if the rate is made too high, the reference signal spreading will be excessive relative to the filter bandwidth, and group delay introduced by the filter will complicate the correlation process required for reference recovery.

The group delay of the filter depends both on the filter bandwidth and on which control loop is being analyzed. The worst case is found to be the delay for the frequency control loop. For low frequency components of the reference modulation waveform this delay is given by:

$$\tau_g = \frac{2}{\pi B_o} \tag{7.24}$$

where B_o is the 3dB bandwidth of the filter begin tuned. For proper correlation, this should be held to a fraction of the PRBS period. Hence, the constraint on the PRBS rate may be stated as:

$$R_{PRBS} \ll \frac{\pi}{2} B_o \tag{7.25}$$

In the prototype implementation described below, however, the relaxed constraint:

$$R_{PRBS} < B_o \tag{7.26}$$

has been found to give satisfactory results.

Effects on the Demodulation Process

To a first-order approximation, the reference signal used in the SS-ORT technique may be treated as additive white Gaussian noise in estimating the effects on signal-to-noise (S/N) or bit error rate (BER) at the demodulator output. This approximation is a good one if the PRBS rate is on the order of the filter bandwidth. The demodulator output S/N or BER can then be found from established formulas or graphs.

Demodulation theory for wideband FM systems predicts a thresholding effect at carrier-to-noise (C/N) values near 10 dB and substantial S/N improvement factors above threshold (depending on the modulation index) [179]. For example, S/N at the demodulator output can be on the order of 50 dB for a C/N value of only 15 dB at the demodulator input. Digital modulations such as QPSK also exhibit a similar thresholding behavior in the neighborhood of 10 - 15 dB C/N depending on BER requirements, and at a C/N ratio of 20 dB, the demodulator output is virtually error free. Hence, a C/R ratio of 20 dB in the SS-ORT technique should yield similarly error-free performance.

Effects on Receiver Sensitivity

Since the reference signal behaves approximately as additive white Gaussian noise, the noise floor of the receiver will be raised and the sensitivity of the receiver will be reduced by the presence of the reference signal. However, the effect of the reference on receiver sensitivity will be small provided that the C/R used is at least several dB higher than the demodulator threshold. For example, if the demodulator threshold is 10 dB and C/R is set to 20 dB, then the effective C/N seen by the demodulator is found to be 9.6 dB. Thus, the receiver sensitivity is decreased by only 0.4 dB.

Experimental Verification

A board-level prototype of the SS-ORT technique was built to verify the technique's viability and to check the analytical predictions discussed above. The tuned filter shown in Figures 7.13 and 7.14 was designed to implement a simple second-order bandpass response with a nominal center frequency of 10.7 MHz and a nominal Q value of 100. These values allow the filter to be placed in the IF section of a commercial FM broadcast receiver, providing a realistic demodulator and the ability to assess S/N at the demodulator output through critical listening tests in addition to more traditional laboratory measurements.

The filter was tested first under manual control to check short term stability. Both frequency and Q were found to be stable to within less than 5 percent of the nominal bandwidth and quality factor, respectively, over periods of several seconds at Q values as high as 1000. These tests confirmed that the small control loop bandwidth used ($B_N = 1.6$ Hz) would be sufficient to tune the filter transfer function.

The filter was then placed in the control loop implemented with the circuits shown in Figures 7.15 and 7.16 and locked at a frequency of 10.7 MHz and a Q of 100 using a PRBS rate of 100 KHz. C/R was adjusted to 20 dB and swept frequency measurements were performed

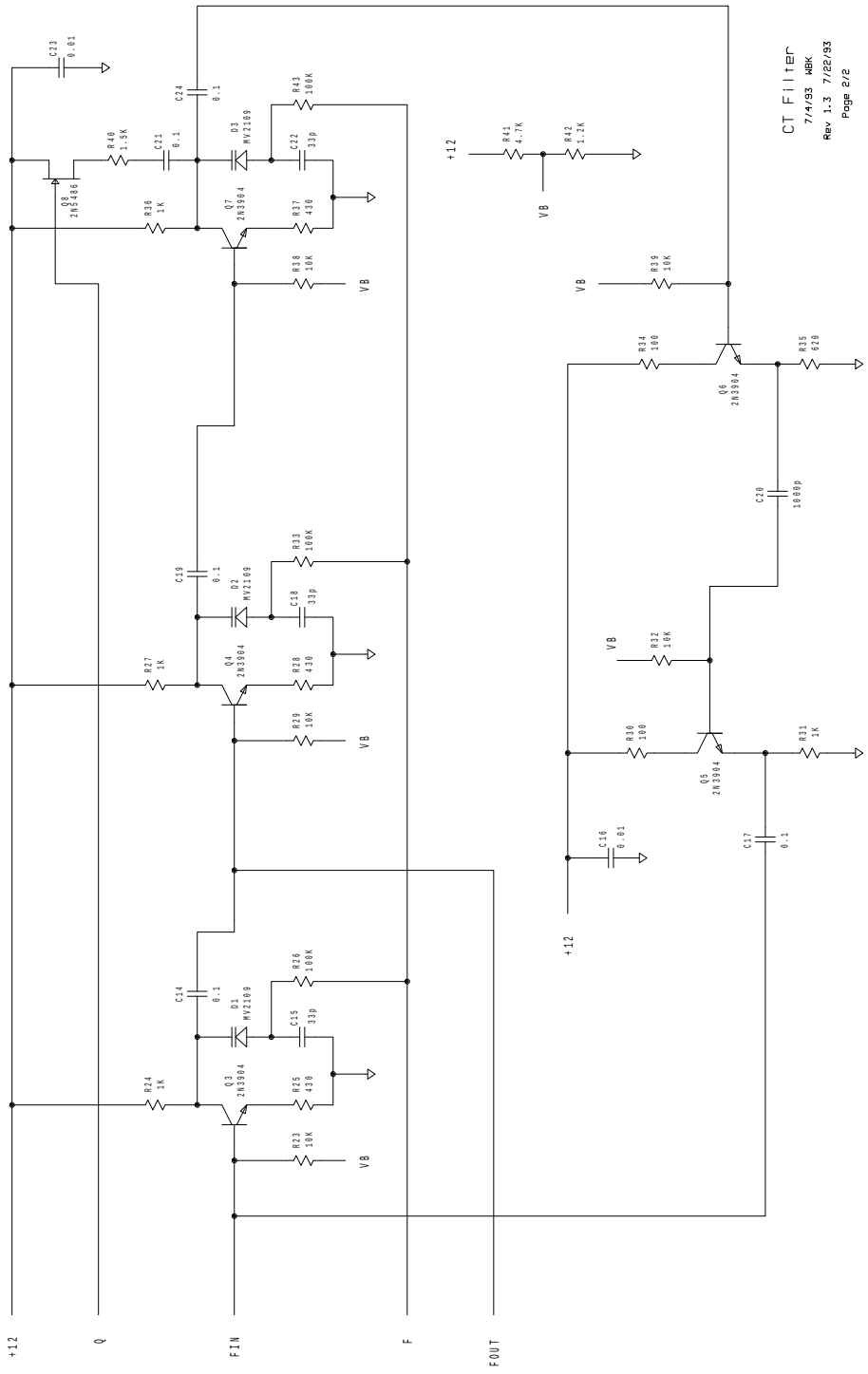

Figure 7.13: Tunable active filter used for ORT technique prototype.

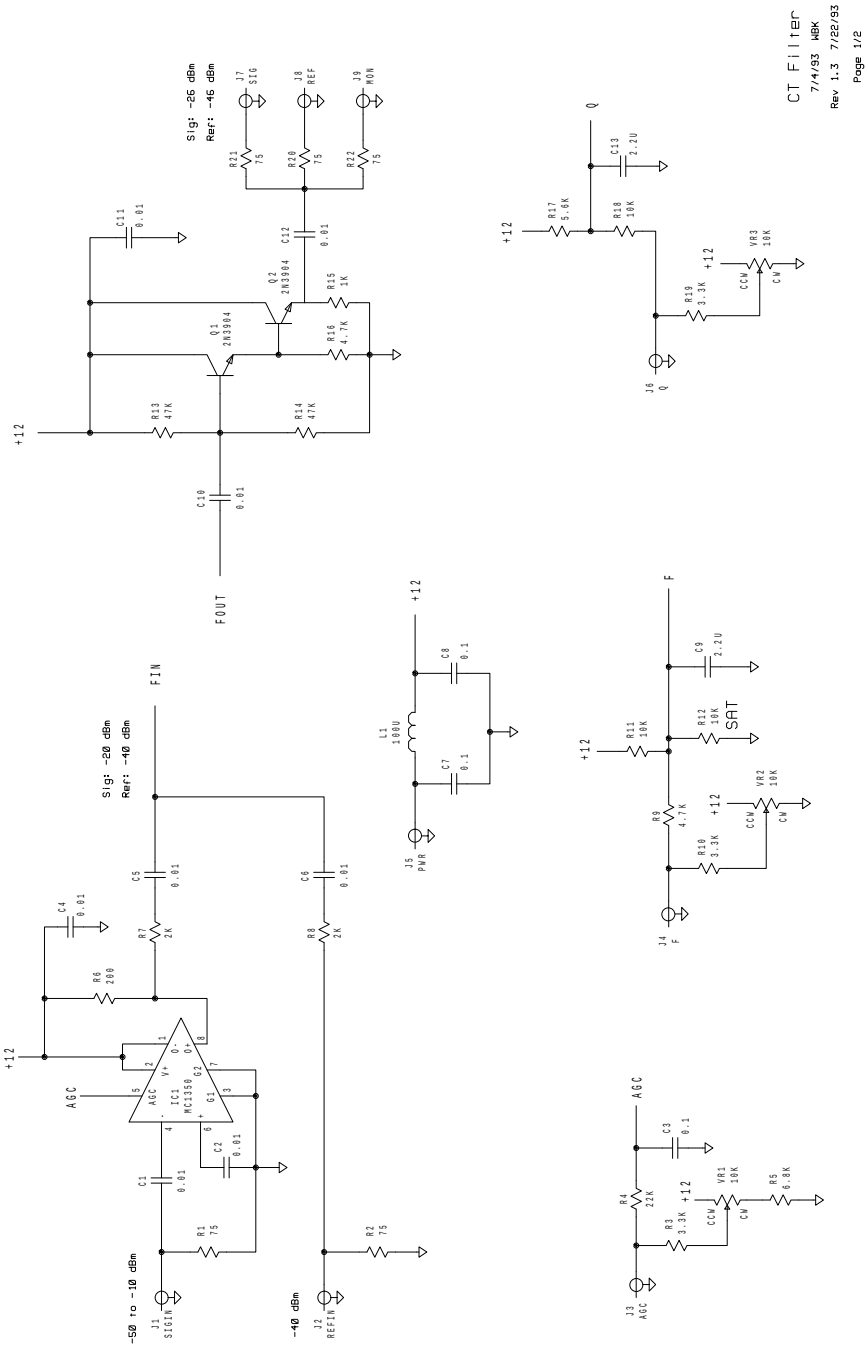

Figure 7.14: Tunable active filter used for ORT technique prototype.

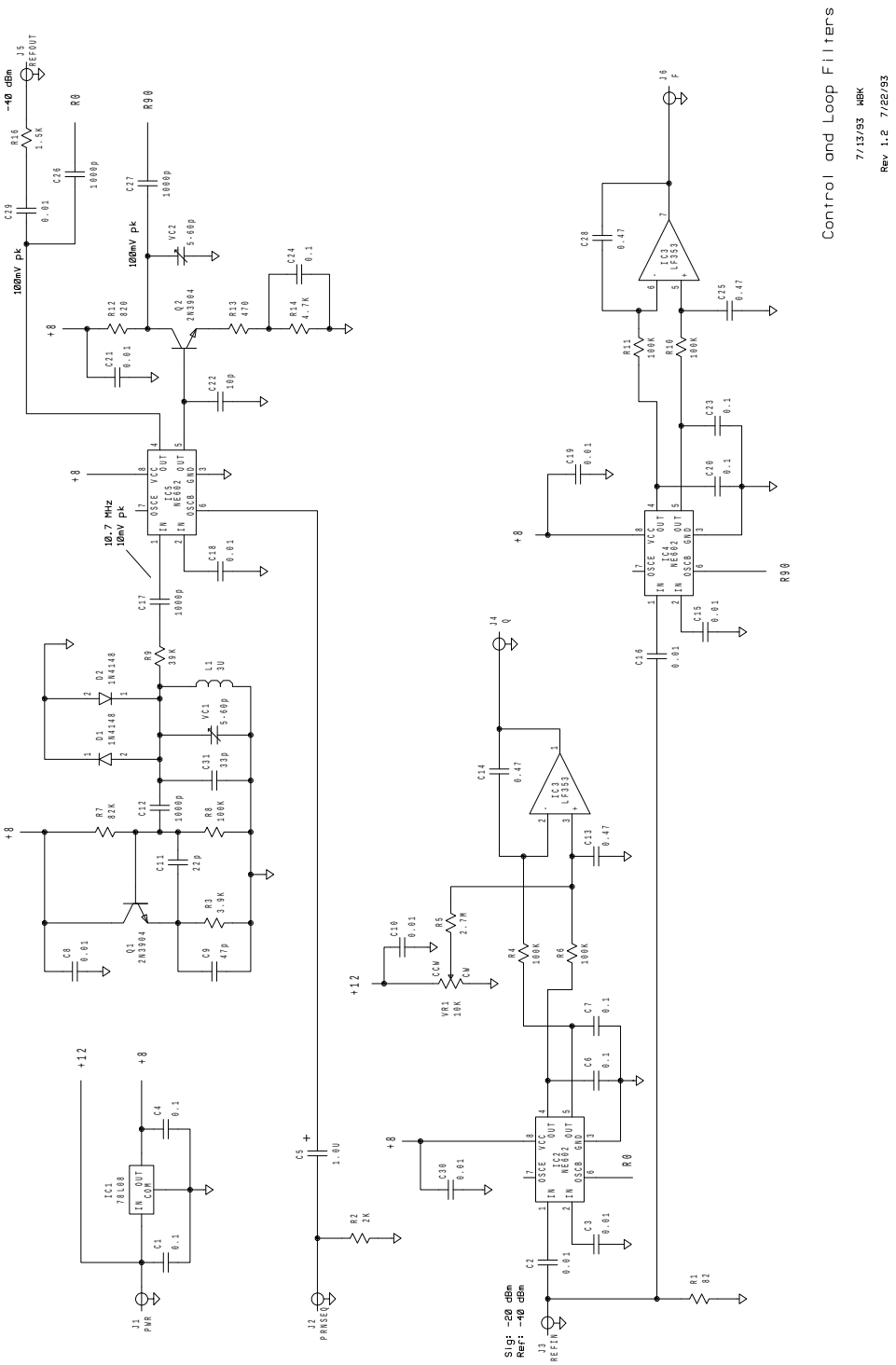

Figure 7.15: Prototype ORT technique control system circuitry.

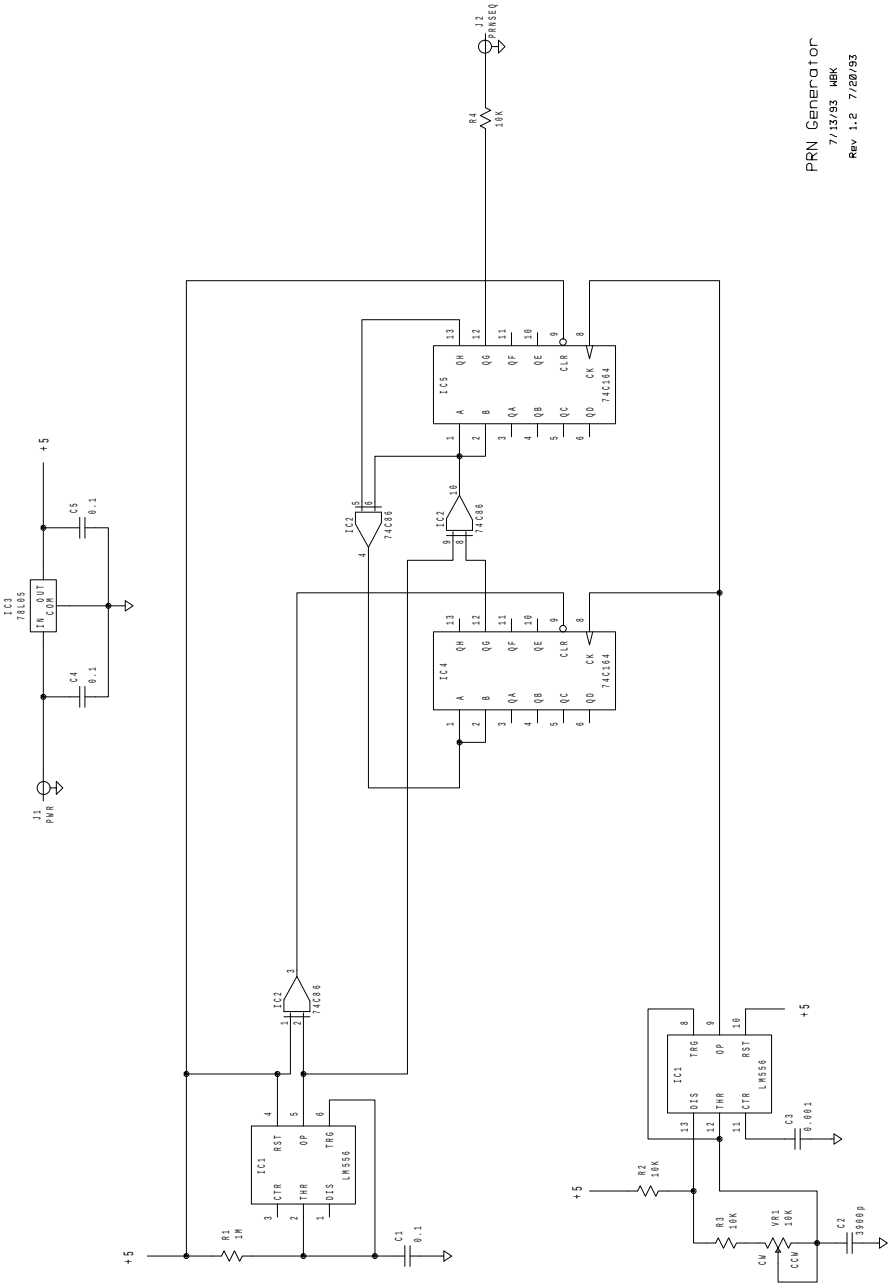

Figure 7.16: Prototype ORT technique PRBS generator circuitry.

to check the filter response. Stability of the control loops and variations in frequency and Q caused by finite processing gain were also assessed. The frequency and Q of the filter in lock were found to be correct to within the accuracy of the 90 degree phase shift setting and the Q-adjustment setting provided on the control board. Both loops remained stable at all input signal frequencies inside and outside the filter bandwidth, and the expected variations of frequency and Q were observed at zero beat. With a PRBS rate of 100 KHz ($G_p = 48$ dB), RMS variations on the order of a few percent were observed as predicted by Equations (7.12) and (7.12).

With the PRBS rate set to 10 KHz, the control system was also tested at a filter Q value of 400 (the limit of the adjustment range in the control loop circuitry). Swept frequency measurements showed proper filter operation and good stability.

Effects of the reference on demodulator performance were measured by placing the locked filter into the IF section of a commercial FM broadcast receiver. The PRBS rate was set to 100 KHz and the filter Q was set to 100. With the receiver's multiplex switch set to monaural mode the expected high S/N was observed in the audio output. S/N improvement threshold was observed at the predicted value of 10 dB C/R and at a C/R value of 20 dB the presence of the reference was virtually undetectable in listening tests. Measurements performed with the receiver set to stereo mode, however showed clearly perceptible noise. This behavior is expected since the stereo modulation format for commercial broadcast uses essentially narrowband FM modulation for the L-R channel information. Hence, the S/N improvement is substantially reduced and the reference signal injects noise into the demodulation process.

7.2.6 KIS Tuning

All of the tuning techniques discussed in this chapter have been found to have important technical and practical limitations, and in some cases, relatively high levels of complexity.

Complexity was clearly evident in the SS-ORT technique described in the previous section, but is also a potential problem in other techniques. In this final section, the issue of complexity is examined more carefully to determine which techniques, if any, are suitable for use in commercial products.

The importance of simplicity should not be overlooked in any design endeavor. Intuitively, simple techniques are often attractive because they possess a certain level of elegance and robustness. However, from a purely pragmatic viewpoint, simplicity helps to keep development cost and time within allowable limits, and to minimize overall project risk. In the design of any real system or device, these issues often become deciding factors in what is implemented and what is not. Thus, the concept of Keep-It-Simple (KIS) tuning is proposed and examined in this section. Where possible, new approaches designed to reduce complexity and supporting circuitry are also suggested.

Master-slave tuning

The basic master-slave technique discussed in Section 7.2.1 qualifies as a KIS technique in many ways. Typically, only a simple second-order master oscillator is needed, and the design and layout of this oscillator can be copied from that of a resonator section used within the filter being tuned. Design of the remaining amplitude and phase-locked-loop circuits may require additional time, but is straightforward and involves relatively low risk.

However, the master-slave tuning approach does require significant chip real-estate and power consumption, and can suffer from problems with clock signal feedthrough into the signal processing circuits. In addition, for filters operating at very high Q, matching and tracking may be insufficient to realize a desired level of accuracy. Thus, additional techniques should be considered before committing to this approach.

Self-Tuning

Self-tuning offers the potential for very high levels of tuning accuracy, but may be difficult to implement in systems which require continuous processing of the input signal. In newer digital radio designs however, where continuous reception is not necessarily required, simplifications may be found by carefully integrating filter tuning requirements into the overall system design.

For example, in systems employing time division multiple access or time division duplex, it may be possible to tune the filter during timeslots which are not of interest to the host receiver. In this case, only a single copy of the filter would be needed as shown in Figure 7.7, and any potential problems associated with reference feedhrough could be eliminated by disabling the tuning reference signal when tuning is not in progress. Both of these features represent significant advantages over the master-slave technique, apart from the ability to obtain theoretically unlimited tuning accuracy.

The need for an external reference and tuning control loop circuitry in the self-tuning approach is still a potential problem. However, simplifications in this area may also be found if the filter design is considered together with that of the host system. One interesting possibility arises in the case of direct conversion receivers as illustrated in Figure 7.17. In this design, the preselect filter is self-tuned using the receiver's existing local oscillator as a reference, and the receiver's demodulator circuits and microprocessor are used to measure and adjust the filter's frequency and Q. Thus, on-chip circuitry required to support tuning is reduced to a switch or adder at the filter input, a simple passive attenuator, and any digital control ports, registers, and D/As needed on the filter die to accept tuning commands and data and provide suitable control voltages or currents to frequency and Q circuits.

One final possibility for simplification of the self-tuning technique is illustrated in Figure 7.18. This approach could be used in traditional superheterodyne receivers as well as direct-

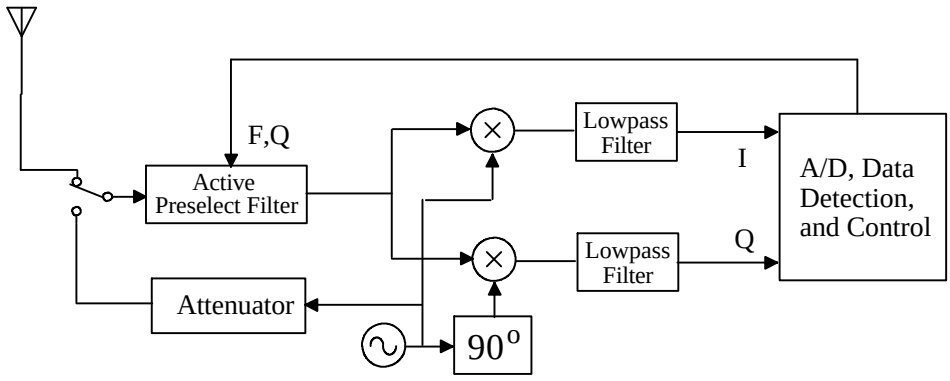

Figure 7.17: Self-tuning simplifications in direct conversion receivers.

conversion designs.

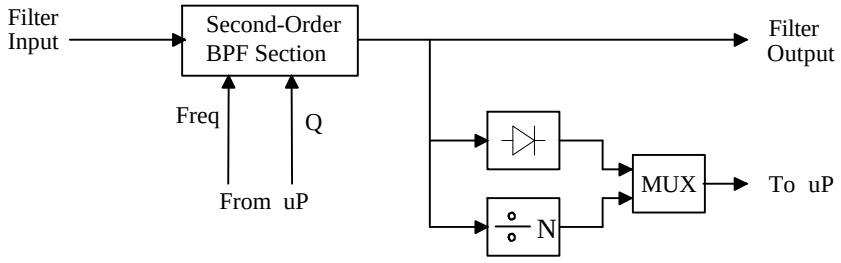

Figure 7.18: Self-tuning simplifications in superheterodyne receivers.

As before, filter frequency and Q control inputs are derived from the host receiver's microprocessor. However, measurement of frequency and Q is now performed using an amplitude detector and frequency prescaler incorporated into the filter die. Periodically, the filter is taken off-line and the Q is increased until the amplitude detector indicates that oscillation is present. The frequency of oscillation is then measured by the microprocessor's built-in

counter-timer and used to derive frequency correction signals to be fed to the filter. Finally the microprocessor restores the filter to a finite Q by applying a preset offset from the Q control setting needed to achieve oscillation. With this approach, no reference signal is needed, and on-chip supporting circuitry is reduced to a simple amplitude detector, frequency prescaler, and associated circuits for accepting tuning control updates[2].

Additional Techniques

Of the remaining tuning techniques, both the correlated tuning loop and the adaptive filter approach are relatively complex. The spread-spectrum orthogonal reference technique is also potentially complex, but simplifications may be found in a few special cases.

The need for generating and correlating with a spreading code can be eliminated when the technique is used within a direct-conversion receiver designed to receive direct-sequence spread-spectrum signals as shown in Figure 7.19. In this design, no spreading waveform is needed since the signal itself is spread and therefore approximately orthogonal to the LO sinusoid. As in the technique illustrated in Figure 7.17, supporting circuitry can be minimized by the use of the receiver's existing LO, detector, and data processing circuits.

One additional simplification of the orthogonal reference technique may be possible in the case of receivers designed for use with satellites. In this case, the potentially complex AGC function may be unnecessary since the signal being received is relatively constant in amplitude. At most, a simple AGC with a 10 to 20 dB range would be required.

[2]The frequency reference in this case is implicit in the microprocessor's counter/timer.

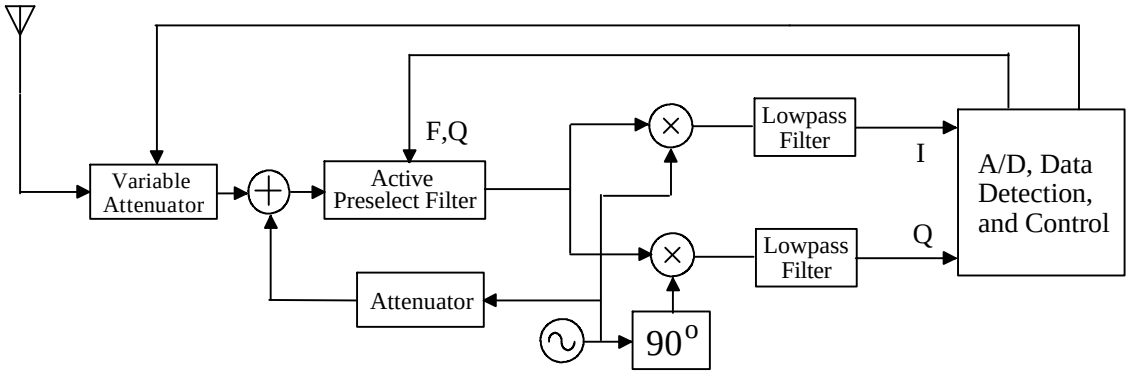

Figure 7.19: Orthogonal reference tuning simplifications.

Chapter 8

Q-Enhanced LC Filter Design

In previous chapters, the primary considerations for selecting an on-chip filter implementation technology were identified as operating frequency, Q, dynamic range, and filter tuning. The need to operate at high frequencies with low power consumption ruled out digital as well as switched-capacitor options, while non-standard IC processing required to form on-chip electro-acoustic designs placed this technology outside the scope of the current research. A detailed comparison between Gm-C and Q-enhanced LC filters then led to the conclusion that the latter technology is the only viable option. Q-enhanced filters provide an improvement of Q_o^2 in dynamic range over comparable Gm-C designs, making on-chip bandpass filters with Q values as high as 50 or above practical in low-power receiver designs. Moreover, the frequency of operation for these filters extends from about 100 MHz to well into the microwave range, due to the ability to resonate out inevitable circuit parasitic capacitances. Thus, this technology is ideally suited to the design of both RF preselect filters, and first-IF filters in modern cellular and PCS products.

Q-enhanced LC filtering is a relatively new area of research within the discipline of active filter design, and to date, only a few investigators have considered this option [57] [77] [94].[1] Indeed, at the time of this writing, no fully integrated Q-enhanced LC filters implemented in silicon have been reported, and circuit-level design techniques are largely unexplored. Therefore, this chapter will concentrate on detailed circuit-level design issues, complement-

[1]Portions of this chapter have been submitted to the IEEE for possible publication. Copyright may be transferred from the author to the IEEE without notice.

ing and extending the high-level issues presented in Chapters 2 through 7. Further detail on designing these filters will then be provided in Chapter 9, where two prototype ICs are described and their measured performance is reported.

The most critical circuits in any Q-enhanced LC design are the on-chip inductors employed. The quality factors in these devices must be carefully optimized to provide the best possible dynamic range performance, at the lowest possible power consumption. Thus, the first section in this chapter investigates the design and characterization of spiral inductors and presents techniques for estimating a spiral's inductance, quality factor, and self-resonant frequency. The following section then turns to the issue of Q-enhancement, the implementation of differential circuits, and the design of basic second-order resonator filters. Next, the accuracy and temperature stability of frequency and Q are studied and methods for varying frequency and Q to achieve a desired response are considered. Finally, the design of higher-order transfer functions using magnetically coupled resonators is discussed.

8.1 On-Chip Spiral Inductors

Inductors can be implemented in standard IC processes using planar spiral geometries. The design and characterization of these devices has been studied for many years within the field of microwave and millimeter wave integrated circuits (MMICs), where usable inductances can be fabricated in acceptable chip areas. However, their use in silicon IC processes is comparatively new, and the properties of spiral inductors in silicon are sufficiently different from those in GaAs MMIC devices that new modeling techniques are needed.

In a typical two-metal silicon IC process, spiral inductors can be fabricated using techniques similar to those used in MMIC devices. A typical geometry is illustrated in Figure 8.1 [131]. Top layer metallization usually provides the lowest resistivity and capacitance to the underlying substrate, and is therefore used for the spiral turns, while the lower metallization

layer is used for connection to the spiral center. The inductance values of spirals constructed in silicon technology are similar to those of spirals operating in free space. This is in contrast to spirals implemented in GaAs technology where the presence of a high conductivity ground plane a short distance under the turns lowers the inter-turn magnetic coupling and hence the overall inductance value [133].

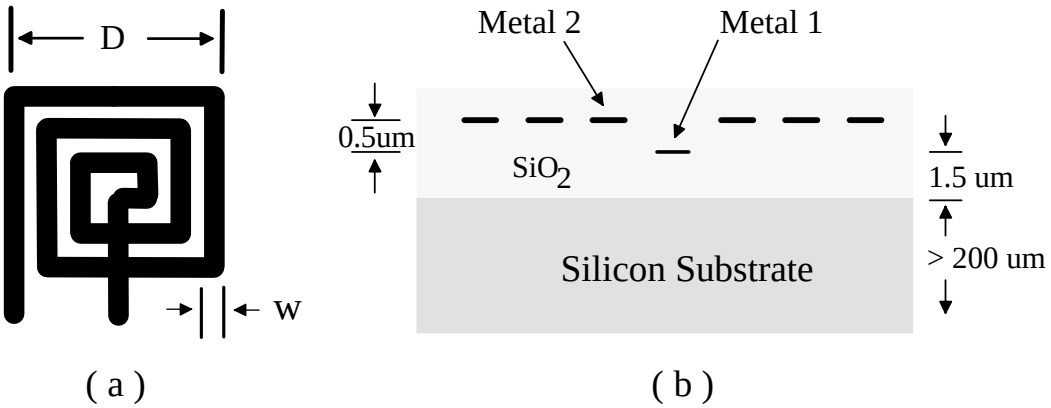

Figure 8.1: Spiral inductor layout. a) Top view. b) Side view.

8.1.1 Inductance Value

For the square spiral illustrated in Figure 8.1, operating in free space, Bryan and Dill have suggested that the inductance value can be approximated by [121], [123]:

$$L \approx \alpha D N^{\beta} \tag{8.1}$$

where L is the inductance in nH, D is the outer dimension in μm, N is the number of turns, and α and β are empirically determined constants. Dill [123] provides values of 8.5×10^{-4} and 1.67 for α and β, respectively, for PC board and hybrid spirals. However, the author has found that values of 8.9×10^{-4} and 1.8 provide a better fit to measurements reported

in [131] for spirals implemented in silicon technology. For improved accuracy, numerical techniques such as those employed by Grover [125] and Greenhouse [124] may also be used.

8.1.2 Inductor Q

A complete characterization of a spiral inductor for circuit design purposes generally involves developing an equivalent circuit to model finite inductor Q and self resonance effects, in addition to the low-frequency inductance value. A simplified equivalent circuit is shown in Figure 8.2 and will be used initially to illustrate important concepts. More accurate modeling usually requires either more complex lumped circuit models such as those described later in this section [128], or the use of two-port S parameters taken from analytic models, EM field simulations, or prototype measurements [136], [130].

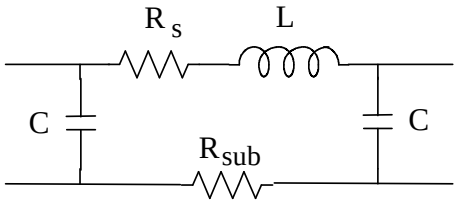

Figure 8.2: Simplified spiral inductor model.

Finite inductor Q results primarily from series resistance in the inductor turns (modeled as R_s in Figure 8.2) [131]. Additional losses result from currents conducted through the turn-to-substrate capacitances (C) and the underlying semiconducting substrate resistance (R_{sub}). The dominant losses resulting from series resistance can be estimated directly from the outer dimension D, trace width W, number of turns N, and metallization sheet resistance r_s as:

$$R_s \approx \frac{N}{2}\frac{4D}{W}r_s \tag{8.2}$$

where R_s is in Ohms, D and W are in μm, and r_s is in Ohms/$\square$.

If the metallization thickness is less than the skin depth (2.1 μm at 2 GHz for AlSiCu metallization), this resistance can be treated as approximately constant with frequency. Assuming that R_s is the primary inductor loss mechanism, an upper bound on the inductor quality factor Q_o can then be estimated at a frequency f in Hz from Equations (8.1) and (8.2) as:

$$Q_o \leq \frac{2\pi f L}{R_s} \approx 10^{-9} \frac{\alpha \pi f N^{\beta-1} W}{r_s} \tag{8.3}$$

Letting W scale with the outer dimension D as:

$$W = \frac{D}{4N} \tag{8.4}$$

to provide a gap between traces equal to the trace width, and noting that $(\beta - 1) \approx 1$, the following general observations can be made:

- Q_o increases linearly with frequency when skin effect can be ignored.
- For a given frequency and number of turns, Q_o increases approximately linearly with W, and hence with outer dimension D.
- For a given frequency and outer dimension D, W decreases with increasing N, so that Q_o is relatively independent of N, and hence of L.

Values of Q_o achievable in practice depend on the operating frequency of the filter, the resistivity of the metallization layers in the target process, the chip real estate that can be allocated to the spiral inductor, and additional losses from the underlying substrate and connected circuitry. Achievable values of Q_o also depend indirectly on the spiral's

self resonant frequency, which upper bounds the outer dimensions and inductance values possible at a given operating frequency.

8.1.3 Modeling of Inductor Q and Self-Resonant Frequency

An accurate prediction of self-resonance and Q_o requires modeling distributed turn-to-substrate capacitances as well as substrate resistances between turns. These difficulties have driven most designers to fabrication and measurement of prototypes, or to the use of 3-D field simulations. An alternative approach involves simulating the detailed lumped element model shown in Figure 8.3 using SPICE [128].

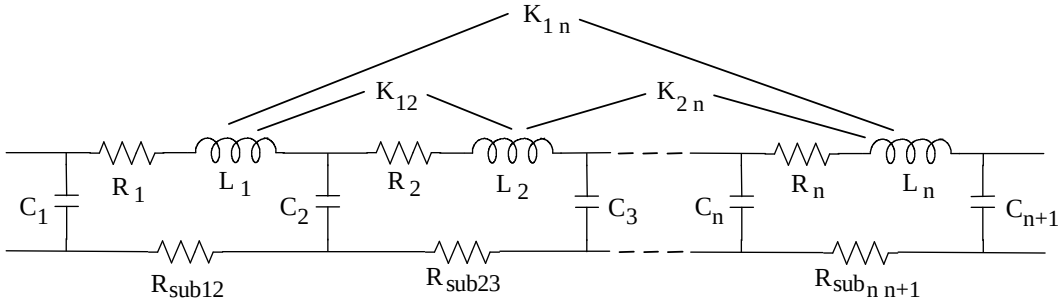

Figure 8.3: Detailed circuit model of spiral inductor.

The accuracy of this approach rests on the ability to predict circuit element values from spiral geometry and process parameters. For the design described in this paper, values for self inductances of individual turns L_i and coupling coefficients between turns K_{ij} were obtained using a finite element calculation of flux densities, while values for per-turn capacitance and resistance elements were computed directly from geometry and IC process data. The resulting model was validated against data published in [131] and [122], and then run to generate the data shown in Table 8.1, based on typical CMOS process parameters (r_s = 0.025 $\Omega/\Box$, metal-to-substrate capacitance C_A = 0.02 fF/μm^2, and substrate resistivity r_{sub} = 25 $\Omega/\Box$ (doped active to maximize Q)). For all simulations, the trace width W was

set to $W = \frac{D}{4N}$, giving a turn pitch of $2W$, and skin effect and substrate eddy currents were assumed negligible.

Table 8.1: Simulated inductance L, self-resonant frequency f_R, and quality factor Q for grounded spiral inductors.

D (μm)	N	L (nH)	f_R (MHz)	Q_o at f_R
330	4	3.5	3900	11
330	8	11	2300	8.1
330	16	39	1200	4.5
1000	12	71	300	3.4
1000	24	250	160	1.8
1000	48	980	65	< 1

8.2 Circuit Design Considerations

From Table 8.1, it is clear that achieveable Q_o values are quite low, especially at frequencies in the VHF range. Therefore, if a high selectivity filter is desired, some form of Q enhancement is needed. Two possible solutions to this problem are discussed in references [57] and [93]. In [57], the effective Q of a lossy inductor is raised through the insertion of an active negative resistance placed in series with the inductor. Difficulties with this approach include the need to measure current within the inductor, and the potential degradation to dynamic range that results from the insertion of current sensing resistors. Alternatively, a series-to-parallel impedance transformation can be performed on the lossy inductor and a negative resistance can be added, yielding the "parallel mode" Q-enhanced resonator shown in Figure 8.4 [93], where:

$$R_p = (1 + Q_o^2)R_s \tag{8.5}$$

and:

$$L_p = \left(\frac{1 + Q_o^2}{Q_o^2} \right) L \tag{8.6}$$

In this approach, the negative resistance has been implemented as a transconductor with positive feedback to cancel losses represented by R_p.

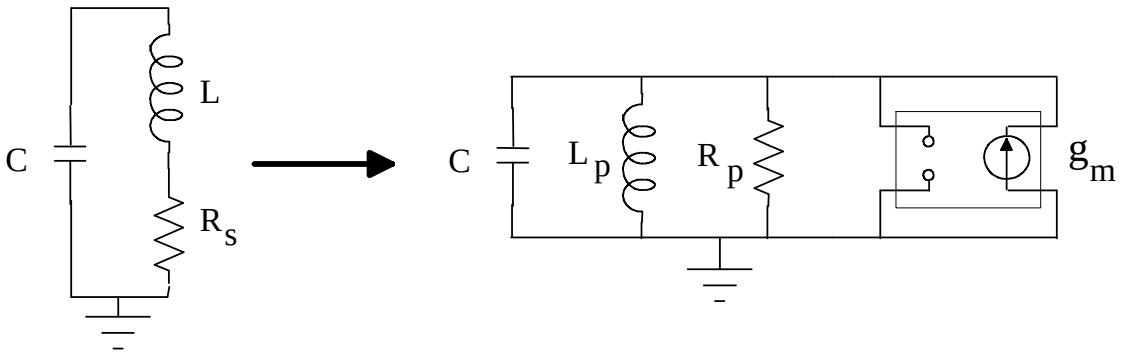

Figure 8.4: Parallel mode Q-enhancement.

To form a complete Q-enhanced second-order filter, input and output transconductors may be added to this circuit, as shown in Figure 8.5. In this configuration, the input transconductor provides a current source drive to the parallel RLC impedance, creating a second-order bandpass response, while the output transconductor isolates the RLC impedance from the load.

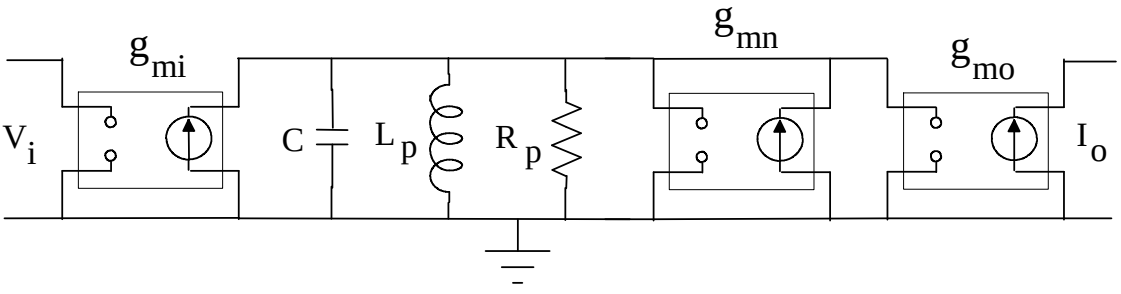

Figure 8.5: Parallel mode Q-enhanced filter.

As shown in Chapter 5, the effective parallel resistance R_{eq} of the resonator, and the effective quality factor Q_{enh} of the resulting filter can be found from:

$$R_{eq} = R_p \parallel \frac{-1}{g_{m_n}} = \frac{1}{1 - g_{m_n} R_p} R_p \tag{8.7}$$

and:

$$Q_{enh} = \frac{R_{eq}}{X_{L_p}} = \frac{1}{1 - g_{m_n} R_p} Q_o \tag{8.8}$$

and can be set to any desired value above Q_o by controlling g_{m_n} using techniques such as those described in Chapter 7. To proceed with the design beyond this point, however, values for the circuit elements of Figure 8.5 must be chosen.

8.2.1 Component Value Selection

In general, the filter will be excited by a source with resistance R_s as shown in Figure 8.6, and depending on the application, an input load resistor R_i may also be used.[2] [3] Thus, the circuit parameters to be considered in the design process include R_s, R_i, g_{m_i}, C, L_p, R_p, g_{m_n}, g_{m_o}, and R_L.

R_s and R_L are typically set by the system design in which the filter will be used. However, the remaining values must be selected to satisfy various design constraints such as achieving:

- the desired operating frequency f_o, and filter Q,

[2] If the filter interfaces to external (off-chip) circuitry, R_i may be needed to provide good SWR performance. Otherwise, R_i will typically be omitted.

[3] Real valued source and load impedances are assumed here for simplicity, but similar results follow for complex impedances.

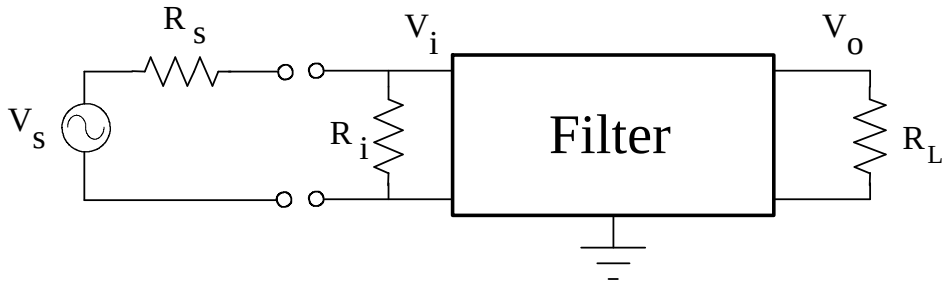

Figure 8.6: Source and load resistances seen by filter.

- a desired value of gain,
- a desired noise figure, and
- the maximum possible dynamic range.

Considering the design of the RLC resonator, note that once the inductor is designed, R_p is determined by Equation 8.5 and C and g_{m_n} can be picked to yield the desired frequency and Q, respectively. However, the only constraint for designing the inductor is to maximize Q_o in order to maximize dynamic range. Since Q_o is determined primarily by the inductor's trace resistivity and outer dimension, and is relatively independent of the number of turns used, the actual inductance value must be chosen based on other considerations.

To constrain the inductance value, the impedance of the RLC resonator must be related to the filter's input and output transconductances, and the input, source, and load resistances. These factors combine to determine the overall filter gain and noise figure, as well as the extent to which dynamic range improves at large frequency offsets.

An interesting and useful case occurs if R_s and R_L are known[4] and g_{m_i}, g_{m_n}, and g_{m_o} are

[4]These impedances are typically determined by the operating voltage and power level of the source and load circuitry, and therefore set the overall system dynamic range.

chosen according to:

$$g_{m_i} = g_{m_o} = g_{m_n} \approx \frac{1}{R_L} \tag{8.9}$$

Under this condition, the inductive reactance X_L and hence the inductance L_p are fixed by the required condition between g_{m_n} and R_p, and can be found from:

$$X_L = \frac{R_p}{Q_o} = \frac{1}{Q_o} g_{m_n} \tag{8.10}$$

where Q_o is assumed known from the process parameters and outer dimension D of the spiral used.

With these values selected, the voltage gain from the resonator core to the load is found to be unity and the gain from the filter input voltage V_i to the resonator core voltage V_c is:

$$\frac{V_c}{V_i} = g_{m_i} R_{eq} \tag{8.11}$$

which, when combined with (8.8) under the condition $Q_{enh} \gg Q_o$, can be reduced to the form:

$$\frac{V_c}{V_i} \approx \frac{Q_{enh}}{Q_o} \tag{8.12}$$

Thus, the filter provides a substantial gain equal to the Q enhancement, and a reasonably low noise figure may be expected.

An approximate expression for the filter's noise figure when $R_i \to \infty$ can be found by writing the noise figure in terms of voltages as:

$$\begin{aligned} F &= \frac{S_i/N_i}{S_o/N_o} \equiv \frac{V_s^2/V_{n_s}^2}{V_c^2/V_{n_c}^2} \\ &= \frac{1}{A_v^2}\frac{V_{n_c}^2}{V_{n_s}^2} \end{aligned} \tag{8.13}$$

where V_{n_s} and V_{n_c} are the noise voltages at the filter input and within the resonator core, respectively, and A_v is the voltage gain given by (8.11) (since R_i is assumed infinite). Combining (8.13) with (8.11) and with the following approximations for the noise voltages:

$$\begin{aligned} V_{n_s} &= \sqrt{4kTR_sB} \\ V_{n_c} &\approx \sqrt{4kT\left(g_{m_i} + g_{m_n} + \frac{1}{R_p}\right)BR_{eq}^2 + A_v^2V_{n_s}^2} \end{aligned} \tag{8.14}$$

yields:

$$F \approx 1 + \frac{g_{m_i} + \frac{1}{R_p} + g_{m_n}}{g_{m_i}^2 R_s} \tag{8.15}$$

which, with the assumed relationship in (8.9), reduces to:

$$F \approx 1 + \frac{3}{g_{m_i}R_s} \tag{8.16}$$

A similar relationship can be found under the matched input condition $R_i = R_s$, giving:

$$F \approx 1 + \frac{12}{g_{m_i}R_s} \tag{8.17}$$

Both (8.16) and (8.17) indicate that the filter noise figure depends on the relationship between the input transconductance and the source resistance, and can be minimized by

making the product $g_{m_i}R_s$ large.[5] Under the condition $R_s = R_L$, (8.9) implies that $g_{m_i}R_s \approx 1$ and noise figures of 6 and 11 dB result for the two cases of $R_i = \infty$ and $R_i = R_s$, respectively. These values may be acceptable for filters intended for use in RF preselection, but may actually be too low for IF filters, as discussed in Chapter 3. For IF designs, a larger noise figure can be obtained either by lowering g_{m_i}, or by lowering R_s. If g_{m_i} is lowered, the noise injected into the resonant circuit from the input transconductance will be less and slight improvements (e.g. 1 - 2 dB) in in-band dynamic range will result. However, a better choice is to lower R_s while maintaining the relationship in (8.9). This choice retains the voltage gain in the filter, but effectively lowers the voltage produced by the source. The advantage offered by this approach is that the ultimate out-of-band dynamic range improvement described in Chapter 6 is increased since the input is generally voltage limited and a lower input impedance implies a larger input power.

8.2.2 Balanced Circuits

Having selected values for the essential components in Figure 8.5, the task of circuit-level design and layout can begin. A critical decision at this stage is whether to adopt single-ended or differential circuit design techniques. For Q-enhanced filters which operate at high frequencies, several considerations favor the use of differential design approaches, including:

- Negative resistances can be implemented by cross-coupling gate and drain circuits, avoiding problems of intermediate nodes and associated parasitic poles.
- Coupling to power supply noise and to other circuits on the same die can be significantly reduced.

[5] This product cannot be increased arbitrarily because of problems with gate-drain feedback capacitance. At high frequencies, this feedback results in modifications of the expected input impedance and potential stability problems if $g_{m_i}R_s \gg 1$.

- Second-order non-linearities are canceled, leading to better dynamic range and noise performance.
- Higher voltage swings can be supported.

A simple balanced circuit design for the second-order filter of Figure 8.5 was briefly presented in Chapter 2 and is repeated in Figure 8.7 for convenience. In this design, the primary resonance is between the series connected inductors L_{1A} and L_{1B}, and capacitor C1. However, to determine the value of C1 needed to achieve a given frequency, stray capacitances C_{SA} and C_{SB} must be taken into account. These capacitances represent both the effects of self-resonance in the inductor and the parasitic capacitances associated with all interconnects and devices attached to these nodes.

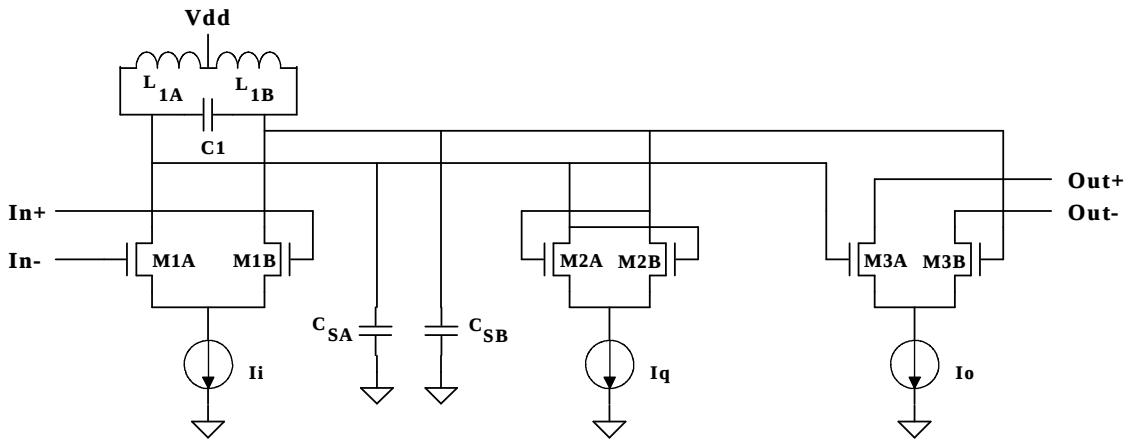

Figure 8.7: Q-enhanced filter circuit design.

In an alternative design, C1 could be eliminated and capacitances of 2 C1 could be paralleled with C_{SA} and C_{SB} to achieve the same frequency of operation. This technique has the advantage that the capacitances are larger and can be more accurately realized at high frequencies. In either case, however, two inductors are required for a fully balanced design, adding significantly to the overall area consumption and the die size. This problem can be solved if an approach similar to that used to build transmission-line transformers is

adopted, in which two sprials are inter-wound as illustrated in Figure 8.8, to form a single, *center-tapped* spiral inductor.

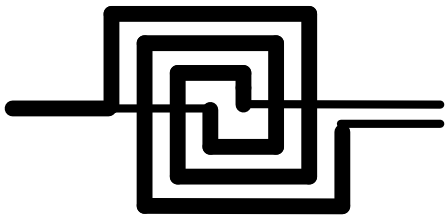

Figure 8.8: Center-tapped spiral inductor geometry.

8.2.3 Center-Tapped Spiral Inductors

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To compare the performance of the proposed center-tapped spiral geometry with that of the traditional spiral shown previously in Figure 8.1, simulations were performed and then checked with a board-level, scaled prototype. These investigations, described below, revealed that the center-tapped geometry consumes only 63% of the area required by two traditional sprials, and delivers a common-mode rejection ratio approaching 40 dB. Moreover, the self-resonance frequency is twice that of a traditional grounded spiral of the same value, enabling higher reactances and Q values to be obtained.

[6] Portions of this subsection are extracted from the following paper by the author: W. B. Kuhn, A. Elshabini-Riad, and F. W. Stephenson, "Centre-tapped Spiral Inductors for Monolithic Bandpass Filters," Electron. Lett., vol. 31, no. 8, pp. 625-626, 13 April 1995.

Performance Comparison

First, the resonance frequency and Q of a traditional spiral were investigated using the circuit of Figure 8.3 with substrate losses excluded. A resonance curve simulated with SPICE for a 100 nH, 28 turn inductor with outer dimension $D = 450\mu m$, trace width $w = 4\mu m$, area capacitance $C = 0.016fF/\mu m^2$, trace resistivity $r_s = 0.026\Omega/\Box$, and $\epsilon_r = 4$ is shown in curve *a* of Figure 8.9. This curve was generated with a current source applied to one end of the spiral with the opposite end grounded - the appropriate condition for circuits reported in the literature. If the source is applied across the inductor with neither end grounded, the self-resonant frequency is found to be approximately doubled, contrary to the $\sqrt{2}$ increase predicted by the simplified model assumed in [131]. At the grounded spiral's resonant frequency of 560 MHz, the Q calculated from the simulated peak impedance is 2.3, in general agreement with the value predicted from (8.3).

A model for the center-tapped spiral of Figure 8.8 was then derived from the model of Figure 8.3 by modifying the connections between turns, and grounding the center tap node. Since the connections between turns are the only substantial change, the total inductance, the total series resistance, and the Q of the center-tapped spiral can be predicted to be approximately equal to that of a traditional spiral with the same total number of turns. To determine the self-resonant frequency, a SPICE simulation was performed for a center-tapped inductor with the same dimensions and total number of turns as the traditional spiral above. The results, shown in curve *b* of Figure 8.9 indicate a factor of two improvement over the traditional grounded spiral. Hence, the center-tapped spiral behaves essentially as a floating inductor with respect to resonance. To determine the balance of the center-tapped spiral, additional simulations were performed with the two ends of the inductor driven in-phase. The result shown in curve *c* of Figure 8.9, indicates a common mode rejection ratio (CMRR) on the order of 40 dB.

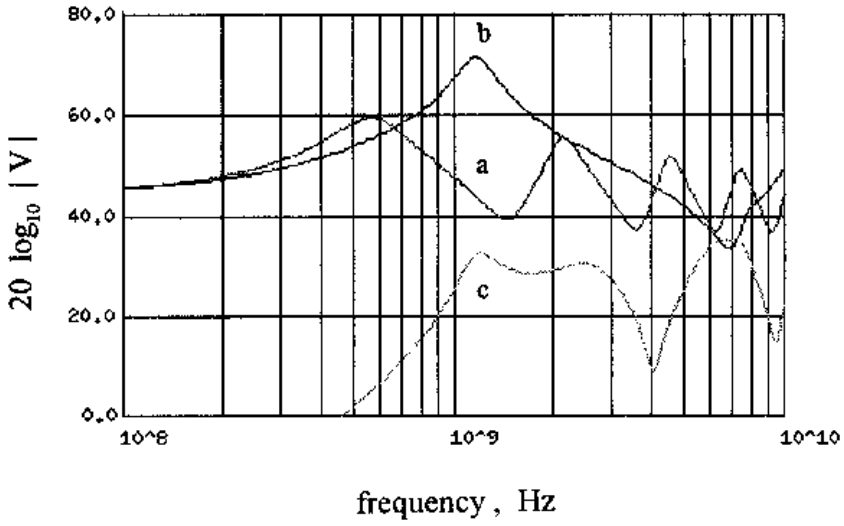

Figure 8.9: Center-tapped versus traditional spiral performance. (Simulated inductor voltage produced by unity amplitude current source inputs for a) grounded traditional spiral, b) center-tapped spiral, and c) center-tapped spiral driven with in-phase currents.)

Size Comparison

Representative circuits employing the traditional spiral and the center-tapped spiral geometries are shown in Figure 8.10. For equal load impedance to be presented to the differential amplifier transistors, the circuit of Figure 8.10a requires two inductors, each with half the inductance of the single center-tapped inductor in the circuit of Figure 8.10b. To achieve the same electrical performance from the two circuits, however, one must also guarantee that the Q value of the inductors in the circuits are equal. Evaluations of (8.3) shows that Q scales roughly linearly with D, and for any given D, is comparatively independent of L and N (assuming w scales proportional to D and inversely proportional to N). Each of the two inductors employed in Figure 8.10a must therefore be approximately equal in size to the single inductor in Figure 8.10b. An exact analysis based on (8.3) shows that the center-tapped spiral based circuit requires 63% of the chip area used by the traditional spiral based design.

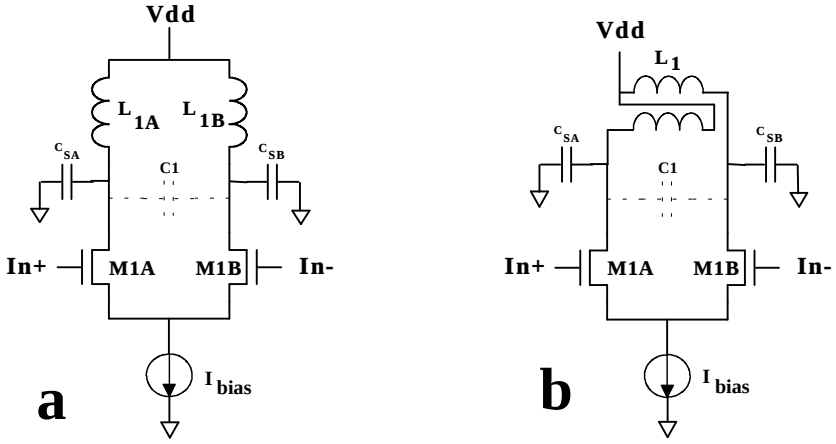

Figure 8.10: Representative balanced filter circuit designs using a) two traditional spirals, and b) a single center-tapped spiral.

Experimental Verification

To validate the simulation results, dimensionally scaled prototypes of center-tapped and traditional spiral inductors were constructed. The prototypes were built using a scale factor of 400 with 1/32" thick double-sided epoxy glass printed circuit board ($\epsilon_r = 4.7$). Trace widths were scaled by the ratio of the board thickness to the thickness of a typical field oxide layer between substrate and top-level metal (2 μm), resulting in w = 62.5 mil and D = 7.0". To approximate the ground plane behavior of the substrate in a typical silicon IC process, 8 radial, 62.5 mil wide cuts were made in the ground plane, extending from the spiral center to 0.25" beyond the outer trace, with one cut extending completely to the board edge. These cuts provide low resistance between inter-turn capacitances, but high resistance to major eddy current loops – properties characteristic of spiral inductors constructed over a moderate resistivity substrate.

Simulation predictions and measured results for inductance L and self-resonant frequency f_R are compared in Table 8.2. As expected, the overall inductance values for the two coils are essentially equal and the self-resonant frequency of the center-tapped spiral is approximately twice that of the grounded traditional spiral. To validate the coil balance simulation, the center-tapped spiral was used as the inductive load in a bipolar transistor amplifier circuit similar to the FET circuit of Figure 8.10b. A CMRR of 36 dB was measured at 1 MHz, and 37 dB at the in-circuit resonance frequency of 2.14 MHz.

Table 8.2: Comparison of traditional and center-tapped spiral performance.

	Simulated		Measured	
	$L(\mu H)$	$f_R(MHz)$	$L(\mu H)$	$f_R(MHz)$
Traditional spiral (grounded)	47.1	1.33	47.9	1.10
Traditional spiral (floating)	47.1	2.54	46.4	2.42
Center-tapped spiral	47.1	2.69	46.5	2.38

8.3 Filter Tuning

For high-Q filter implementations ($Q \geq 50$), fractional bandwidths will be small compared with the deviations in center frequency expected due to fabrication tolerances. In addition, the Q enhancement required will be large, leading to problems in obtaining accurate Q values. These issues, together with circuits that can be used to vary the filter's frequency and Q are considered in the following paragraphs.

8.3.1 Frequency Tolerance and Temperature Coefficient

The center frequency f_o of a Q-enhanced filter is a function of the spiral inductance and of the capacitance of inductor turns and connected circuitry. The inductance value is primarily controlled by the spiral's dimensions and is therefore relatively unaffected by process variations. Capacitances, however, may vary considerably. For example, field oxide thicknesses, and therefore inductor turn-to-substrate capacitances may vary by $\pm 10\%$ or more. Since the sensitivity of f_o to C is 0.5, a $\pm 10\%$ capacitance tolerance implies a manufacturing tolerance for frequency of $\pm 5\%$. Recalling that the bandwidth B of a second-order response is given by $B = \frac{f_o}{Q}$, the maximum filter Q possible without an initial trim is therefore found to be on the order of 10 or less, depending on the filter precision required.

The temperature coefficient of f_o depends on variations in oxide and circuit capacitances. For oxide capacitances, the temperature coefficient of capacitance can be as low as ± 100 ppm/^oC [97]. If capacitance variations of connected circuitry can be neglected, this results in a 0.35% frequency shift for a temperature change of $0 - 70^oC$, implying a maximum filter pole Q on the order of 100 without real-time tuning. In practice, however, this level of stability may be difficult to achieve. For example, in a parallel mode Q enhancement design, the effective inductance L_p is a function of Q_o, making frequency also dependent on trace series resistance tolerances and temperature coefficients. The sensitivity of f_o to

R_s can be found using the well known expression for f_o in conjunction with equation (8.6), yielding:

$$S_{R_s}^{f_o} = -\frac{1}{1+Q_o^2} \tag{8.18}$$

For AlSiCu metallization, the temperature coefficient of resistivity, and hence of R_s is on the order of 4000 ppm/^oC [185]. Thus, for the case of a relatively low Q inductor with $Q_o = 2.5$, the expected frequency drift due to R_s alone is -550 ppm/^oC.

8.3.2 Q Tolerance and Temperature Coefficient

Effects of manufacturing tolerance and temperature coefficients on Q_{enh} are even more severe than those for center frequency f_o, especially for large Q enhancements ($\frac{Q_{enh}}{Q_o} \gg 1$). To determine these effects, variations in both the negative resistance circuit's g_m value and the spiral's series resistance must be considered. Using Equations (8.5) and (8.8) to solve for the sensitivities of Q_{enh} to g_m and R_s for a parallel mode filter yields:

$$S_{g_m}^{Q_{enh}} = \frac{Q_{enh}}{Q_o} - 1 \tag{8.19}$$

$$S_{R_s}^{Q_{enh}} \approx -\frac{Q_{enh}}{Q_o} \tag{8.20}$$

Manufacturing tolerances on g_m are functions of both FET channel mobility μ and threshold voltage V_T, with values of $\pm 15\%$ and ± 0.2V being typical [180]. Manufacturing tolerances on R_s can be even broader since metallization thicknesses are not tightly controlled in a typical CMOS process. Deviations as high as $\pm 25\%$ are possible. Thus, even for low Q enhancements, at least a one-time trim will be required.

Temperature coefficients for g_m and R_s are also significant. As stated, the temperature coefficient of R_s is on the order of +4000 ppm/^{o}C. For g_m, the temperature coefficient is determined by variations in both μ and V_T. Assuming operation at low gate-source voltage V_{gs} so that:

$$g_m \approx \mu C_{ox} \frac{W}{L}(V_{gs} - V_T) \tag{8.21}$$

one can find a first-order estimate of these effects. Sze [180] shows data indicating coefficients for μ and V_T on the order of -5000 ppm/^oC and -3 mV/^oC, respectively. Since the effects of μ and V_T on g_m are opposite in sign, some first order temperature compensation of the combined effects may be possible by careful design. However, even if a reduction to $\pm$1000 ppm/^oC is achieved, and the Q enhancement is limited to 10, variations in Q_{enh} of up to 60% can result for a 70^oC temperature change, and some form of real time tuning becomes necessary.

8.3.3 Frequency and Q Adjustment

Both one-time tuning and real-time tuning require mechanisms for adjusting frequency and Q. For Q adjustment, the negative resistance circuit can be implemented with tunable transconductors. A popular architecture for balanced circuits is a differential pair such as shown in Figure 5.5, whose gain can be varied through bias current adjustments. This circuit has the advantages of very high frequency operation and provision for positive feedback by cross-coupling transistor gates and drains. Other tunable transconductor circuits can be borrowed from the design of Gm-C filters to the extent that they function at high frequencies. For example, linearized differential pairs have been proposed in the literature [68]. However, since increases in supported signal voltages can be offset by increased noise injected into the LC circuit, limiting potential dynamic range improvements and degrading

the filter's noise figure, the excess noise behavior of these techniques should be carefully assessed.

For frequency adjustment, variable capacitances can be provided either in the form of varactor diodes (if supported in the process), or by switching capacitances in and out of the circuit [70]. In either case, the Q of the tuning capacitances must be large enough to avoid significant degradation of the base LC circuit Q. An interesting alternative proposed in [77] is to vary the effective *inductance* value through tunable reactance multiplication circuits. If this approach is adopted, care must be taken to avoid degradation of the circuit's dynamic range due to the additional active circuitry. An alternative approach which obtains similar results, but does not require the insertion of a resistor to detect inductor current is suggested in Figure 8.11. Here, a small valued inductor is simulated with a gyrator, and paralleled with the RLC resonator to provide fine adjustment of frequency.

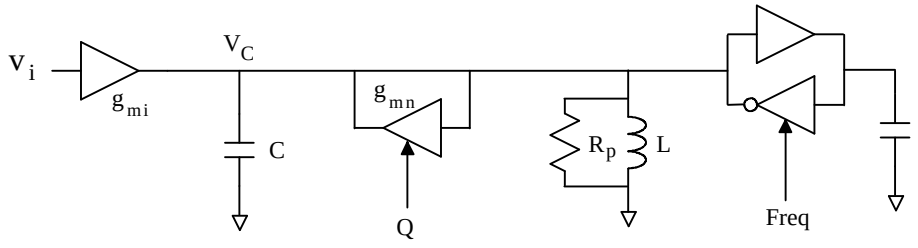

Figure 8.11: Frequency fine tuning using capacitively loaded gyrator.

An analysis of the noise behavior of these two approaches using the techniques of Chapter 6 suggests that significant dynamic range degradation occurs if the tuning range is on the order of $\frac{1}{Q_o}$ or higher. Thus, for $Q_o \geq 5$, it may not be possible to implement a sufficient tuning range with these techniques alone. In this case, some combination of switchable capacitances to achieve coarse control (e.g. to within 1% with 3 to 4 bits of digital adjustment), combined with fine tuning over a $\pm 1\%$ range could be used.

8.4 Higher-Order Filter Design

In the previous sections, a single resonator was used within the filter design, providing only a single-pole response. To obtain higher-order filter designs, such filters could be cascaded, or a coupled-resonator design similar to that considered in Chapter 5 could be adopted. The coupled-resonator option has the advantage that identical resonator sections can be used, simplifying the tuning process. In the following discussion, considerations for the design of coupled-resonator higher-order Q-enhanced LC filters are presented using a fourth-order design as an example. The approaches discussed can be extended to higher-order filters provided that magnetic coupling from non-adjacent resonators can be suitably controlled.

A fourth-order coupled-resonator design is shown in Figure 8.12 in single-ended form. For differential circuits, the same considerations apply, with the components shown representing one half-circuit of the differential design. In this simplified equivalent circuit, g_{mi} and g_{mo} provide input and output buffering to the two resonant circuits which are assumed identical and magnetically coupled. Resistors R_1 and R_2 represent the combination of equivalent inductor parallel loss resistance and the negative resistance used for Q enhancement.

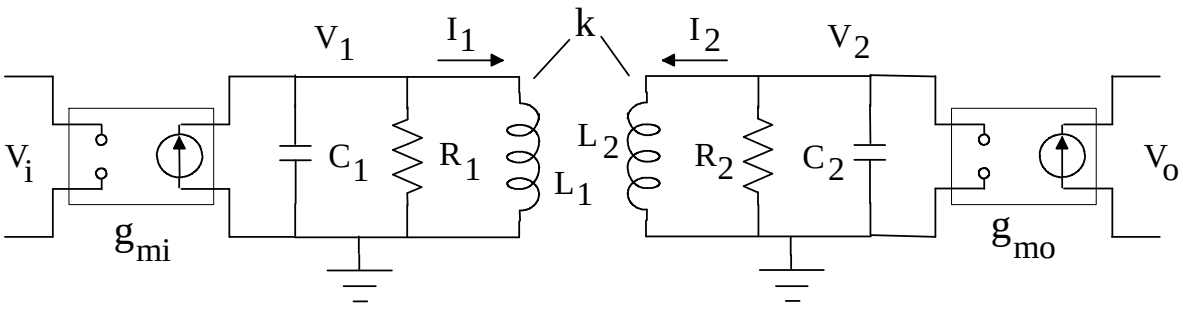

Figure 8.12: Coupled resonator filter architecture.

The response of this circuit can be derived in several ways. The approach taken below is intended to provide some insight into the coupling coefficient's effects on transfer function

formation. This approach can also help in analyzing effects of oscillator signal feedthrough due to magnetic coupling when one of the tuned circuits is used as the master in a master/slave tuning architecture.

The voltage V_2 in Figure 8.12 can be written in terms of currents I_1 and I_2 in inductors L_1 and L_2 as:

$$V_2 = sL_2I_2 + sMI_1 \tag{8.22}$$

where M is related to the magnetic coupling coefficient k by $M = k\sqrt{L_1L_2}$. If the two resonant circuits are assumed identical, one may set $L_1 = L_2 = L$ to obtain:

$$M = kL \tag{8.23}$$

From (8.22), the parallel resonant circuit composed of L_2, C_2, and R_2 can be modeled by the equivalent circuit shown in Figure 8.13a, where V_k is found from Equations (8.22) and (8.23) to be given by:

$$V_k = skLI_1 \tag{8.24}$$

or, since $I_1 = V_1/sL$:

$$V_k = kV_1 \tag{8.25}$$

Thus, from Figure 8.13a, V_2 is seen to be k times V_1, magnified by the effects of series resonance (since $R_2 \gg X_{C_2}$). At the resonant frequency:

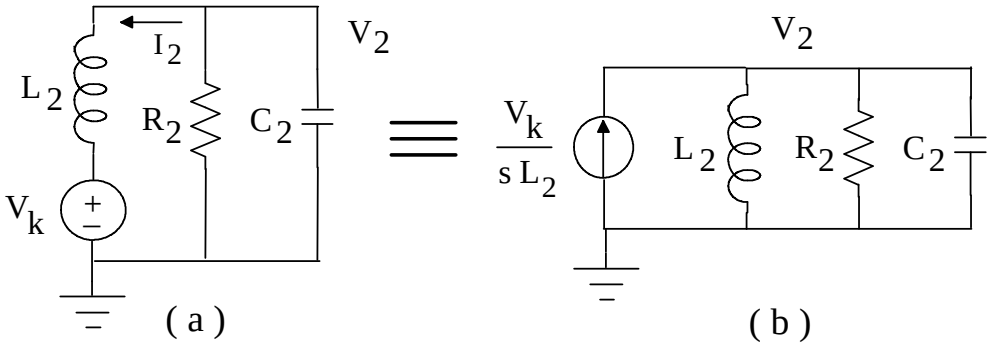

Figure 8.13: Circuit models of magnetic coupling.

$$|V_2| \approx kQ|V_1| \tag{8.26}$$

and if k is on the order of $\frac{1}{Q}$ or above, essentially full coupling results.

To find an exact expression for V_1 and V_2 in Figure 8.12, the Norton equivalent circuit in Figure 8.13b may be used to write:

$$V_2 = \frac{kV_1}{sL_2} Z(s) \tag{8.27}$$

where $Z(s)$ is the impedance of the parallel resonant LCR circuit. Similarly, the expression for V_1 in Figure 8.12 may be written as:

$$V_1 = g_{mi} V_i Z(s) + \frac{kV_2}{sL_1} Z(s) \tag{8.28}$$

Solving Equations (8.27) and (8.28) for the transfer functions from V_i to V_1 and V_2 with $L_1 = L_2 = L$, yields:

$$\frac{V_1}{V_i} = g_{mi} Z(s) \left[\frac{1}{1 - \left(\frac{k}{sL} Z(s) \right)^2} \right] \tag{8.29}$$

$$\frac{V_2}{V_i} = \frac{k}{sL} Z(s) \frac{V_1}{V_i} \tag{8.30}$$

Thus, the response from V_i to V_1 is second-order bandpass, modified by an additional term that depends on the coupling coefficient and the Q value. The response from V_i to V_2 is then found by cascading that to V_1 with an additional second-order section, yielding a fourth-order response. These transfer functions are plotted in Figure 8.14 for the cases of $k < \frac{1}{Q}$ (under coupling), $k = \frac{1}{Q}$ (critical coupling), and $k > \frac{1}{Q}$ (over coupling), a normalized frequency of 1 Hz, and a Q of 100.

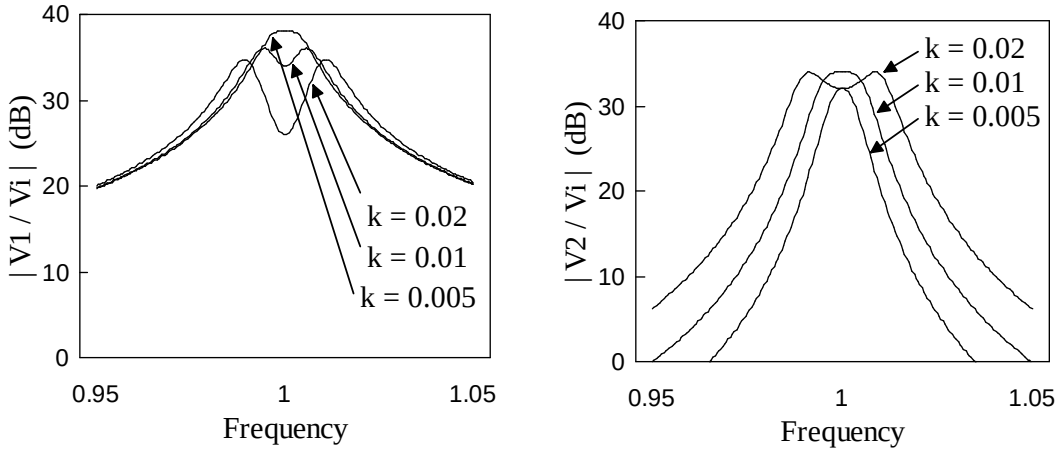

Figure 8.14: Calculated transfer functions for coupled resonators with $Q = 100$, and $f_o = 1$.

In practice, Q is determined by the desired filter transfer function, while the coupling coefficient k is a function primarily of inductor placement on the die. To determine expected coupling values, simulations were performed using a finite element model of flux linkages for two identical spirals in free space. Results are shown in Figure 8.15 for the cases of

lateral and diagonal displacements. These results were found to be relatively independent of absolute inductor size or number of turns.

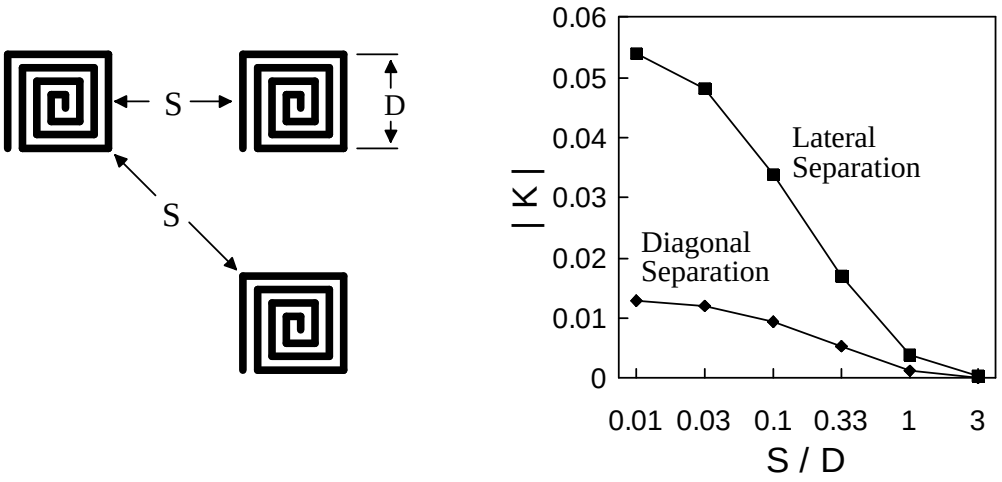

Figure 8.15: Simulated coupling coefficients versus inductor separations.

If the available chip area is insufficient to provide adequate separation for a desired k, some method of coupling neutralization will be required. One solution to this problem is suggested in Figure 8.13. Since the Norton current source value is $\frac{kV_1}{sL}$, the effect of coupling is to inject a current proportional to the integral of the voltage present in the opposite resonant circuit. Hence, the coupling can be reduced by injecting a current of the opposite sign using an integrating transconductance.

Measurements conducted on the prototype filter described in the following chapter together with subsequent simulations indicate that when Q_o is low (e.g. < 10), the use of a pure integration results in an asymetric response characteristic. For the case of low Q_o, the solution to this problem is to employ a *lossy* integrator providing both in-phase and quadrature neutralization. This can be observed by repeating the above analysis with a series RL circuit in place of the ideal inductors, and using this RL model to find the value of the Norton source.

Chapter 9

Q-Enhanced LC Filter Implementations

This chapter describes two Q-enhanced LC filters designed and fabricated during the course of this research.[1] The main purpose of these circuits was to demonstrate the overall feasibility of Q-enhanced filter technology and to validate theoretical performance predictions of earlier chapters. However, each filter was also designed with an application in mind, and with additional development, could potentially be used within commercial products.

The first design, described in Section 9.1, is a simple 100 MHz second-order filter with *off-chip* inductors, developed early in the research. The purpose of this design was to prototype essential components including negative resistance transconductors, and to validate performance predictions including dynamic range, noise figure, and short-term tuning stability. Since the inductors in this filter were off-chip, relatively high Q_o values could be realized (e.g. $Q \approx 100$), and ultra-high Q values could be achieved through Q enhancement (e.g. $Q = 10,000$). Thus, the application envisioned is a narrowband VHF receiver front-end approximating the ideal receiver described in Chapter 4.

The second design, described in Section 9.2, is a more elaborate fourth-order filter with fully integrated inductors. This filter was designed to validate several issues including the performance of the newly developed center-tapped spiral inductor, the use of magnetic coupling and coupling compensation circuits for realizing higher-order filter designs, and

[1]Portions of this chapter have been submitted to the IEEE for possible publication. Copyright may be transferred from the author to the IEEE without notice.

the potential viability of KIS tuning control systems such as those proposed in Chapter 7. With an operating frequency of 200 MHz and a nominal Q of 100, this design was targeted at use within the IF section of a modern cellular or PCS radio receiver.

Both filters were fabricated through the MOSIS service in a 2 μm, 2-poly, 2-metal, N-well BiCMOS process, and were packaged in standard 0.6" wide, 40 pin, ceramic DIP carriers. Hence, the frequency of both designs was confined to the VHF-UHF range. Based on the performance observed with this technology, scaling of the techniques demonstrated here to finer-line processes coupled with the use of modern surface-mount RF packaging should allow similar filters to be constructed at operating frequencies of 900 and 1800 MHz.

9.1 Ultra-High Q VHF Receiver Front-End

A block diagram of circuits implemented on this IC is shown in Figure 9.1. The design includes a differential transconductor at the input, driving an off-chip LC tank circuit connected to pins P1 and P2. Negative resistance circuits on the IC provide Q enhancement to raise the effective Q of the tank circuit to values determined by the control input V_q. A mixer then buffers the signal at pins P1 and P2 and converts this signal to an IF frequency for further processing.

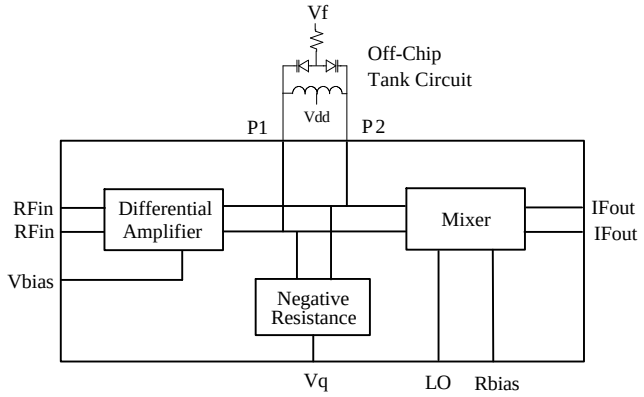

Figure 9.1: Block diagram of ultra-high Q VHF receiver front-end IC.

Use of a mixer, rather than a simple transconductor at the filter output allows the design to be used as a receiver front-end as shown in Figure 9.2. Moreover, operation of the filter at ultra-high Q values (e.g. 10,000) allows the preselection bandwidth to be narrowed to that of the signal being received (assumed to be 10 KHz in the application shown), thereby approximating the design of the ideal receiver of Chapter 4.

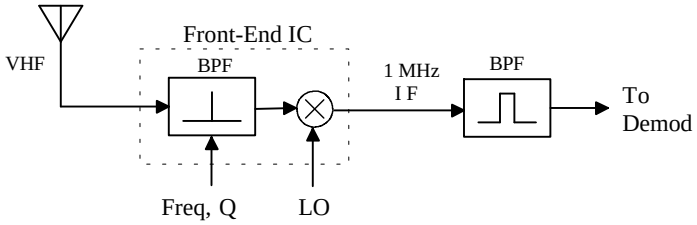

Figure 9.2: VHF receiver architecture block diagram.

In the envisioned application shown in Figure 9.2, VHF signals from the antenna are delivered directly to the filter, which is tuned in conjunction with the LO signal using the receiver's control microprocessor to select different RF channels within the service band. Since the filter operates at a small fractional bandwidth, a simple second-order filter topology can provide good image rejection, allowing the mixer to convert VHF signals to a low IF in a single step. Final channel selection can then be implemented at this IF using conventional fixed-tuned switched-capacitor or gm-C filter designs. Dynamic range requirements on the mixer and subsequent circuits are reduced significantly by the narrow preselection, decreasing the probability of producing spurious (intermod) responses and thereby allowing these circuits to be implemented at very low power.

9.1.1 Design and Layout

Circuits used to implement the input transconductor, negative resistance, and mixer blocks of Figure 9.2 are shown in Figures 9.3, and 9.4.

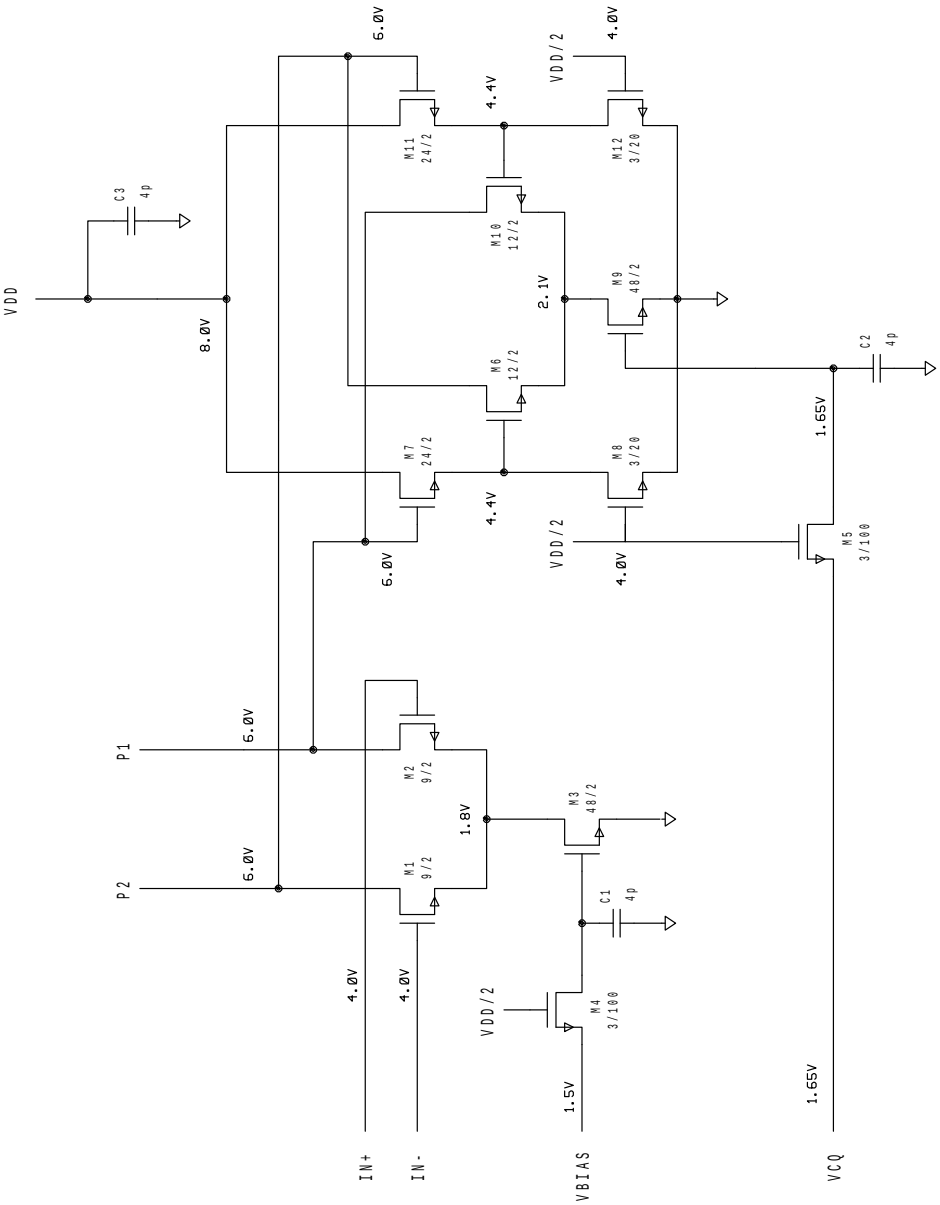

Figure 9.3: Input transconductor and negative resistance designs.

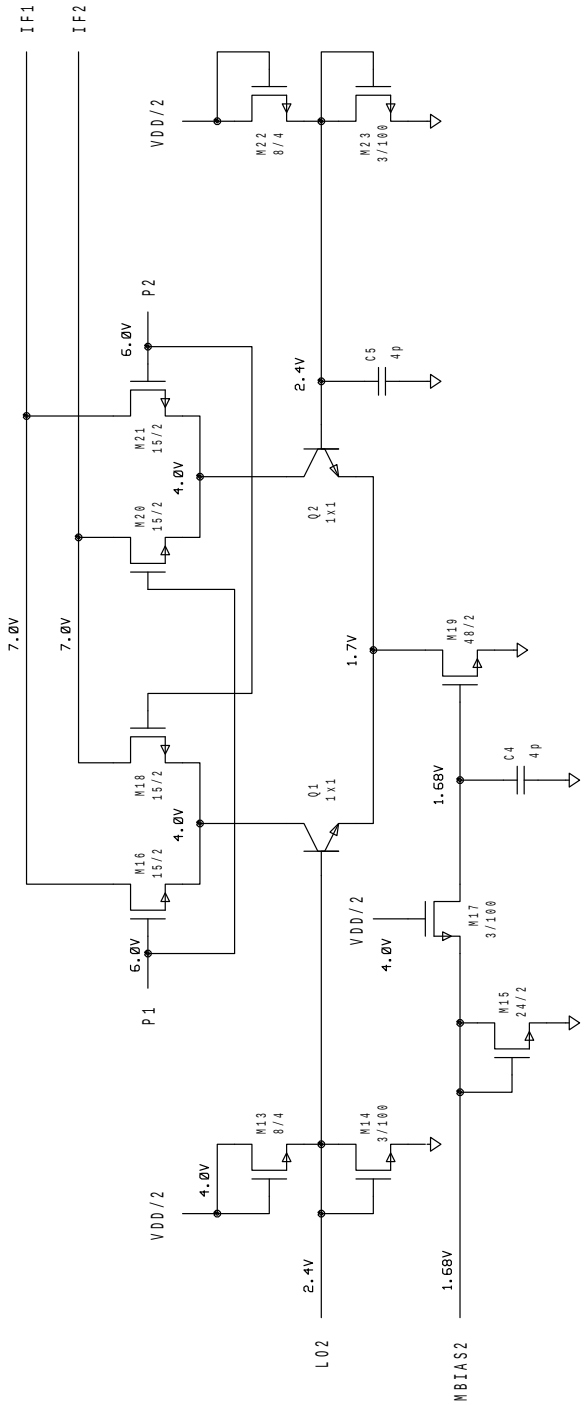

Figure 9.4: Mixer circuit design.

A principle goal in the design of these circuits was to provide good dynamic range performance at very low power. Thus, nominal operating currents for the three circuit blocks were selected as 500 μA, 500 μA, and 1 mA, respectively, and signal processing circuits were designed to support maximum possible voltage swings.

For example, for the differential transconductor of Figure 9.3, a bias level ($g_{gs} - v_T$) of 1.5 volts was chosen to allow large out-of-band signals to be present without saturating the input transconductor's I/V characteristic. This choice fixed the transconductor β at:

$$\beta = \frac{2I_D}{(v_{gs} - v_T)^2} = 220\mu A/V^2 \tag{9.1}$$

and the (half-circuit) transconductance at:

$$g_{m_i} = \beta(v_{gs} - v_T) = 333\mu A/V \tag{9.2}$$

To provide both good dynamic range and good voltage gain, the condition $g_{m_n} = g_{m_i}$ was then adopted as discussed in Chapter 8 to establish the value of R_p at 3000 Ω, and hence, the inductive reactance (assuming $Q_o = 100$) as:

$$X_L = \frac{R_p}{Q_o} = 30\Omega \tag{9.3}$$

Finally, to provide good noise figure performance, the condition $g_{m_i}R_s \approx 1$ was adopted, setting the source resistance at 3 KΩ for the half-circuit, or 6 KΩ for the differential input. Although this is substantially higher than the 50 Ω terminal impedance of typical antennas and test equipment, a simple L-type matching network will transform between these impedance levels with a Q of 11.

The nominal 500 μA bias current for the input transconductor is set by an off-chip control

voltage, providing some flexibility in testing. Similar externally-controlled biasing is used in the negative resistance and mixer circuits, for similar reasons. Within the negative resistance circuit of Figure 9.3, the bias voltage V_q establishes the tail current and thus the transconductance of cross-coupled transconductor M6, M10, thereby controlling the filter Q. The additional transistors M7, and M11 act as source followers to increase the allowable voltage swing at pins P1, P2 to approximately 1 V RMS.

Finally, the mixer shown in Figure 9.4 is implemented as a Gilbert cell in which the lower bipolar differential pair switches the bias current between the two upper MOS transconductor pairs on alternate half-cycles. This somewhat non-standard configuration was adopted to allow the upper transconductors to be implemented with FETs, minimizing loading and pulling of the resonant circuit Q and frequency. Bipolar transistors were then used below to allow full switching to be obtained with minimum possible LO voltages.

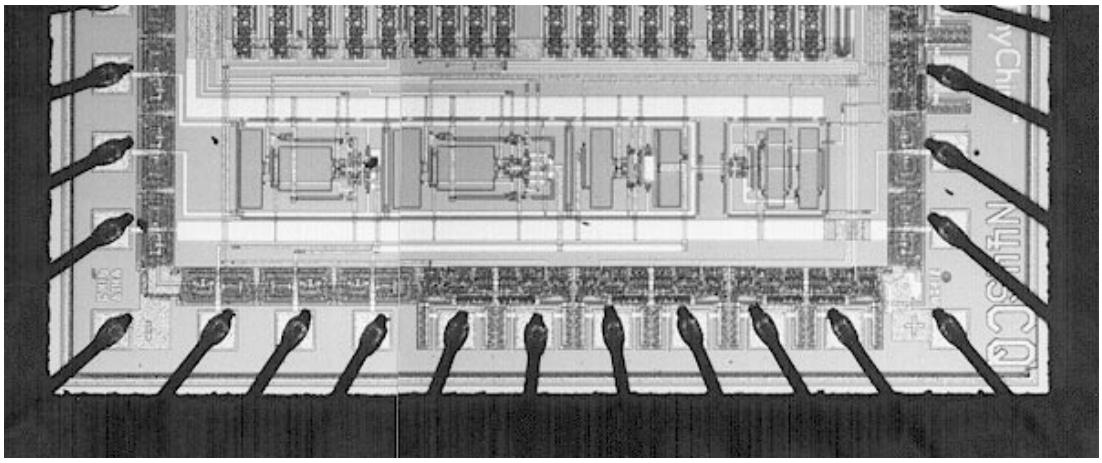

Figure 9.5: VHF front-end IC photograph.

The layout for the circuit was constrained by the need to share space between these circuits and an un-related digital design on the same die. Nevertheless, the relatively small amount of circuitry described here was easily accommodated in the available area as shown in the photograph of Figure 9.5. The only critical layout consideration was the placement of the

input, output, and tank circuit pins which were separated and paired with power and ground pins to the extent possible to maximize signal isolation.

9.1.2 Experimental Results

The IC was tested using the circuits in Figures 9.6 and 9.7 to provide the required bias voltages, tuning controls, and I/O matching networks. Test circuits were constructed on double-sided, glass-epoxy PC board with one side serving as a ground plane. All filter tuning was performed manually with potentiometer controls.

The tank circuit inductors were constructed as air-wound coils with a (calculated) value of 30 nH. The remaining inductors used in the I/O matching networks were commercially acquired, ferrite-core, adjustable units. The two output pins (IF+ and IF-) and their associated matching networks were used to provide outputs at the RF and IF frequencies, respectively. During the majority of tests, the mixer circuit was bypassed by grounding pin 29 through R10, reducing the mixer to a simple transconductor output stage and providing a direct RF output. This allowed the filter to be tested independently of the mixer's performance.

Experimental results obtained are summarized in Figures 9.8 and 9.9, and Tables 9.1 – 9.3. Figures 9.8 and 9.9 show the effects of the Q control input. The base Q of the external tank circuit was found to be approximately 70 with the Q control voltage at zero volts, and a Q of 10,000 was achieved at 1.73V, corresponding to approximately 650 μA of transconductor current. The manual settability of the filter Q was found to be excellent, with Q values of up to 100,000 possible with careful adjustment.[2] In addition, no hysteresis effects were noted when adjusting the Q control to enter and leave oscillation, and good orthogonality was observed between frequency and Q control inputs – important considerations for automatic

[2]The primary limitation here was the potentiometer itself, and the small rotation angles needed between Q = 100,000 and oscillation.

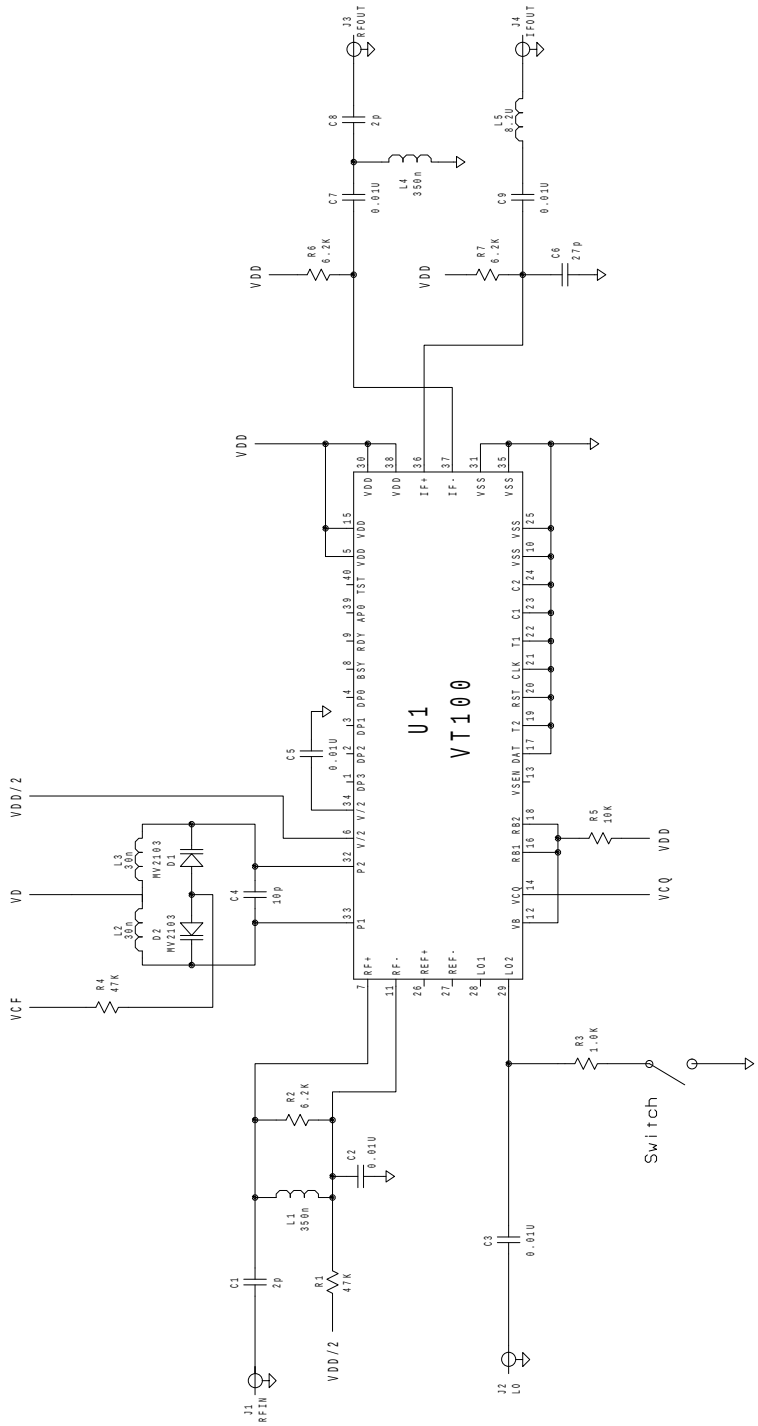

Figure 9.6: Test circuits for VHF front-end IC.

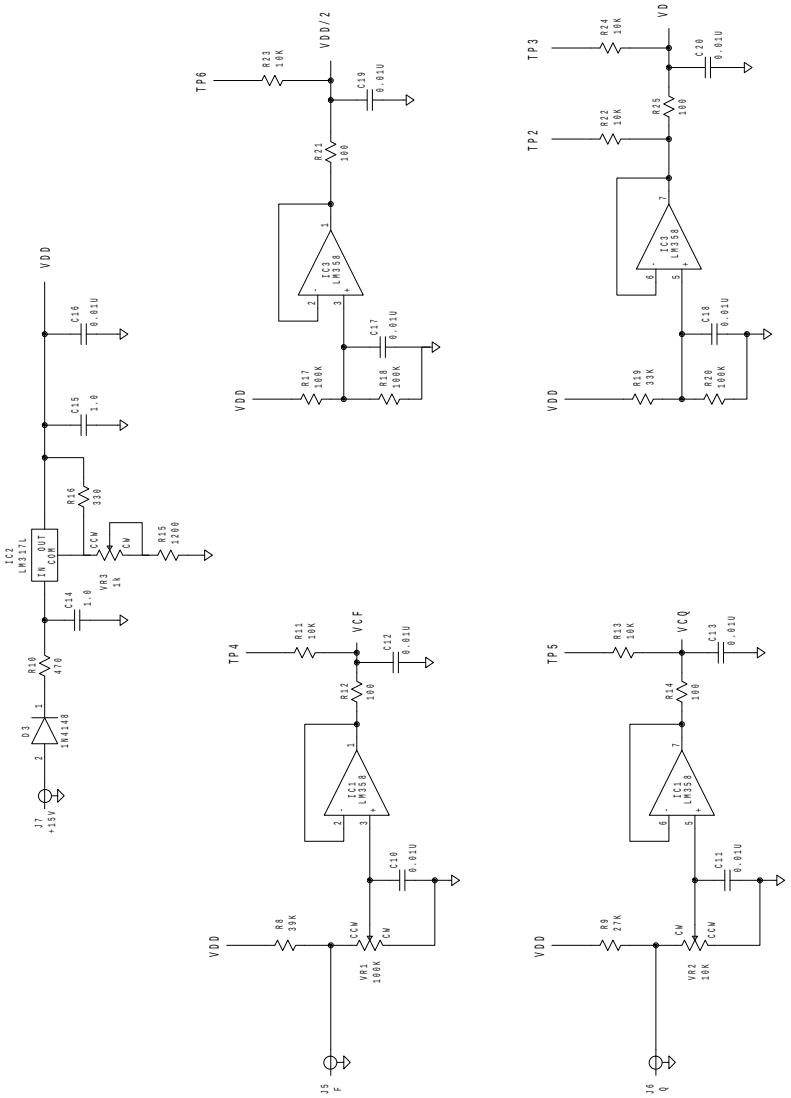

Figure 9.7: Test circuits for VHF front-end IC.

control system design.

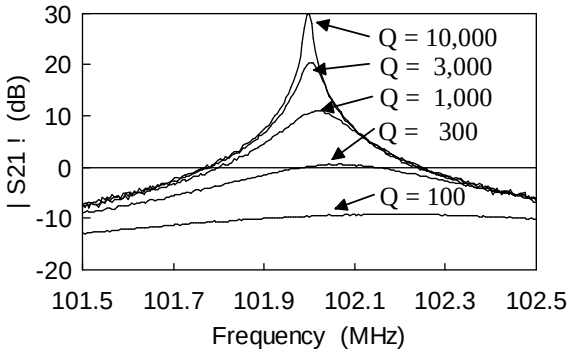

Figure 9.8: Measured transfer functions of Q-enhanced filter.

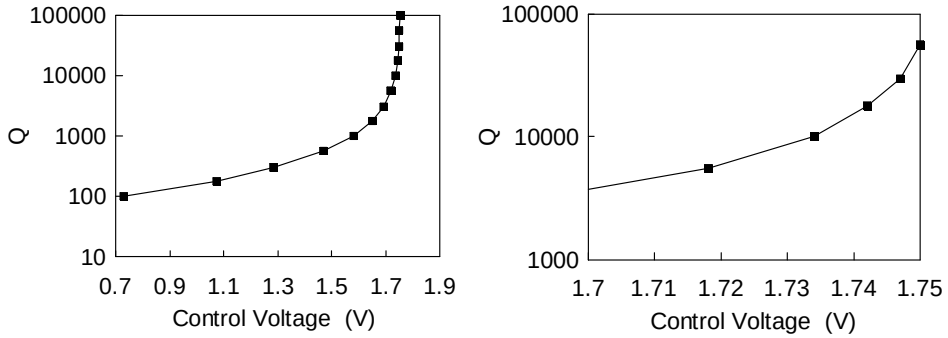

Figure 9.9: Measured Q factor versus control voltage.

Short-term stability of both frequency and Q were found to be excellent as shown in Table 9.1, indicating that the filter is suitable for use with either the self-tuning or orthogonal reference tuning techniques and their simplifications discussed in Chapter 7.

In-band dynamic range and noise figure goals for the design, derived from expressions developed in Chapters 6 and 8 were 71 dB and 11 dB, respectively. These targets were computed based on an assumed maximum capacitor voltage of 1 V RMS, and a matched input condition. As shown in Table I, neither goal was met. The measured in-band dynamic range of 56 dB is attributed to a substantially lower voltage within the tank circuit than

Table 9.1: Measured performance of VHF front-end IC.

Performance Measure	Value
Minimum Q (Base Q of tuned circuit)	70
Maximum Q (Manually controlled)	10^5
Q stability	30% / hour
Frequency tuning range	88 - 102 MHz
Frequency Stability	5 KHz / hour
Minimum discernable signal	-117 dBm
Noise figure	15 dB
Gain (mixer bypassed)	31 dB
Gain (to IF)	22 dB
Blocking dynamic range	
In-band	56 dB
1 MHz offset	102 dB
Spurious free dynamic range	
In-band	42 dB
1 MHz offset	87 dB
Current Consumption ($V_{DD} = 8V$)	
Filter	1.3 mA
Mixer	1.0 mA

that assumed ($v_{max} \approx 200mV$ versus 1 V). Subsequent simulations and study showed this problem to be related to non-linearities in the negative resistance transconductor circuit – a problem common in transconductors used in Gm-C filter designs as well [64]. At large Q enhancements, a drop in transconductor gain as small as 1% results in substantial lowering of the filter Q, and hence lowering of the filter gain (compression) and widening of the bandwidth. This problem could be corrected to some extent in future implementations by employing more linear transconductors within the negative resistance block. In conjunction with this method, designing for lower impedance levels could provide somewhat higher efficiencies.

The higher than expected noise figure was attributed to problems in the input matching network implementation. PC board trace capacitances, combined with the matching network inductor's self-resonance effects, raised the effective inductance value and required the substitution of a lower-valued device. In turn, the loss resistance associated with this new inductor resulted in a lower effective value of R_s seen by the input transconductor. This problem could be corrected in future implementations by designing for lower impedance levels throughout the circuits.

Table 9.2: Blocking dynamic range versus frequency offset.

$\frac{\Delta f}{B/2}$	Measured BDR (dB)	Calculated BDR (dB)
0	56	–
20	81	82
100	96	96
200	102	102
1000	111	116

Finally, Tables 9.2 and 9.3 compare the dynamic range performance with the predicted behavior discussed in Chapters 3 and 6. The relationship between measured in-band dynamic range and spurious-free dynamic range agrees closely with that predicted by Equation (3.24), while the improvement with frequency offset is in excellent agreement with (6.40)

Table 9.3: Spurious-free dynamic range versus frequency offset.

$\frac{\Delta f}{B/2}$	Measured SFDR (dB)	Calculated SFDR (dB)
0	42	–
2	49	50
4	55	56
20	70	70
100	83	84
200	87	90

and (6.41).[3]

Despite the IC's somewhat limited *in-band* dynamic range performance, the ultimate dynamic range at large frequency offsets is excellent. BDR and SFDR measurements of 102 and 87 dB respectively were measured at only 1 MHz offset. Thus, the performance of the circuit makes it an excellent candidate for use within receivers designs for VHF satellites operating under the harsh interference conditions described in Chapter 3.

9.2 Cellular and PCS Receiver IF Filter

The second IC fabricated in the course of this research was a fourth-order (2-pole) coupled-resonator design with *on-chip* inductors and partial on-chip frequency and Q tuning. The nominal operating frequency and selectivity Q are 200 MHz and 100 respectively, and the application envisioned for this design is a first IF filter in a receiver intended for use in new PCS services such as DECT (see Chapters 4 and 10).

[3]Values at the largest offsets diverge from those calculated due to expected saturation effects within the input transconductor. These saturation effects are not accounted for by the equations, but can be predicted as discussed in Chapter 6.

9.2.1 Design and Layout

The prototype filter was implemented using two identical copies of the circuitry shown in the block diagram of Figure 9.10. With this architecture, the circuits can be operated in a variety of modes. For example, with one section disabled, a single second-order filter can be evaluated. Alternatively, with both sections enabled, a coupled resonator 4th order response is obtained. Finally, a master/slave tuned second-order filter can be created by using one section for filtering and configuring the other section as an oscillator.

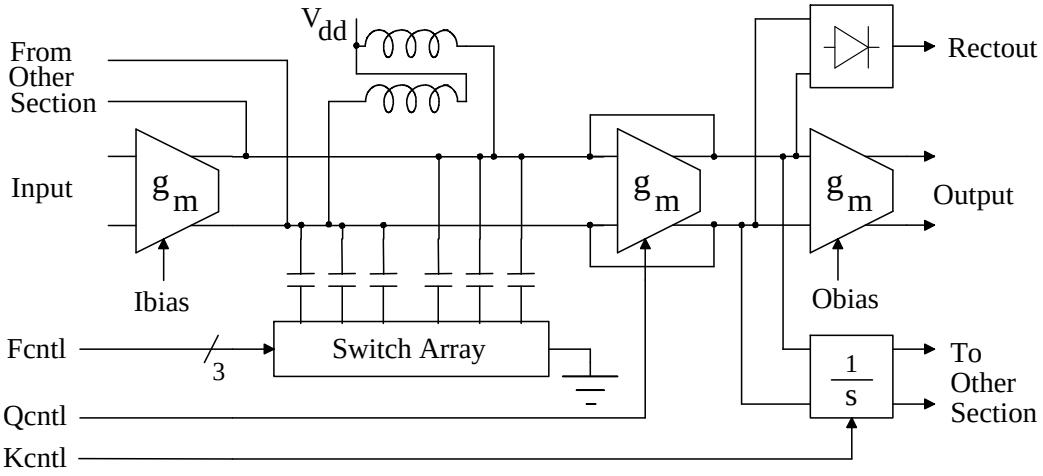

Figure 9.10: Block diagram of IF filter second-order section.

As indicated in the block diagram, balanced circuitry was adopted throughout the design to provide good power supply rejection and signal isolation, while simplifying the implementation of negative resistance circuitry. Circuitry used to implement the input buffer amplifier, spiral inductor load, controlled negative resistance, and output buffer amplifier are shown in Figure 9.11.

The on-chip, center-tapped inductor $L1$ consists of 26 turns with an outer dimension of 850

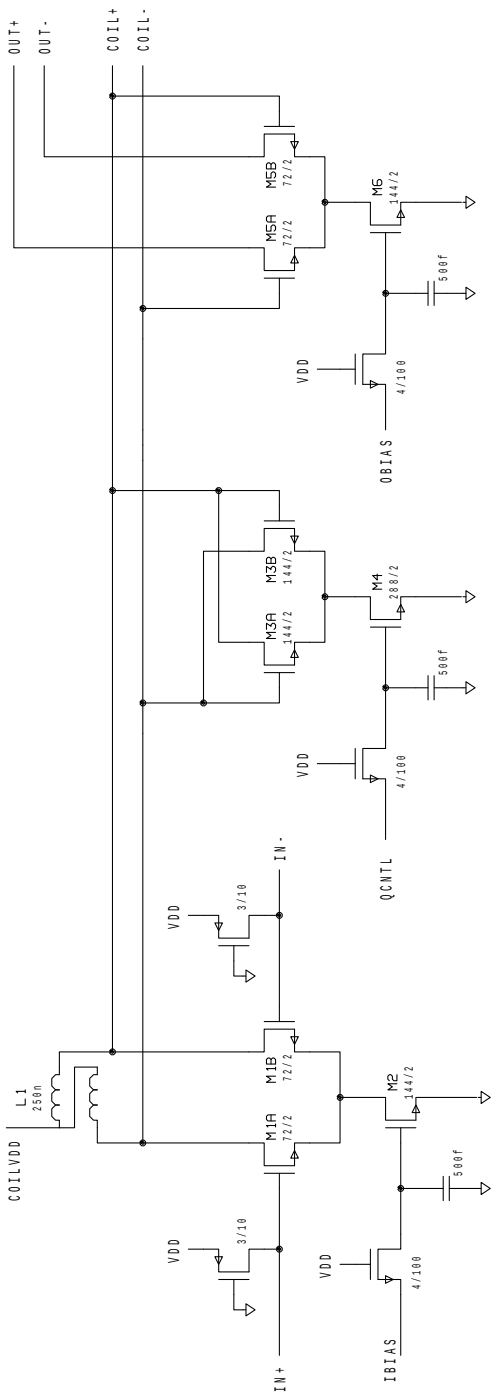

Figure 9.11: Core circuits of IF filter.

μm, yielding a series equivalent circuit inductance value of approximately 250 nH, and a simulated self-resonant frequency of 270 MHz. Trace width and turn pitch are 12 μm and 16 μm, respectively, and nominal process parameters are: metal2 to substrate capacitance = 0.016 fF/μm^2, metal resistivity = 0.03$\Omega/\Box$, and substrate resistivity = 2500$\Omega/\Box$. The substrate resistivity is that of an N well region, which was used in place of a lower resistance active region to achieve thicker oxide separation and a higher self-resonant frequency.[4]

At 200 MHz, the equivalent parallel inductance is found from Equation 8.6 to be 300 nH, for an effective parallel reactance of 377 Ω, and a parallel loss resistance of 830 Ω.[5] This loss resistance is in parallel with the voltage-controlled negative resistance transconductor consisting of M3A, M3B, and M4.

Despite the problem of limited voltage swings encountered in the first IC design, a simple cross-coupled differential design was adopted for the negative resistance function. The reasons for this decision were three-fold. First, by accepting a small voltage swing, the source followers previously used to provide DC voltage offsets between gate and drain nodes could be eliminated, allowing operation of the filter down to 3 V and below. Second, difficulties in simulating designs with transconductors such as those described in [68] left too many unknowns and the overall risk of adopting a new design approach was judged too high. Finally, the 830 Ω impedance level established by the inductor design used, meant that reasonable efficiency could be obtained (signal currents are a higher fraction of the transconductor bias current than for the IC described in the previous section).

The negative resistance circuit was designed to provide the required g_{m_n} value of $\frac{1}{R_p}$ =

[4]Based on these values, the simulated quality factor Q_o at self resonance, including effects of substrate losses, but excluding connected circuitry is 3.0. When operating at the nominal frequency of 200 MHz, a Q_o value of 2.2 is therefore expected.

[5]Inductor self-resonance and inductor Q have strong effects on filter operating frequency and Q, and must be carefully considered. An initial design and fabrication of the chip had to be repeated because simplified calculations were used. The second chip fabricated is described here and used more accurate simulations including substrate losses, inter-turn sidewall and fringing capacitances, and turn-to-turn crossover trace capacitances.

$1.2mA/V$ with a current of 1 mA, implying the transistor W/L values shown in Figure 9.11. Similar, but slightly smaller transistor sizes were then used in the input and output transconductors as shown. The selected values yield a nominal filter gain on the order of 0 dB with 50 Ω source and load impedances when operating at bias currents of approximately 500 μA each.

Frequency tuning is implemented with three copies of the capacitor switching circuit of Figure 9.12a, providing 8 steps of approximately 1.2 MHz each. Four to five bits of control would be provided in practice for more range and finer resolution, but was not implemented in the prototype due to pinout limitations.

Each copy of the capacitor switching circuit consists of a pair of pulldown transistors M7A and M7B which ground tuning capacitors C1A and C1B when on. Since these pulldown transistors must be large to minimize Q degradation, drain capacitance is significant when the transistors are off and must be taken into account. When M7A and M7B are off, the additional circuitry shown biases the switching transistor drains to approximately 2V to lower the junction capacitance and minimize non-linearities for large signal swings. Further drain junction capacitance reduction is achieved by implementing M7A, M7B with arrays of square transistors, each consisting of an annular gate surrounding a minimum size central drain diffusion and contact, a geometry adopted throughout the filter design where possible to limit the effect of parasitic capacitance on filter operation.

Coupling neutralization is performed by the integrating transconductor shown in Figure 9.12b. The RC filters provide approximately 75^o of phase shift, with the remaining 15^o provided by source followers M8A, M8B and transconductor M9A, M9B.

Finally, an amplitude detection circuit is implemented as shown in Figure 9.13 with full wave rectifier M11A - M12B, smoothing filter C2, and DC amplifier M13, M14. The rectifier threshold is set by R1 in conjunction with resistor programmable current source M15, M16.

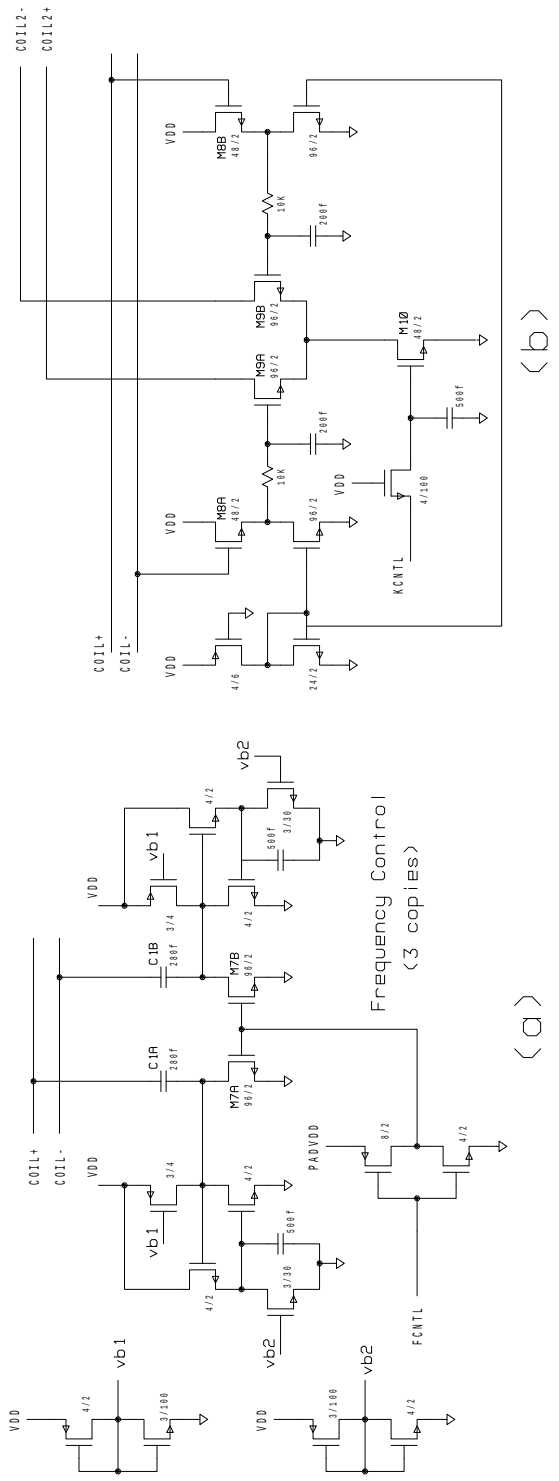

Figure 9.12: Switched tuning capacitors and coupling neutralization circuits.

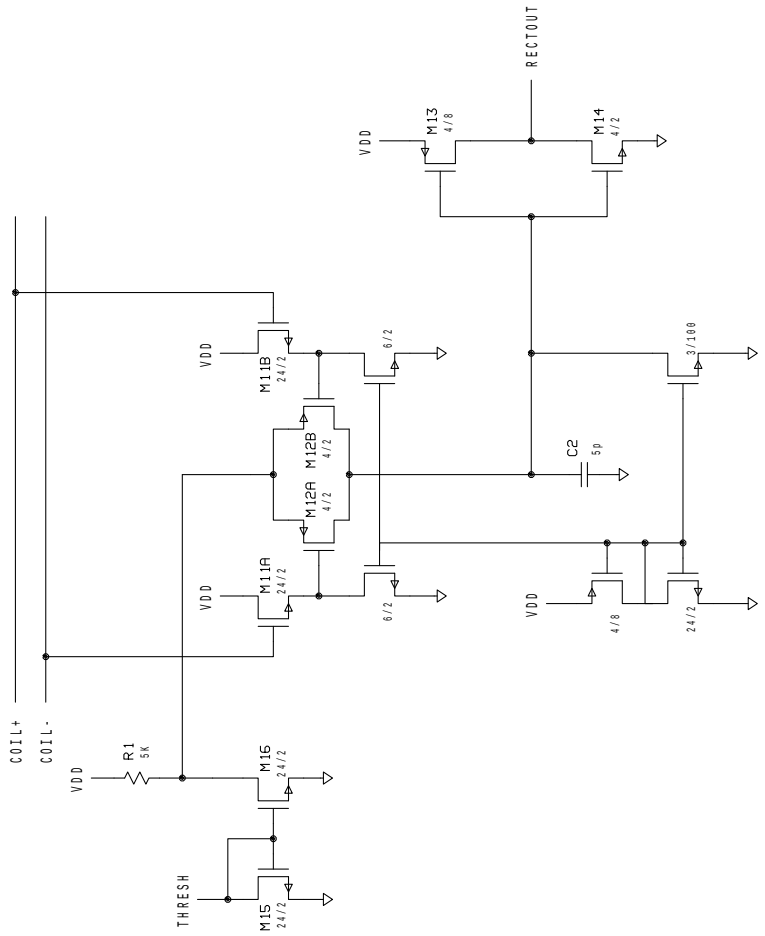

Figure 9.13: Amplitude detection circuit.

A photograph of the fabricated circuitry is shown in Figure 9.14. To provide minimum possible inductor coupling between the two identical second-order sections implemented on the die, the inductors were oriented diagonally opposite to each other. Chip area not used by the circuits discussed above was used to provide on-chip decoupling and supply bypass capacitors and to implement test structures. Total chip area for both second-order sections, excluding pads, is 3.3 mm^2.

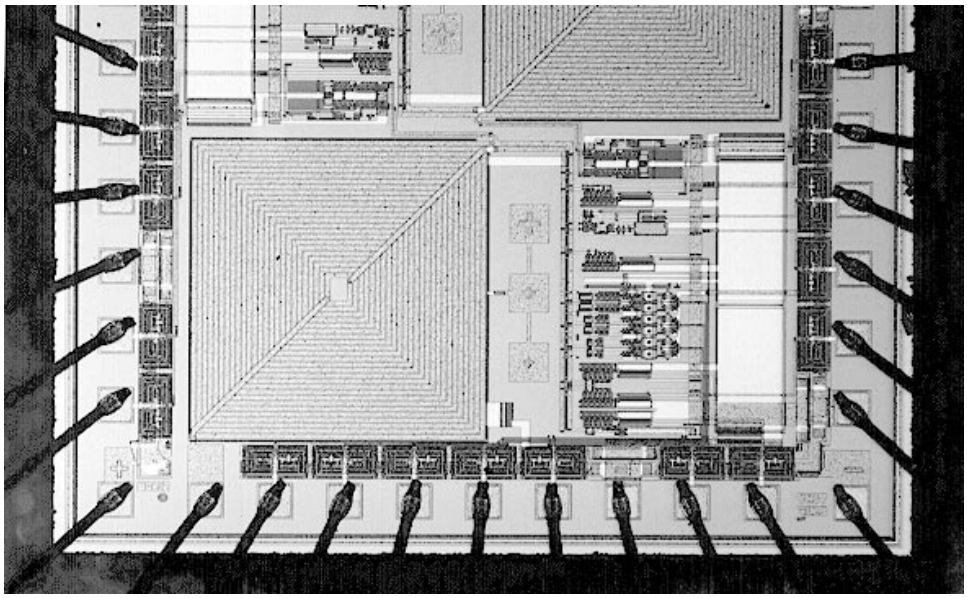

Figure 9.14: Photograph of chip layout.

9.2.2 Experimental Results

The IC was tested using the circuits shown in Figures 9.15 and 9.16 to provide I/O terminations and frequency and Q adjustments.

Figure 9.17 shows measured gain $|S_{21}|$ of a single second-order section at varying values of Q enhancement with the opposite section disabled and powered down. The base Q of

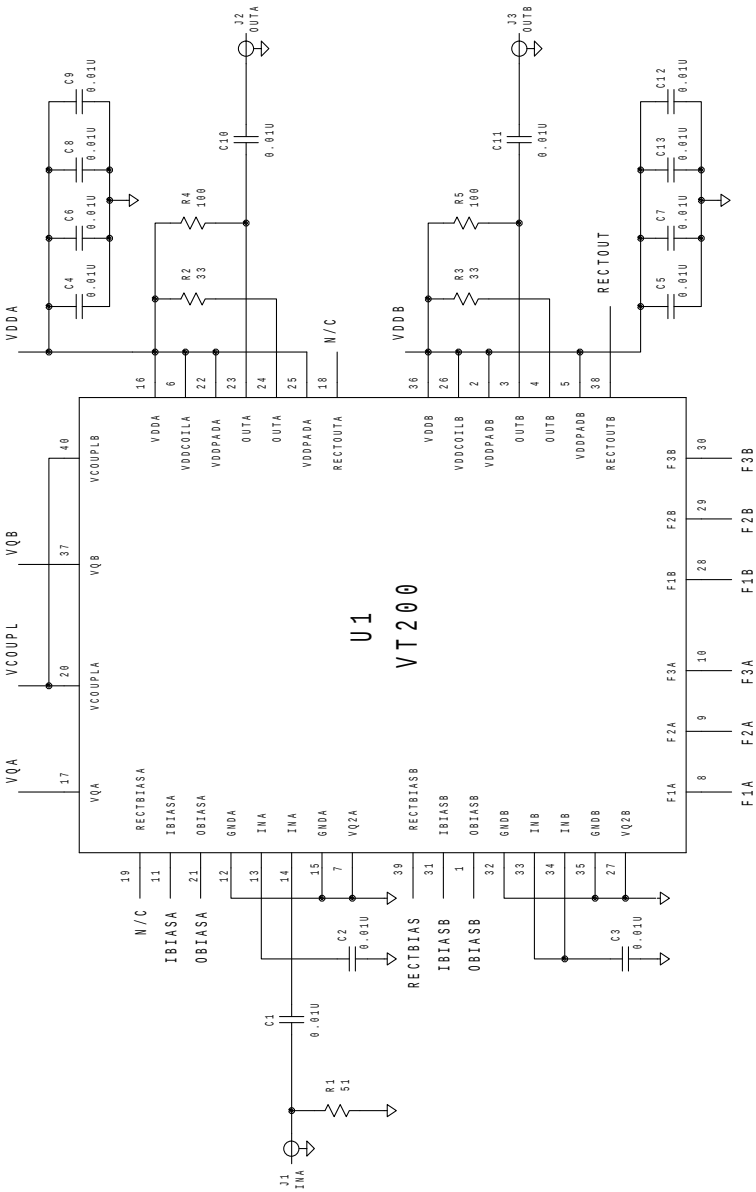

Figure 9.15: Test circuits for IF filter.

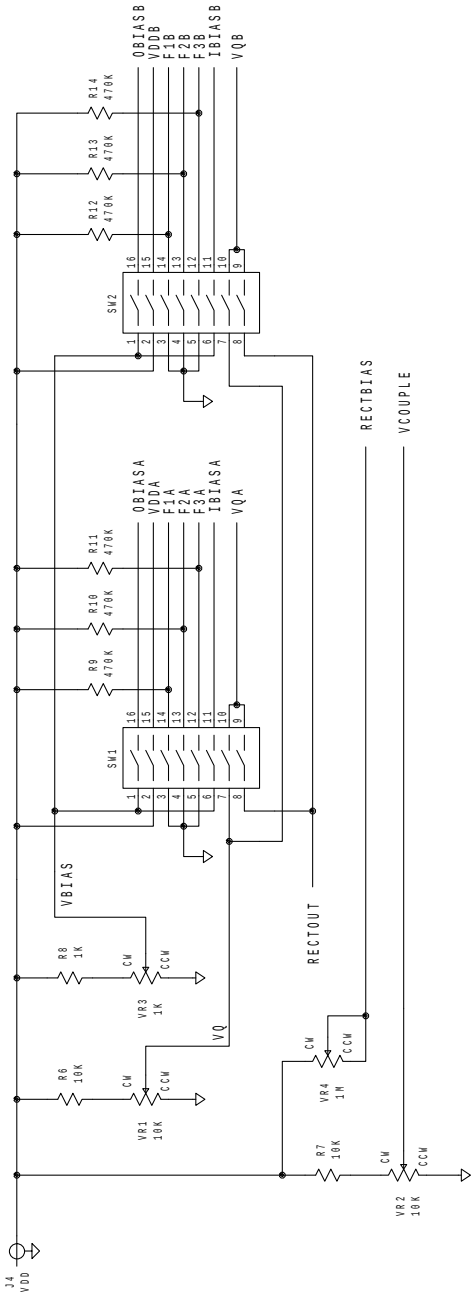

Figure 9.16: Test circuits for IF filter.

the resonant circuit was estimated from the lowest curve as 2.3, in general agreement with results predicted through simulation. For minimum and maximum Q conditions, current consumptions were measured at 2.54 and 3.88 mA, respectively, with a 5V supply, and 1.81 and 2.94 mA, respectively, with a 3V supply.

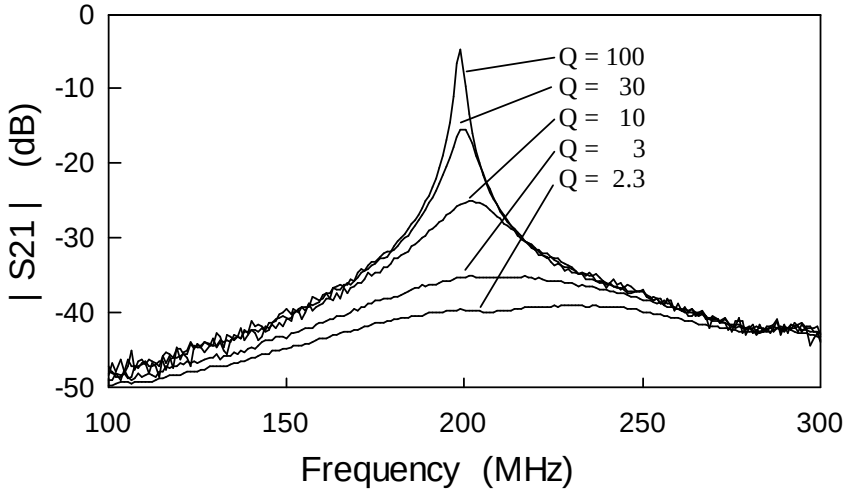

Figure 9.17: Measured $|S_{21}|$ of second-order section at different Q enhancements.

Measured blocking dynamic range (BDR) and spurious free dynamic range (SFDR) are plotted in Figure 9.18 with the second-order section set to a Q of 100 (3 dB bandwidth of 2 MHz). The dynamic range figures shown are in general agreement with predictions and are respectable for filters of this bandwidth. Overall receiver dynamic range would be higher if the received signal were subsequently downconverted to a lower IF with a narrower bandwidth prior to demodulation. For example, the increase in BDR would be 18 dB for a receiver with a 30 KHz signal bandwidth.

A significant limitation on dynamic range was found to be gain compression in the resonant circuits, and associated broadening of the filter bandwidth. These factors were expected based on the results of the first chip design effort. The 1 dB output compression point was found to be -37 dBm, approximately 10 dB lower than the maximum signal output power.

This behavior can be traced to non-linearities in the negative resistance circuitry, indicating that dynamic range performance may be improved through better transconductor design in this area. Additional improvements in dynamic range are possible if a lower resistivity metallization can be used in the spiral inductor implementation, as seen through Equation (8.3) in Chapter 8.

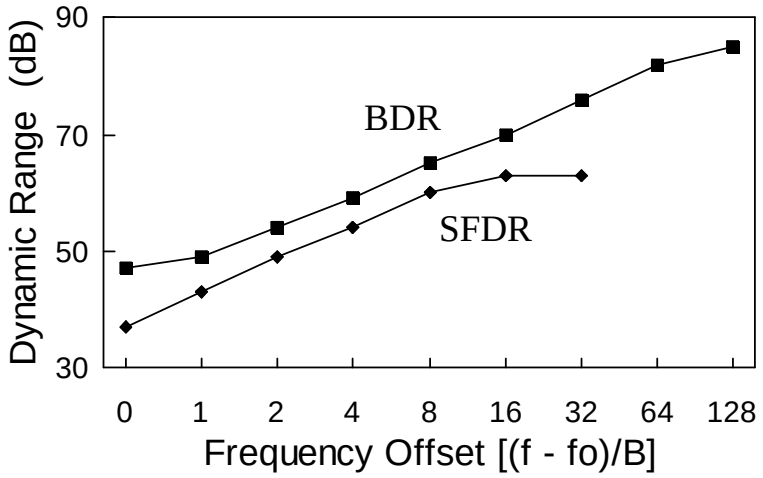

Figure 9.18: Measured blocking and spurious-free dynamic range.

Temperature coefficients of f_o and Q_o were found to be -735 ppm/^{o}C and -15%/^{o}C, respectively, in agreement with predictions in Chapter 8. To investigate the possibility of applying master-slave tuning to compensate for the relatively large Q temperature drift, the opposite second-order section was powered up to serve as a master oscillator and its amplitude detector output was connected to the Q control input of both sections. To provide a lower finite Q in the slave section and to reduce oscillator feedthrough, the master oscillator was operated at maximum frequency, while the slave filter was operated at minimum frequency. Filter response curves measured at 20 to 50^o C are plotted in Figure 9.19, where the oscillator feedthrough is clearly visible.

Frequency tuning was not included in these tests, but could be provided by a suitable

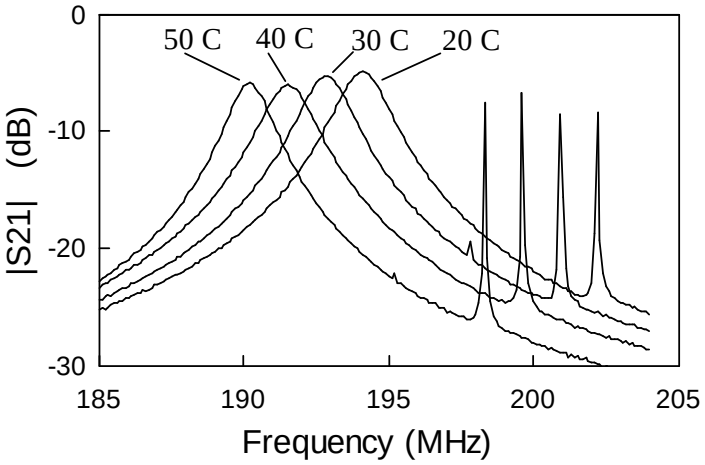

Figure 9.19: Master/slave Q tuning from 20^{o}C to 50^{o}C.

control arrangement designed to monitor and adjust the master oscillator's frequency. In a typical application, this function could be implemented in software through a host receiver's microprocessor and associated counter/timer, thereby limiting additional on-chip circuitry to a simple frequency prescaler as described in Chapter 7. Q stability and frequency tracking between master and slave seen in Figure 9.19 suggest that Q values up to 100 or higher could be supported with this approach.

Oscillator output power was adjusted to -32 dBm for these tests by resistor programming of the amplitude detector. At this level, the oscillator signal feedthrough in the filter output was -47 dBm, which is relatively large compared with the -37 dBm output compression point. Single-sided phase noise of the master oscillator in a 1 Hz bandwidth was measured as -84 dBc at 10 KHz offset and -105 dBc at 100 KHz offset. These are acceptable levels to allow the master oscillator to double as a local oscillator for downconversion to a subsequent IF, as will be shown in Chapter 10.

Finally, the chip was configured as a fourth-order filter by applying equal frequency and Q control signals to both sections using manual adjustments. To maintain Q balance, the input and output buffers of both sections were enabled. The resulting filter response is

shown in Figure 9.20a.

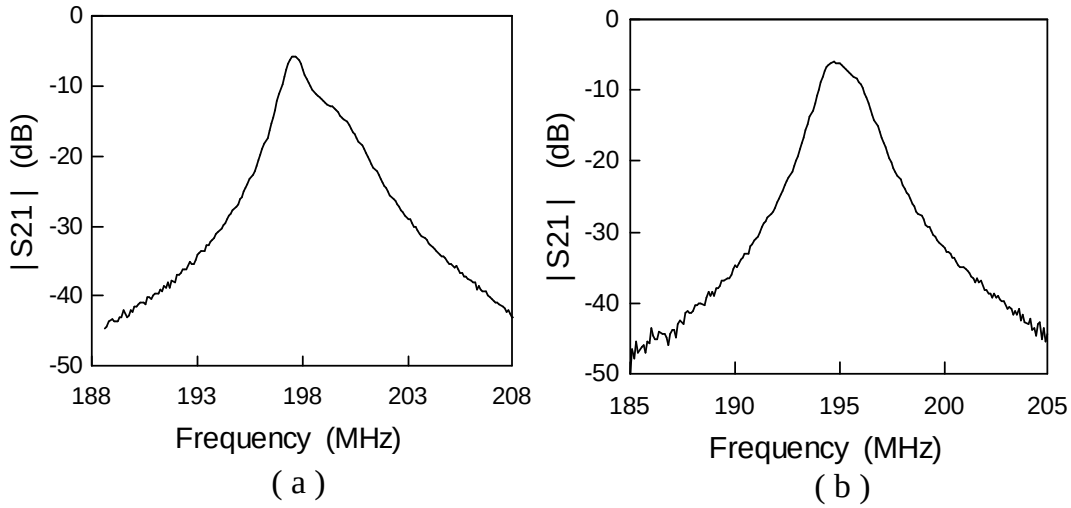

Figure 9.20: Measured fourth-order response. a) Without neutralization. b) With neutralization.

The assymetry seen in the passband is due to the presence of in-phase as well as quadrature coupling between the two coupled resonators, as discussed in Section 9.2.1. Since no in-phase neutralization circuitry was included in the prototype filter, an alternative technique consisting of offsetting the frequency of the second resonator by 2.5 MHz was used to equalize the passband ripple. The coupling adjustment control was then applied to achieve the response shown in Figure 9.20b. Future designs will incorporate both in-phase and quadrature neutralization to provide a more ideal response characteristic. Simulations indicate that demands on stability of the coupling neutralization circuitry are not excessive. Variations as high as 10% result in less than 1 dB of passband assymetry if a Q_o of 5 can be achieved.

Tuning of frequency and Q for the fourth-order filter was not implemented in the prototype, but could be provided using either a Master/Slave approach, or the Self-Tuning approach reviewed earlier in Chapter 7. Measurements made on the prototype filter indicate that the short term stability of both f_o and Q are sufficient to support the latter technique. Short

Table 9.4: Measured performance of IF filter second-order section.

Performance Measure	Value
Frequency tuning range	194 - 203 MHz
Q tuning range	2.3 - ∞
Nominal 3 dB bandwidth	2 MHz
Nominal gain (50Ω I/O)	-5 dB
Ultimate rejection	40 dB
Blocking dynamic range	
In-band	47 dB
4 MHz offset (alternate channel)	54 dB
32 MHz offset	72 dB
Spurious free dynamic range	
In-band	37 dB
4 MHz offset (alternate channel)	49 dB
32 MHz offset	63 dB
Temperature coefficients (open loop)	
Frequency	-735 ppm/^{o}C
Q	-15%/^{o}C
Supply voltage	3 - 5 V
Supply current (3 V)	2.94 mA
Chip area (excluding pads)	1.7 mm^2

term frequency drift was measured as less than 10 KHz in 5 seconds and less than 50 KHz in 5 minutes at room temperature. Short term drift for Q was negligible over periods of several minutes at Q values as high as 200.

Chapter 10

Integrated Receiver Design

In this final chapter, the issue of integrating local oscillators is briefly considered, completing the analysis of receiver components which have so far resisted integration in commercial products. System level design considerations and circuit-level design techniques developed throughout this dissertation are then combined in developing a hypothetical, fully integrated receiver. The intent of this receiver design exercise is not to embark on a full-scale receiver development, but rather to show how the complete theory developed thus far can be used in future commercial products. Thus, only a top-level design is presented, and circuit level implementation is left to future work.

10.1 Integration of Local Oscillators

In addition to bandpass filters, a fully integrated receiver will typically need to include integrated local oscillators. Oscillators, like filters, can be implmented in integrated form using either Gm-C, or LC based active circuits. Indeed, such oscillators are routinely used within integrated filters to serve in master-slave tuning. However, before using these techniques to implement receiver LOs, the issue of oscillator spectral purity must be addressed.

In the first subsection below, the phase noise performance of LOs will be examined and phase noise estimates will be found through simple extensions of the dynamic range expressions for filters developed in Chapter 6. Following this derivation, the effects of phase noise on

receiver performance are considered, and expressions for determining required phase noise performance are developed.

10.1.1 Phase Noise in Oscillators

An oscillator may be created from a simple second-order resonator (filter) by letting $Q \rightarrow \infty$, and most practical oscillator designs can be reduced to this form. A critical study of oscillator operation shows that the actual Q of the oscillator is large, but finite. Thus, the spectrum of the oscillator is that of filtered noise, rather than the single-frequency spectral line normally assumed in a simplified analysis.

A study of oscillator noise based on these concepts was carried out as early as 1964 by Robins [147] who showed that the ratio of phase noise in a 1 Hz bandwidth N_{op} to oscillator power P_{osc} may be written in the form:

$$\frac{N_{op}(\Delta f)}{P_{osc}} = \frac{FkT}{P_{osc}} \frac{1}{8Q^2} \left(\frac{f_o}{\Delta f} \right)^2 \tag{10.1}$$

where Δf is the frequency offset from the oscillator center frequency f_o at which the noise is measured, F is a noise figure for the active circuits used, Q is the quality factor of the resonator on which the oscillator is based, and k and T have their usual meanings. This expression is approximately valid for Δf greater than some lower limit in the range of 10 Hz to 100 KHz, depending on the actual oscillator construction. At frequencies below this limit, the noise spectrum varies at rates of $(\Delta f)^{-3}$ or higher due to 1/f noise in the active components used in the realization [147].

Although Robin's derivation is straightforward and could be reviewed here in more depth to illustrate the factors and assumptions involved, similar results can be obtained with less effort by leveraging the dynamic range expressions for Gm-C and Q-enhanced LC filters

developed in Chapter 6. This analysis, detailed below, provides expressions directly relevant to the cases of oscillators constructed using Gm-C and LC based on-chip resonators.

Phase Noise in Gm-C and LC Oscillators

Consider the dynamic range of a Gm-C, second-order resonator derived in Chapter 6 and repeated in Equation (10.2) below for convenience:

$$DR \equiv \frac{V_{max}^2}{V_{noise}^2} = \frac{\eta P_{DC}}{4\pi kTBFBQ^2} \tag{10.2}$$

This resonator will become an oscillator when Q is raised to the point where $V_{noise} = V_{max}$, or equivalently, when $DR = 1$. Substituting this value for DR and the expression for Q in terms of center frequency and bandwidth into (10.2), the 3 dB bandwidth of the oscillator's noise spectrum can be found from:

$$B_{Gm-C} = \frac{4\pi kTFf_o^2}{\eta P_{DC}} \tag{10.3}$$

The denominator ηP_{DC} in this expression is simply the oscillator signal power P_{osc} within the resonator core:

$$\eta P_{DC} \equiv P_{osc} = v_{max} i_{max} \tag{10.4}$$

so that (10.3) may be rewritten in the form:

$$B_{Gm-C} = \frac{4\pi kTFf_o^2}{P_{osc}} \tag{10.5}$$

Evaluation of (10.5) for low power, high frequency operation (e.g. $P_{osc} = 100\mu$W, $f_o = 100$ MHz), gives a bandwidth $B_{Gm-C} = 5$ Hz. While this result gives some indication of the oscillator's purity, one is generally more interested in finding an expression similar to that of (10.1) from which the noise density as a function of frequency offset can be evaluated. To derive such a result, note that the oscillator power can be written in terms of the noise density N_o at the center frequency ($\Delta f = 0$) as:

$$P_{osc} \equiv N_o B_N = N_o \frac{\pi}{2} B \tag{10.6}$$

where B_N is the resonator's noise bandwidth. At frequencies outside the 3 dB bandwidth B, the noise is shaped by the second-order resonator's response characteristic to give:

$$N_{o_{Gm-C}}(\Delta f) = N_o \left(\frac{B/2}{\Delta f} \right)^2 \tag{10.7}$$

Thus, combining (10.5) - (10.7), the noise density at any frequency outside the oscillator's bandwidth may be written as:

$$N_{o_{Gm-C}}(\Delta f) = 2kTF \left(\frac{f_o}{\Delta f} \right)^2 \tag{10.8}$$

or, dividing by the oscillator power to give a normalized expression similar to the form in Equation (10.1):

$$\frac{N_{o_{Gm-C}}(\Delta f)}{P_{osc}} = \frac{2kTF}{P_{osc}} \left(\frac{f_o}{\Delta f} \right)^2 \tag{10.9}$$

The noise in this expression contains half its power in amplitude noise and half its power in phase noise. Hence, an expression for the phase noise alone may be found by dividing (10.9) by 2 to give:

$$\frac{N_{op_{Gm-C}}(\Delta f)}{P_{osc}} = \frac{kTF}{P_{osc}} \left(\frac{f_o}{\Delta f}\right)^2 \tag{10.10}$$

Repeating the above analysis starting with the dynamic range expression for the Q-enhanced LC filter developed in Chapter 6, yields similar results, except for an improvement of Q_o^2:

$$\frac{N_{op_{LC}}(\Delta f)}{P_{osc}} = \frac{1}{Q_o^2} \frac{kT(F+1)}{2P_{osc}} \left(\frac{f_o}{\Delta f}\right)^2 \tag{10.11}$$

Example Phase Noise Calculations

As an example of numerical values, consider the oscillator used in the Q-enhanced filter prototype of Section 9.2. The oscillator power required in Equation (10.11) is that within the resonator core, and can be found for the case of the prototype filter design discussed in Section 9.2 from:

$$P_{osc} = \frac{V_{diff_{RMS}}^2}{R_p} \tag{10.12}$$

where the resistance R_p is known from the design to be approximatly 830 Ω. The voltage $V_{diff_{RMS}}$ however, was not specified in Chapter 9 and must be found from the measured oscillator output power of -32 dBm by solving for the output voltage across the 50 Ω load and dividing by the output buffer gain. At -32 dBm, the voltage across the 50 Ω load is 5.62 mV, and at a bias current of 500 μA, the gain of the output stage (differential to single-ended) is found to be 0.015. Thus, the value of $V_{diff_{RMS}}$ is found to be 375 mV, and from (10.12), the oscillator power is found 170 μW.

The expected phase noise in a 1 Hz bandwidth at a 10 KHz frequency offset can now be found from (10.11) to be 450 fW/Hz (with $F = 2$ and $Q_o = 2.3$), or, dividing by P_{osc}:

$$\frac{N_{op_{LC}}(\Delta f)}{P_{osc}} = 2.7x10^{-9} \equiv -86dBc \tag{10.13}$$

This result compares favorably with the measured value of - 84 dBc reported in Section 9.2. At a frequency offset of 100 KHz, the expected noise level is computed to be -106 dBc, and is within 1 dB of the measured result of -105 dBc.

10.1.2 Phase Noise Effects on Receiver Operation

Oscillator phase noise results in two main degradations in radio receiver designs:

- Phase (or frequency) deviations are added to the received signal, degrading the demodulator output signal-to-noise ratio or bit-error-rate, and
- Phase noise mixed with strong adjacent channel interferers translates noise into the IF passband, limiting the receiver's selectivity and dynamic range.

These effects are illustrated in Figure 10.1 and are discussed quantitatively in the following sections.

Phase/Frequency Deviations Added to Received Signal

As illustrated in Figure 10.1, the noise of the local oscillator is directly impressed onto the received signal as a result of the mixing process. Whether or not this noise is significant depends on the modulation type and bandwidth used in the radio system, and must be determined by comparing the total RMS phase (or frequency) deviations induced, to the phase or frequency deviations expected in the desired signal.

From [147], the RMS *phase* deviation resulting from the LO phase noise can be found from:

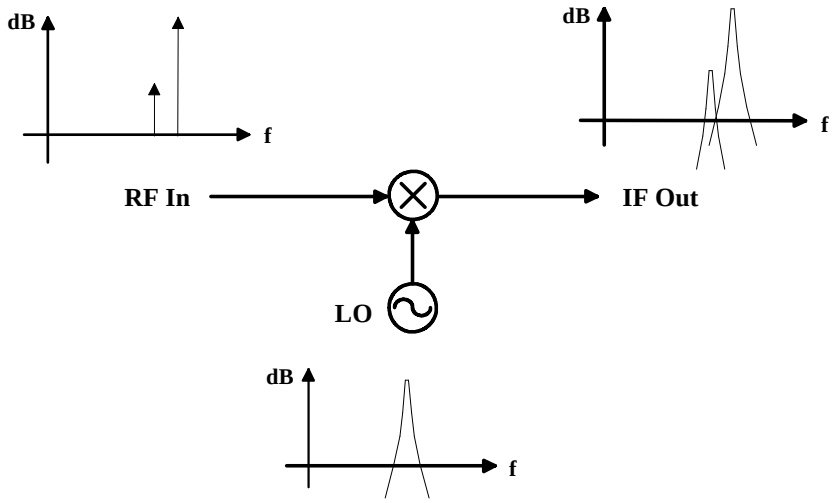

Figure 10.1: Effects of phase noise on received signals.

$$\Delta\Phi_{RMS} = \sqrt{\int_{f_1}^{f_2} \frac{2N_{op}(f)}{P_{osc}} df} \tag{10.14}$$

where f_1 and f_2 define the range of frequencies over which the noise is significant. For example, assuming QPSK modulation and a matched filter in the receiver's IF, f_2 will be approximately $R_s/2$, where R_s is the symbol rate. The remaining frequency f_1 depends on whether coherent or differential demodulation is employed, and on the particular demodulator implementation used (e.g. the carrier recovery loop bandwidth).

Based on (10.10) and (10.11), the phase noise of an oscillator may be written in the form:

$$N_{op}(f) = N_{op}(f_A)\left(\frac{f_A}{f}\right)^2 \tag{10.15}$$

where f_A is an arbitrary reference frequency at which the phase noise is known. Substituting this result into (10.14) and assuming coherent demodulation and a carrier recovery loop with

bandwidth $f_1 = R_s/10$, Equation (10.14) can be solved to give:

$$\Delta\Phi_{RMS} = \sqrt{16\frac{N_{op}(R_s)}{P_{osc}}R_s} \tag{10.16}$$

As an example, a QPSK signal with $R_s = 500$ Ks/s mixed with the oscillator in Section 9.2 where:

$$\frac{N_{op}(500KHz)}{P_{osc}} = 10^{\frac{-105dB}{10}}\left(\frac{100KHz}{500KHz}\right)^2 = 1.27x10^{-12} \tag{10.17}$$

would, according to (10.16) have an RMS phase deviation of 3.2 milli radians added to it by the LO. Since this noise is significantly below the 1.6 radian minimum phase deviation for a QPSK signal, the phase noise of the oscillator is not a significant problem in this example.

In the case of FM or FSK modulated systems, the RMS *frequency* noise in the demodulated output is the parameter of interest. From [147], the frequency noise induced by the LO can be found from:

$$\Delta F_{RMS} = \sqrt{\int_{f_1}^{f_2}\frac{2N_{op}(f)}{P_{osc}}f^2df} \tag{10.18}$$

Solving this expression with (10.15) then gives:

$$\Delta F_{RMS} = \sqrt{2\frac{N_{op}(f_2)}{P_{osc}}f_2^2(f_2 - f_1)} \tag{10.19}$$

and for the case of a FSK system with a 500 Kb/s data rate, $f_2 = 500$ KHz, and $f_1 = 0$ Hz, the oscillator of Section 9.2 would induce a frequency deviation of $\Delta F_{RMS} = 400$ Hz. Again, this is well below the peak modulation of such a system and oscillator phase noise influence on demodulation performance can be ignored.

Phase Noise Limitations on Selectivity and Dynamic Range

The second and most severe effect of LO phase noise on receiver performance is the translation of noise at large frequency offsets into the receiver's passband. This problem occurs when large adjacent channel signals are present as shown in Figure 10.1, and can limit the receiver's selectivity and dynamic range performance.

To find the magnitude of these effects, suppose that the ratio of the interferer signal power I to the desired signal power S in Figure 10.1 is I/S with $I/S \gg 1$. Let the interferer be displaced from the desired signal by a distance Δf, and let the receiver's IF bandwidth be B_{IF}. Then, if we assume for simplicity that the LO phase noise in a range $B_{IF}/2$ either side of the frequency offset Δf is approximately constant and the mixer's gain is 1.0, the noise power N_{out} translated into the IF passband by the mixing process will be:

$$N_{out} = I \frac{N_{op}(\Delta f)}{P_{osc}} B_{IF} \tag{10.20}$$

and the ratio of the desired signal power S_{out} to the added noise will be

$$\frac{S_{out}}{N_{out}} = \frac{1}{\frac{I}{S}\frac{N_{op}(\Delta f)}{P_{osc}} B_{IF}} \tag{10.21}$$

For the case of a sufficiently large interferer and a sufficiently noisy LO, this ratio will fall below the minimum carrier-to-noise ratio $(C/N)_{min}$ required at the demodulator input and reception will be lost. Solving (10.21) for the required phase noise performance to keep $S_{out}/N_{out} \geq (C/N)_{min}$, gives:

$$\frac{N_{op}(\Delta f)}{P_{osc}} \leq \frac{1}{\frac{I}{S}(C/N)_{min} B_{IF}} \tag{10.22}$$

Suppose, for example that I/S represents a desired adjacent or alternate channel selectivity performance level of 50 dB, and that the receiver's IF bandwidth is 1 MHz. Then, for a demodulator with $(C/N)_{min} = 15$ dB, the required phase noise is found from (10.22) to be -125 dBc, which is comparable to the noise of the oscillator in Section 9.2 evaluated at a 1 MHz offset. Note that in this case, a Gm-C oscillator operating at a comparable power level would not provide suitable performance since its phase noise is higher by a factor of Q_o^2. Moreover, neither oscillator would meet the 50 dB requirement if it was operating at 2 GHz, since the phase noise at the same offset would be a factor of $(\frac{2000}{200})^2$ higher at this frequency. For operation at frequencies in the GHz range, the only solutions would be to employ an LC oscillator with a higher inductor Q, to increase the oscillator power, or to relax the performance requirement.[1]

10.2 Receiver Design Example

With the issue of LO purity put to rest, this section turns to the main thrust of this final chapter — a top-level design for a fully integrated receiver. The design considered will be a Digital European Cordless Telephone (DECT) receiver with power consumption and cost targets at or below those of current DECT chip sets discussed in [39] and [28] and overviewed in Chapter 2. The DECT service was selected for this exercise for several reasons, including:

- There is widespread commercial interest in this standard.
- The standard operates in the newly allocated 1800 MHz portion of the radio spectrum and employs wideband modulation typical of many newer digital wireless services.
- DECT employs time-division duplexing (TDD), which is more integration-friendly than frequency-division duplexing system architectures.

[1]The subject of frequency synthesis has not been covered here, but was discussed briefly in Chapter 2. There it was concluded that LOs operating at the RF frequency are needed since multiplication of lower frequency signals to RF by a factor N results in a factor of N^2 increase in phase noise and spurious products.

The final point is particularly important because the use of TDD eliminates the need for antenna duplex filters, which would be required to handle the full transmitted power, and therefore cannot be integrated using active filter techniques.[2]

In the first subsection below, the DECT standard is reviewed, and requirements for DECT receivers are examined. These requirements set the minimum performance that a fully integrated DECT receiver must have to receive type-approval and to compete with existing implementations constructed from commercially available chip sets and off-chip ceramic/SAW filters. In the next subsection, a design for a fully integrated, dual-conversion receiver is proposed and the performance of the filters and local oscillators employed are computed using techniques developed in the preceding section and in earlier chapters. Finally, the last two sections examine possible approachs to improve the receiver's performance and reduce the power consumption by employing direct-conversion techniques and a simplified single-conversion architecture.

10.2.1 DECT System Requirements

The DECT standard defines a wireless architecture for implementing next-generation cordless phones, as well as a variety of digital personal communications services. As shown in Table 10.1, DECT products operate at approximately 1.9 GHz and employ frequency division multiple access (FDMA) and time division multiple access (TDMA) techniques to allow high capacity cellular-like systems to be built. Time division duplexing (TDD) is used to simulate simultaneous transmission and reception of data, allowing bulky and expensive duplex filters to be replaced with smaller and more integration-friendly RF switches.

DECT specifies the use of Gaussian frequency-shift keying (GFSK) modulation with a bit

[2]Some form of "roofing" filter may still be needed at the antenna in TDD systems for the transmitter side of the product. However, such a filter would be required only to attenuate harmonics and therefore may be constructed with on-chip LC *lowpass* filter designs such as those described in [131]

Table 10.1: DECT System Requirements.

Parameter	Requirement
RF Frequency	1881 - 1898 MHz
Modulation	GFSK (BT = 0.5)
Data Rate	1.152 Mb/s
Access/Duplex Method	FDMA/TDMA/TDD
Number of RF Channels	10
Channel Spacing	1.728 MHz
Peak Deviation	288 KHz
Timeslots	12 / frame
Frame Length	5 ms TX, 5 ms RX
Frequency Accuracy	50 KHz (26 ppm)
Sensitivity (BER = 10^{-3})	≤ -83 dBm
Noise Figure (Eb/No = 14 dB)	≤ 16 dB
Noise Floor	≤ -97 dBm
Input Compression	≥ -36 dBm
Dynamic Range	≥ 61 dB
Input Intercept	≥ -27 dBm
Spurious Free Dynamic Range	≥ 47 dB
Selectivity (IF filter attenuation)	
Adjacent Channel	≥ 30 dB
Alternate Channel	≥ 45 dB
Current Consumption	≤ 50 mA
Die Size	≤ 10 mm^2

rate of 1.152 Mb/s and a bandwidth-time product of 0.5. Thus, most designs will employ channel select filters with a bandwidth in the neighborhood of 1.1 MHz. The defined channel spacing of 1.728 MHz then provides the equivalent of guard bands, permitting use of adjacent as well as alternate channels in many applications.

Unlike many older wireless systems, requirements for DECT receivers are specified in the DECT standard and type-approval documents. A recent article by Madsen and Fague [13] provides an excellent summary of these requirements and was used as the basis for many of the performance parameters listed in Table 10.1, including sensitivity, noise figure, and dynamic range. Although no data was provided in the article directly for channel selectivity, a Murata SAFC110.6MA50T SAW filter was suggested, and reference to this and other similar filters' data sheets provided the adjacent and alternate channel performance specifications shown. Finally, the current consumption and die size values shown, although not strictly DECT requirements, are important factors in the design of commercial products and play a critical role in assessing receiver integration technology. The values listed for these parameters were estimated from the DECT chipset described in [39].[3]

10.2.2 Dual Conversion Superheterodyne Receiver Design

A block diagram for a future, fully integrated DECT receiver based on the techniques developed in this dissertation is proposed in Figure 10.2. This design adopts a conservative dual conversion superheterodyne architecture to provide the required channel selectivity of 1.1 MHz while limiting the Q of all filters to a maximum of 200. Both the preselect and first IF filters are Q-enhanced designs which could be implemented using the techniques discussed in Chapters 8 and 9, while the lower-Q second IF filter employs traditional Gm-C filter techniques. The Q-enhanced designs have companion oscillators used for master-slave

[3] Although the 50 mA current consumption shown may appear high, these receivers implement power-down modes to allow the average consumption to be reduced.

tuning of filter Q as demonstrated in Section 9.2, and which double as local oscillators for down conversion to the next IF. In both cases, oscillator and filter frequency tuning is performed through the simplified approach discussed in Chapter 7 wherein a frequency prescaler is provided on-chip and used in conjunction with the host receiver's microprocessor to form a frequency locked loop. Finally, note that no amplifier circuits are employed. In this design, the Q-enhanced filters provide all the front-end gain needed to achieve the required noise figure performance. Hence, the power normally consumed by amplifiers in discrete filter based receivers can be used within the integrated filters to achieve a comparable total receiver power consumption.

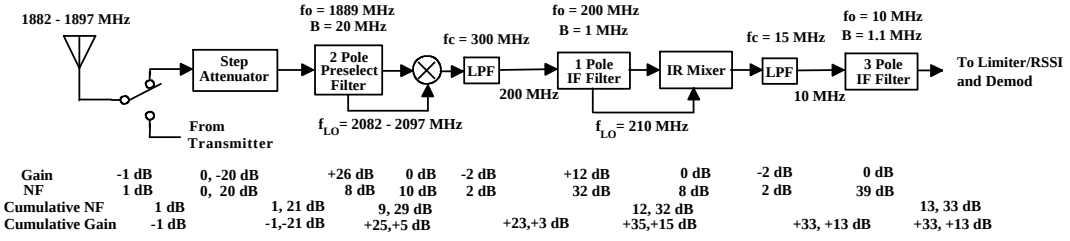

Figure 10.2: Dual conversion integrated receiver design.

As shown below, the weakest link in this design is the first IF filter which operates at the maximum selectivity Q of 200, and therefore has the lowest dynamic range. This filter employs a design similar to that of the prototype IF filter of Section 9.2. Since the inductor Q is relatively low for Q-enhanced LC filters operating at these frequecies, the *in-band* dynamic range possible in this design with reasonable chip areas and power consumptions is less than that required in the overall receiver. This difficulty is handled by adding a 20 dB step attenuator immediately in front of the receiver's preselect filter. The attenuator could be implemented with simple MOSFET switches and would be controlled by the host receiver's microprocessor in response to the received signal strength indicator (RSSI) level measured in the IF limiter/amplifier chain (not shown). This design allows the

receiver to handle the required variations in the level of the desired signal due to changes in distance from receiver to transmitter. Dynamic range improvements with frequency offset described in Chapter 6 then provide the necessary blocking and spurious-free dynamic range performance relative to adjacent and alternate channel signals.

The image rejection performance of the first IF filter is improved by using an image rejection (IF) mixer in the down conversion to the second IF. Without this mixer, substantial additional chip area and power consumption would be required to implement a multiple-pole filter design, and potential problems of providing tight control over the filter passband centering and shape would have to be addressed. However, with a simple, untrimmed image reject mixer, the number of filter poles can be reduced to one while maintaining good image (spurious) response performance as discussed in Chapter 4. Even if the mixer image rejection is limited to only 20 dB, the additional 32 dB provided by the filter brings the total spurious response attenuation to over 50 dB. Trying to achieve a full 50 dB with *only* an image reject mixer is generally impractical, even if trimming is permitted, due to requirements to set and hold amplitude and phase balances of better than 1 % and 1^o respectively. Thus, the second IF filter is required in this design, despite its limitations.

Finally, a 3-pole filter in the second IF supplies the majority of channel selectivity. Since this filter operates at a relatively low frequency of 10 MHz, and a low selectivity Q of 9.1, established Gm-C techniques can be applied to achieve accurate response and good dynamic range while keeping power consumption to manageable levels.

Detailed Peformance Estimates

A complete circuit-level design for the proposed receiver is a significant engineering effort and is therefore outside the scope of this dissertation. However, the performance of the receiver can be predicted using the equations developed in previous chapters and by extrapolating from the prototype performance of Section 9.2. These techniques have been used to

generate the performance estimates shown in Tables 10.2 - 10.4 and to arrive at the overall gain and noise figure allocations shown previously in the receiver block diagram of Figure 10.2. The resulting data was then combined to determine the overall receiver performance estimates shown in Table 10.5 where the design is compared with the requirements of Table 10.1 and with the performance of the DECT receivers reported in [39] and [28].

Table 10.2 summarizes the performance of the RF preselect filter and local oscillator. The preselect filter assumed is a 2-pole coupled resonator design similar to that of the prototype filter of Section 9.2, but scaled in frequency to 1900 MHz. Thus, this filter assumes the use of an advanced, fine-geometry IC process with gate lengths in the neighborhood of 0.5 μm. Apart from this potentially aggressive scaling of operating frequency, the design is otherwise easier to implement than that of the prototype filter due to the smaller inductors and higher Q_o values possible at higher frequencies. Based on inductor Q simulations discussed in Chapter 8, a Q_o value of 8 is assumed for an inductor outer dimension of 500 μm. The required Q enhancement is therefore substantially less than that in the prototype filter design, leading to better dynamic range and lower temperature drifts. With smaller inductors, the coupling can be set in this filter with inductor spacing alone, and lower oscillator feedthrough can be achieved in acceptable chip areas. In addition, the higher base Q minimizes the passband asymetry problems experienced in the prototype design, so that all coupling neutralization circuitry can be eliminated.

The LO associated with this filter is designed to operate at 2082 to 2097 MHz, resulting in a 200 MHz first IF. Frequency tuning is provided as in the prototype design with switched tuning capacitors, but with 5 to 6 bits of control to allow a resolution down to approximately 2 MHz, while still maintaining the necessary range to tune out manufacturing tolerances and temperature related drift. Although this resolution is not fine enough to address the 50 KHz tuning increment required for accurate demodulation, the operating frequency of the LO can be measured to within 25 KHz by the host microprocessor with an N = 128 prescaler ratio and a 5 ms counter gate time. The IF frequency is then known to this level

of accuracy and the ± 1 MHz error can be corrected by suitable control of the first IF filter's center frequency and LO.

The design and performance of the first IF filter and LO is summarized in Table 10.3. Except for minor modifications and additions, this design is essentially equivalent to the prototype filter configured to provide master-slave tuning of filter Q. To allow operation at a higher Q (Q = 200 versus Q = 100), the power consumption of the filter has been increased by a factor of 2, and to provide finer frequency control, a digital-to-analog converter controlled, simulated inductance is assumed to be used in both the filter and oscillator. Finally, the coupling neutralization circuits provided in the prototype implementation are eliminated since only a 1-pole filter is used.

An interesting feature of the first IF filter is the relatively high noise figure used. A noise figure of 32 dB is specified for the reasons described in Chapter 3. This value is equal to the (decibel) sum of the gain and noise figure of upstream circuits, guaranteeing that the noise floor produced by these circuits will be equal in magnitude to the noise floor within the filter. Although this choice increases the effective noise figure of the overall receiver by 3 dB, it guarantees minimal degradation of the first IF filter's already limited dynamic range.

The final filter used is described in Table 10.4. As previously mentioned, this filter can be implemented using Gm-C techniques due to the low selectivity Q of 9.1 that results from the 1.1 MHz bandwidth operating at a second IF frequency of 10.0 MHz. The low Q value allows a higher dynamic range than that of the first IF filter, despite the Gm-C technique's inherent limitations. In turn, a noise figure of 39 dB, 6 dB less than the sum of the upstream circuits's gain and noise figures is specified. While this noise figure means that the incoming noise will be 6 dB higher than the noise generated within the filter and that the filter's effective dynamic range will therefore be cut by 6 dB, it reduces the impact of the filter on the overall receiver noise figure to only 1 dB.

Table 10.2: RF Preselect Filter and LO Performance.

Parameter	**Value**
Preselect Filter	
Type	Q-Enhanced LC
Tuning Q Frequency	 Master-Slave μP Assisted FLL
Center Frequency	1890 MHz
Bandwidth	20 MHz
Selectivity Q	95
Number of Poles	2
Image Rejection	64 dB
Inductor Size	500 μm
Resonator Base Q	8
Q Enhancement	11.9
Supply Voltage	3 - 5 V
DC Current Consumption Resonator core Total	 2 mA $\leq$ 10 mA
Resonator 1 dB Compression	200 μW (-7 dBm)
Dynamic Range (B_{IF} = 1.1 MHz)	73 dB
Spurious Free Dynamic Range	54 dB
Gain	26 dB
Noise Figure	8 dB
Local Oscillator	
Frequency	2082 - 2097 MHz
Resolution	2 MHz
Accuracy (N=128 prescaler, 5 ms count)	25 KHz
DC Current	5 mA
Oscillator Power	350 μW
Inductor Size	500 μm
Resonator Base Q	8
Phase Noise (Δf = 1.728 MHz)	-124 dBc
FM Noise ($\Delta f = 0 - 550$ KHz)	1.1 KHz
Noise Limited Adjacent Channel Selectivity (at 15 dB C/N)	 48 dB

Table 10.3: First IF Filter and LO Performance.

Parameter	**Value**
Preselect Filter	
Type	Q-Enhanced LC
Tuning	
Q	Master-Slave
Frequency	μP Assisted FLL
Center Frequency	199 - 201 MHz
Bandwidth	1 MHz
Selectivity Q	200
Number of Poles	1
Image (Spurious) Rejection	
Filter	32 dB
Filter + IR Mixer	$\geq$ 52 dB
Inductor Size	850 μm
Resonator Base Q	2.5
Q Enhancement	80
Supply Voltage	3 - 5 V
DC Current Consumption	
Resonator core	2 mA
Total	$\leq$ 6 mA
Resonator 1 dB Compression	60 μW (-12 dBm)
Dynamic Range	
In-Band	52 dB
Adjacent Channel	63 dB
Spurious Free Dynamic Range	
In-Band	41 dB
Adjacent Channel	54 dB
Gain	12 dB
Noise Figure	32 dB
Local Oscillator	
Frequency	209 - 211 MHz
Resolution	
Switched Capacitors	1 MHz
Gyrator Simulated Inductor	25 KHz
Accuracy (N=16 prescaler, 5 ms count)	3.2 KHz
DC Current	6 mA
Oscillator Power	350 μW
Inductor Size	850 μm
Resonator Base Q	2.5
Phase Noise ($\Delta f = 1.728$ MHz)	-133 dBc
FM Noise ($\Delta f = 0 - 550$ KHz)	144 Hz
Noise Limited Adjacent Channel	
Selectivity (at 15 dB C/N)	57 dB

Table 10.4: Second IF Filter Peformance.

Parameter	**Value**
Type	Gm-C
Tuning	
Q	Master-Slave
Frequency	Master-Slave
Center Frequency	10.00 MHz
Bandwidth	1.1 MHz
Selectivity Q	9.1
Number of Poles	3
Supply Voltage	3 - 5 V
DC Current Consumption	
Resonator core	1 mA
Total	$\leq$ 8 mA
Resonator 1 dB Compression	100 μW (-10 dBm)
Dynamic Range	
In-Band	72 dB
Adjacent Channel	78 dB
Spurious Free Dynamic Range	
In-Band	54 dB
Adjacent Channel	62 dB
Gain	0 dB
Noise Figure	39 dB

Table 10.5: Overall Receiver Performance.

Parameter	Requirement	Proposed Design	Design in [13]	Design in [39]
Noise Figure	≤ 16 dB	13 dB	12.6 dB	8 dB
Sensitivity	≤ -83 dBm	-86 dBm	-87 dBm	-91 dBm
Input Noise Floor	≤ -97 dBm	-100 dBm	-101 dBm	-105 dBm
Dynamic Range (In-Band)	≥ 61 dB	68 dB	67 dB	75 dB
Spurious Free Dynamic Range (Adj Ch)	≥ 46 dB	50 dB	52 dB	55 dB
Selectivity (IF Filter Attn.)				
Adjacent Channel	30 dB	40 dB	-	-
Alternate Channel	45 dB	64 dB	-	-
Current Consumption	≤ 50 mA	35 mA + mixer/demod	-	50 mA
Die Size	≤ 10 mm^2	2.2 mm^2 + active circuits	-	< 8.5 mm^2

Based on the performance of these individual components, and the gain and noise distributions shown in Figure 10.2, the overall performance of the proposed receiver is summarized in Table 10.5. As indicated by comparison with the required performance and the performance of the receivers described in the references,[4] the proposed integrated receiver design is competitive in all areas. The integrated receiver meets or exceeds performance requirements and compares favorably with designs based on commercial chip sets and ceramic/SAW off-chip filters. Thus, with a suitable engineering effort, full integration of DECT receivers is indeed feasible. Moreover, the relatively small chip area consumed by the required inductors indicates that the cost of production can be kept low, and by eliminating external filters, overall system cost can be reduced at the same time product size is decreased.

10.2.3 Direct Conversion Receiver Design

The design of the previous section can be improved (in theory) if the dynamic range bottleneck at the first IF filter is eliminated by the use of a direct conversion architecture such as shown in Figure 10.3. In this implementation, the preselect filter is retained to

[4]Values for the design described in [39] are computed based on stated performance of the chip set combined with a 12 dB gain, 4 dB noise figure GaAs preamp.

provide good out-of-band rejection while achieving a front-end gain in the neighborhood of 30 dB. However, all channel selectivity is now provided by integration-friendly lowpass filter designs, and the power consumption of the first IF filter and LO, and of the second IF filter are eliminated. In addition, since the preselect filter performance shown previously in Table 10.2 meets the dynamic range requirements of the DECT specification, it may also be possible to eliminate the step atteunator from the design.

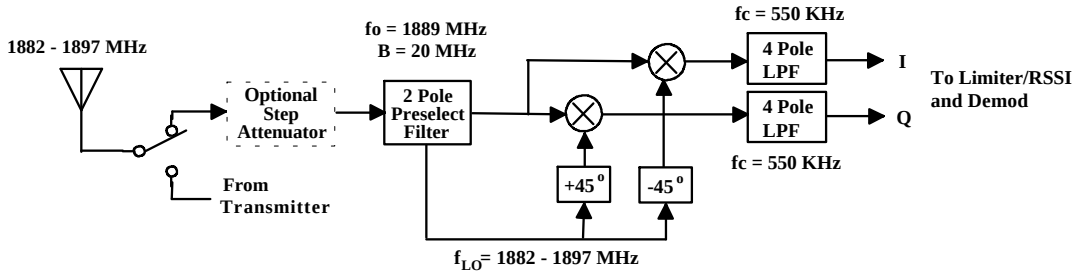

Figure 10.3: Direct conversion integrated receiver design.

Unfortunately, closer consideration indicates that this design is probably not feasible. The most severe problem is coupling of the LO oscillator to the filter circuits. Even if the on-chip coils can be spaced by several inductor diameters to lower the coupling coefficient to 0.001, the 350 μW oscillator signal will induce a signal in the filter on the order of 30 μW, or -15 dBm. This signal will create DC offsets in the mixer outputs several orders of magnitude higher than the desired signal level. Moreover, the reverse isolation of the input transconductor used in the filter design may not be sufficient to limit radiation of the LO signal to acceptable limits. Additional problems with this design include the LO tuning resolution needed to achieve accuracies on the order of 50 KHz or less, and the the need to maintain accurate mixer phase shifts and amplitude balance over the full RF tuning range.

10.2.4 Single Conversion Receiver Design

All of the problems of the direct conversion design listed above can be reduced if the receiver architecture is modified as shown in Figure 10.4. Strictly speaking, this design is a single-conversion receiver architecture with a non-coherent quadrature demodulator. However, it can also be viewed as a fixed-tuned direct conversion receiver operating at 200 MHz preceeded by a block down converter. This latter interpretation allows the design to be contrasted with the direct conversion design to see how the problems of the previous receiver are addressed.

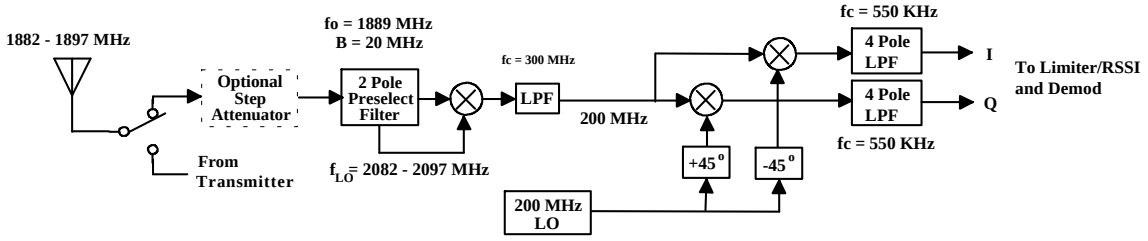

Figure 10.4: Single conversion integrated receiver.

In the new design, the LO operates at a frequency offset from the frequency to which the filter is tuned, reducing oscillator feedthrough by 25 to 30 dB (depending on filter bandwidth). Hence, the oscillator signal coupled into the filter circuits will now be at a level on the order of -40 dBm or less. Since two LOs are used, one at the RF and one in the 200 MHz IF, the techniques used in the dual conversion architecture can be applied to solve the tuning resolution problem. Coarse steps in the range of 2 MHz can be used in the preselect filter, while fine tuning to within 50 KHz can be achieved using the 200 MHz LO. Unlike the earlier dual conversion design however, the new architecture does not employ IF filtering, so there is no inductor coupling problem within the 200 MHz direct conversion receiver block. Moreover, the power consumption is reduced over the dual conversion design

by approximately 16 mA through the elimination of the first and second IF filters. While the lowpass filters now used to provide channel selection will consume power, their pole Q values will be low ($Q < 5$), so that they can provide good dynamic range at very low currents.

Finally, we note that the quadrature mixing should be simplified over that of the previous direct conversion design by operation at a low and relatively fixed 200 MHz IF. While the addition of the 200 MHz LO will consume power not used in the direct conversion design, the total power of the single conversion receiver may actually be lower since only a single 2 GHz mixer is now required.

Chapter 11

Conclusions and Future Directions

Worldwide allocations of radio frequency spectrum for cellular and PCS services in recent years have placed new emphasis on the development of small, low cost wireless products. As shown in Chapter 2, RF device manufacturers have responded by introducing chip sets with increasing levels of integration. However, to date, virtually all high performance wireless products continue to rely on discrete LC, crystal, ceramic, or SAW devices for the realization of RF preselection filters, IF channel selection filters, and local oscillator tuned circuits.

During the past decade, considerable research has been directed at developing suitable switched-capacitor and Gm-C based on-chip replacements for discrete filters now in use. Although this work has produced several potentially viable designs at IF frequencies from 455 KHz to 10.7 MHz, these designs have yet to see substantial commercial application. A critical problem faced by switched-capacitor and Gm-C filters was found to be the power consumption required to simultaneously achieve narrow fractional bandwidths and acceptable dynamic range. This power consumption, which can reach several hundred milliwatts, is incompatible with portable wireless product design.

These problems have caused some researchers to look for alternatives to the classic superheterodyne architecure as a means to integrate receiver hardware. Thus, the issues of receiver system requirements and alternative receiver designs were investigated in Chapters 3 and 4 respectively. In the superheterodyne architecture on which virtually all present-day receiver designs are based, RF and IF bandpass filters with small fractional bandwidths

(e.g ≤ 2 %) are needed to suppress image responses, to provide required channel selectivity, and to achieve good dynamic range in the presence of large amplitude inteferers on nearby frequencies and within other service bands. Alternative receiver designs such as direct conversion (or "zero-IF") architectures have no image frequency and can theoretically provide all channel selectivity using integration-friendly *lowpass* filters. Unfortunately, direct conversion receivers with performance matching that of present-day superheterodynes are difficult to implement in practice. Problems include LO to RF coupling, resulting DC offsets and receiver radiation, and the need for precision quadrature mixers operating directly at RF. Moreover, as shown in Chapters 3 and 4, direct conversion designs possess the same fundamental design tradeoffs faced by superheterodyne receivers in the critical areas of dynamic range, gain, and noise figure. Thus, even if the practical problems of implementing the direct conversion architecture can be overcome, narrowband preselect filters will still be required, and good dynamic range must still be maintained in all circuits preceeding the final channel-select filters.

Potential technologies for implementing on-chip bandpass filters at both RF and IF frequencies were reviewed in Chapter 5, and energy storage in resonant circuits was identified as a critical factor for achieving good dynamic range at low power. On-chip electro-acoustic filters possess this property and offer the potential of purely passive filtering, but require IC fabrication process modifications, and have not yet reached a suitable level of maturity. On-chip LC filters also possess this property and are fully compatibility with current IC processing techniques. Thus, filter design using integrated inductors was chosen as a potentially viable solution to the on-chip bandpass filtering problem and studied in depth in later chapters.

A study of the literature on integrated inductors in silicon processes showed that a few passive on-chip filters had been reported, but that no high-Q bandpass designs existed. A principle problem was found to be the low Q values of spiral inductor designs. With Q values of less than 10 at frequencies of 1 GHz and below, purely passive high-Q bandpass

filters cannot be realized. However, a few researchers have noted that by adding active circuits, inductor losses can be compensated for, and arbitrarily high Q values can be achieved. Proposals for constructing such Q-enhanced LC filters had appeared in circuits and systems conferences, but no fully integrated realizations had been reported.

In Chapters 5 and 6, the dynamic range performance of Q-enhanced LC filter designs was investigated and found to be limited by the active circuits used. However, a detailed study of this problem revealed that even a small inductor Q results in significant dynamic range and power consumption advantages over Gm-C and other fully active designs. For example, an inductor with $Q_o = 5$ results in a dynamic range advantage of $Q_o^2 = 25$ or 14 dB. Alternatively, for a given dynamic range requirement and receiver bandwidth, the Q-enhanced filter design consumes over an order of magnitude less power.

The issue of how much dynamic range is *required* was then considered to determine if these advantages are sufficient to allow integrated, low-power receivers to be built. Specification of dynamic range in receivers involves at least three separate definitions of performance. In Chapter 3, blocking and spurious-free dynamic range were identified as the most important characteristics since the *total* dynamic range needed to compensate for varying distances between transmitter and receiver can be increased through the addition of attenuator and AGC circuits. However, the dynamic range of filters is nearly always quoted for in-band signals only, using the filter's noise bandwidth to define the total integrated noise power. Thus, to allow comparisons with receiver performance to be made, the relationship of this measure of performance to blocking and spurious-free dynamic range was investigated in considerable depth.

Blocking and spurious-free dynamic range were shown in Chapter 6 to depend on the receiver's IF bandwidth, rather than on the bandwidth of the filter itself. For IF filters, these bandwidths are approximately equal, but for RF preselect filter designs, the preselect bandwidth is many times that of the signal and the dynamic range when used within a receiver

is higher than that of the filter alone. Moreover, blocking and spurious-free dynamic range are fundamentally defined relative to signals which fall *outside* the filter passband, and for a properly designed active filter, this fact was shown to result in dynamic range values significantly above that of the filter's in-band performance. With these factors in hand, the dynamic range of Gm-C and Q-enhanced LC filters was then compared with the dynamic range of traditionally designed receiver circuits and expressions were developed to determine fundamental limits on the Q values allowed within receivers having restricted power consumption budgets. This study revealed that the Q of Gm-C filters must be limited to less than 30, while the Q of LC based designs can be as high as 100 or more depending on the base inductor Q that can be achieved.

An additional consideration in on-chip filter design is the accuracy and temperature stability of the transfer functions that can be realized. Thus, Chapter 7 considered the need for tuning in integrated filters, and surveyed the design of control systems which can be used to achieve a desired level of tuning precision. In Q-enhanced filters, as in more traditional Gm-C filter designs, both frequency and Q tuning were found to be needed during use and the basic problem of controlling the filter transfer function was shown to be the same in both cases. Thus, control systems developed for Gm-C filters can be adapted to the tuning of Q-enhanced filters as well. A review of these control system designs showed that the common master/slave technique offers a simple and robust solution for filters with Q values up to about 50, but that other techniques may provide better performance in particular situations. A new orthogonal-reference-tuning (ORT) technique was proposed and examined in detail as a method to tune high-Q designs to very high levels of precision. The concept of keep-it-simple (KIS) was then investigated and several simplifications of existing techniques were proposed.

Having established bounds on filter performance and the theoretical viability of the Q-enhanced filter approach, detailed design considerations for implementing these filters were investigated in Chapter 8. On-chip inductor Q was found to be primarily dependent on

frequency of operation and on inductor size, and relatively independent of the actual inductance value. Significant additional losses however, can occur due to the underlying substrate, making detailed modeling of inductors critical to the successful design of high Q filters. A lumped circuit simulation model was used to determine representative performance achievable in standard CMOS processes with inductor outer dimensions ranging from 330 μm to 1000 μm. Q values from 2 to 8 were found depending on frequency of operation, inductor size, and other properties of the fabrication process.

Techniques for Q enhancement were then investigated and criteria for selecting values of essential components were shown to depend on the terminating impedances, filter gain, and noise figure desired. A study of balanced filter design led to the developement of a novel center-tapped sprial inductor geometry which allows higher self-resonant frequencies and Q values to be achieved. In turn, this development allows better dynamic range and lower power operation to be realized, and allows the usable frequency range of operation of Q-enhanced filters to be extended down to about 200 MHz — far lower than the 1 GHz suggested in the literature.

The full viability of Q-enhanced filtering was then demonstrated in Chapter 9 through the design, fabrication, and testing of two prototype ICs. In addition to serving as a vehicle to work out device-level implementation issues for these filters, these prototypes were constructed to validate dynamic range performance predictions and to assess the viability of various tuning options considered in previous chapters.

The first IC, which operated at a nominal frequency of 100 MHz, employed off-chip inductors and tuning capacitors and served primarily as an early prototype of the proposed technique. Starting from an LC tank circuit Q of 70, the filter exhibited excellent short-term tuning stability and good dynamic range when operating at Q values up to 10,000. A gain of 31 dB and an in-band dynamic range of 56 dB were achieved at a current consumption of less than 2 mA (excluding the on-chip mixer). Dynamic range increases with frequency offset were

found to be in excellent agreement with predictions in previous chapters, with blocking and spurious-free dynamic range performance reaching 100 and 85 dB respectively at 1 MHz offset from the filter center.

The second IC was a fourth-order, fully integrated design, with two on-chip center-tapped spiral inductors, each with an outer dimension of 850 μm. This IC, which consumed approximately 3.3 mm^2 of chip area, operated at a nominal frequency of 200 MHz with a selectivity Q of 100, and consumed less than 6 mA from a 3 V supply, making it potentially suitable for use as a first IF filter in modern wideband cellular and PCS products. Base Q of the resonant circuit at 200 MHz was measured at 2.3, and when enhanced to the nominal Q of 100, provided respectable in-band dynamic range, and good dynamic range at frequency offsets. Experiments with filter tuning showed excellent agreement with theory and demonstrated the viability of using the master/slave technique to control filter Q. Short-term, open-loop stability of both frequency and Q were also excellent (frequency drift of less than 50 KHz in 5 minutes, and negligable Q drift at Q values up to 200) indicating that the simplified tuning techniques proposed in Chapter 7 can be applied in the design of these filters. Although the prototype IC was constructed for use at 200 MHz, this choice was primarily dictated by the available 2 μm IC process and by the low frequency, 40 pin, DIP packaging used. Thus, scaling of the demonstrated design techniques to finer-line fabrication processes and the use of RF compatible packaging is expected to allow extension to RF preselect applications as well.

Finally, Chapter 10 investigated performance requirements and performance bounds for on-chip local oscillators — the remaining obstacle to full receiver integration. This problem was found to be related to, but less severe than that of filter dynamic range, at least for newer wideband wireless system designs. A top-level design for a hypothetical, fully integrated receiver was then proposed and evaluated to investigate the possibility of constructing a complete "receiver-on-a-chip". This study, combined with results obtained from the filter prototypes confirms the theoretical as well as practical viability of the technology. Using

the theory developed throughout this disseration, a detailed set of performance data for the three filters and two local oscillators used in the design was generated. The performance of these components was then used to determine overall receiver performance, which was shown to not only meet the required specifications, but to compete well with two different designs based on current technology chipsets employing off-chip ceramic and SAW filters.

Nevertheless, several practical issues remain to be addressed before this new technology can be used to its full potential and adopted for routine commercial receiver designs. First, the design and characterization of spiral inductors should be examined in more depth. On-chip inductor Q is critical to the optimization of dynamic range and minimization of power consumption, and to the simplification of filter tuning. Techniques should therefore be investigated for realizing higher Q inductors in newer, multi-layer metal processes. Higher inductance values, and hence, higher quality factors may also be achievable if thin-film ferrites can be incorporated into the fabrication process. In addition, design tools should be developed to accurately predict the inductance values, self-resonant frequencies, and quality factors that result, so that filter designs can be created with minimal iteration.

Second, the design of improved linearity transconductors should be investigated. A simple, long-tailed differential pair was used in the prototype designs to assure working devices, at the expense of limited voltage swings at large Q enhancements. Several linearized transconductors have been proposed in the literature for use in Gm-C filters, and may be adapted to the design of Q-enhanced filters to the extent that they operate at high frequencies. The effects of these techniques on dynamic range, and on filter stability when operating at high Q values however, must be assessed.

Third, additional work is needed to determine the best and least costly tuning techniques, and to refine the design of tuning circuits. In particular, a more detailed design is needed to determine what, if any, practical problems may arise in implementing the simplified tuning techniques proposed in Chapter 7 for use in TDMA/TDD wireless systems. In addition,

techniques for implementing coupling neutralization should be studied in more detail.

Finally, the practical tradeoffs discussed in Chapters 4 and 10 with respect to superheterodyne and direct conversion receiver architectures should be assessed. These tradeoffs are perhaps best studied through a full circuit-level design effort with subsequent fabrication and testing. Such a detailed engineering effort is needed to determine which receiver architecture will ultimately win approval in the design of completely integrated, low power, radio receivers, and to prepare the technology for transfer from the laboratory to commercial product development.

REFERENCES

Receiver Architectures and System Requirements

[1] K. Anvari, M. Kaube, and B. Hriskevich, "Performance of a Direct Conversion Receiver with pi/4-DQPSK Modulated Signal," 41st IEEE Veh. Tech. Conf., pp. 822-827, 1991.

[2] *The Radio Amateur's Handbook*, West Hartford, Connecticut: American Radio Relay League, pp. 139, 1939.

[3] M. Buehrer, F. Cheng, R. Dhawan, F. Dominique, A. Doradla, O. Hazim, R. He., and M. Iatrou, *Wireless Standards of the United States,* MPRG Technical Report, Virginia Tech, Blacksburg, VA, 1994.

[4] R. T. Buesing, "Modulation Methods and Channel Separation in the Land Mobile Service," IEEE Trans. Veh. Tech., vol. VT-19, pp. 187-206, May 1970.

[5] N. J. Colmenares, "The FCC on Personal Wireless," IEEE Spectrum, pp. 39-46, May 1994.

[6] M. J. Darcy, "Digital Down-Conversion," GEC Journal of Research, vol. 10, no. 1, pp. 29-35, 1992.

[7] R. Edwards, J. Durkin, and D. H. Green, "Selection of intermodulation-free frequencies for multiple-channel mobile radio systems," Proc. IEE, vol. 116, no. 8, pp. 1311-1318, Aug. 1969.

[8] C. G. Eilers, "Stereophonic FM Broadcasting," IEEE Trans. Broadcast and Television, pp. 73-80, July 1961.

[9] G. E. Hardman, "Engineering Orbcomm: A Digital Satellite Communications System Exploiting a Range of Modern Technologies," Third IEE Conf. on Telecomm., pp. 251-256, 1991.

[10] K. Henney, Editor, *Radio Engineering Handbook,* New York: McGraw-Hill, 1959, pp. 3-18.

[11] W. C. Y. Lee, *Mobile Cellular Telecommunications,* New York, McGraw-Hill, 1995.

[12] A. J. Leitich, and D. L. Linder, "Portable Telephones for Cellular Systems," IEEE Veh. Technology Conference. pp. 1-7, 1980.

[13] B. Madsen, and D. E. Fague, "Radios for the Future: Designing for DECT," RF Design, pp. 48-53, April 1993.

[14] J. H. McMahon, "Interference and Propagation Formulas and Tables Used in the Federal Communications Commission Spectrum Management Task Force Land Mobile Frequency Assignment Model," IEEE Trans. Veh. Technol., vol. VT-23, pp. 129-134, Nov. 1974.

[15] N. Parker, and D. W. Ruby, "Some Notes on the Calculation of the S/N Ratio for a FM System Employing a Double Sideband AM Multiplex Signal," IEEE Trans. Broadcast and Television, pp. 42-46. April 1962.

[16] D. C. Schoen, and P. A. Locke, "The ORBCOMM Data Communications System," International Mobile Satellite Conference (IMSC '93), pp. 267-272, 1993.

[17] J. Sevenhans, A. Vanwelsenaers, J. Wenin, and J. Baro, "An integrated Si Bipolar RF Tranceiver for a Zero IF 900 MHz GSM Digital Mobile Radio Frontend of a Hand Portable Phone," IEEE Custom Integrated Circuts Conference, pp. 7.7.1-7.7.4, 1991.

[18] Y. Shemesh, and A. Breitbard, "RF Front End for Portable Satellite Terminal," IEEE MTT-S Digest, pp. 801-804, 1993.

[19] S. Sheng, A. Chandrakasan, and R. W. Brodersen, "A Portable Multimedia Terminal," IEEE Communications Magazine, pp. 64-75, December 1992.

[20] F. E. Terman, *Radio Engineers' Handbook*, New York: McGraw-Hill, pp. 662-664, 1943.

[21] H. Tsurumi, and T. Maeda, "Design Study on a Direct Conversion Receiver Front-End for 280 MHz, 900 MHz, and 2.6 GHz Band Radio Communication Systems," 41st IEEE Veh. Tech. Conf., pp. 457-462, 1991.

[22] A. J. Viterbi, "The Evolution of Digital Wireless Technology from Space Exploration to Personal Communication Services," IEEE Trans. on Vehicular Technology, pp. 638-643, August 1994.

[23] R. E. Ziemer, and R. L. Peterson, *Introduction to Digital Communication,* New York, Macmillan Publishing Company, 1992.

[24] W. M. Dalton *The Story of Radio, Volumes 1-3*, Adam Hilger, London, 1975.

Commercial Products

[25] T. D. Antes, "Chip Set Addresses European Digital Phone Standards," Microwaves & RF, pp. 218-222, December 1994.

[26] M. Burkett, and D. Krudop, "RF ICs Require Only 1 V in Pager Designs," Microwaves & RF, pp. 127-130, October 1994.

[27] W. R. Davis, and J. E. Solomon, "A High-Performance Monolithic IF Amplifier Incorporating Electronic Gain Control," IEEE Journal of Solid-State Circuits, vol. SC-3, no. 4, pp. 408-416, December 1968.

[28] M. Eccles, "Gigahertz Systems on a Chip," Electronics World + Wireless World, pp. 662-663, August 1993.

[29] GEC Plessy Semiconductor, "Global Positioning Core in One IC," Electronics World + Wireless World, pp. 156-157, February 1994.

[30] M. Gill, "Chip Set Combines Small Size with Low Cost and Power," Microwaves & RF, pp. 147-150, December 1994.

[31] J. Neal, "HBT Technology Adds Power to CDMA Chip Set," Microwaves & RF, pp. 205-207, December 1994.

[32] T. Stanley, "The RF Design Revolution 2: integrating the front end," Electronics World + Wireless World, pp. 922-926, November 1992.

[33] T. Stanley, "The RF Design Revolution 3: Devices for Frequency Synthesis," Electronics World + Wireless World, pp. 999-1003, December 1992.

[34] Tandy Corporation, *Service Manual, CT-302 Cellular Handportable Telephone and Accessories*, 1991.

[35] Texas Instruments, "Three-Chip Set Supports Digital Cellular Phones," Microwaves & RF, pp. 227, December 1994.

[36] TriQuint Semiconductor, "Packaged GaAs RF ICs Simplify Wireless Designs," Microwaves & RF, pp. 204, April 1994.

[37] TriQuint Semiconductor, "Chip Set Tunes in to 2.4-GHz WLAN Range," Microwaves & RF, pp. 134-136. October 1994.

[38] M. Williams, F. Bonn, C. Gong, and T. Quach, "GaAs RF ICs Target 2.4-GHz Frequency Band," Microwaves & RF, pp. 111-118, July 1994.

[39] B. Wuppermann, S. Atkinson, B. Fox, B. Jansen, G. Jusuf, "A 2.7 V Two Chip Set Tranceiver for DECT," Fourth International Symposium on Personal, Indoor and Mobile Radio Communications (PIMRC'93), pp. 407-411, 1993.

Integrated Receivers/Tranceivers

[40] A. A. Abidi, "Radio-Frequency Integrated Circuits for Portable Communications," IEEE 1994 Custom Integrated Circuits Conference, pp. 8.1.1-8.1.8, 1994.

[41] T. Apel, E. Creviston, S. Ludvik, L. Quist, and B. Tuch, "A GaAs MMIC Transceiver for 2.45 GHz Wireless Commercial Products," IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium, pp. 15-18, 1994.

[42] J. W. Th. Eikenbroek, *Development of an Integrated AM Shortwave Upconversion Receiver Front-End,* Ph.D. Thesis, Delft University of Technology, The Netherlands, 1989.

[43] W. G. Kasperkovitz, "FM Receivers for Mono and Stereo on a Single Chip," Philips Technical Review, vol. 41, no. 6, pp. 169-182, 1983/84.

[44] V. Nair, R. Vaitkus, D. Scheitlin, J. Kline, and H. Swanson, "Low Current GaAs Integrated Down Converter for Portable Communication Applications," IEEE GaAs IC Symposium, pp. 41-44, 1993.

[45] H. C. Nauta, *Fundamental Aspects and Design of Monolithically Integrated AM Radio Receivers,* Ph.D. Thesis, Delft University of Technology, The Netherlands, 1986.

[46] K. Negus, B. Koupal, J. Wholey, K. Carter, D. Millicker, C. Snapp, and N. Marion, "Highly-Integrated Transmitter RFIC with Monolithic Narrowband Tuning for Digital Cellular Handsets," IEEE Int. Solid-State Cir. Conf., pp. 38-39, 1994.

[47] E. H. Nordholt, H. C. Nauta, and C. A. M. Boon, "A High-Dynamic-Range Front End For an Upconversion Car-Radio Receiver," IEEE JSSC, vol. SC-20, no. 3, pp. 688-696, June 1985.

[48] T. Okanobu, H. Tomiyama, and H. Arimoto, "Advanced Low Voltage Single Chip Radio IC," IEEE Transactions on Consumer Electronics, vol. 38, no. 3, pp. 465-475, August 1992.

[49] J. van der Plas, *Synchronous Detection in Monolithically Integrated AM Upconversion Receivers,* Ph.D. Thesis, Delft University of Technology, The Netherlands, 1990.

[50] B-S. Song, and J. R. Barner, "A CMOS Double-Heterodyne FM Receiver," IEEE Journal of Solid-State Circuits, vol. SC-21, no. 6, pp. 916-923, December 1986.

[51] I. A. W. Vance, "Fully Integrated Radio Paging Receiver," IEEE Proceedings, vol. 129, Pt. F, No. 1, pp. 2-6, February 1982.

[52] J. F. Wilson, R. Youell, T. H. Richards, G. Luff, and R. Pilaski, "A Single-Chip VHF and UHF Receiver for Radio Paging," IEEE J. Solid-State Circuits, vol. SC-26, no. 12, pp. 1944-1950, December 1991.

[53] P. T. M. van Zeijl, *Fundamental Aspects and Design of an FM Upconversion Receiver Front-End with On-Chip SAW Filters,* Ph.D. thesis, Delft University of Technology, The Netherlands, 1990.

Integrated Active Filters

[54] T. Adachi, A. Ishikawa, K. Tomioka, S. Hara, K. Takasuka, H. Hisajima, and A. Barlow, "A Low Noise Integrated AMPS IF Filter," IEEE 1994 Custom Integrated Circuits Conference, pp. 8.2.1-8.2.4, 1994.

[55] C-F Chiou, and R. Schaumann, "Design and Performance of a Fully Integrated Bipolar 10.7-MHz Analog Bandpass Filter," IEEE Transactions on Circuits and Systems, vol. CAS-33, no. 2, pp. 116-124, February 1986.

[56] T. C. Choi, R. T. Kaneshiro, R. W. Brodersen, P. R. Gray, W. B. Jett, and M. Wilcox, "High-Frequency CMOS Switched-Capacitor Filters for Communications Application," IEEE Journal of Solid-State Circuits, vol. SC-18, no. 6, pp. 652-663, December 1983.

[57] R.. A. Duncan, K. W. Martin, and A. S. Sedra, 'A Q-Enhanced Active-RLC Bandpass Filter', IEEE Int. Symp. on Circuits and Systems, 1993, pp. 1416-1419.

[58] A. M. Durham, J. B. Hughes, and W. Redman-White, "Circuit Architectures for High Linearity Monolithic Continuous-Time Filtering," IEEE Transactions on Circuits and Systems II, vol. 39, no. 9, pp. 651-657, September 1992.

[59] A. A. Gaash, R. S. Pepper, and D. O. Pederson, "Design of Integrable Desensitized Frequency Selective Amplifier," IEEE Journal of Solid-State Circuits, vol. SC-1, no. 1 pp. 29-35, September 1966.

[60] J. C. Haartsen, "Development of a Monolithic, Programmable SAW Filter in Silicon," IEEE MTT-S Digest, pp. 1115-1118, 1990.

[61] D. G. Haigh, C. Toumazou, S. D. Harrold, K. Steptoe, J. I. Sewell, and R. Bayruns, "Design Optimization and Testing of a GaAs Switched-Capacitor Filter," IEEE Transactions on Circuits and Systems, vol. 38, no. 8, pp. 825-837, August 1991.

[62] B. Hopf, I. Wolff, and M. Guglielmi, "Coplanar MMIC Active Bandpass Filters Using Negative Resistance Circuits," IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium, pp. 229-231, 1994.

[63] J. E. Kardontchik, *Introduction to the Design of Transconductor-Capacitor Filters*, Norwell, MA: Kluwer Academic Publishers, 1992.

[64] H. Khorramabadi, and P. R. Gray, "High Frequency CMOS Continuous-Time Filters", IEEE J. Solid State Circuits, pp.939-948, Dec. 1984.

[65] J. M. Khoury, and Y. P. Tsividis, "Analysis and Compensation of High-Frequency Effects in Integrated MOSFET-C Continuous-Time Filters," IEEE Trans. Circuits and Systems, vol. CAS-34, no. 8, pp. 862-875, August 1987.

[66] M. Koyama, H. Tanimoto, and S. Mizoguchi, "A 10.7 MHz Continuous-Time Bandpass Filter Bipolar IC," IEEE Proc. CICC, pp. 25.2.1-25.2.4, 1989.

[67] F. Krummenacher, and N. Joehl, "A 4-MHz CMOS Continuous-Time Filter with On-Chip Automatic Tuning," IEEE Journal of Solid-State Circuits, vol. 23, no. 3, pp. 750-758, June 1988.

[68] F. Krummenacher, "Design Considerations in High-Frequency CMOS Transconductance Amplifier Capacitor (TAC) Filters," IEEE ISCAS, pp. 100-105, 1989.

[69] F. Krummenacher, and G. Van Ruymbeke, "Integrated Selectivity for Narrow-Band FM IF Systems," IEEE J. Solid-State Circuits, pp. 757-760, June 1990.

[70] K-H Loh, D. L. Hiser, W. J. Adams, and R. L. Geiger, "A Versatile Digitally Controlled Continuous-Time Filter Structure with Wide-Range and Fine Resolution Capability," IEEE Transactions on Circuits and Systems II, vol 39, no. 5, pp. 265-276, May 1992.

[71] K. W. Moulding, J. R. Quartly, P. J. Rankin, R. S. Thompson, and G. A. Wilson, "Gyrator Video Filter IC with Automatic Tuning," IEEE J. Solid-State Circuits, vol. SC-15, no. 6, Dec. 1980, pp. 963-968.

[72] B. Nauta, *Analog CMOS Filters for Very High Frequencies*, Norwell, MA: Kluwer Academic Publishers, 1993.

[73] B. Nauta, "A CMOS Transconductance-C Filter Technique at Very High Frequencies,"IEEE JSSC, vol. SC-27, no. 2, pp. 142-153, Feb. 1992.

[74] N. M. Nguyen, and R. G. Meyer, "A Si Bipolar RF Bandpass Amplifier," IEEE J. of Solid State Circuits, 1992, pp. 123-127.

[75] C. S. Park, and R. Schaumann, "Design of a 4-MHz Analog Integrated CMOS Transconductance-C Bandpass Filter," IEEE J. Solid-State Circuits, August 1988, pp. 987-996.

[76] S. Pipilos, and Y. Tsividis, "RLC Active Filters with Electronically Tunable Centre Frequency and Quality Factor," Electronics Letters, vol. 30, no. 6, pp. 472-474, 17 March 1994.

[77] S. Pipilos, and Y. Tsividis, "Design of Active RLC Integrated Filters with Application in the GHz Range," IEEE International Symposium on Circuits and Systems, pp. 5.645-5.648, 1994.

[78] L-J Pu, and Y. P. Tsividis, "Transistor-Only Frequency-Selective Circuits," IEEE Journal of Solid-State Circuits, vol. SC-25, no. 3, pp. 821-832, June 1990.

[79] G. A. Rigby, and D. G. Lampard, "Integrated Frequency-Selective Amplifiers for Radio Frequencies," IEEE Journal of Solid-State Circuits, vol. SC-3, no. 4, pp. 417-422, December 1968.

[80] P. H. Saul, "Design Techniques for VHF and UHF Monolithic Silicon Filters," IEE Colloquium on 'Digital and Analogue Filters and Filtering Systems', pp. 7/1-4, 1990.

[81] R. Schaumann, "Design of Continuous-Time Fully Integrated Filters: A Review," IEE Proceedings, vol. 136, Pt. G, no. 4, pp. 184-190, August 1989.

[82] R. Schaumann, "Continuous-Time Integrated Filters – A Tutorial," in *Integrated Continuous-Time Filters,* Tsividis, Y. P., and Voorman, J. O., Ed., New York, IEEE Press, pp. 3-14.

[83] J. Silva-Martinez, M. S. J. Steyaert, and W. Sansen, "A 10.7-MHz 68-dB SNR CMOS Continuous-Time Filter With On-Chip Automatic Tuning," IEEE Journal of Solid-State Circuits, vol. 27, no. 12, pp. 1843-1853, Dec. 1992.

[84] J. Silva-Martinez, M. Steyaert, and W. Sansen, *High Performance CMOS Continuous-Time Filters*, Norwell, MA: Kluwer Academic Publishers, 1993.

[85] B-S. Song, and P. R. Gray, "Switched-Capacitor High-Q Bandpass Filters for IF Applications," IEEE Journal of Solid-State Circuits, vol. SC-21, no. 6, pp. 924-933, December 1986.

[86] B-S. Song, "A 10.7-MHz Switched-Capacitor Bandpass Filter," IEEE Custom Integrated Circuits Conference, pp. 12.3.1-12.3.4, 1988.

[87] M. S. J. Steyaert, S. Gogaert, W. Dehaene, J. Silva-Martinez, and J. Sevenhans, "Full CMOS Continuous Time Filters for GSM Applications," Ann. Telecommun, 48, pp. 224-232, 1993.

[88] S. Szczepanski, A. Wyszynski, and R. Schaumann, "Highly Linear Voltage-Controlled CMOS Transconductors," IEEE Trans. Circuits and Systems I, pp. 258-262, April 1993.

[89] K-S. Tan, and P. R. Gray, "Fully Integrated Analog Filters Using Bipolar-JFET Technology," IEEE J. Solid-State Circuits, vol. SC-13, no. 6, pp. 814-821, December 1978.

[90] M. K. Tanimoto, and S. Mizoguchi, "A 10.7 MHz Continuous-Time Bandpass Filter Bipolar IC," IEEE Proc. CICC, pp. 25.2.1-25.2.4, 1989.

[91] Y. Tsividis, M. Banu, and J. Khoury, "Continuous-Time MOSFET-C Filters in VLSI," IEEE Transactions on Circuits and Systems, vol. CAS-33, no. 2, pp. 125-139, February, 1986.

[92] Y. P. Tsividis, and J. O. Voorman, *Integrated Continuous-Time Filters - Principles, Design, and Applications,* New Jersey, IEEE Press, 1992.

[93] Y. P. Tsividis, "Integrated Continuous-Time Filter Design," IEEE 1993 Custom Integrated Circuits Conference, pp. 6.4.1-6.4.7, 1993.

[94] Y. P. Tsividis, "Integrated Continuous-Time Filter Design - An Overview," IEEE J. Solid State Circuits, pp 166-176, March 1994.

[95] G. A. De Veirman, and R. G. Yamasaki, "Design of a Bipolar 10-MHz Programmable Continuous-Time 0.05o Equiripple Linear Phase Filter," IEEE Journal of Solid State Circuits, vol. 27, no. 3, pp. 324-331, March 1992.

[96] J. O. Voorman, A. van Bezooijen, and N. Ramalho, "On Balanced Integrator Filters," in *Integrated Continuous-Time Filters,* Tsividis, Y. P., and Voorman, J. O., Ed., New York, IEEE Press, pp. 66-86.

[97] J. O. Voorman, "Continuous-Time Analog Integrated Filters," in *Integrated Continuous-Time Filters,* Tsividis, Y. P., and Voorman, J. O., Ed., New York, IEEE Press, pp. 15-46.

[98] Y-T Wang, F. Lu, and A. A. Abidi, "A 12.5 MHz CMOS Continuous Time Bandpass Filter," IEEE International Solid-State Circuits Conference, pp. 198-199, 1989.

[99] Y-T Wang, and A. A. Abidi, "CMOS Active Filter Design at Very High Frequencies," IEEE J. Solid State Circuits, pp. 1562-1574, Dec. 1990.

Filter Tuning

[100] T. L. Brooks, and P. M. VanPeteghem, "Simultaneous Tuning and Signal Processing in Integrated Continuous-Time Filters: the Correlated Tuning Loop," IEEE Intl. Symp. on Circ. and Syst., pp. 651-654, 1989.

[101] J. E. Franca, and F. Nunes, "Successive Approximation Tuning of Monolithic Continuous-Time Filters," Electronics Letters, vol. 28, no. 18, pp.1696-1697, 27 August 1992.

[102] W. J. A. de Heij, K. Hoen, and E. Seevinck, "Accurate Automatic Tuning Circuit for Bipolar Integrated Filters," IEEE ISCAS, pp. 1159-1162, 1990.

[103] K. A. Kozma, D. A. Johns, and A. S. Sedra, "Automatic Tuning of Continuous-Time Integrated Filters Using an Adaptive Filter Technique," IEEE Trans. Circuits Syst., 11, pp. 1241-1248, 1991.

[104] K. A. Kozma, D. A. Johns, and A. S. Sedra, "Tuning of Continuous-Time Filters in the Presence of Parasitic Poles," IEEE Trans. on Circuits and Systems I, pp.13-20, January 1993.

[105] W. B. Kuhn, A. Elshabini-Riad, and F. W. Stephenson, 'A New Tuning Technique for Implementing Very High Q, Continuous-Time, Bandpass Filters in Radio Receiver Applications', IEEE Int. Symp. on Circuits and Systems, 1994, pp 5-257 - 5-260.

[106] R. Schaumann, and M. A. Tan, "The Problem of On-Chip Automatic Tuning in Continuous-Time Integrated Filters," IEEE Intl. Symp. on Circ. and Syst., pp. 106-109, 1989.

[107] J. Silva-Martinez, M. Steyaert, and W. Sansen, "A Novel Approach for the Automatic Tuning of Continuous-Time Filters," Proceedings of the International Symposium on Circuits and Systems, pp. 1452-1455, 1991.

[108] Y. Tsividis, "Self-Tuned Filters," Elect. Lettr., pp. 406-407, 11 June 1981.

[109] P. M. VanPeteghem, T. L. Brooks, W. J. Adams, and H. M. Fossati, "Fully-Integrated Correlated Tuning Processor for Continuous-Time Filters," IEEE CICC, pp. 25.7.1-25.7.4, 1990.

Filter Dynamic Range

[110] A. A. Abidi, "Noise in Active Resonators and the Available Dynamic Range," IEEE Trans. on Circuits and Systems I, April 1992, pp. 296-299.

[111] *The ARRL Radio Buyer's Sourcebook - Product Reviews Collected from QST,* The American Radio Relay League, 1991.

[112] N. Ayrandjian, "Simple Computation of Spurious-Free Dynamic Range," RF Design, January 1987, pp. 65-66.

[113] S. Ford, "QST Compares: 2-Meter FM Mobile Tranceivers," QST Magazine, pp. 70-76, January 1995.

[114] S. Ford, "QST Compares: Dual-Band Hand-Held FM Transceivers," QST Magazine, pp. 66-71, July 1995.

[115] G. Groenewold, "The Design of High Dynamic Range Continuous-Time Integratable Bandpass Filters," IEEE Trans. Circuits and Systems, pp. 838-852, Aug. 1991.

[116] G. Groenewold, *Optimal Dynamic Range Integrated Continuous-Time Filters,* Ph.D. Thesis, Delft University of Technology, The Netherlands, 1992.

[117] J. W. Healy, "QST Compares: 2-Meter Hand-Held FM Tranceivers," QST Magazine, October 1992, pp. 54-62.

[118] J. W. Healy, "QST Compares: Dual-Band Mobile FM Tranceivers," QST Magazine, June 1993, pp. 66-71.

[119] Kuhn, W. B., Stephenson, F. W., and Elshabini-Riad, A., "Dynamic Range of High-Q OTA-C and Enhanced-Q LC RF Bandpass Filters," pp. 767-771, 1994 Midwest Symposium on Circuits and Systems, 1994.

[120] van Zeijl, P. T. M., "Noise and Dynamic Range Optimization of SAW Transversal Filters," IEEE Trans. on Ultrasonics, Ferr., and Freq. Contr., vol. 39, no. 4, July 1992.

Spiral Inductors

[121] H. E. Bryan, *Printed Inductors and Capacitors,* Tele-Tech & Electronic Industries, December 1955.

[122] J. Y.-C. Chang, A. A. Abidi, and M. Gaitan, "Large Suspended Inductors on Silicon and Their Use in a 2-um CMOS RF Amplifier," IEEE Electron Device Letters, May 1993, pp. 246-248.

[123] H. G. Dill, "Designing Inductors for Thin-Film Applications," Electronic Design, pp. 52-59, 17 February, 1964.

[124] H. M. Greenhouse, "Design of Planar Rectangular Microelectronic Inductors," IEEE Transactions on Parts, Hybrids, and Packaging, pp. 101-109, June 1974.

[125] F. W. Grover, *Inductance Calculations*, Van Nostrand, Princeton, N.J., 1946; Reprinted by Dover Publications, New York, N.Y., 1962.

[126] S. A. Jamison, A. Podell, M. Helix, P. Ng, and C. Chao, "Inductively Coupled Push-Pull Amplifiers for Low Cost Monolithic Microwave ICs," GaAs IC Symposium, pp. 91-93, 1992.

[127] D. M. Krafcsik, and D. E. Dawson, "A Closed-Form Expression for Representing the Distributed Nature of the Spiral Inductor," IEEE Microwaves and Millimeter Wave Monolithic Circuits Symposium, pp. 87-92, 1986.

[128] W. B. Kuhn, A. Elshabini-Riad, and F. W. Stephenson, "Centre-tapped Spiral Inductors for Monolithic Bandpass Filters," Electron. Lett., vol. 31, no. 8, pp. 625-626, 13 April 1995.

[129] D. Lang, "Broadband Model Predicts S-Parameters of Spiral Inductors," Microwaves & RF, pp. 107-110, January 1988.

[130] D. Lovelace, N. Camilleri, and G. Kannell, "Silicon MMIC Inductor Modeling for High Volume, Low Cost Applications," Microwave Journal, pp. 60-71, August 1994.

[131] N. M. Nguyen, and R. G. Meyer, "Si IC-compatible inductors and LC passive filters," IEEE J. Solid-State Circuits, August 1990, pp. 1028-1031.

[132] A. Olivei, "Optimized Miniture Thin-Film Planar Inductors, Compatible with Integrated Circuits," IEEE Transactions on Parts, Materials and Packaging, Vol. PMP-5, No. 2, pp. 71-88, June 1969.

[133] R. L. Remke, and G. A. Burdick, "Spiral Inductors for Hybrid and Microwave Applications," Proceedings of the 24th Electronic Components Conference, pp. 152-161, 1974.

[134] L. Selmi, and B. Ricco, "Design of an X-Band Transformer-Coupled Amplifier with Improved Stability and Layout," IEEE Journal of Solid State Circuits, pp. 701-703, Vol. 28, No. 6, June 1993.

[135] M. Soyuer, J. N. Burghartz, K. A. Jenkins, S. Ponnapalli, J. F. Ewen, and W. E. Pence, "Multilevel Monolithic Inductors in Silicon Technology," Electronics Letters, vol. 31, no. 5, pp. 359-360, 2 March 1995.

[136] M. Stubbs, L. Chow, and G. Howard, "Simulation Tool Accuragely Models MMIC Passive Elements," Microwaves & RF, pp. 75-79, January 1988.

[137] J. C. M. Toscano, *Wideband Characterization of Thick Film Inductors,* MS Thesis, Virginia Tech, 1988.

[138] H. Yabuki, and M. Makimoto, "Theoretical Analysis and Fundamental Characteristics of Triplate Spiral Inductors," Electronics and Communications in Japan, Part 2, vol. 73, no. 6, pp. 29-39, 1990.

[139] H. Yabuki, and M. Makimoto, "Theoretical Analysis and Fundamental Characteristics of Triplate Spiral Inductors," Electronics and Communications in Japan, Part 2, vol. 74, no. 4, pp. 1-11, 1991.

Frequency Synthesis and Oscillators

[140] G. Chang, A. Rofougaran, M-K. Ku, A. A. Abidi, and H. Samueli, "A Low-Power CMOS Digitally Synthesized 0-13 MHz Agile Sinewave Generator," IEEE Int. Solid-State Cir. Conf., pp. 32-33, 1994.

[141] S. K. Enam, and A. A. Abidi, "A 300-MHz CMOS Voltage-Controlled Ring Oscillator," IEEE J. Solid-State Circuits, vol. 25. no. 1, pp. 312-315, February 1990.

[142] D. B. Leeson, "Simple Model of a Feedback Oscillator Noise Spectrum," Proc. IEEE, vol. 54, pp. 329-330, February 1966.

[143] V. Manassewitsch, *Frequency Synthesizers - Theory and Design, Third Edition*, New York: John Wiley & Sons, 1987.

[144] N. M. Nguyen, and R. G. Meyer, "A 1.8 GHz Monolithic LC Voltage-Controlled Oscillator," IEEE International Solid-State Circuits Conference, pp. 158-159, 1992.

[145] H. T. Nicholas, and H. Samueli, "A 150-MHz Direct Digital Frequency Synthesizer in 1.25-um CMOS with -90-dBc Spurious Performance," IEEE Journal of Solid-State Circuits, vol. 26, no. 12, pp. 1959-1969, December 1991.

[146] C. K. Richardson, "A Novel Synthesizer for Miniture SSB Radio Equipment," Proc. 39th Annual Frequency Control Symp., pp. 189-192, 1985.

[147] W. P. Robins, *Phase Noise in Signal Sources,* Peter Peregrinus Ltd., Short Run Press, Ltd., Exeter, England, 1982.

[148] C. A. Sharpe, "A 3-State Phase Detector Can Improve Your Next PLL Design," EDN, pp. 55-59, September 20, 1976.

[149] M. Steyaert, and J. Craninckx, "1.1 GHz Oscillator Using Bondwire Inductance," Electronics Letters, vol. 30, no. 3, pp. 244-245, Feb. 3, 1994.

Electroacoustic Devices, Filters, and Oscillators

[150] S. G. Burns, and R. J. Weber, "Design and Performance of UHF and L-Band Oscillators using Thin-film Resonators on Semiconductor Substrates," Proceedings of the 34'th Midwest Symposium on Circuits and Systems, 1991.

[151] S. G. Burns, R. J. Weber, and S. D. Braymen, "High Frequency Oscillators Using Cointegrated BAW Thin-Film Piezoelectrics with Microwave BJTs," Forty-fifth Annual Symposium on Frequency Control, pp. 207-211, 1991.

[152] C. Campbell, *Surface Acoustic Wave Devices and Their Signal Processing Applications,* Academic Press, Inc., Boston, 1989.

[153] S. Datta, *Surface Acoustic Wave Devices,* Printice-Hall, Englewood Cliffs, NJ, 1986.

[154] L. N. Dworsky, and C. S. Shanley, "The Motorola Multi-Pole Monolithic Filter Project," Proc 39th Annual Frequency Control Symp., pp. 486-490, 1985.

[155] B. Horine, "Narrowband SAW Filters for IF Applications," 44th Annual Symposium on Frequency Control, pp. 316-322, 1990.

[156] S. Horwitz, and C. Milton, "Application of film bulk Acoustic Resonators," IEEE MTT-S Digest, pp. 165-168, 1992.

[157] R. G. Kinsman, *Crystal Filters - Design, Manufacture, and Application,* John Wiley & Sons, Inc., New York, 1987.

[158] S. V. Krishnaswamy, J. Rosenbaum, C. Vale, and R. A. Moore, "Compact FBAR Filters Offer Low-Loss Performance," Microwaves & RF, pp. 127-136, Sept. 1991.

[159] S. V. Krishnaswamy, J. F. Rosenbaum, S. S. Horwitz, and R. A. Moore, "Film Bulk Acoustic Wave Resonator and Filter Technology," IEEE MTT-S Digest, pp. 153-155, 1992.

[160] K. M. Lakin, "Modeling of Thin Film Resonators and Filters," IEEE MTT-S Digest, pp. 149-152, 1992.

[161] K. M. Lankin, G. R. Kline, and K. T. McCorron, "High Q Microwave Acoustic Resonators and Filters," IEEE MTT-S Digest, pp. 1517-1520, 1993.

[162] J. Machui, G. Muller, W. Ruile, L. Reindl, R. Weigel, and P. Russer, "A New Low Loss SAW Filter Structure with Extremely Wide Bandwidth for Mobile Communication Systems," IEEE MTT-S Digest, pp. 1501-1504, 1993.

[163] C. Vale, J. Rosenbaum, S. Horwitz, S. Krishnaswamy, and R. Moore, "FBAR Filters at GHz Frequencies," Forty-fourth Annual Symposium on Frequency Control, pp. 332-336, 1990

[164] A. Victor, and S. Skiest, "SAW Filters Aid Communications System Performance," Microwaves and RF, pp. 104-111, August 1991.

[165] J. H. Visser, M. J. Vellekoop, A. Venema, E. van der Drift, P. J. M. Rek, A. J. Nederlof, and M. S. Nieuwenhuizen, "Surface Acoustic Wave Filters in ZnO-SiO2-Si Layered Sturctures," IEEE Ultrasonics Symposium, pp. 195-200, 1989.

[166] R. Weigel, B. Bader, G. Fischerauer, P. Russer, "Design and Performance of Wideband IIDT-type SAW Filters with Low Loss and Improved Sidelobe Suppression," IEEE MTT-S Digest, pp. 1505-1508, 1993.

[167] P. T. M. van Zeijl, J. H. Visser, and L. K. Nanver, "FM Radio Receiver Front-End Circuitry with On-Chip SAW Filters," IEEE Trans. on Consumer Elect., vol. 35, no. 3, August 1989.

General References

[168] N. Camilleri, J. Costa, D. Lovelace, and D. Ngo, "Silicon MOSFETs, the Microwave Device Technology for the 90s," IEEE MTT-S Digest, pp. 545-548, 1993.

[169] N. Camilleri, D. Lovelace, J. Costa, and D. Ngo, "New Development Trends for Silicon RF Device Technologies," IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium, pp. 5 - 8, 1994.

[170] M. A. Copeland, "VLSI for Analog/Digital Communications," IEEE Communications Magazine, pp. 25-30, May 1991.

[171] P. R. Gray, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits, Second Edition,* pp. 150-156, John Wiley & sons, New York, 1984.

[172] H. L. Krauss, C. W. Bostian, and F. H. Raab, *Solid State Radio Engineering*, John Wiley & Sons, New York, pp. 38-82, 1980.

[173] J. J. Liu, H. Berg, Y. Wen, S. Mulgaonker, R. Bowlby, and A. Mawer, "PBGA: Pros and Cons," Advancing Microelectronics, pp. 16,17,43-48, January/February 1995.

[174] S. I. Long, and S. E. Butner, "GaAs IC Fabrication with MOSIS – A User's Perspective," IEEE ISCAS, pp. 2562-2565, 1990.

[175] J. L. McCreary, "Matching Properties, and Voltage and Temperature Dependence of MOS Capacitors," IEEE Journal of Solid-State Circuits, vol. SC-16, no. 6, pp. 608-616, December 1981.

[176] R. G. Meyer, and A. K. Wong, "Blocking and Desensitization in RF Amplifiers," IEEE JSSC, pp. 944-946, August 1995.

[177] H. W. Ott, *Noise Reduction Techniques in Electronic Systems,* John Wiley & Sons, New York, 1988.

[178] M. Parameswaran, H. P. Baltes, Lj. Ristic, A. C. Dhaded, and A. M. Robinson, "A New Approach for the Fabrication of Micromechanical Structures," Sensors and Actuators,, 19, pp. 289-307, 1989.

[179] T. Pratt, and C. W. Bostian, *Satellite Communications,* New York, John Wiley & Sons, 1986.

[180] S. M. Sze, *Physics of Semiconductor Devices*, 2nd Edition, John Wiley & Sons, New York, pp. 448-453, 1981.

[181] C. Tomovich, "MOSIS - A Gateway to Silicon," IEEE Circuits and Devices Magazine, pp. 22-23, March 1988.

[182] E. A. Vittoz, "Future of Analog in the VLSI Environment," IEEE ISCAS, pp. 1372-1375, 1990.

[183] D. Walshak, and H. Hashemi, "BGA Technology: Current State of the Art and Future Direction for Plastic, Ceramic, and Tape BGAs," Advancing Microelectronics, pp. 14,15,38-42, January/February 1995.

[184] R. M. Warner, Editor, *Integrated Circuits: Design Principles and Fabrication,* New York: McGraw-Hill, 1965.

[185] S. R. Wilson, C. J. Tracy, and J. L. Freeman Jr., Editors, *Handbook of Multilevel Metallization for Integrated Circuits*, Noyes Publications, Park Ridge, N.J., pp. 117, 1993.

[186] B. Wuppermann, B. Fox, R. Walker, S. Atkinson, D. Budin, C. Lanzl, and S. Bleiweiss, "A 16-PSK Modulator With Phase Error Correction," International Solid-State Circuits Conference, pp. 138-139, 1993.

[187] A. L. Zverev, *Handbook of Filter Synthesis*, John Wiley & Sons, New York, 1967.

Vita

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