

APPLICATION NOTE

A Wideband General Purpose PIN Diode Attenuator

Introduction

PIN diode-based Automatic Gain Control (AGC) attenuators are commonly used in many broadband system applications such as cable or fiberoptic TV, wireless CDMA, etc. A popular attenuator design used over the instantaneous frequency range from 10 MHz to beyond 2 GHz is the PI network. The benefit of this design is its broadband constant impedance, wide dynamic range, and good compatibility with AGC signals.

The PIN diode is used as a current-controlled resistance component in the PI network. PIN diodes are low-cost, low-distortion elements available in commonly used small plastic packages.

This Application Note describes the design of a high-performance, PIN-based four diode PI attenuator, as shown in Figure 1, using Skyworks low-cost SMP1307-011LF diode in a plastic SOD-323 package (see Reference 1 for additional information). Performance is characterized from 10 MHz to 3 GHz. The benefit of the four diode circuit is its symmetry that allows for a simpler bias network and a reduction of distortion due to cancellation of harmonic signals in the back-to-back configuration of the series diodes.

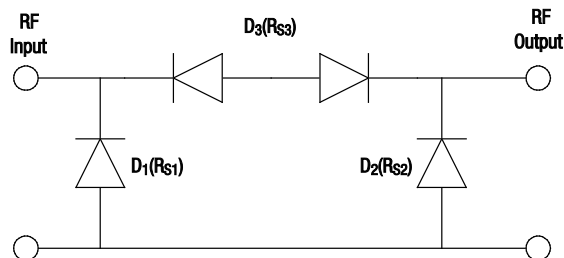


Figure 1. Four-Diode PI Attenuator

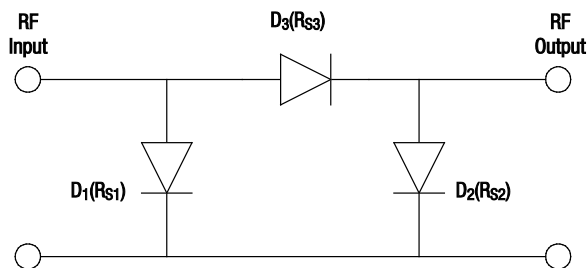


Figure 2. PI Attenuator

PI Attenuator Fundamentals

For matched broadband applications, especially those covering low RF frequencies (to 5 MHz) through frequencies greater than 1 GHz, PIN diode designs are commonly used. The most popular circuit configurations are the TEE, bridged TEE, and the PI. All these designs use PIN diodes as current-controlled RF resistors with resistance values set by DC control and established by an AGC loop.

Figure 2 shows a basic PI attenuator that uses three PIN diodes. It also shows the expressions that determine the resistance values for each PIN diode as a function of attenuation. Figure 3 displays the value of PIN diode resistance for a 50 Ω PI attenuator. Note that the minimum value for the shunt diodes, R_1 and R_2 , is 50 Ω .

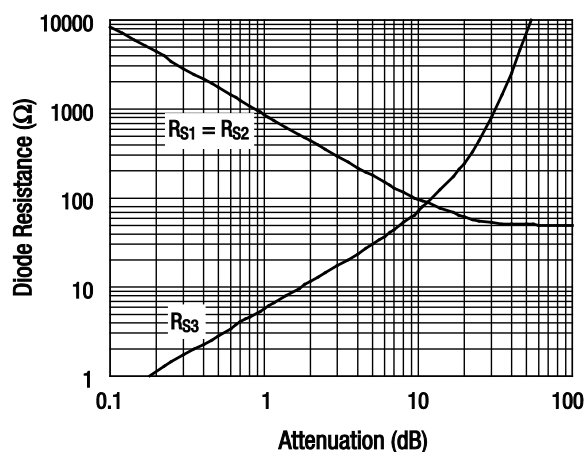


Figure 3. Attenuation of PI Attenuators

Attenuator Circuit Model

In the Libra IV model shown in Figure 4, the PIN diode pairs, X_3/X_4 and X_1/X_2 , are symmetrically biased from two DC sources. A 5 V reference DC voltage source (V_{REF}) provides adequate biasing to keep the RF resistance of the shunt diodes X_2 and X_3 near $50\ \Omega$ at high attenuation while the series diodes, X_4 and X_1 , are at high resistance values.

The values of biasing resistors SRL_3 , SRL_2 , SRL_1 , SRL_5 , and SRL_4 were selected to provide a low Standing Wave Ratio (SWR) for the full attenuation range. Attenuation is controlled by the control voltage source (V_{CTL}), ranging from 1 to 6 V. This source supplies forward bias current to the series diodes, X_4 and X_1 , through a wideband, high impedance ferrite inductor, X_7 (Taiyo-Yuden model FBMH4525) and resistors SRL_5 , SRL_4 , and SRL_6 .

Capacitors $SRLC_{12}$, $SRLC_{10}$, and $SRLC_5$ provide RF ground for the shunt diodes. The separation of the biasing path into two branches, SRL_2 and SRL_1 , was to reduce RF coupling between input and output, which affects maximum attenuation, especially at high frequencies, due to the parasitic series inductances.

Capacitors C_6 and C_7 simulate the effect of the coaxial connectors (SMA connectors were used on test boards). Shunt connected capacitors, $SRLC_7$ and $SRLC_{11}$, were inserted to compensate for the parasitic inductances of the decoupling capacitors, $SRLC_4$ and $SRLC_6$. These parasitic inductances strongly affect attenuator performance at frequencies beyond 2 GHz.

The PI type C-L-C circuit between series diodes $SRLC_8$, L_1 , and $SRLC_9$, was used to increase the maximum isolation at higher frequencies while improving insertion loss at low attenuation.

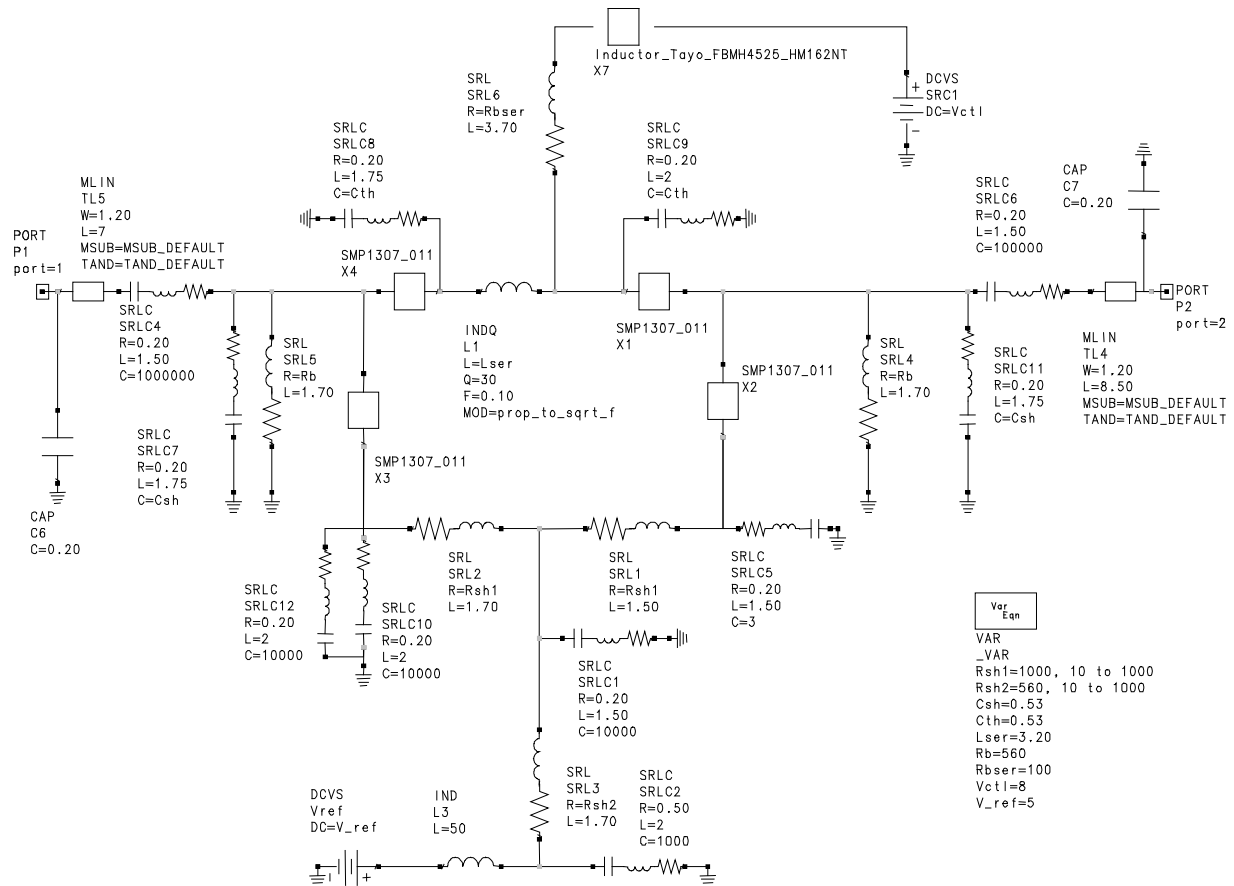
Figure 5 illustrates the effect of connecting or not connecting this C-L-C circuit. A clear 5 to 8 dB improvement in isolation is demonstrated.

The values of the bias resistors were optimized for optimum SWR performance over the entire attenuation range. The intent was to keep the values of SRL_5 and SRL_4 as low as possible to ensure maximum forward current in the series diodes, X_4 and X_1 , but high enough not to affect insertion loss.

The input and output circuits are not symmetrical, as may be seen from the values of capacitors $SRLC_{12}$ and $SRLC_{10}$ (10 nF each), compared to $SRLC_5$ (2 pF). The $SRLC_5$ value was selected to improve high-frequency isolation by compensating the parasitic series inductance of shunt diode, X_2 , and its own parasitic inductance. This compensation helped improve isolation by several dB at frequencies higher than 1 GHz; however, as a result, the SWR of the output port SWR is increased at lower frequencies.

Most applications are not sensitive to high-output SWR, but if necessary, symmetry of the attenuator may be established by increasing $SRLC_5$ to 10 nF. Figure 6 shows the effect of changing $SRLC_5$ from 2 pF to 10 nF. If implemented, there will be no significant effect on the input SWR, because of the high isolation between input and output, and no effect on attenuation or SWR at the minimum attenuation.

The linear test bench used for the analysis of the above attenuator is shown in Figure 7.



DATA	DATA	DATA
TEMP	RREF	MSUB
TEMP_DEFAULT	RREF_DEFAULT	MSUB_DEFAULT
TEMP=27	R=50	ER=4.20
		H=0.80
		T=5.00e-003
		RHO=0.75
		RGH=0
		COND1=cond
		COND2=cond2
		DIEL1=diel
		DATA
		MSUB
		MSUB_HP
		ER=4.20
		H=0.78
		T=5.00e-003
		RHO=0.75
		RGH=0
		COND1=cond
		COND2=cond2
		DIEL1=diel

Figure 4. Attenuator Model for Libra IV

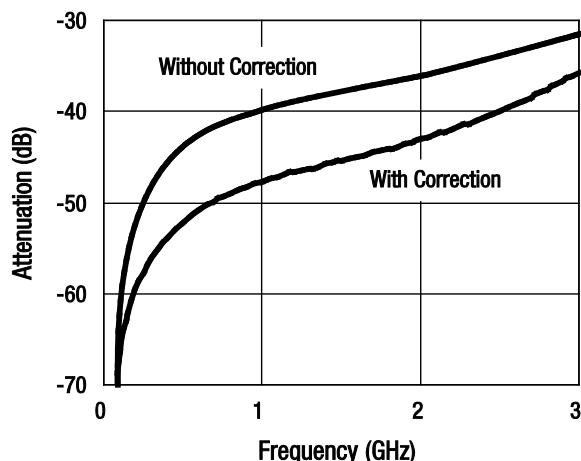


Figure 5. The Effect of Compensation Circuit

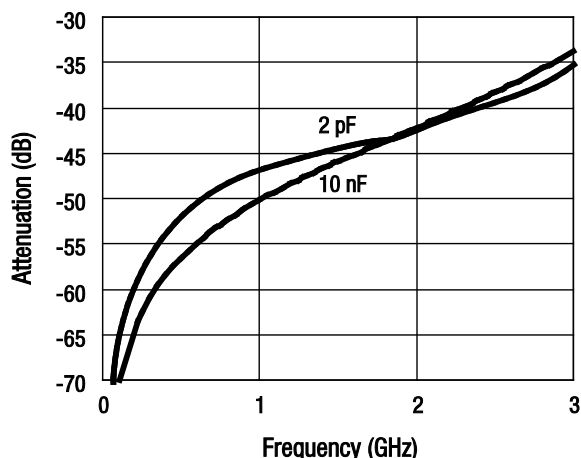


Figure 6. The Effect of Capacitor SRLCs

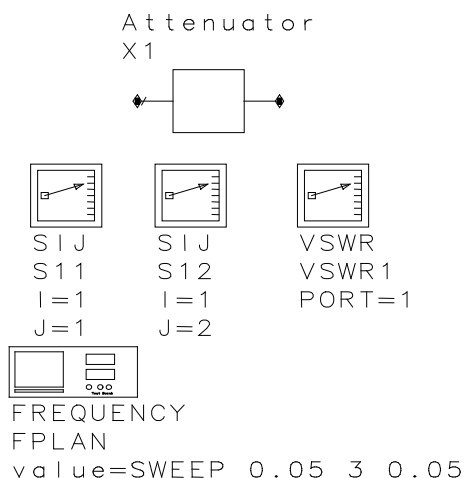


Figure 7. Attenuator Model Test Bench for Libra IV

SMP1307 SPICE Model

The SMP1307-011LF is a silicon PIN diode with a thick I-region (175 μm) and a long carrier lifetime ($\text{TL} = 1.5 \mu\text{s}$). This results in a variable resistance device with a wide variation of resistance versus current that can operate with low distortion as an attenuator element. The diode is provided in an SOD-323 package.

The SPICE model for the SMP1307-011LF varactor diode defined for the Libra IV environment is shown in Figure 8 with a description of the parameters used. In this model, two diodes were used to fit both DC and RF properties of the PIN diode.

The built-in PIN diode Libra IV model was used to model behavior of RF resistance versus DC current, while a PN-junction diode model was used to model DC voltage-current response. Both diodes were connected in series to ensure the same current flow, while the PN-junction diode was effectively RF short-circuited with the capacitor $C_2 = 10^{11} \text{ pF}$.

The portion of the RF resistance that reflects residual series resistance, was modeled with $R_2 = 2.2 \Omega$. This is shunted with the ideal inductor $L_1 = 10^{19} \text{ nH}$ to avoid affecting DC performance. Capacitances C_6 , C_P , and inductor L_2 reflect junction and package properties of the SMP1307-011LF diode.

The described model is a linear model that emulates the DC and RF properties of the PIN diode when the signal frequency is higher than:

$$\frac{1300}{W(\mu\text{m})^2} = \frac{1300}{175^2} = 0.0425 \text{ MHz}$$

For more details on the properties of the PIN diode refer to Reference 2.

Tables 1 and 2 describe the model parameters. They show default values appropriate for silicon varactor diodes that may be used by the Libra IV simulator. Some of the values of the built-in Libra IV PIN diode model were not used. Those are marked "Not Used" in both Tables.

The model DC current voltage response calculated by the Libra IV simulator is shown in Figure 9 together with the measured data. It shows very good compliance of Skyworks model DC properties with measured results.

Figure 10 shows internal RF resistance after the parasitic capacitances, C_6 , C_P , and inductor L_2 were de-embedded. Here again, the measured and simulated results agree.

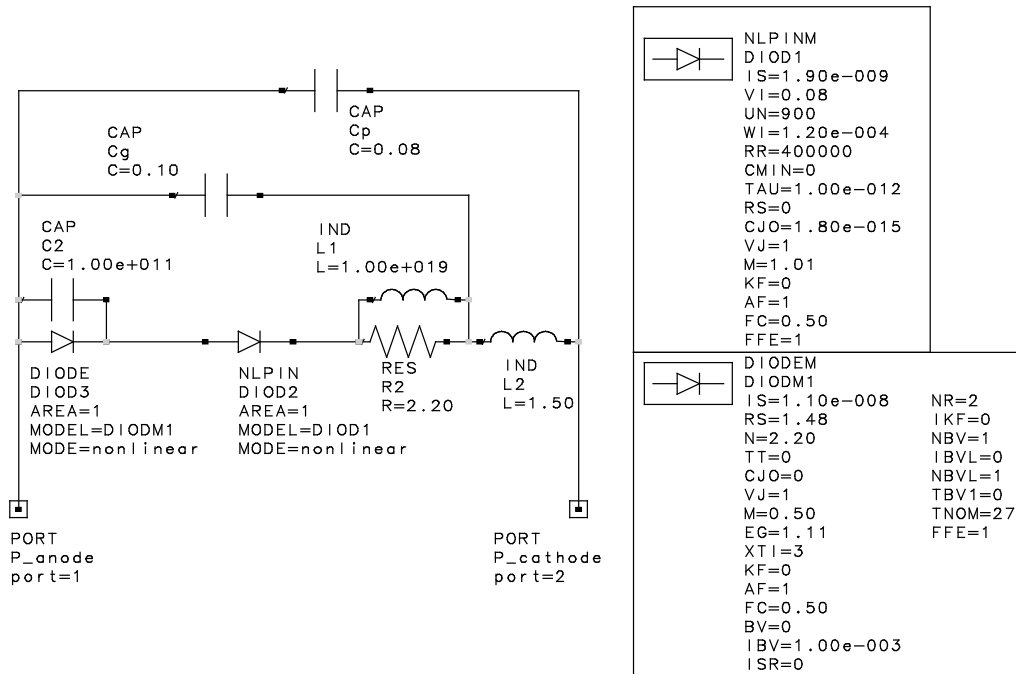


Figure 8. SMP1307-011LF Model For The Libra IV Simulator

Table 1. Libra IV Simulator Silicon PIN Diode Default Values

Parameter	Description	Units	Value
IS	Saturation current (Not Used)	A	1.9×10^{-9}
VI	I-region forward bias voltage drop	V	0.08
UN	Electron mobility (Not Used)	$\text{cm}^2/(\text{V}\cdot\text{s})$	900
WI	I-region width (Not Used)	M	1.2×10^{-4}
RR	I-region reverse bias resistance	Ω	4×10^5
CMIN	PIN punchthrough capacitance	F	0
TAU	Ambipolar lifetime within I-region (Not Used)	s	10^{-12}
RS	Series resistance	Ω	0
CJO	Zero-bias junction capacitance	F	1.8×10^{-15}
VJ	Junction potential	V	1
M	Grading coefficient	–	1.01
KF	Flicker noise coefficient (Not Used)	–	0
AF	Flicker noise exponent (Not Used)	–	1
FC	Forward-bias depletion capacitance coefficient (Not Used)	–	0.5
FFE	Flicker noise frequency exponent (Not Used)	–	1

Table 2. Libra IV Simulator Silicon PIN Diode Values Assumed for the SMP1307-011LF Model

Parameter	Description	Units	Value
IS	Saturation current (Not Used)	A	1.1×10^{-8}
RS	Series resistance	Ω	1.48
N	Emission coefficient (Not Used)	–	2.2
TT	Transit time (Not Used)	S	0
CJO	Zero-bias junction capacitance (Not Used)	F	0
VJ	Junction potential (Not Used)	V	1
M	Grading coefficient (Not Used)	–	0.5
EG	Energy gap (with XTI, helps define the dependence of IS on temperature)	EV	1.11
XTI	Saturation current temperature exponent (with EG, helps define the dependence of IS on temperature)	–	3
KF	Flicker noise coefficient (Not Used)	–	0
AF	Flicker noise exponent (Not Used)	–	1
FC	Forward-bias depletion capacitance coefficient (Not Used)	–	0.5
BV	Reverse breakdown voltage (Not Used)	V	Infinity
IBV	Current at reverse breakdown voltage (Not Used)	A	10^{-3}
ISR	Recombination current parameter (Not Used)	A	0
NR	Emission coefficient for ISR (Not Used)	–	0
IKF	High-injection knee current (Not Used)	A	Infinity
NBV	Reverse breakdown ideality factor (Not Used)	–	1
IBVL	Low-level reverse breakdown knee current (Not Used)	A	0
NBVL	Low-level reverse breakdown ideality factor (Not Used)	–	1
TNOM	Nominal ambient temperature at which these model parameters were derived	$^{\circ}\text{C}$	27
FFE	Flicker noise frequency exponent (Not Used)	–	1

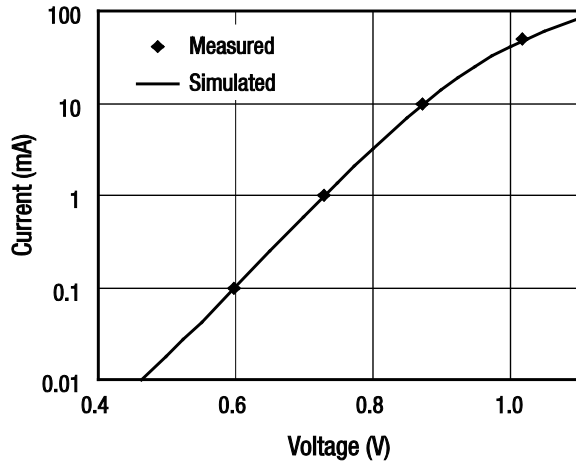


Figure 9. DC Voltage Current Response of SMP1307-011LF

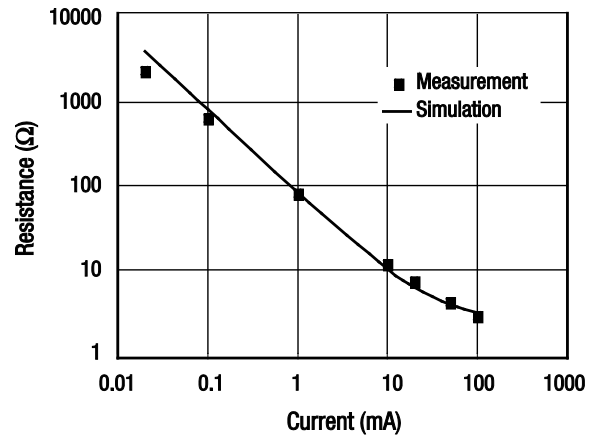


Figure 10. RF Resistance vs Current for SMP1307-011LF

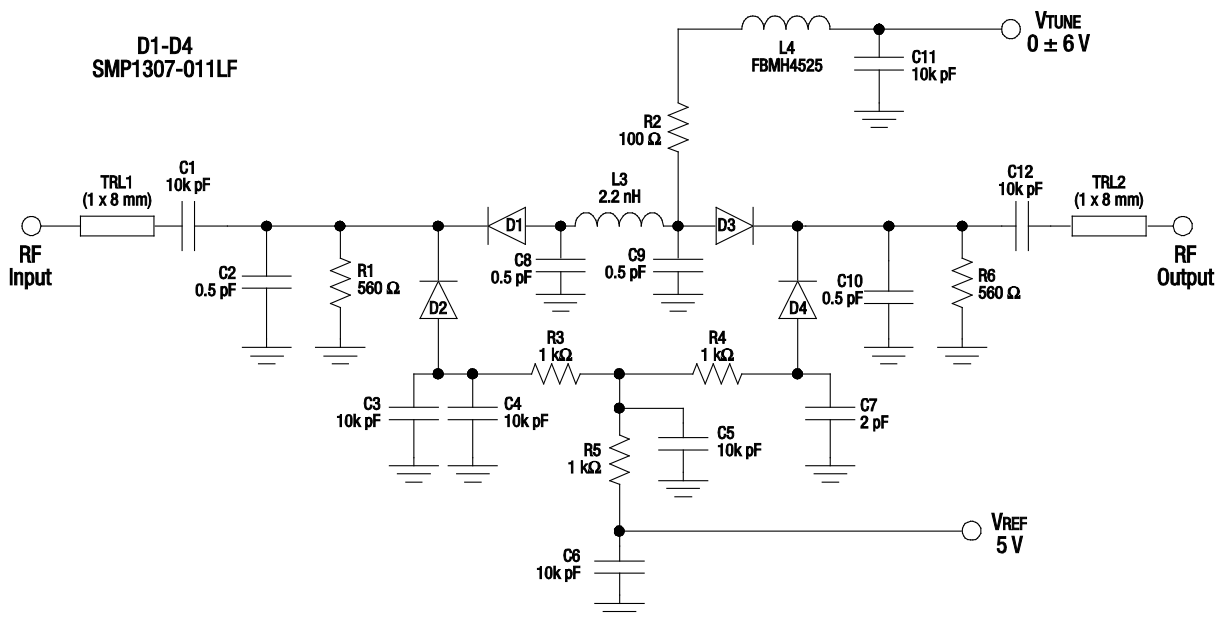


Figure 11. Attenuator Circuit Diagram

Attenuator Design, Materials, Layout, and Performance

The circuit diagram for the four-diode PI attenuator is shown in Figure 11. The PCB layout is shown in Figure 12. The board was made of standard, 30 mil thick, FR4 material. The Bill of Materials (BOM) used is provided in Table 3.

The measured attenuation of this circuit and the simulated results obtained with the model in Figure 8 are shown in Figure 13 and 14, respectively. The model fits measurement results very well in

the attenuation extremes, but has a small deviation from measurements in the middle of the attenuation range. This may be attributed to the imperfection of the diode RF resistance model shown in Figure 10.

Figure 15 shows measured input SWR at different control voltages. The SWR is well below a value of 2 across the entire range of frequencies and attenuation levels as predicted by the model.

A plot of attenuation versus control voltage at temperatures of 23 °C and 85 °C is shown in Figure 16. The graph shows that the temperature performance is very stable, with less than 0.5 dB variation over the 62 °C excursion at the highest attenuation.

Figure 17 shows output third order intercept point (IP3) versus control voltage. The measurement was performed at 900 MHz using a single tone, 1 W input power. The IP3 was derived from the third harmonic using the method described in Reference 3.

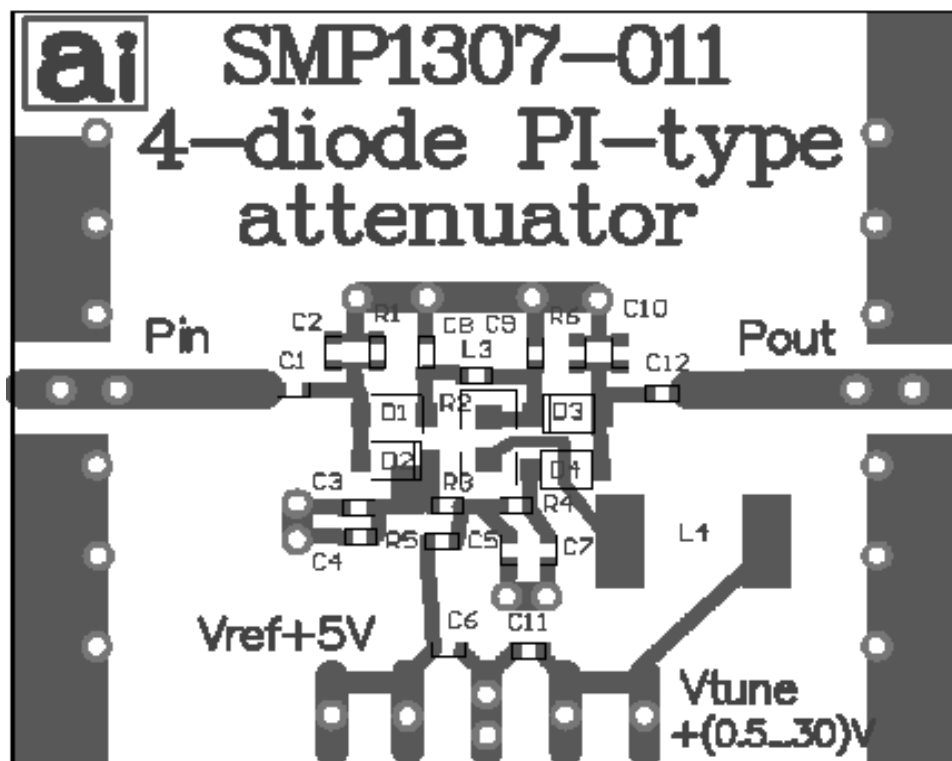


Figure 12. Attenuator PCB Layout

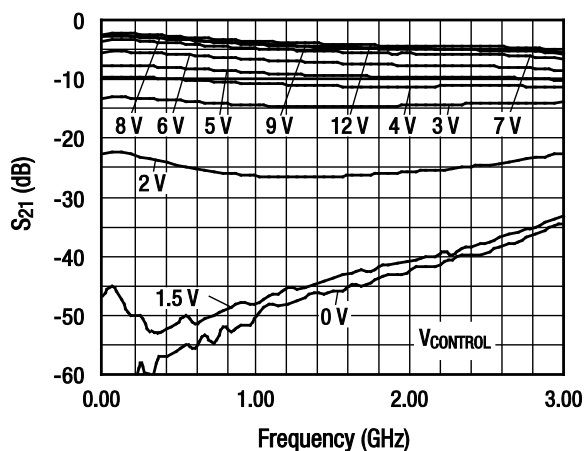


Figure 13. Measured S_{21}

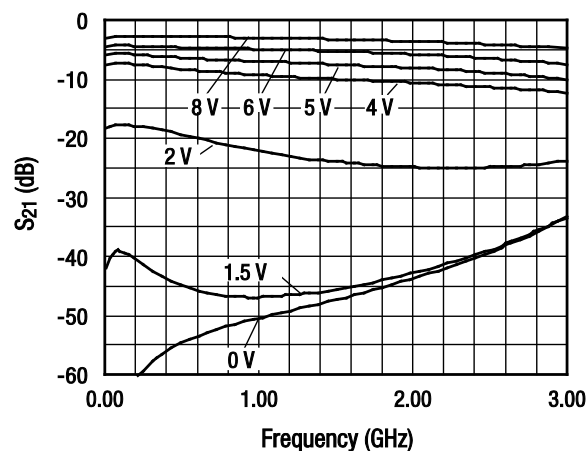


Figure 14. Simulated S_{21}

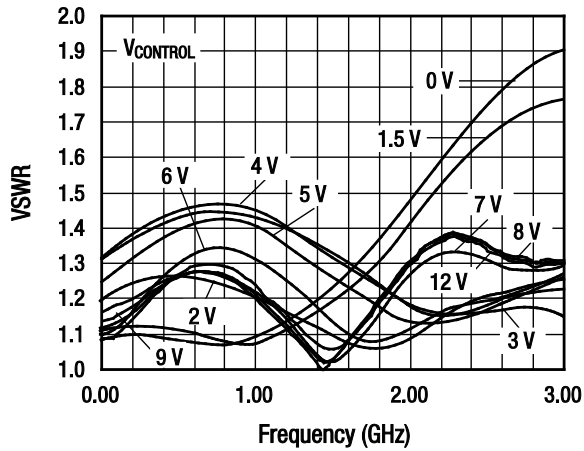


Figure 15. Measured SWR

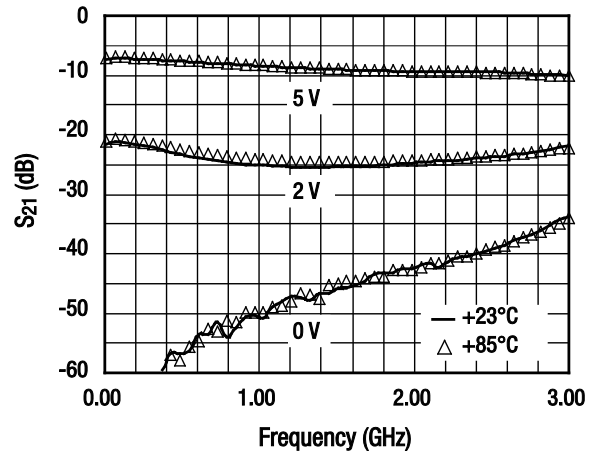


Figure 16. Attenuation vs Temperature

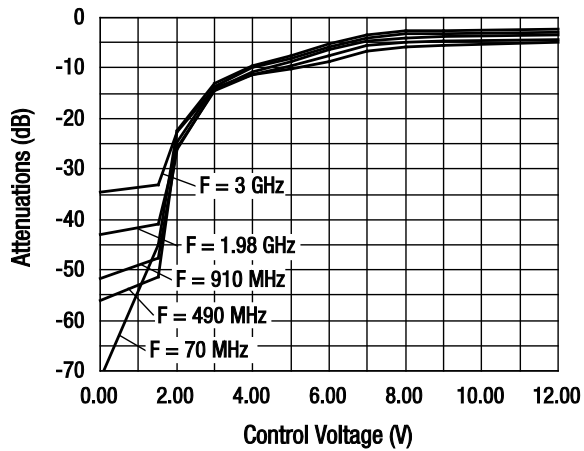


Figure 17. Attenuation vs Control Voltage

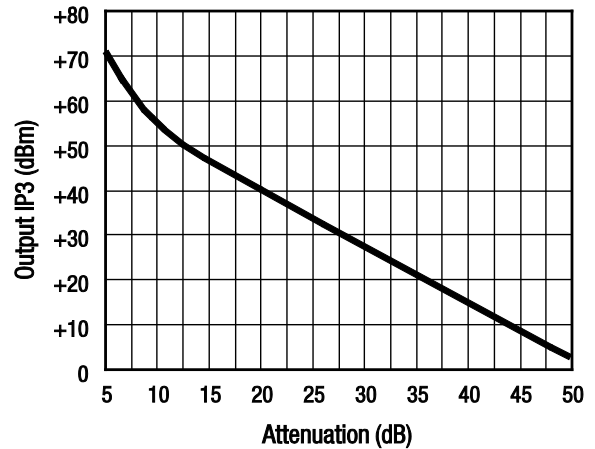


Figure 18. IP3 vs Attenuation @ 900 MHz

References:

1. Skyworks Solutions, Inc., *SMP1307 Series: Very Low Distortion Attenuator Plastic Packaged PIN Diodes* Data Sheet, document #200045.
2. Skyworks Solutions, Inc., *Design with PIN Diodes* Application Note, document #200312.
3. Hiller, G. and R. Caverly. *Predict PIN-Diode Switch Distortion*, *Microwaves and RF*, v. 25(1):111, January 1986.

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