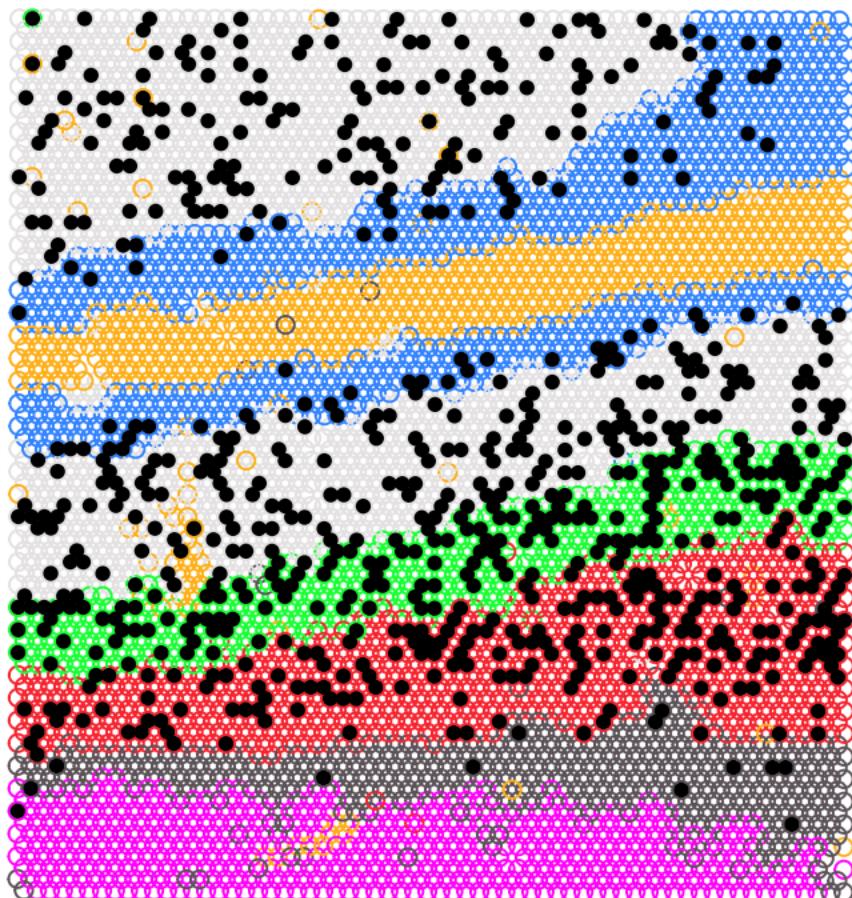


# V12F14-053\_A1



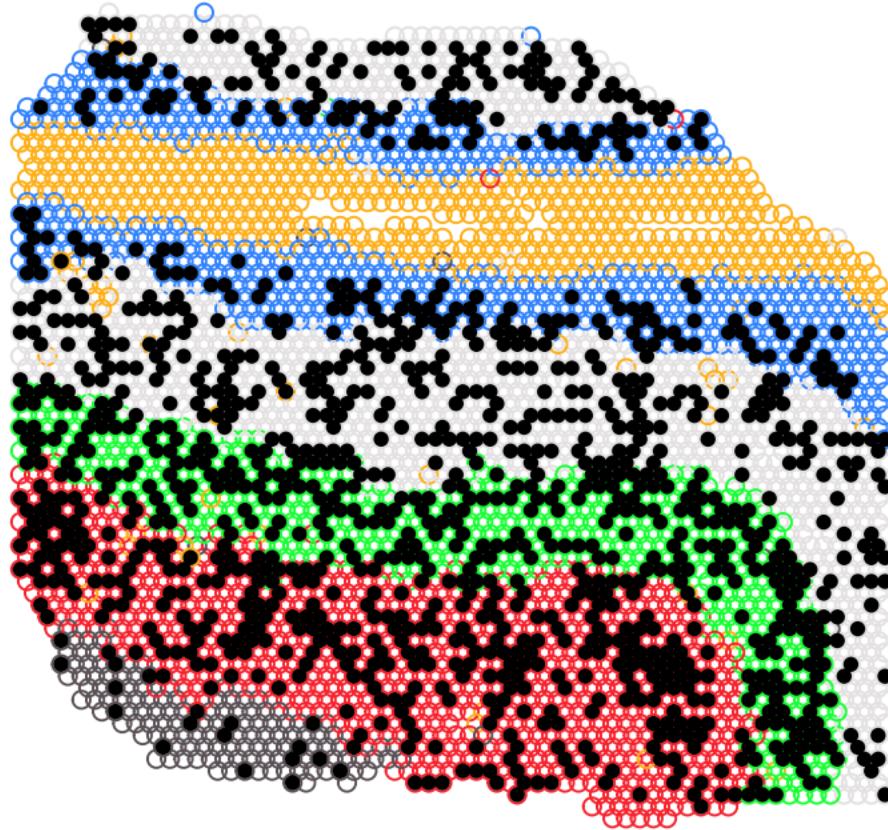
neun\_pos

- FALSE
- TRUE

PRECAST\_07

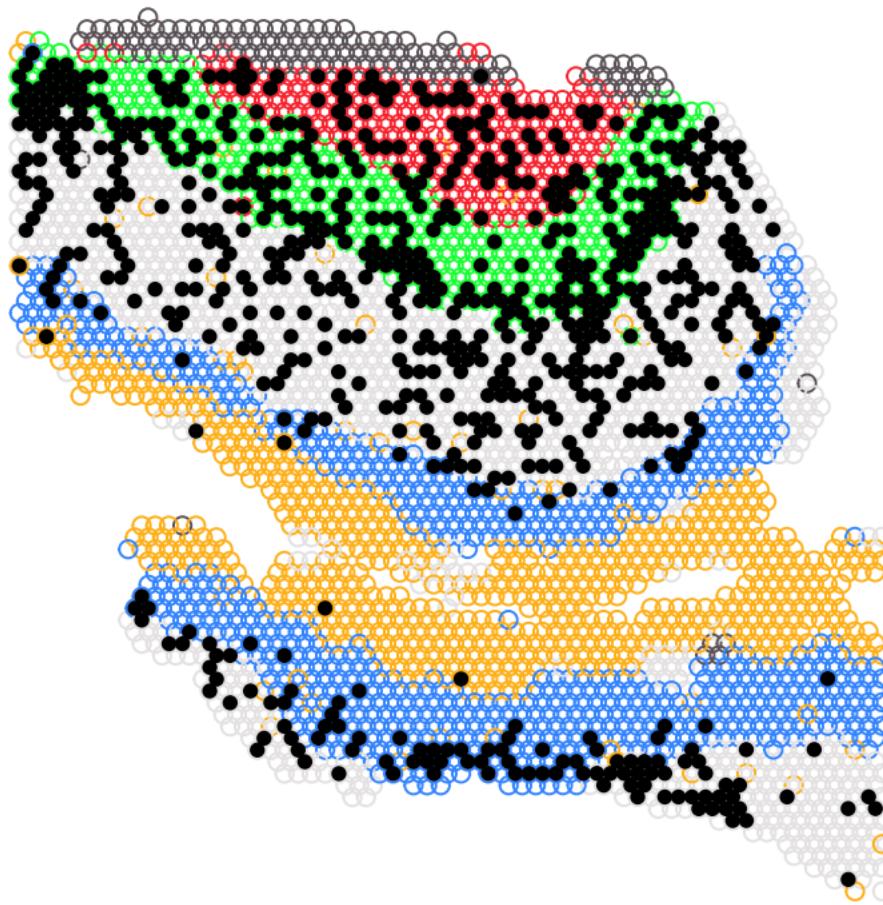
- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

V12F14-053\_C1



- neun\_pos
- FALSE
  - TRUE
- PRECAST\_07
- L1 (spd07)
  - L2/3 (spd06)
  - L3/4 (spd02)
  - L5 (spd05)
  - L6 (spd03)
  - L6/WM (spd01)
  - WM (spd04)

# V12F14-053\_D1



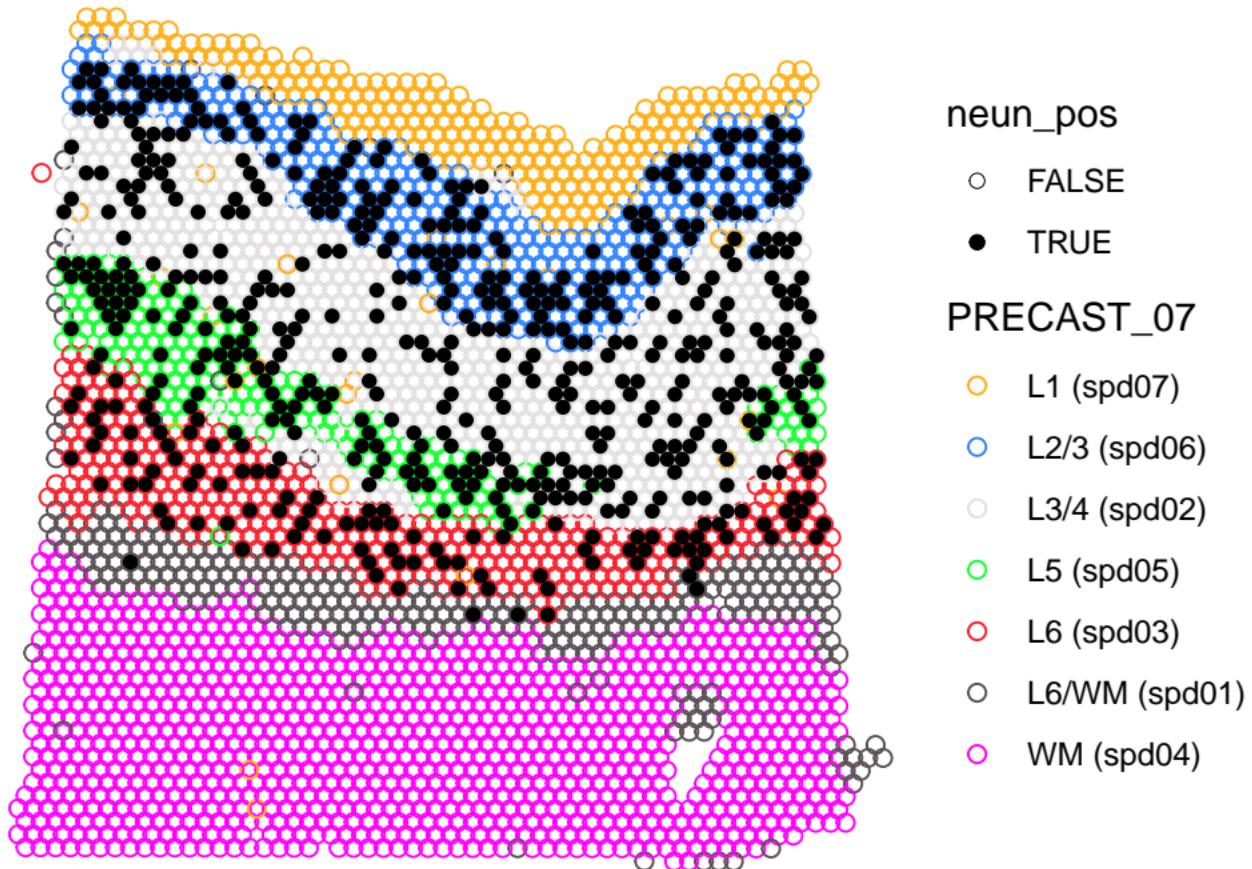
neun\_pos

- FALSE
- TRUE

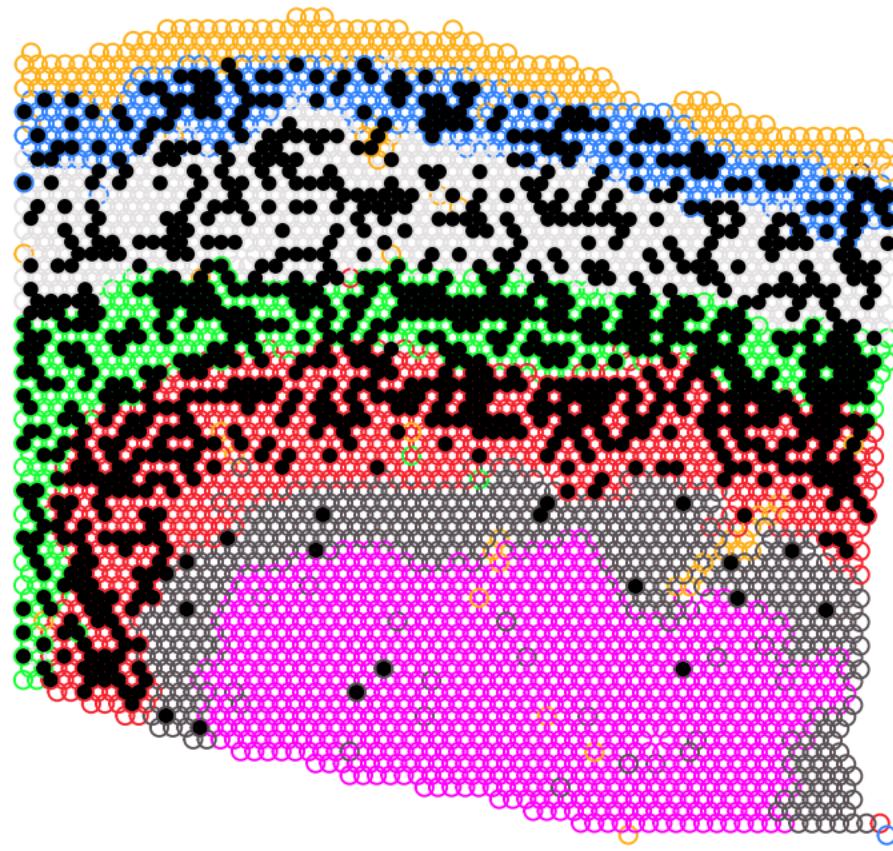
PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

V12F14-057\_A1

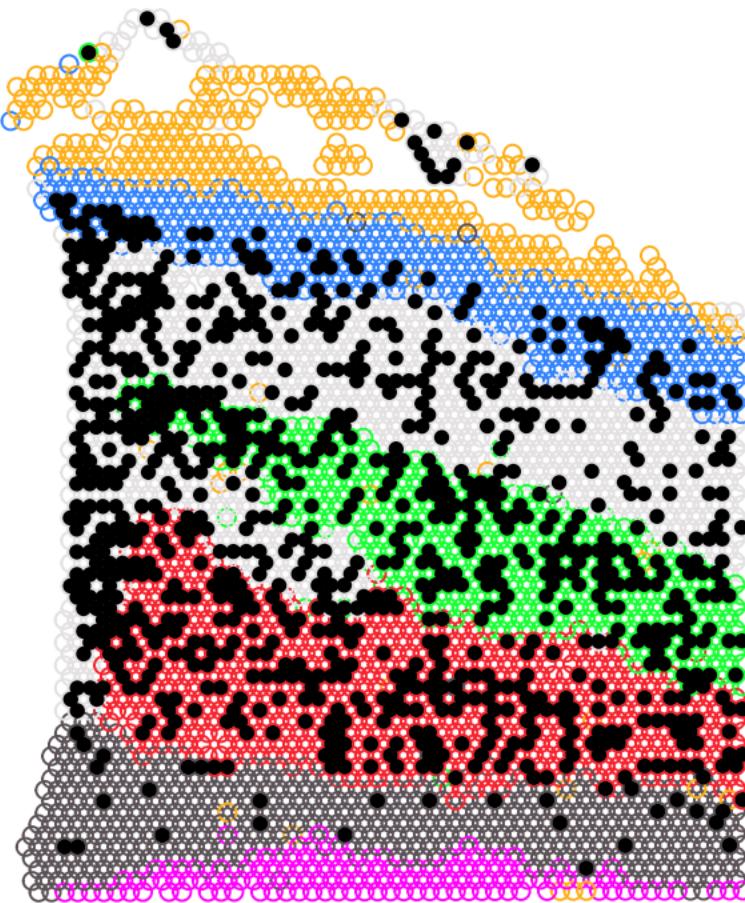


V12F14-057\_B1



- neun\_pos**
  - FALSE
  - TRUE
- PRECAST\_07**
  - L1 (spd07)
  - L2/3 (spd06)
  - L3/4 (spd02)
  - L5 (spd05)
  - L6 (spd03)
  - L6/WM (spd01)
  - WM (spd04)

# V12F14-057\_C1



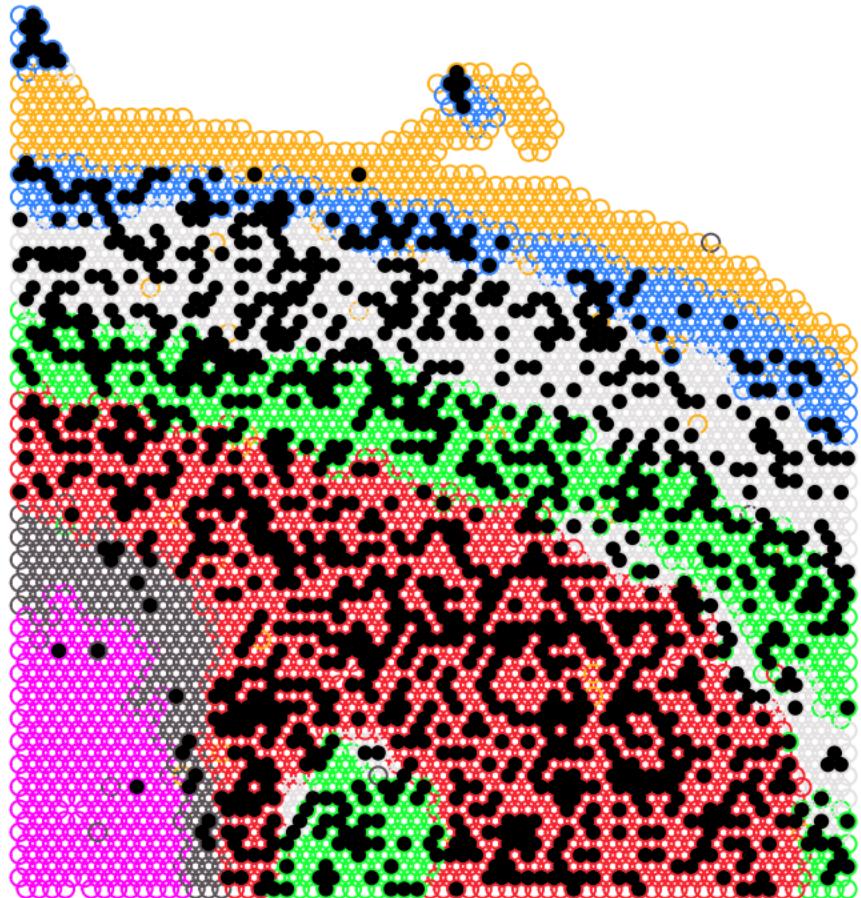
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V12F14-057\_D1



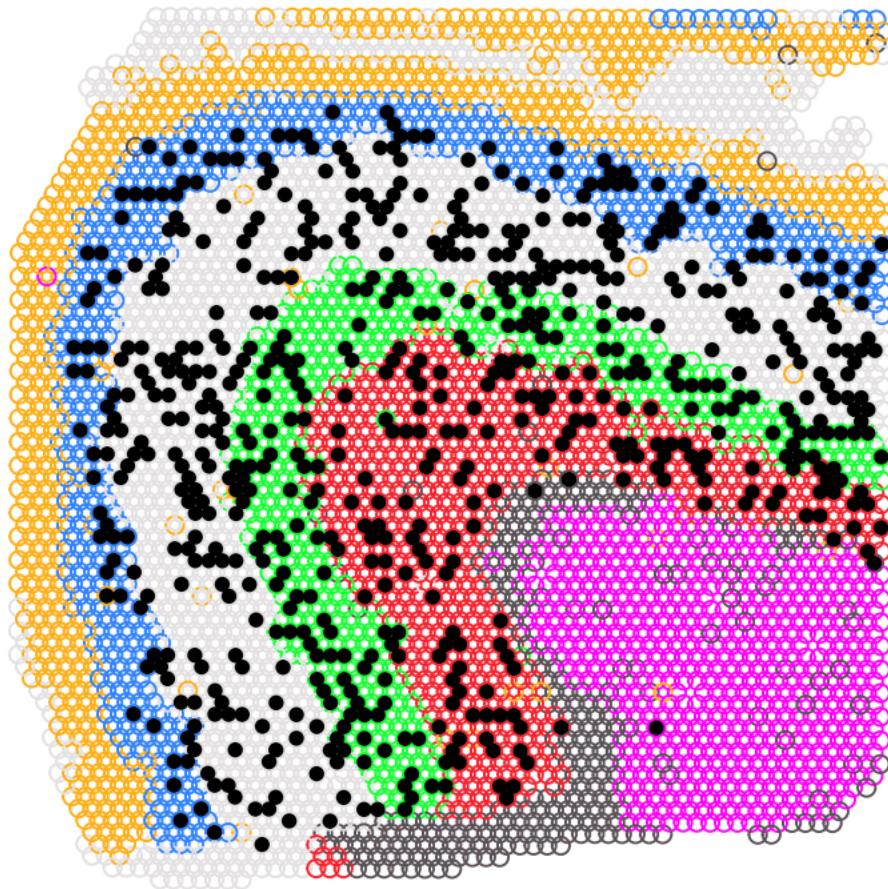
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V12D07-334\_A1



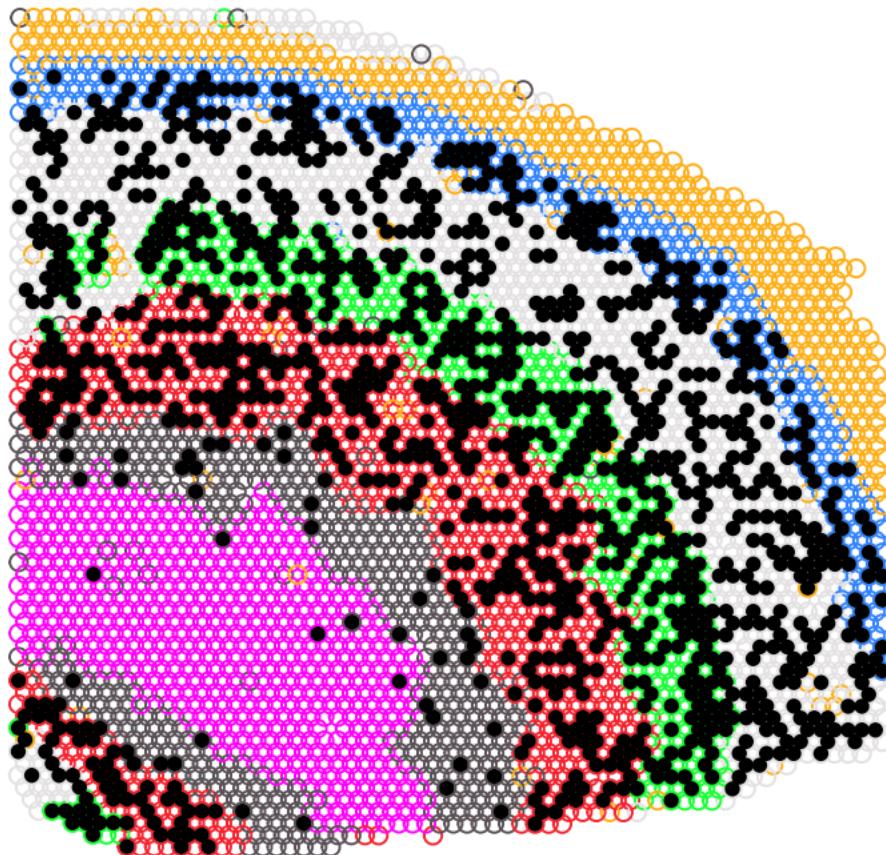
neun\_pos

- FALSE
- TRUE

PRECAST\_07

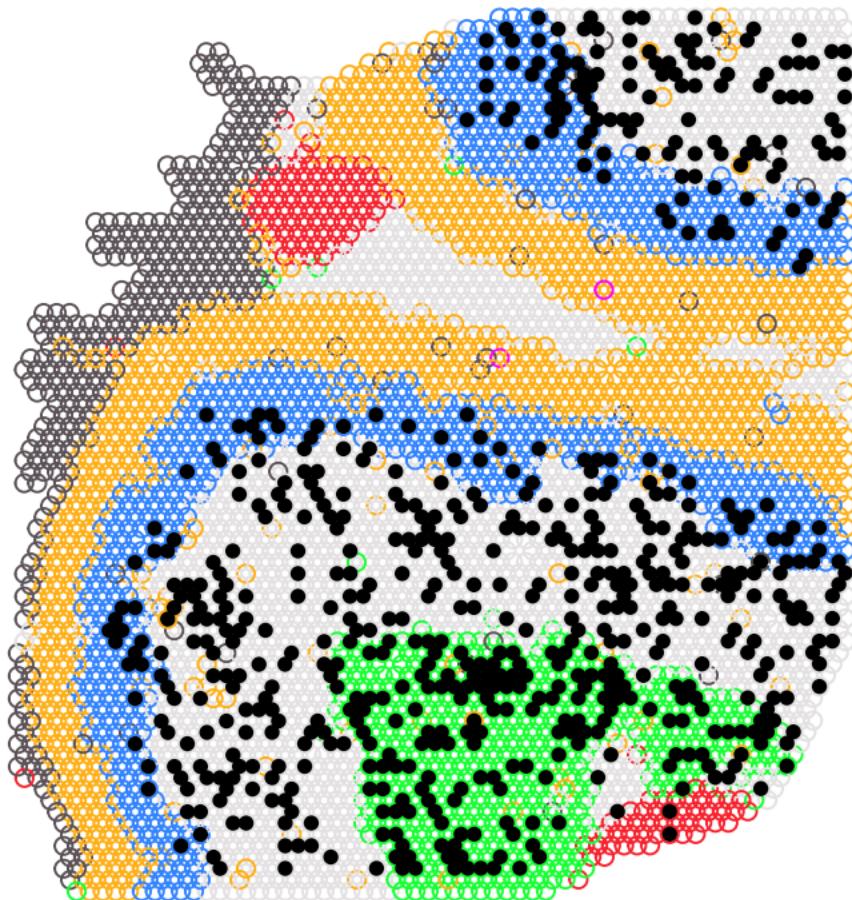
- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V12D07-334\_B1



- neun\_pos**
  - FALSE
  - TRUE
- PRECAST\_07**
  - L1 (spd07)
  - L2/3 (spd06)
  - L3/4 (spd02)
  - L5 (spd05)
  - L6 (spd03)
  - L6/WM (spd01)
  - WM (spd04)

V12D07-334\_C1



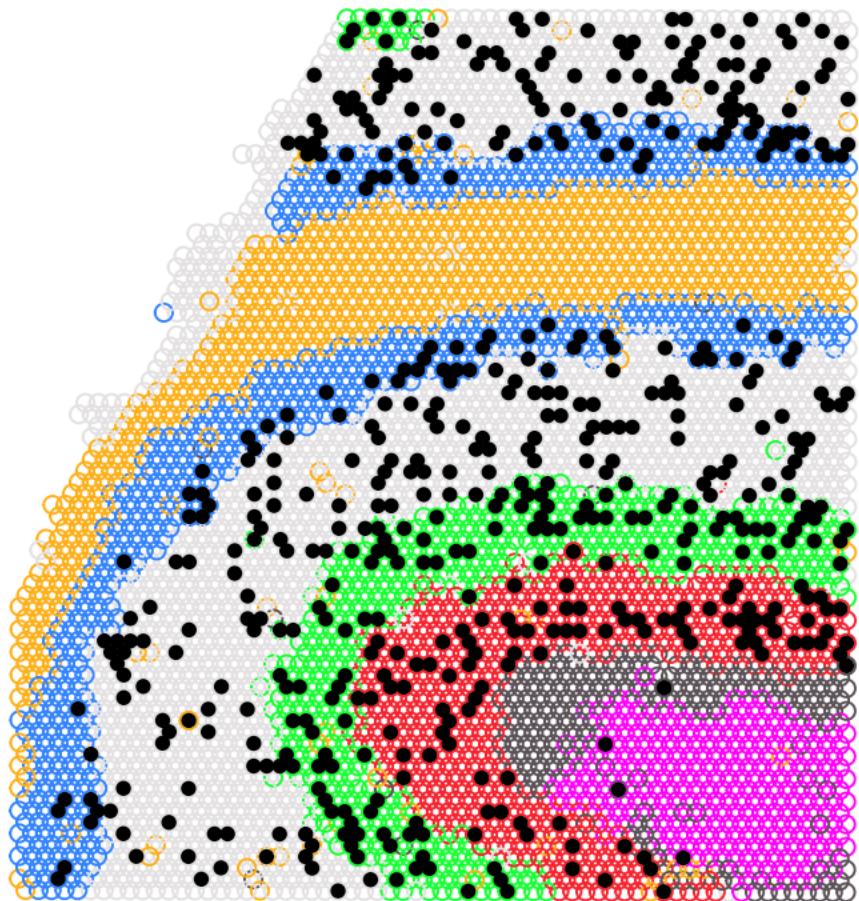
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V12D07-334\_D1



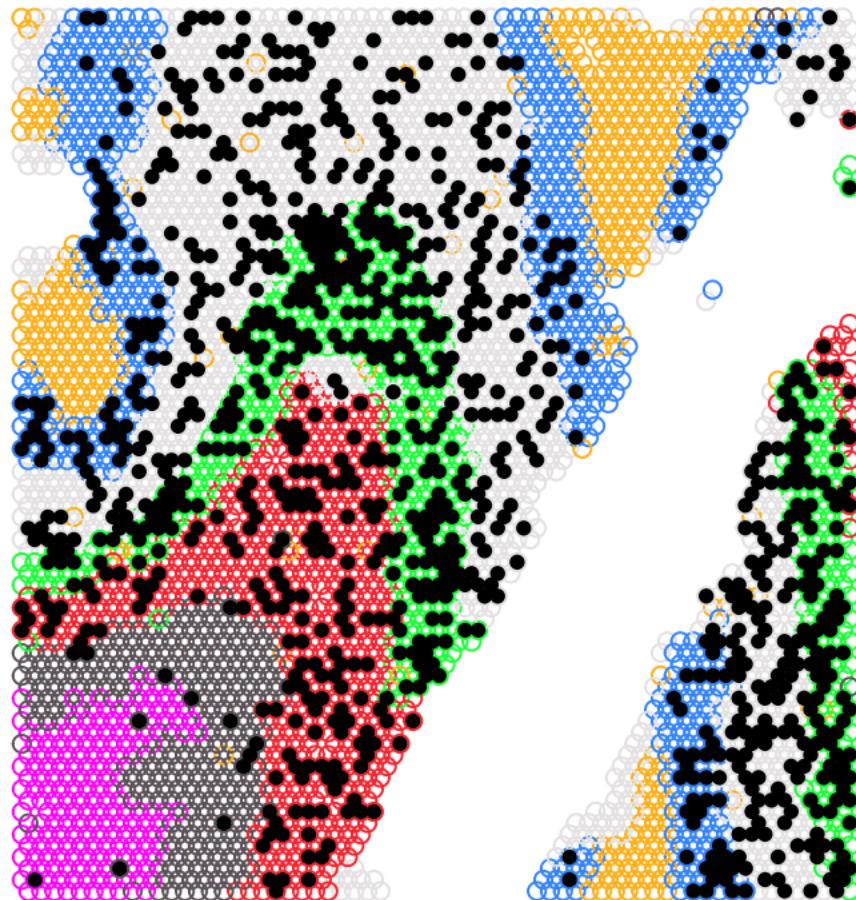
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13M06-279\_A1



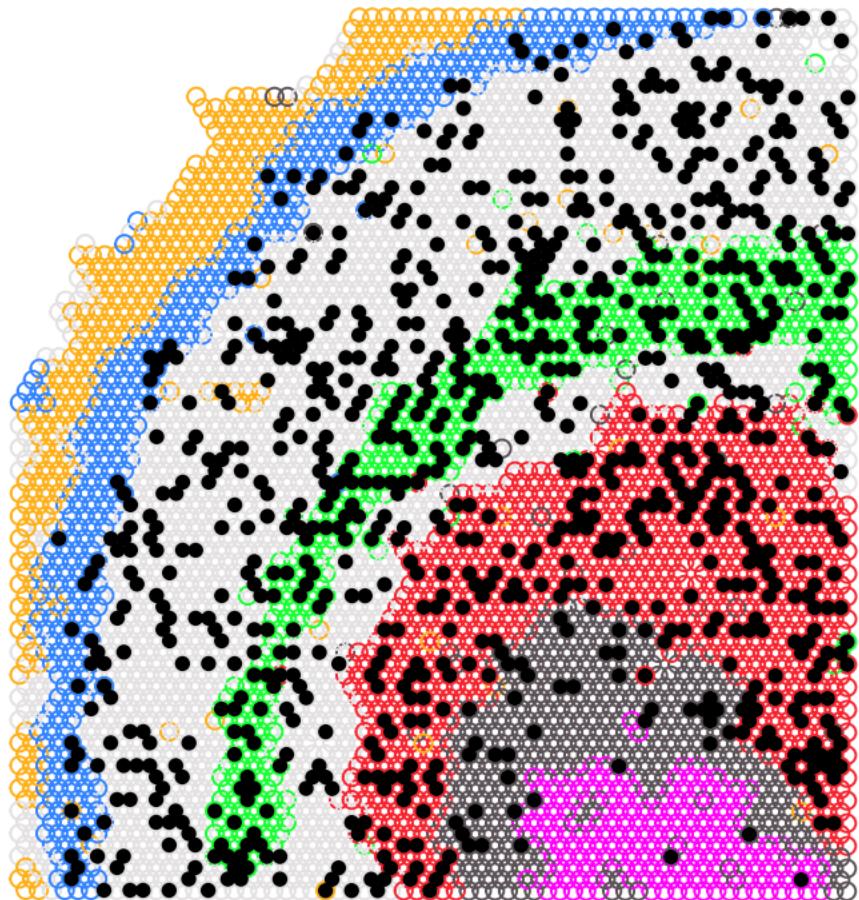
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

V13M06-279\_B1



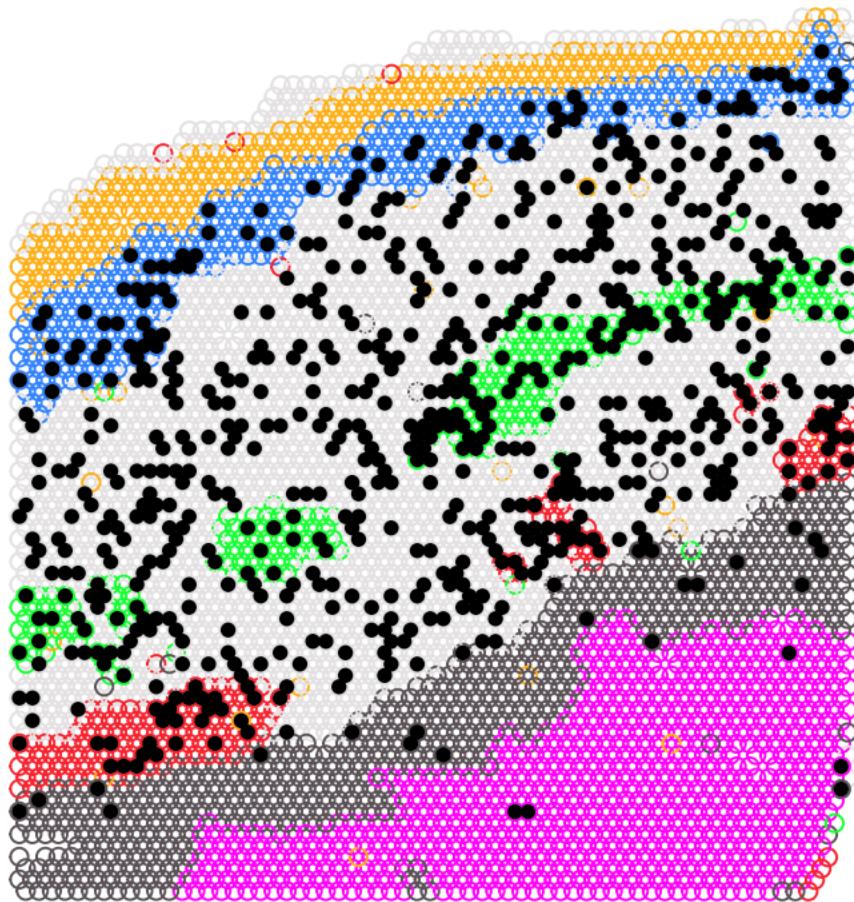
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

V13M06-279\_C1



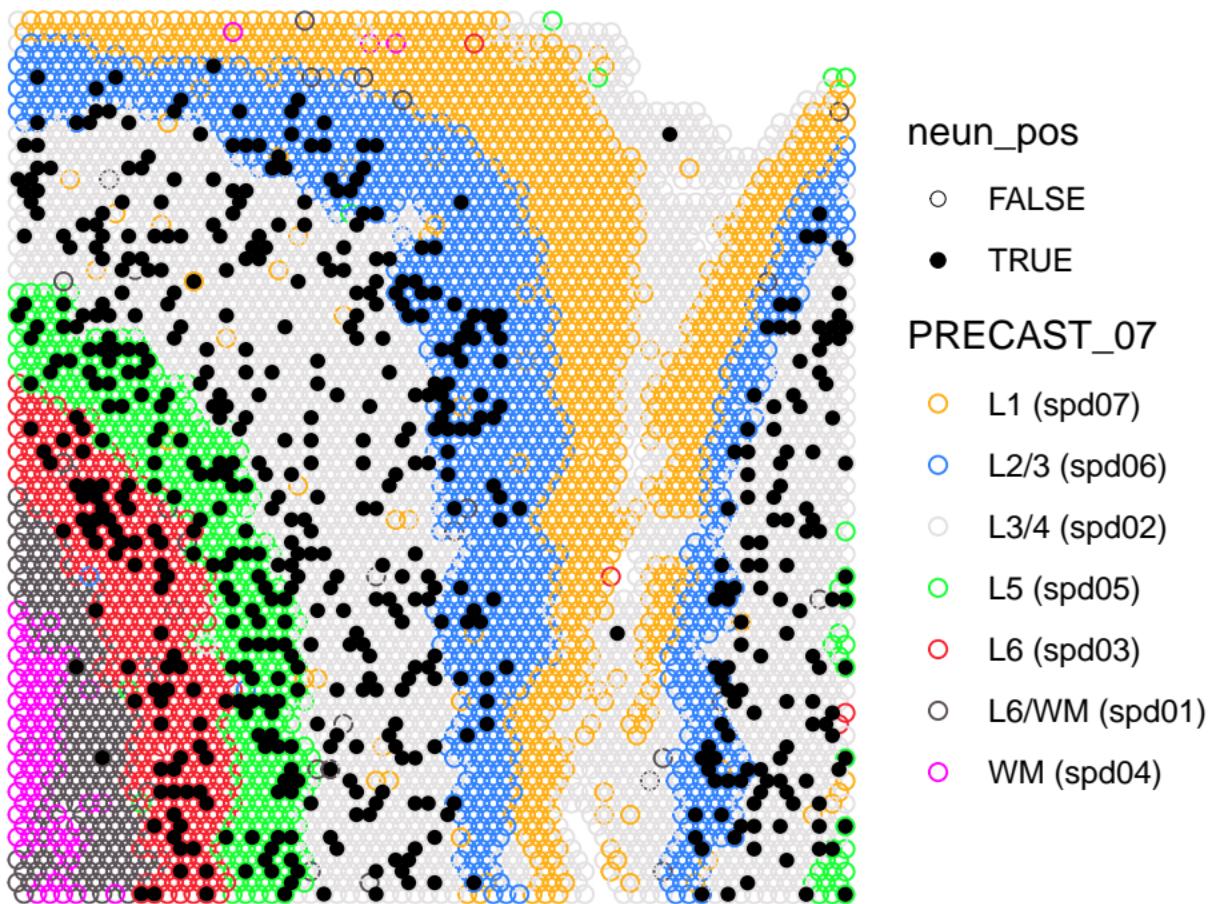
neun\_pos

- FALSE
- TRUE

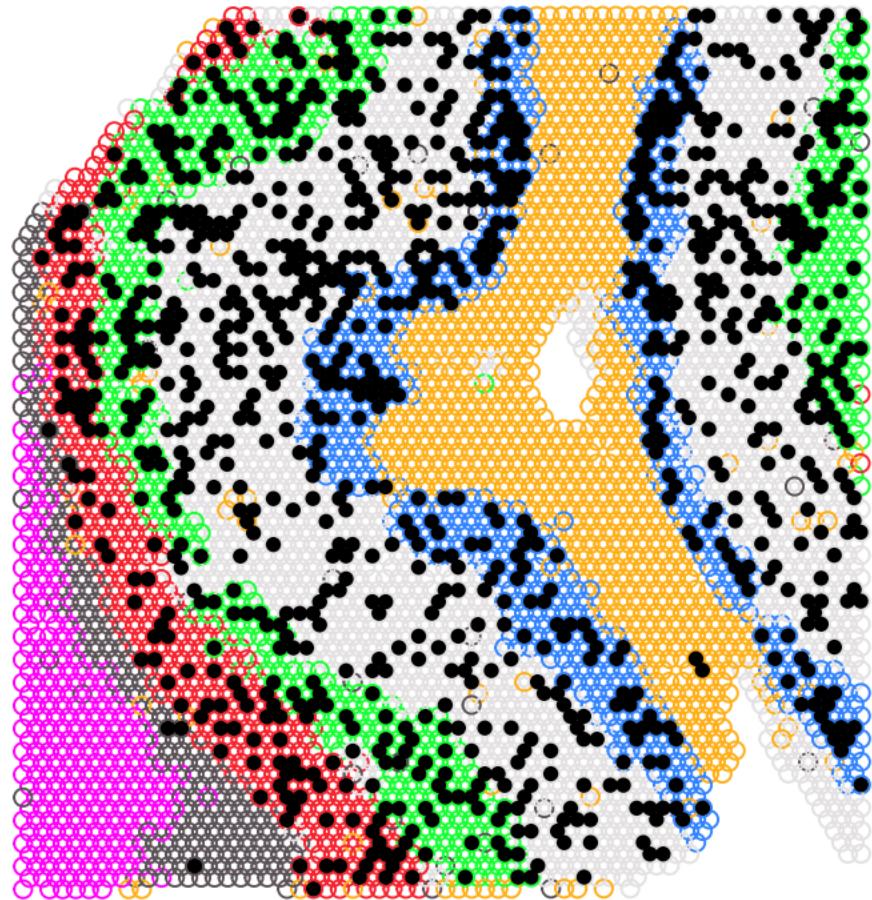
PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13M06-279\_D1



V13M06-280\_A1



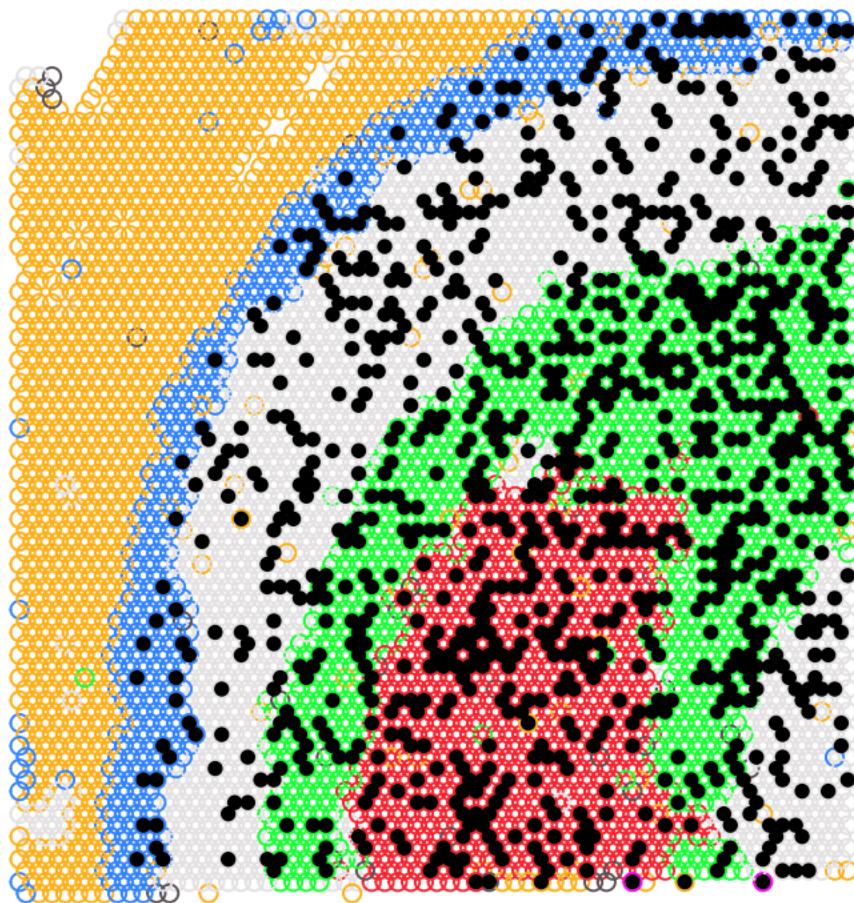
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13M06-280\_B1



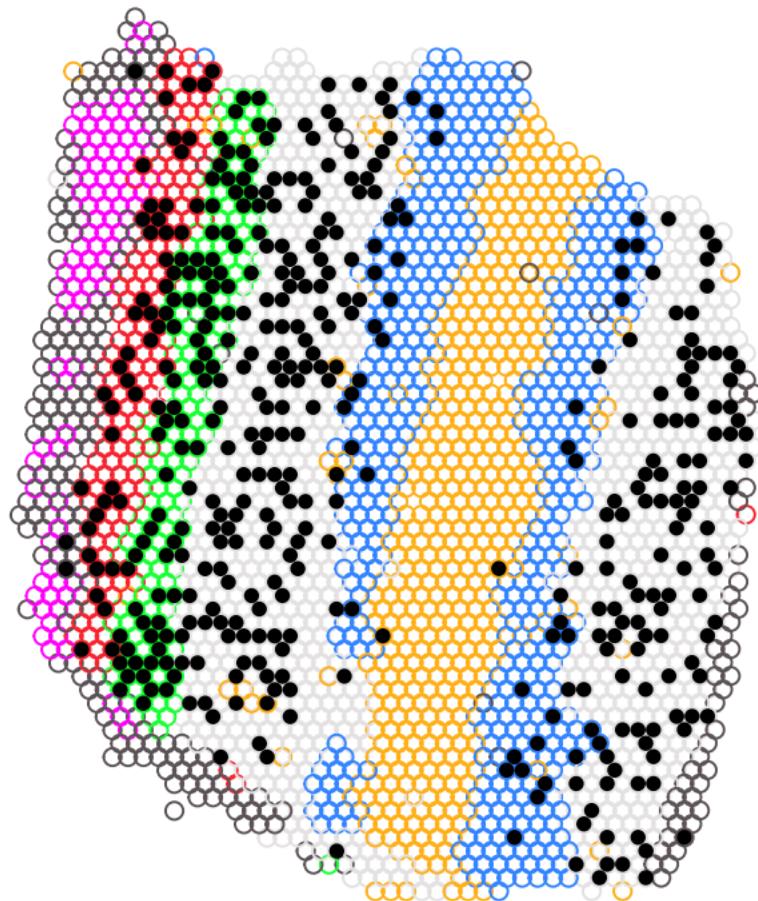
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13M06-280\_C1



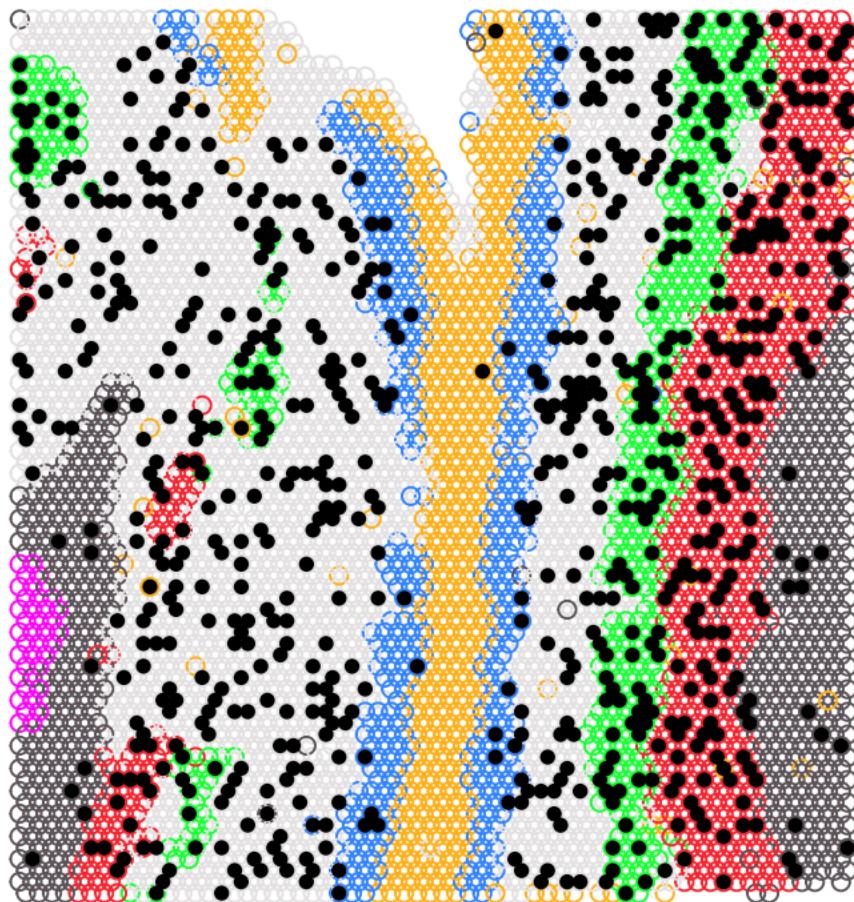
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13M06-280\_D1



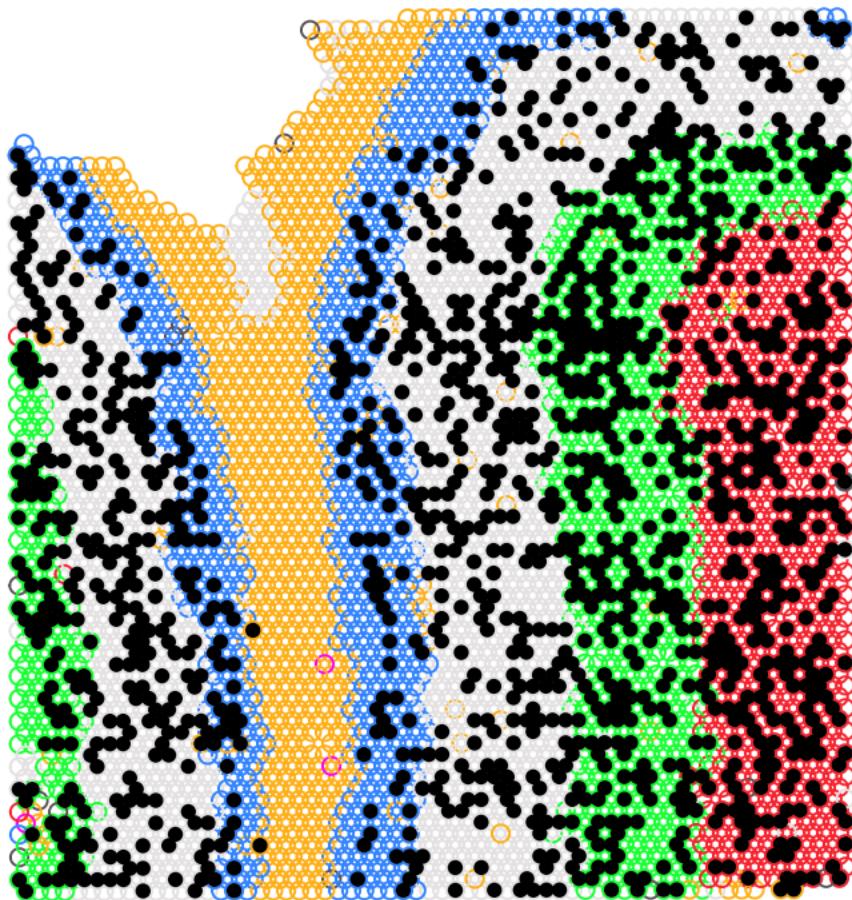
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13M06-281\_A1



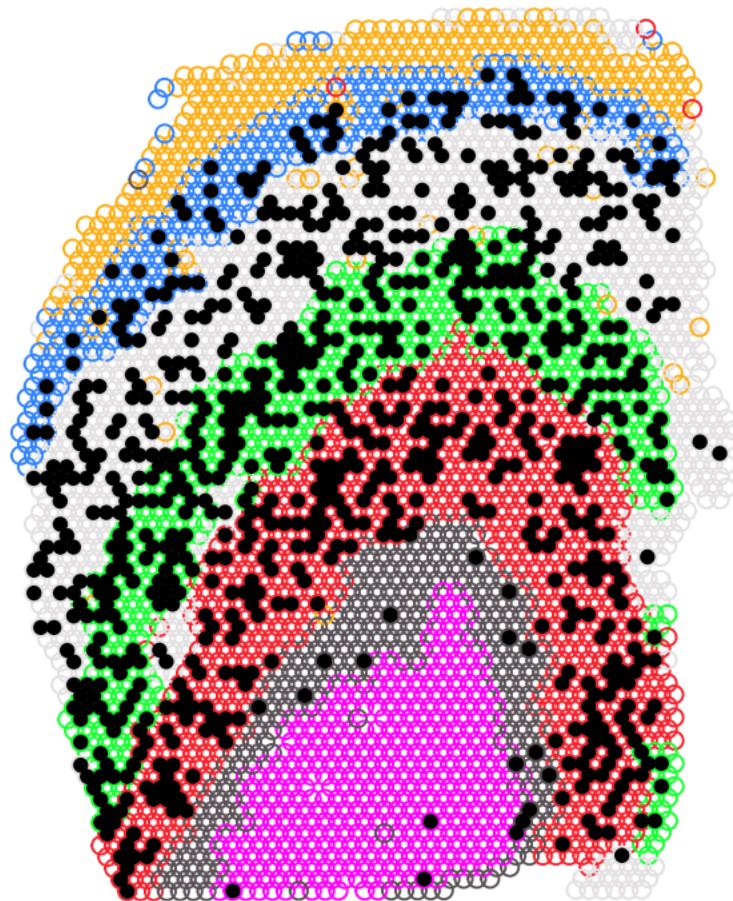
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13M06-281\_B1



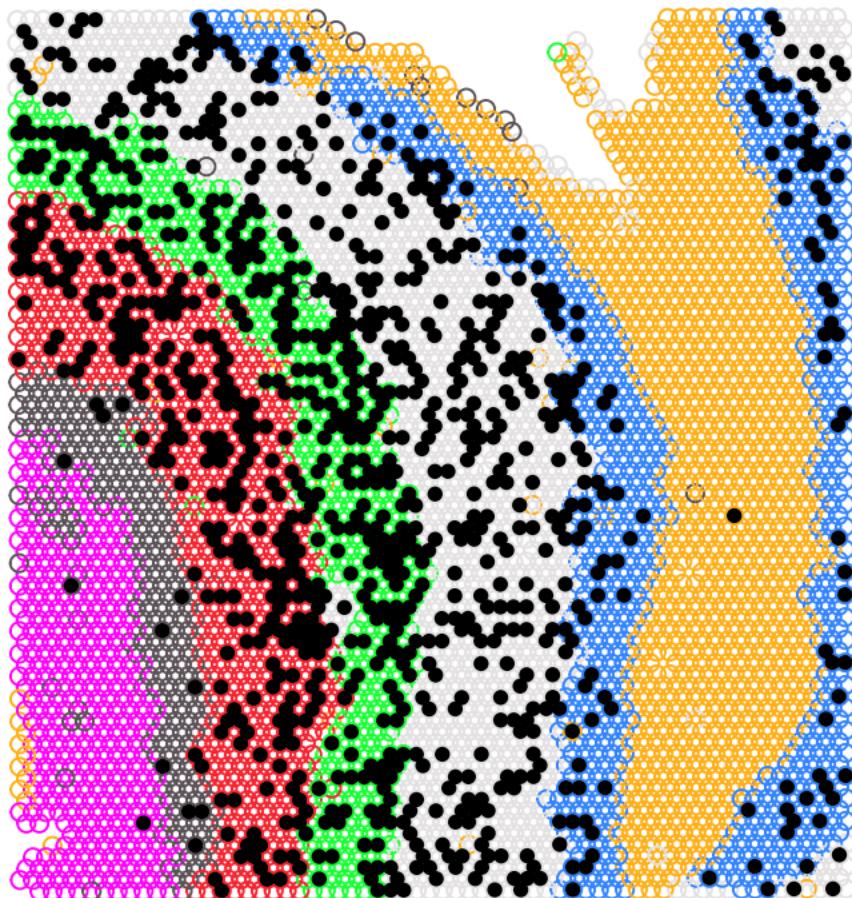
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13M06-281\_C1



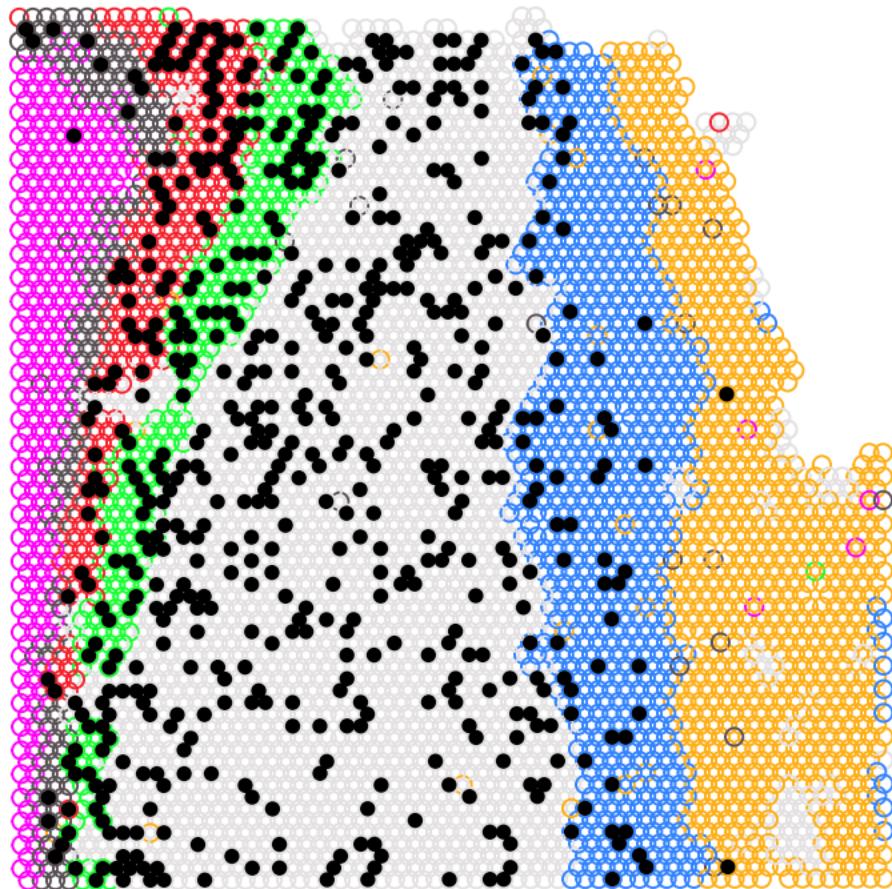
neun\_pos

- FALSE
- TRUE

PRECAST\_07

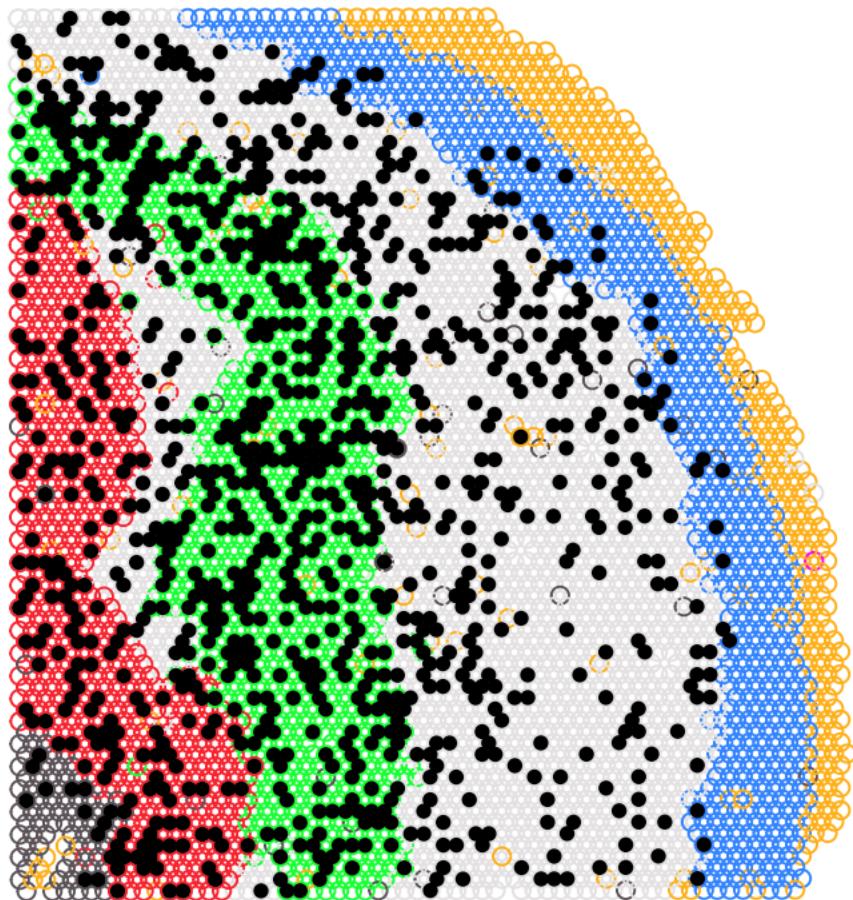
- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13M06–281\_D1



- neun\_pos
  - FALSE
  - TRUE
- PRECAST\_07
  - L1 (spd07)
  - L2/3 (spd06)
  - L3/4 (spd02)
  - L5 (spd05)
  - L6 (spd03)
  - L6/WM (spd01)
  - WM (spd04)

V13M06-282\_A1



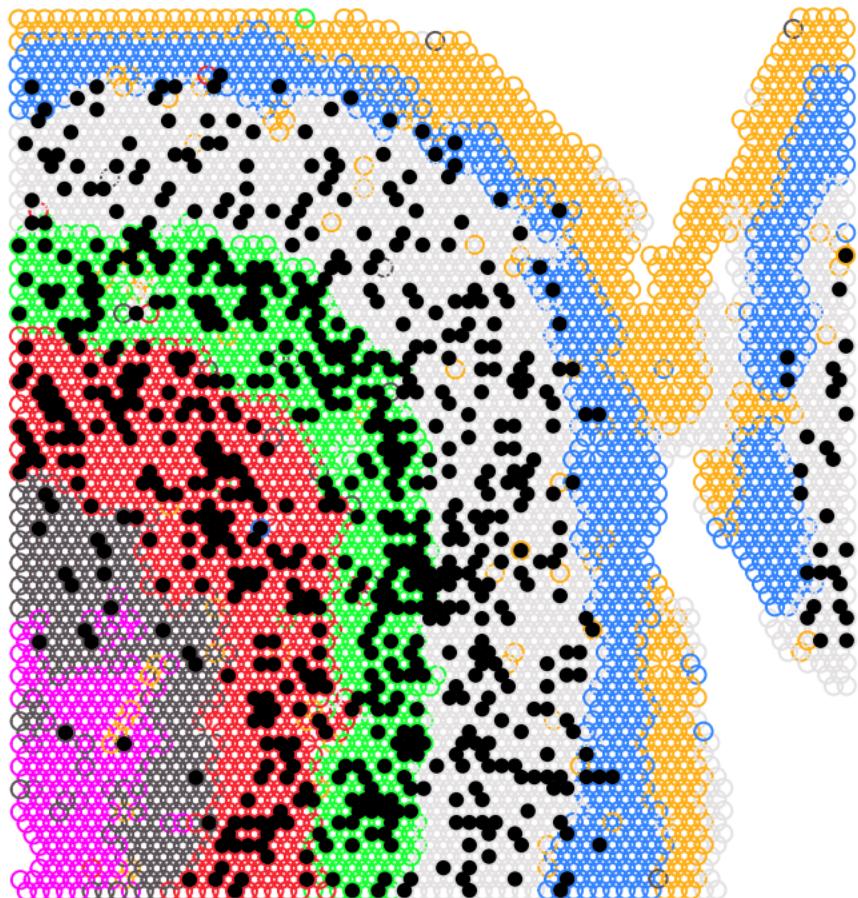
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13M06-282\_B1



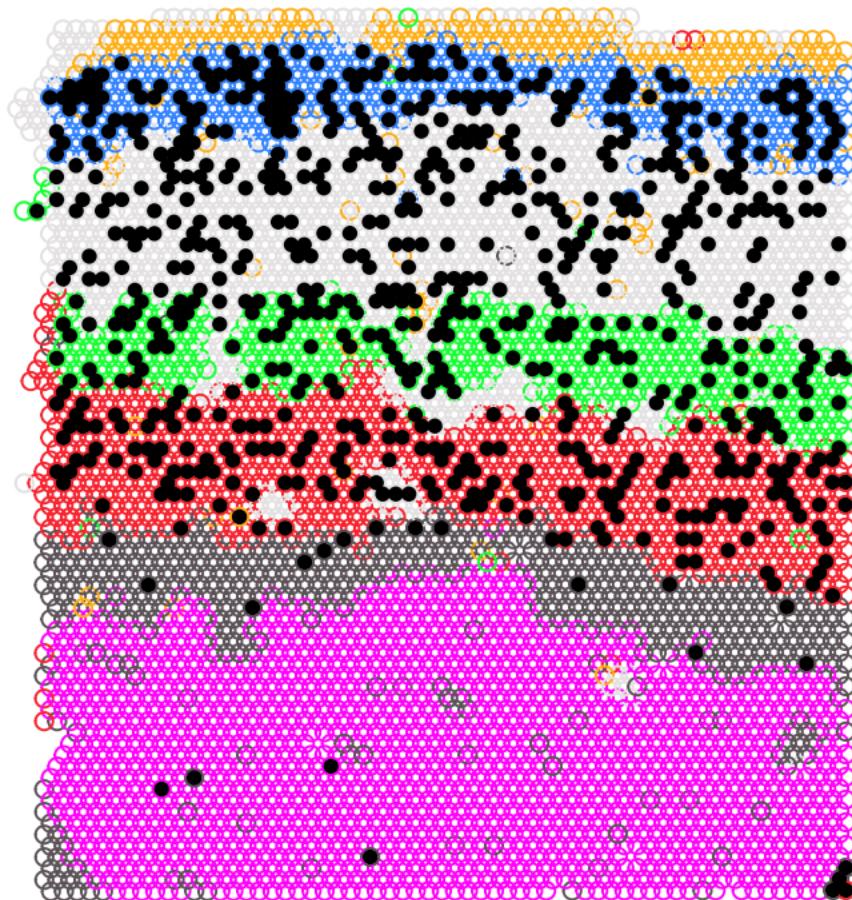
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13M06-282\_C1



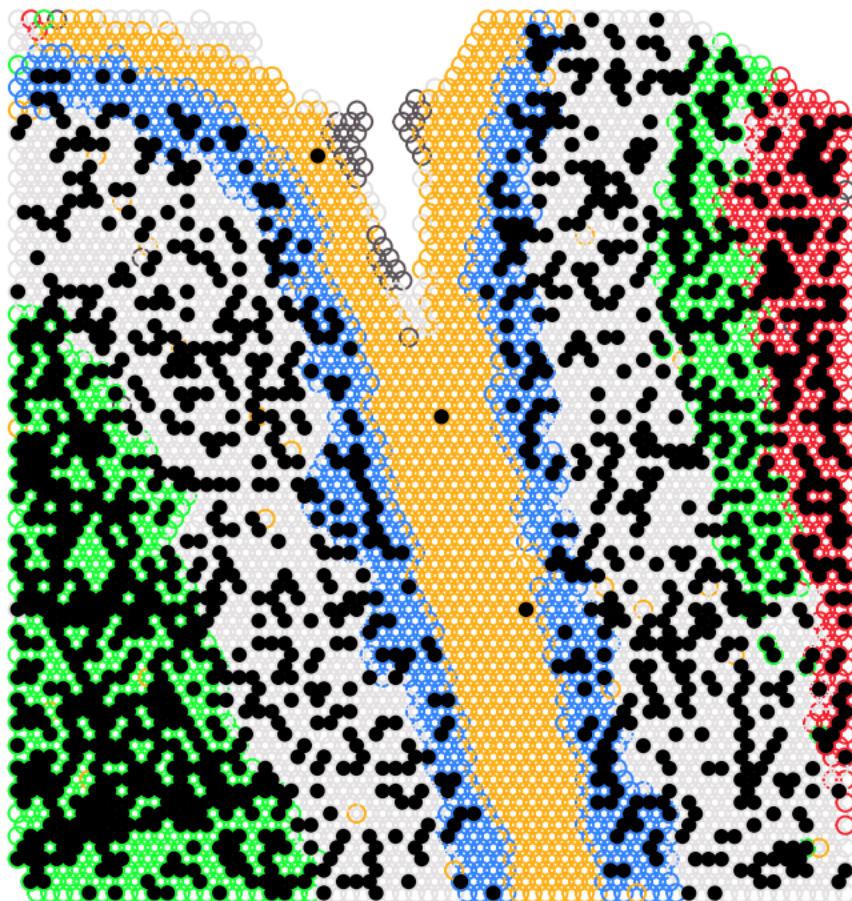
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13M06-282\_D1



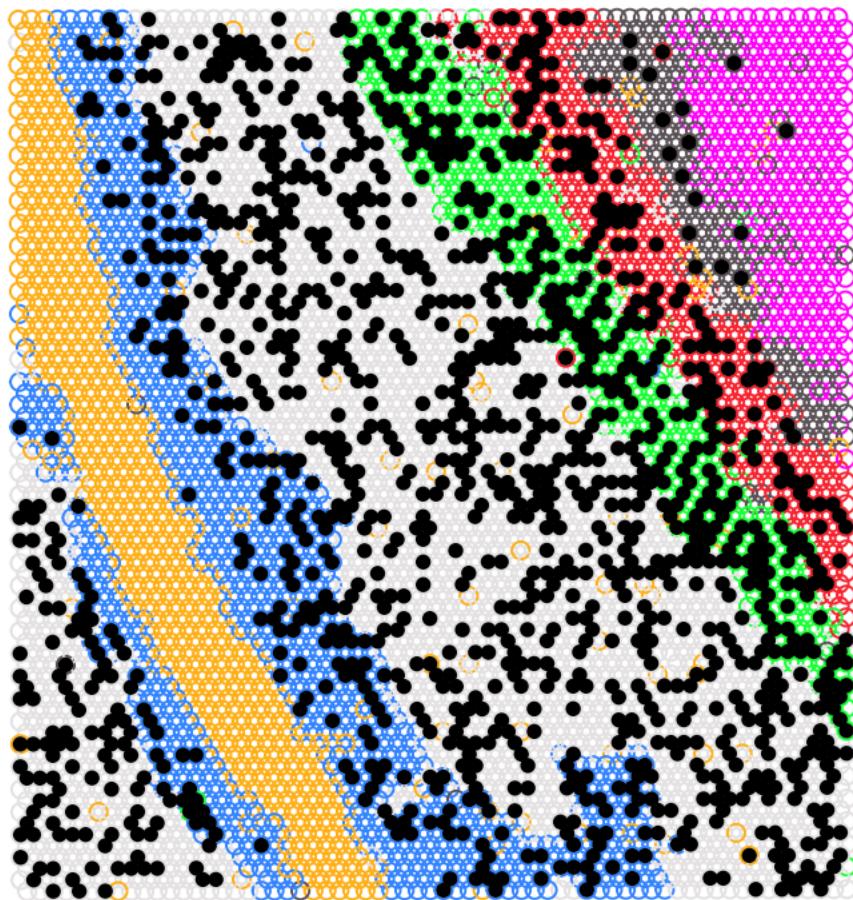
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

V13F27-293\_A1



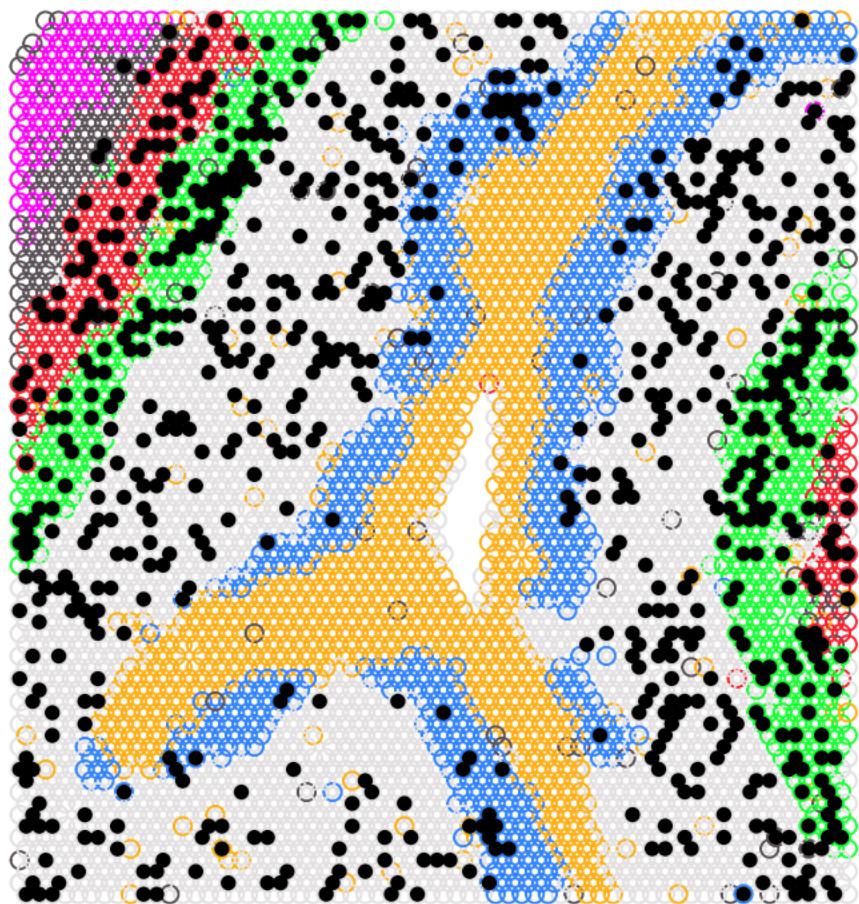
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13F27-293\_B1



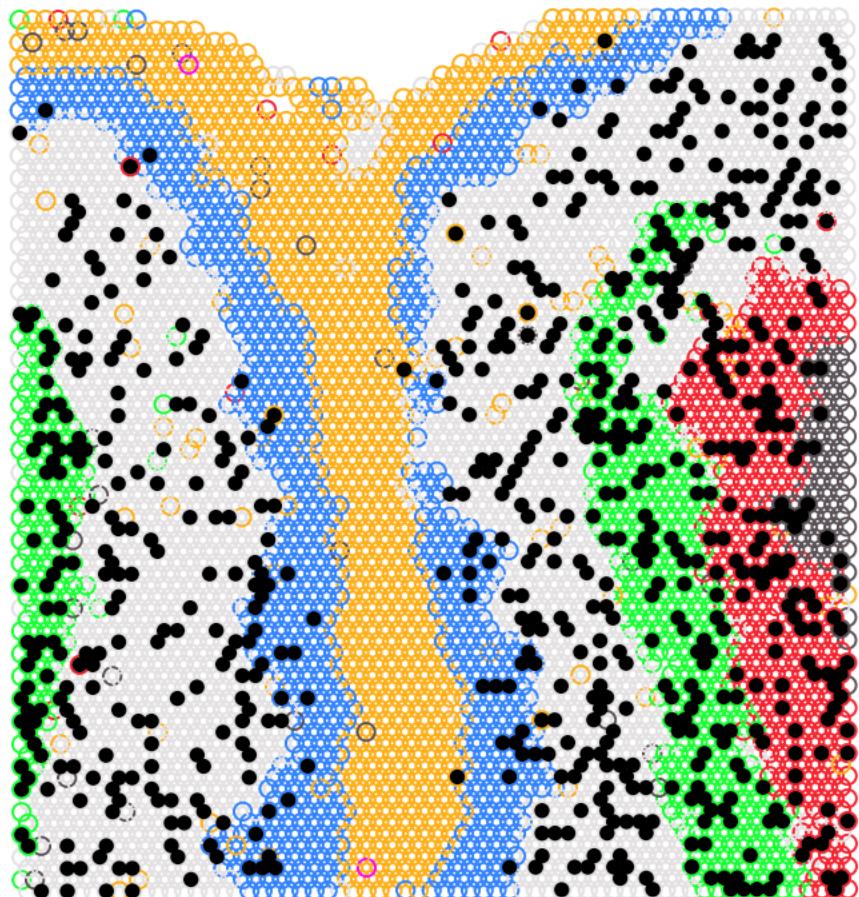
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13F27-293\_C1



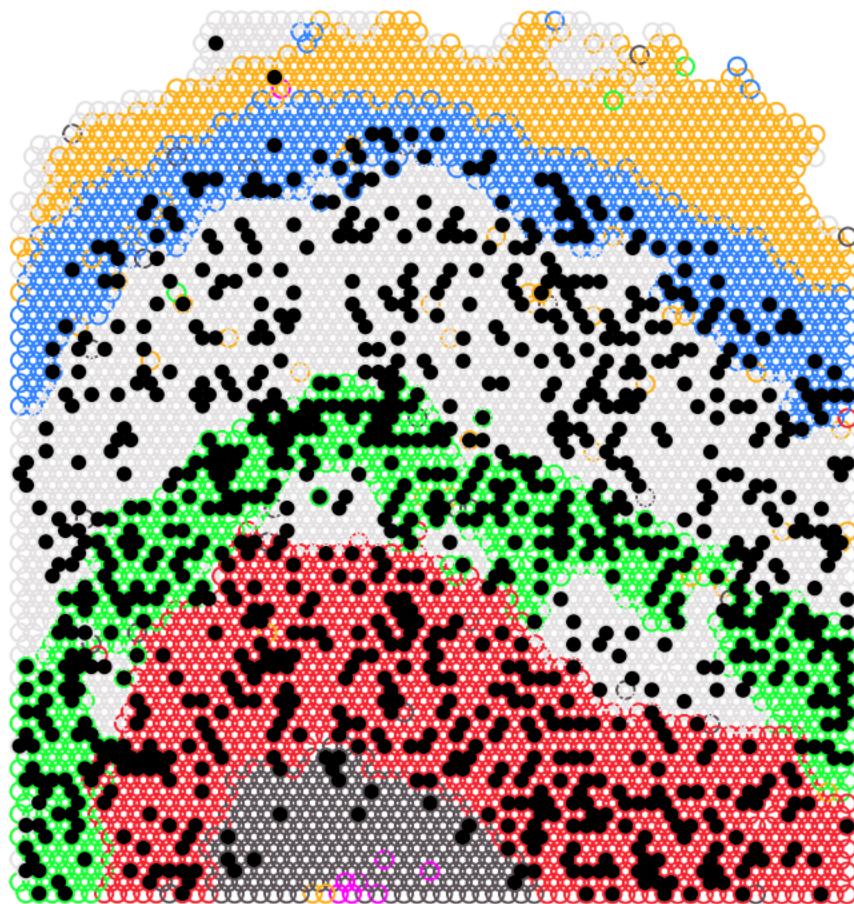
neun\_pos

- FALSE
- TRUE

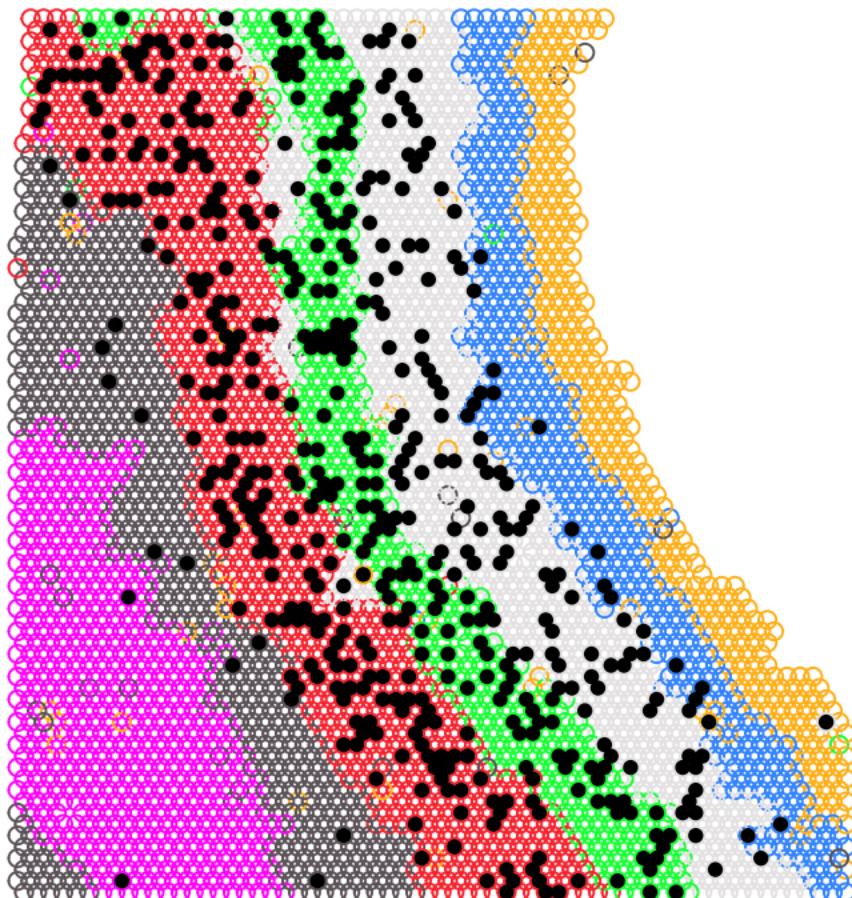
PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

V13F27-293\_D1



V13F27-294\_A1



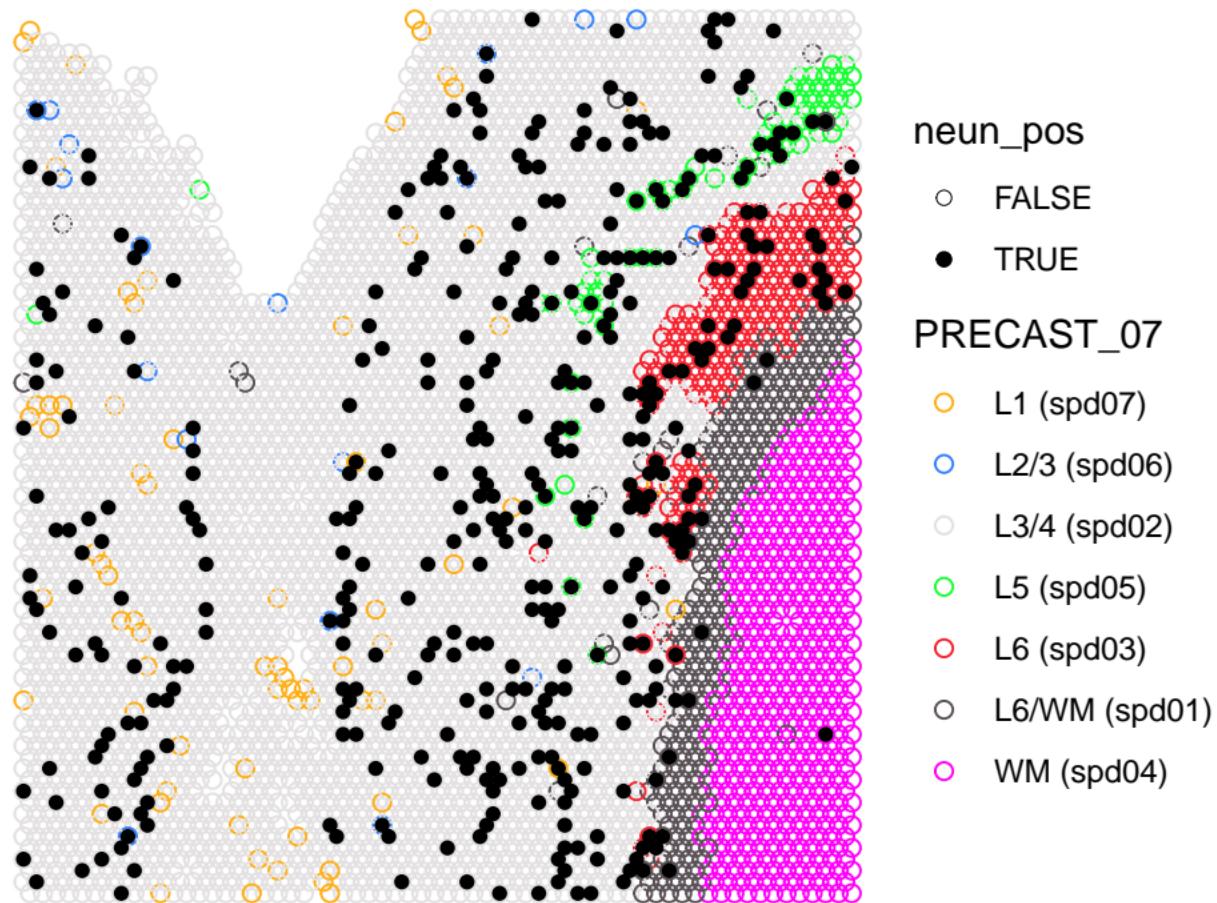
neun\_pos

- FALSE
- TRUE

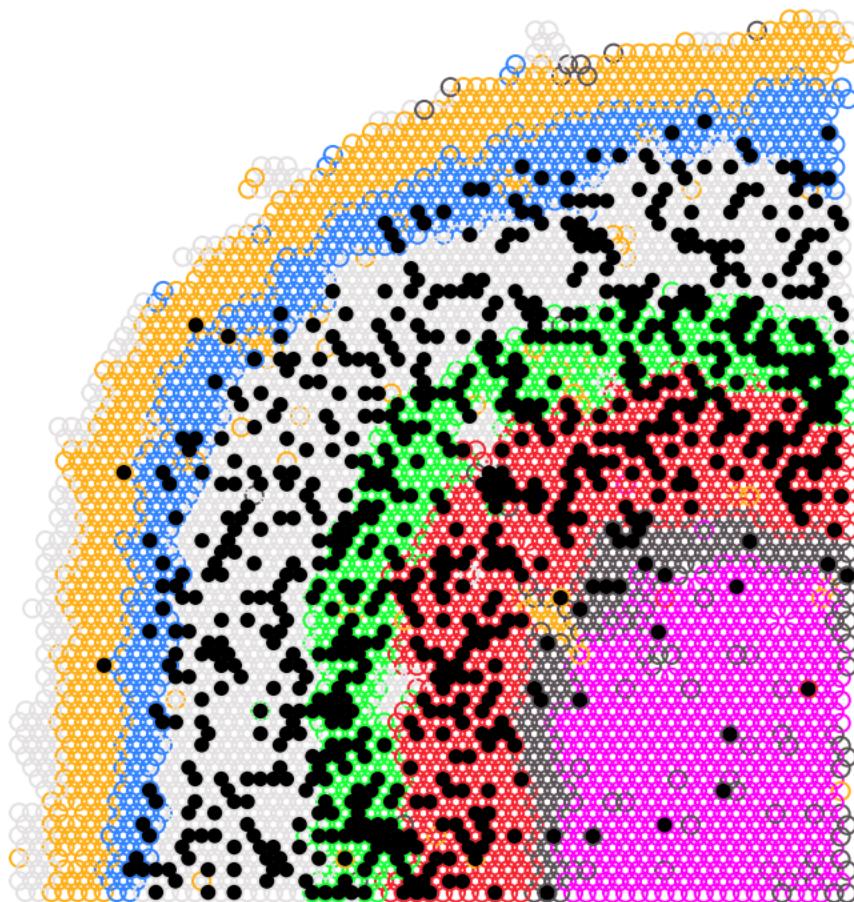
PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13F27-294\_B1



V13F27-294\_C1



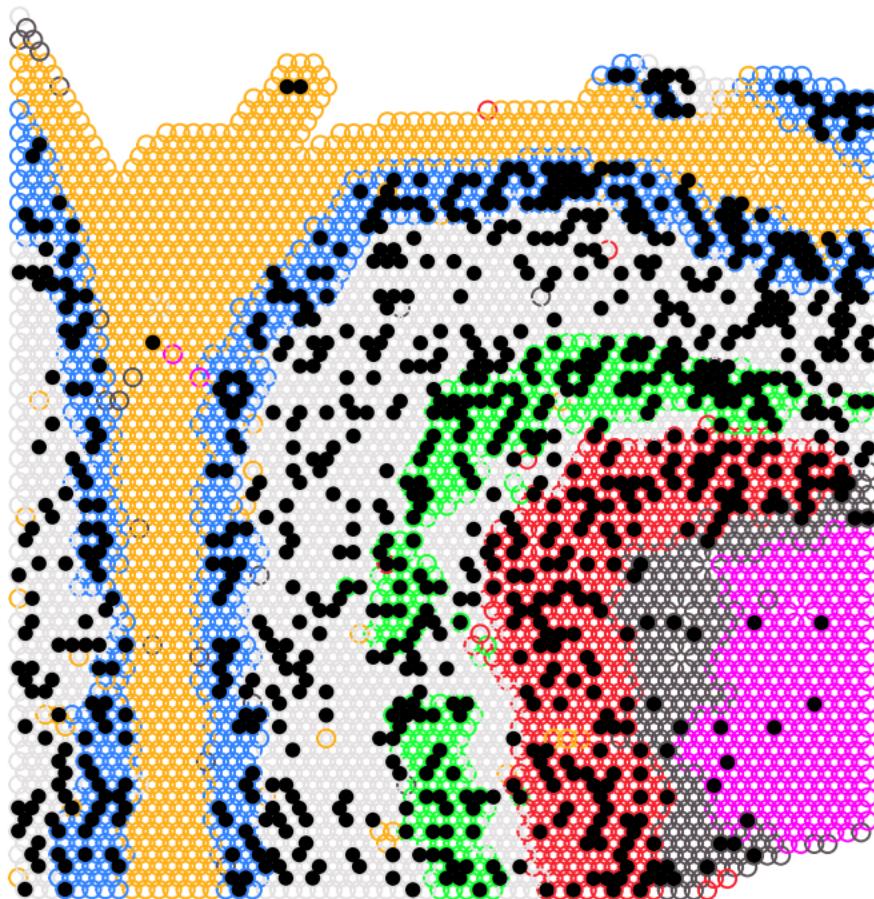
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13F27-294\_D1



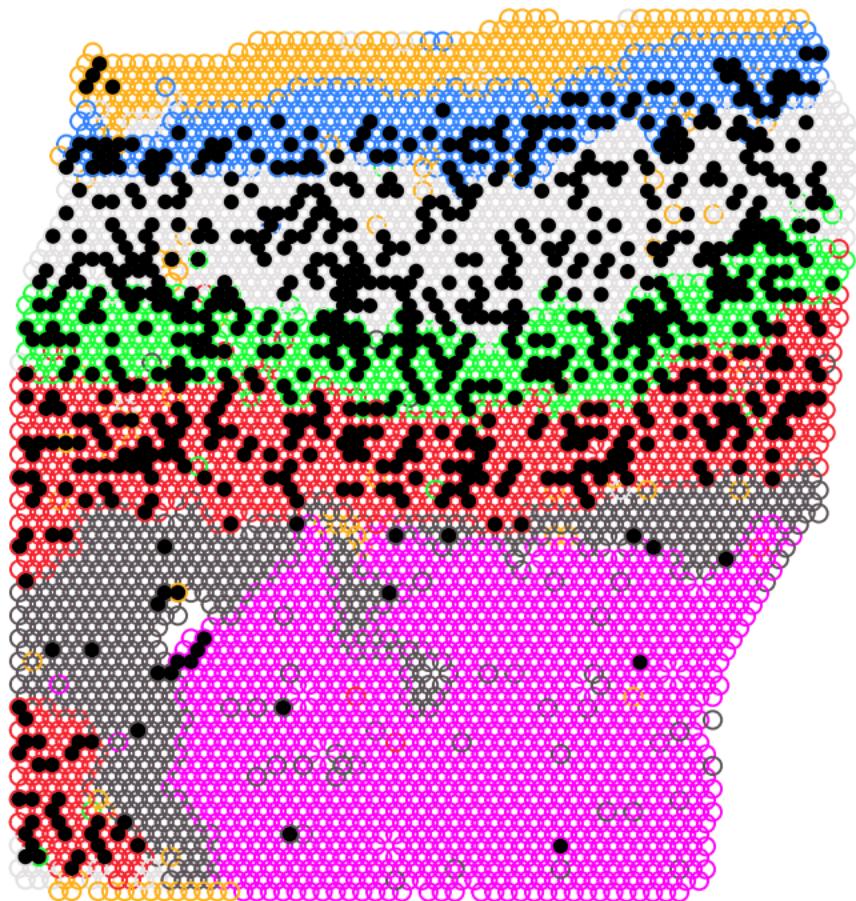
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

V13F27-295\_A1



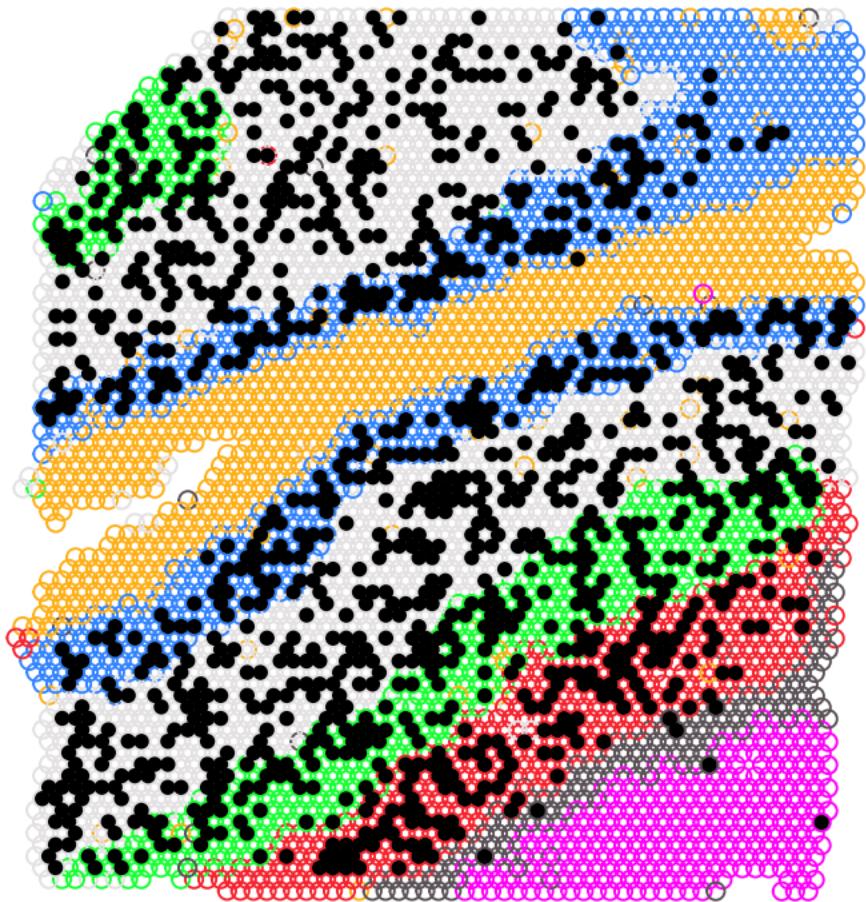
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13F27-295\_B1



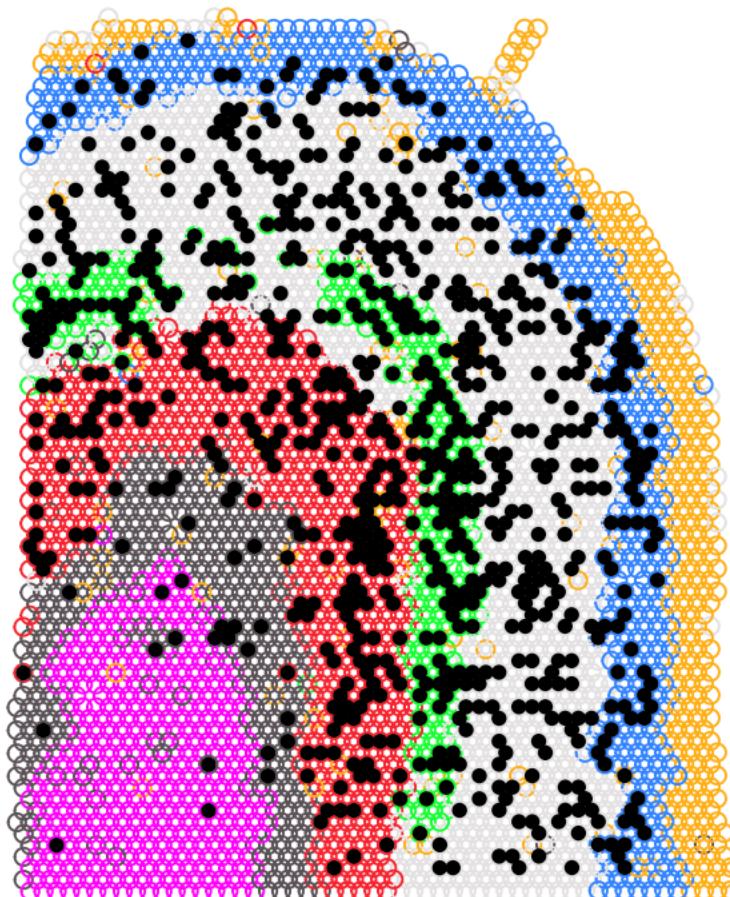
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13F27-295\_C1



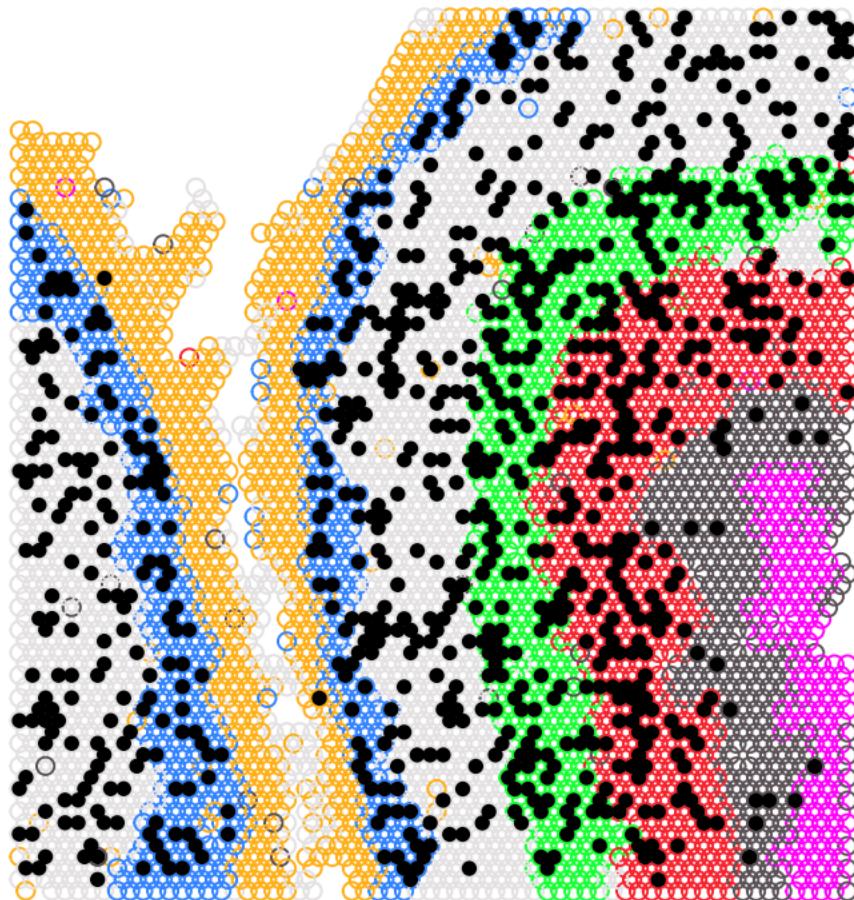
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

V13F27-295\_D1



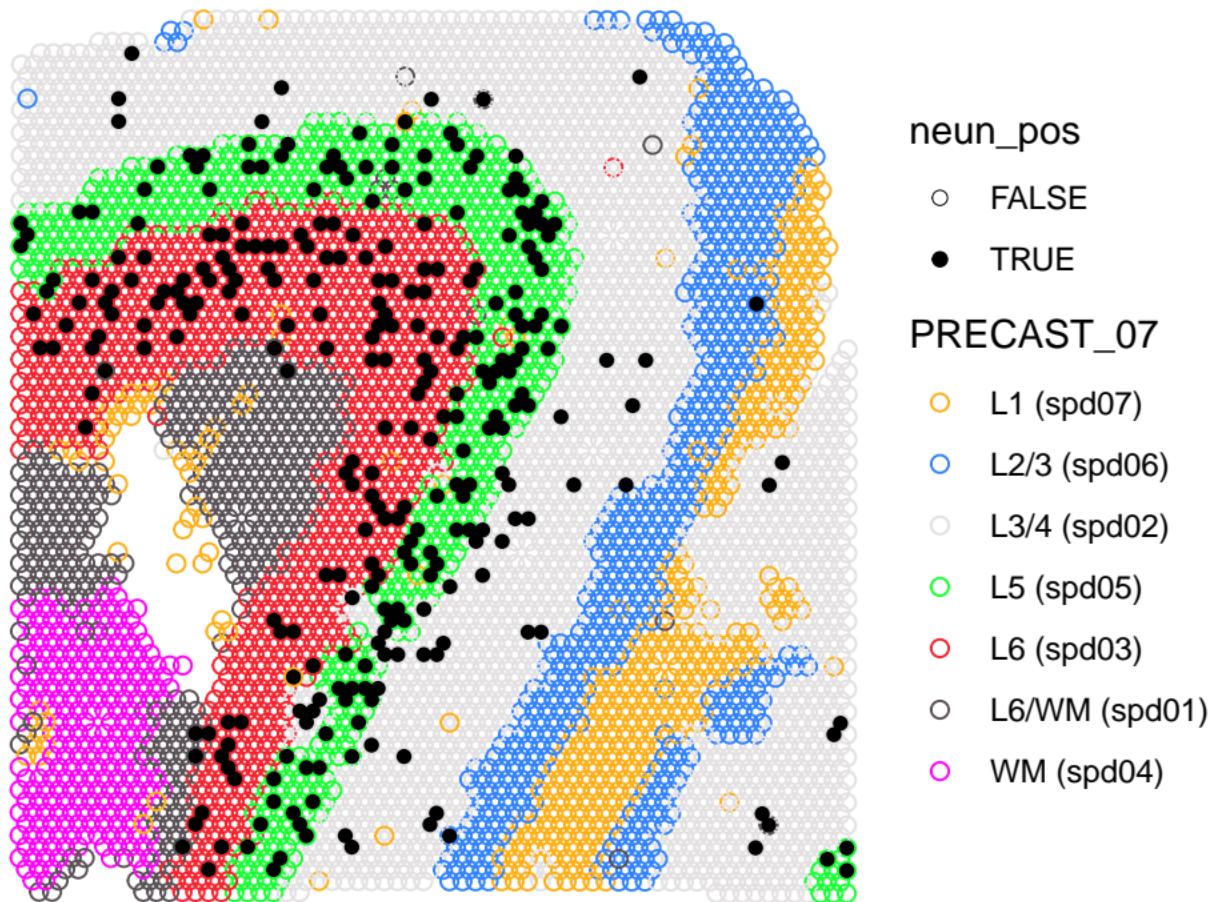
neun\_pos

- FALSE
- TRUE

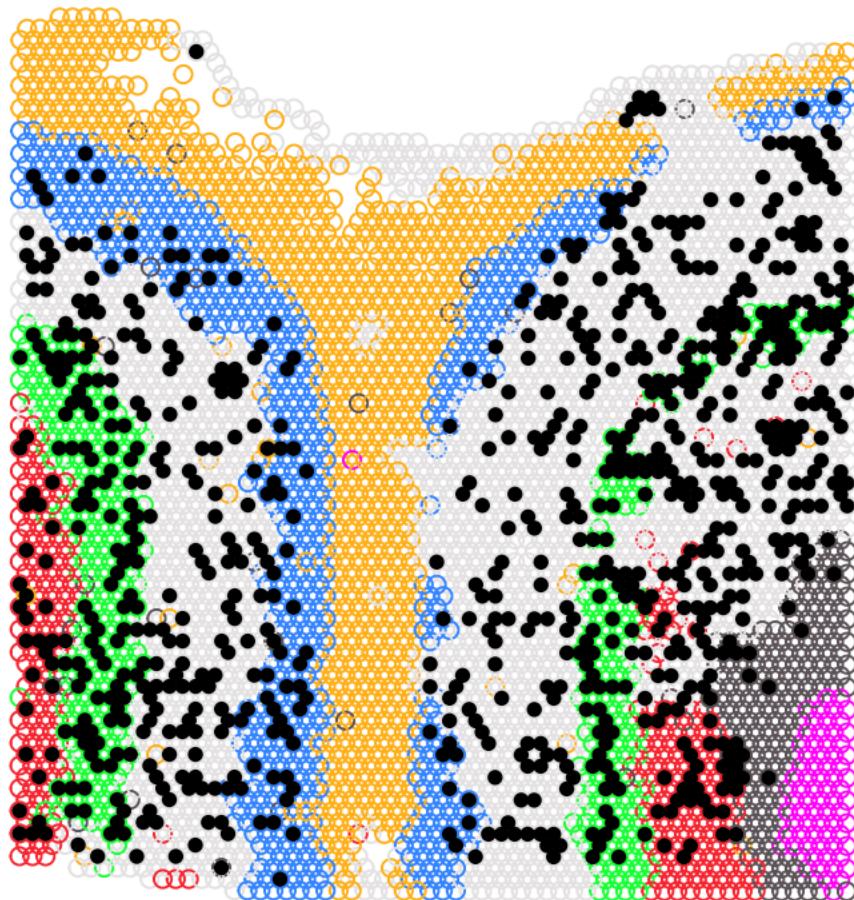
PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13F27-296\_A1



V13F27-296\_B1



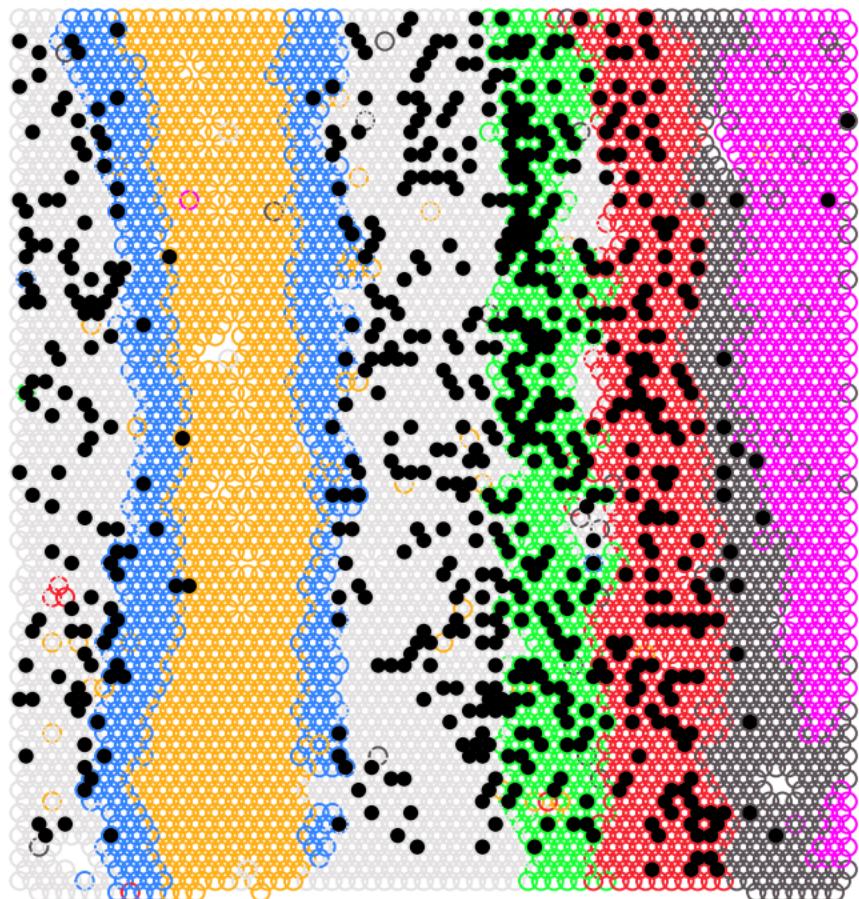
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13F27-296\_C1



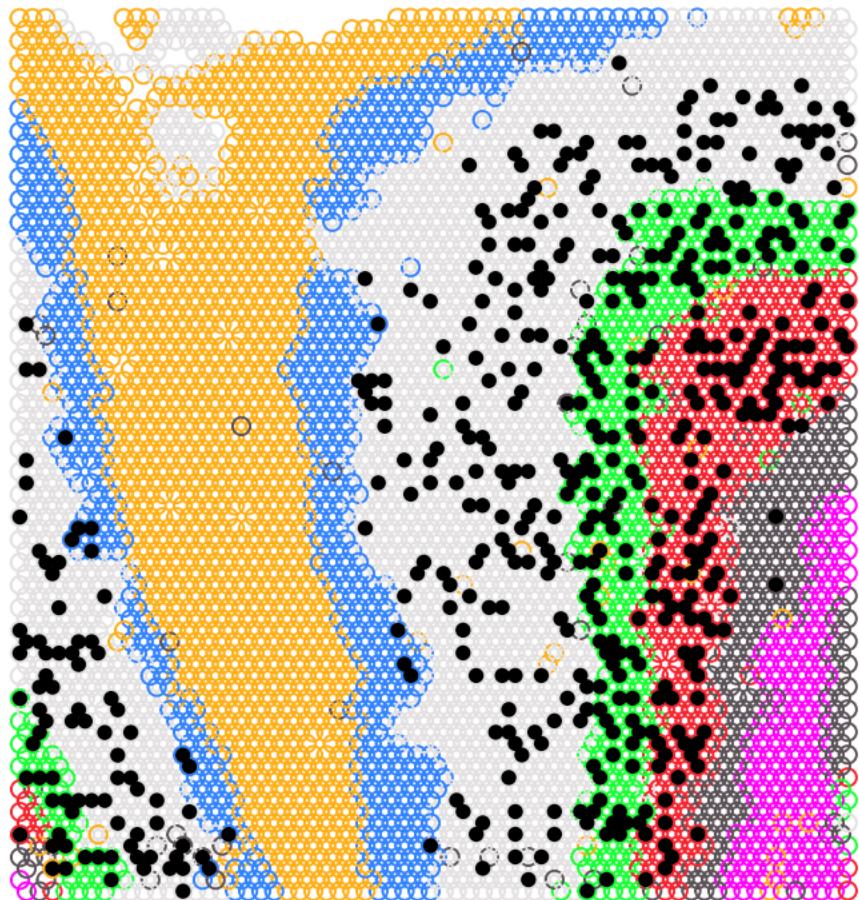
**neun\_pos**

- FALSE
- TRUE

**PRECAST\_07**

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

V13F27-296\_D1



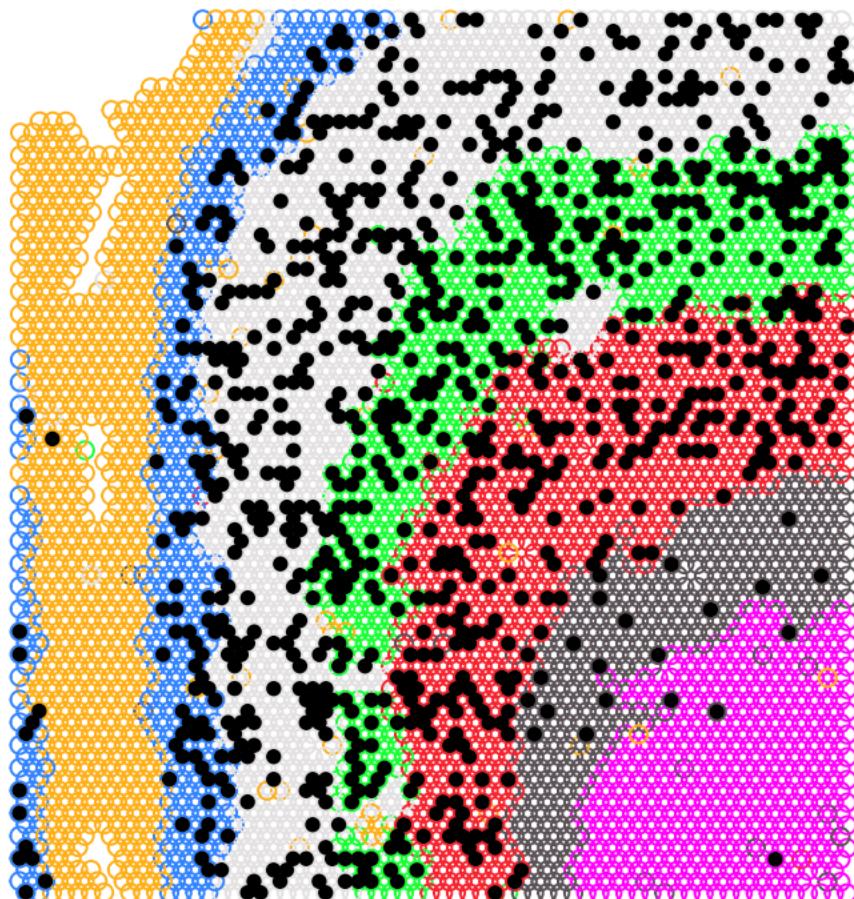
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13M06-340\_A1



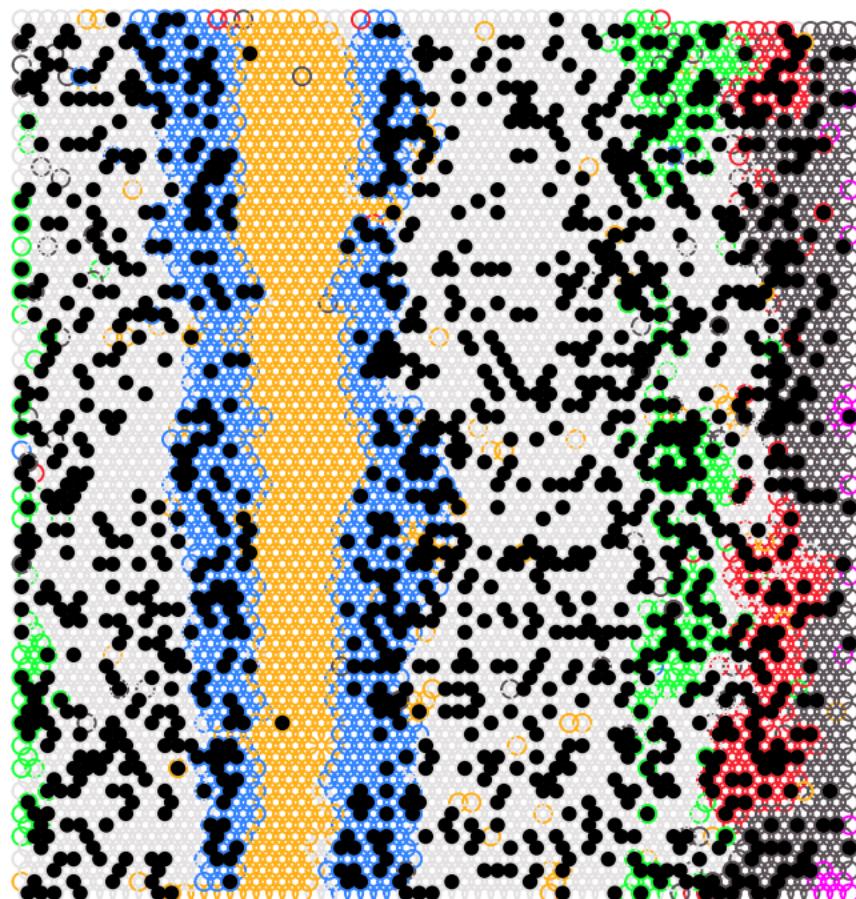
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13M06-340\_B1



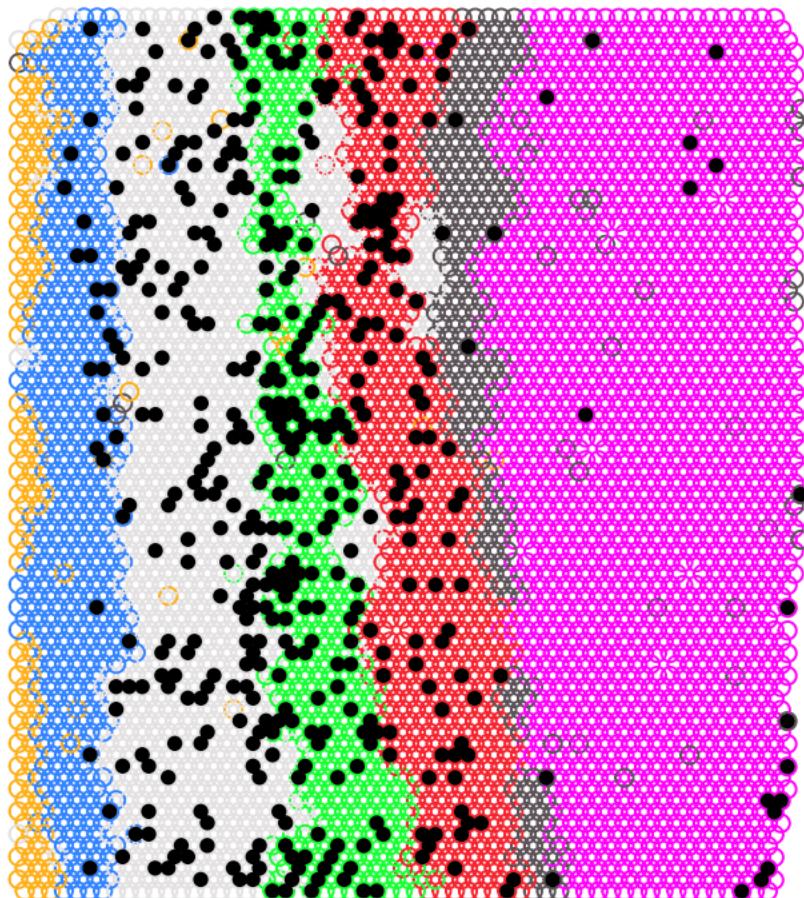
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13M06-340\_C1



## neun\_pos

- FALSE
- TRUE

## PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13M06-340\_D1



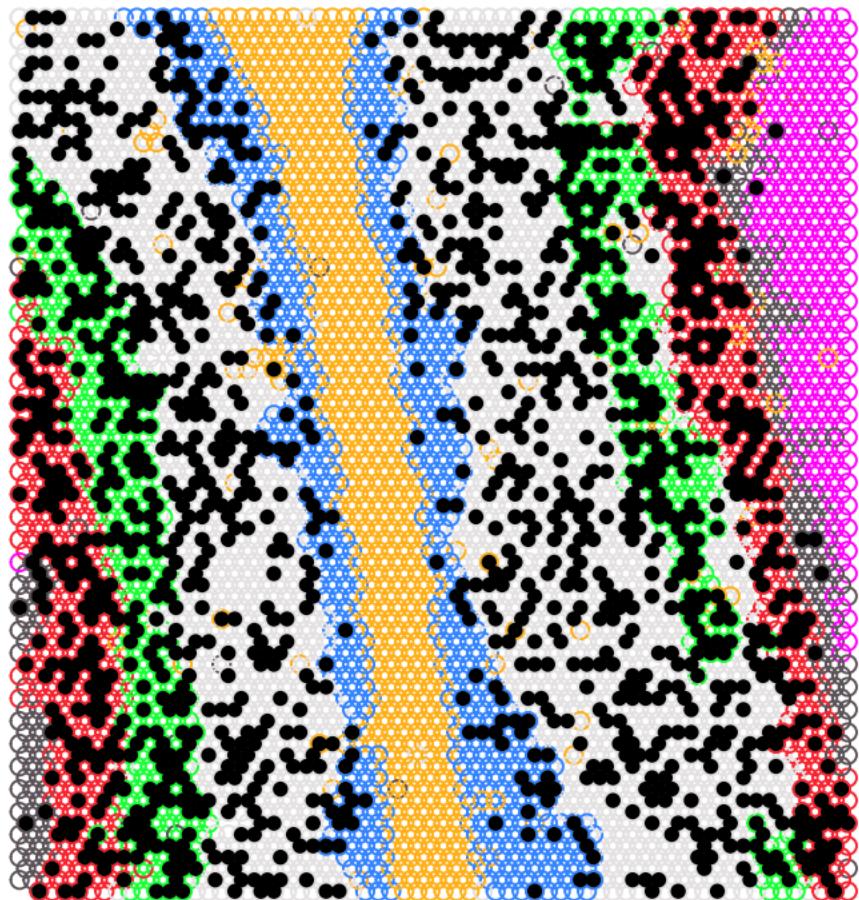
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13M06-342\_A1



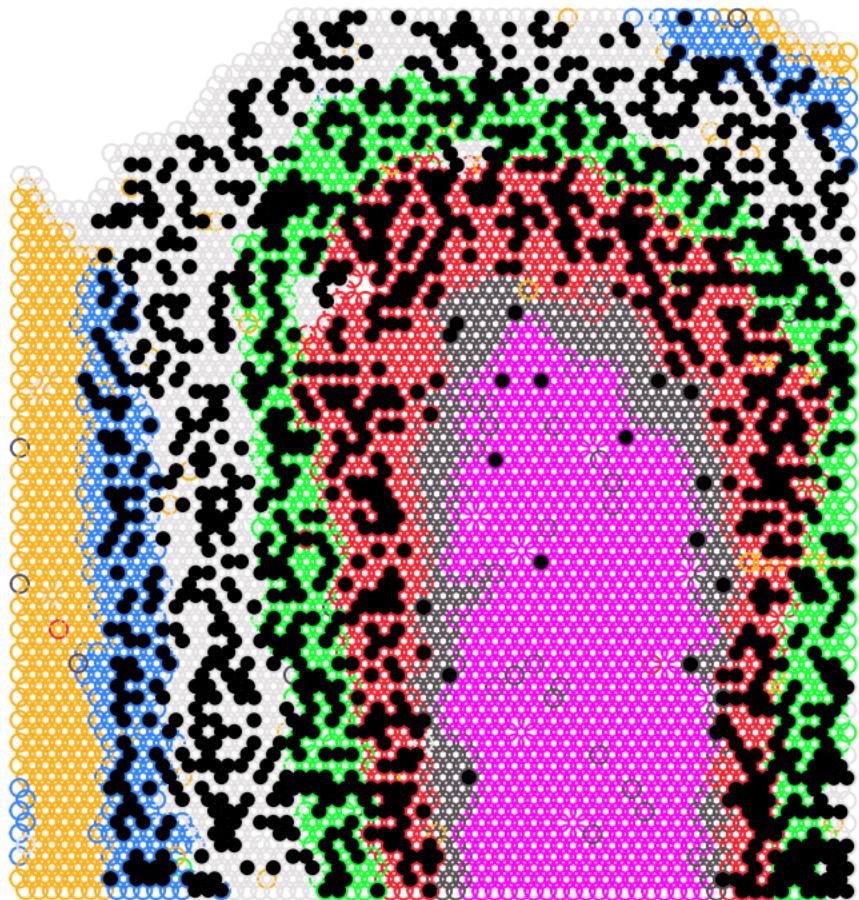
`neun_pos`

- `FALSE`
- `TRUE`

`PRECAST_07`

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13M06-342\_B1



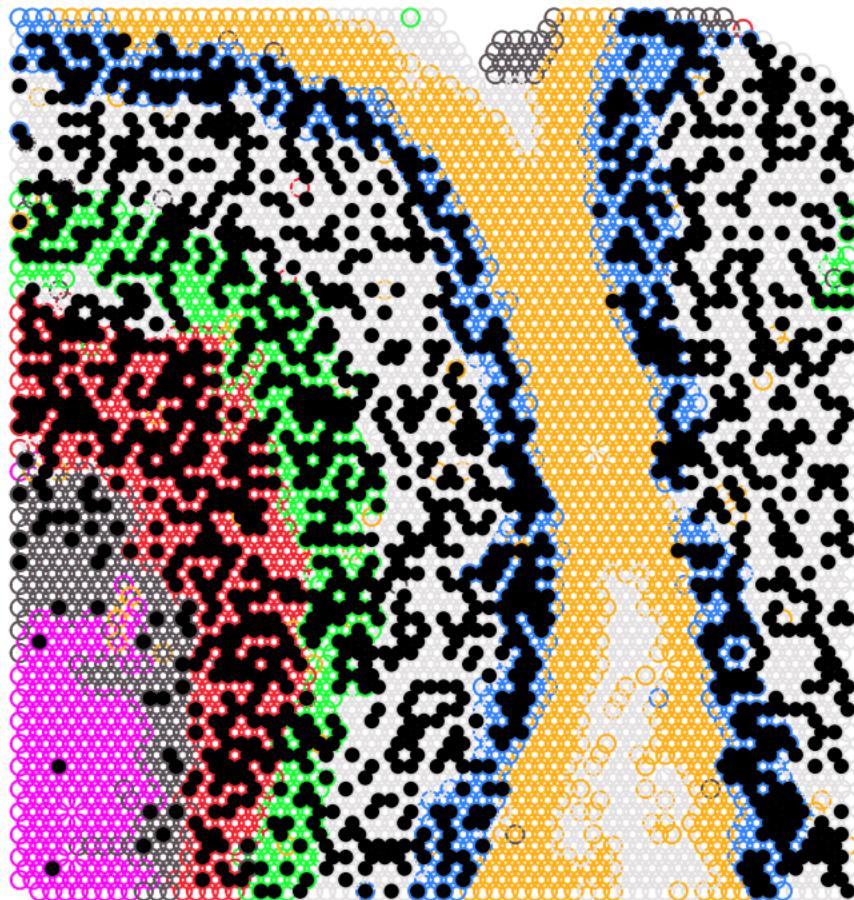
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13M06-342\_C1



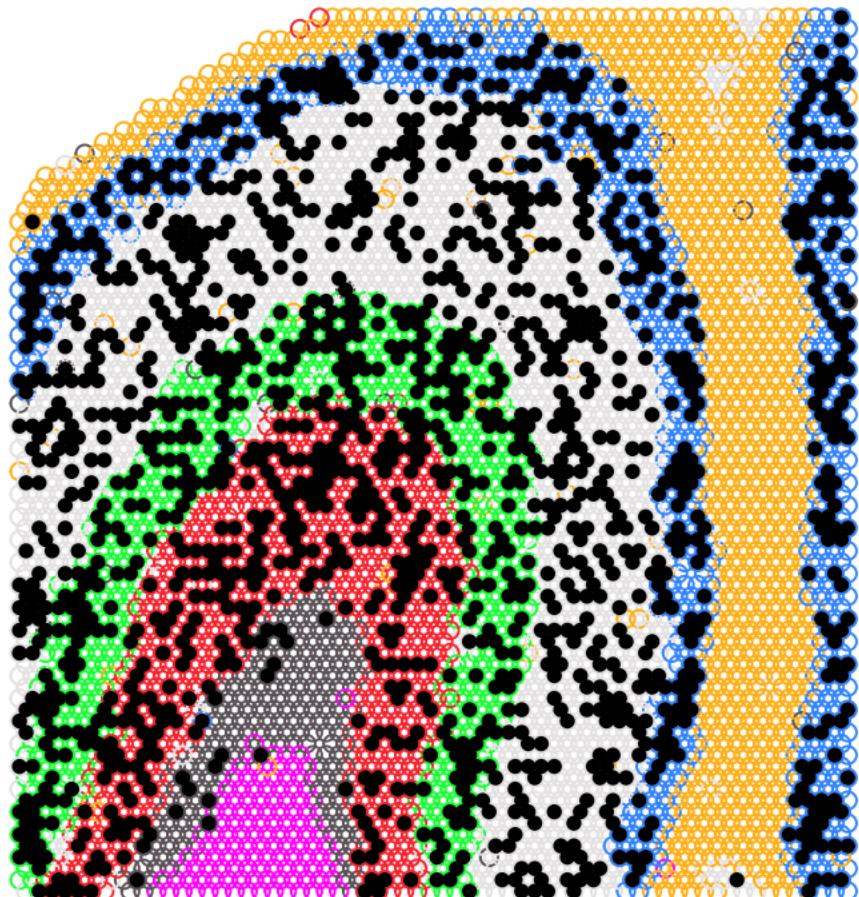
**neun\_pos**

- FALSE
- TRUE

**PRECAST\_07**

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13M06-342\_D1



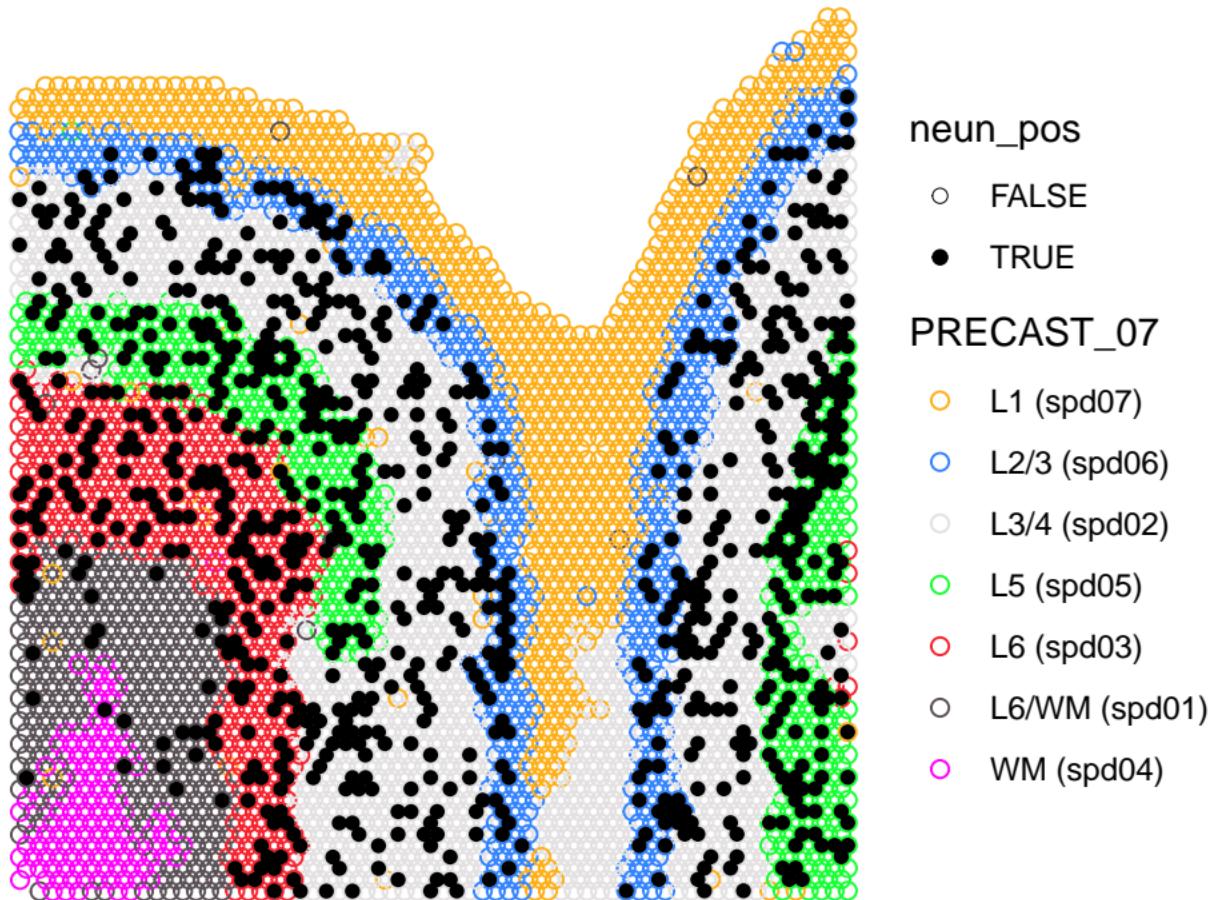
neun\_pos

- FALSE
- TRUE

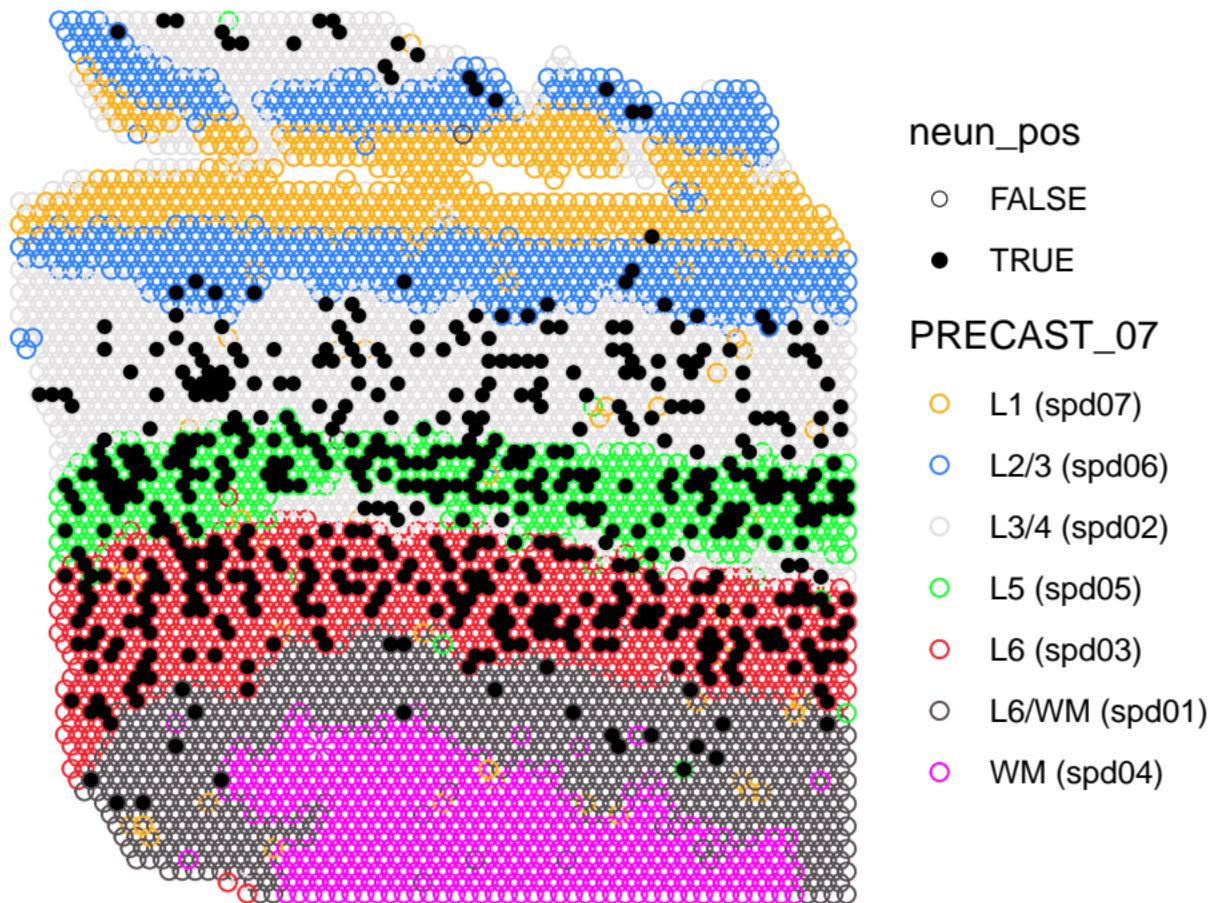
PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

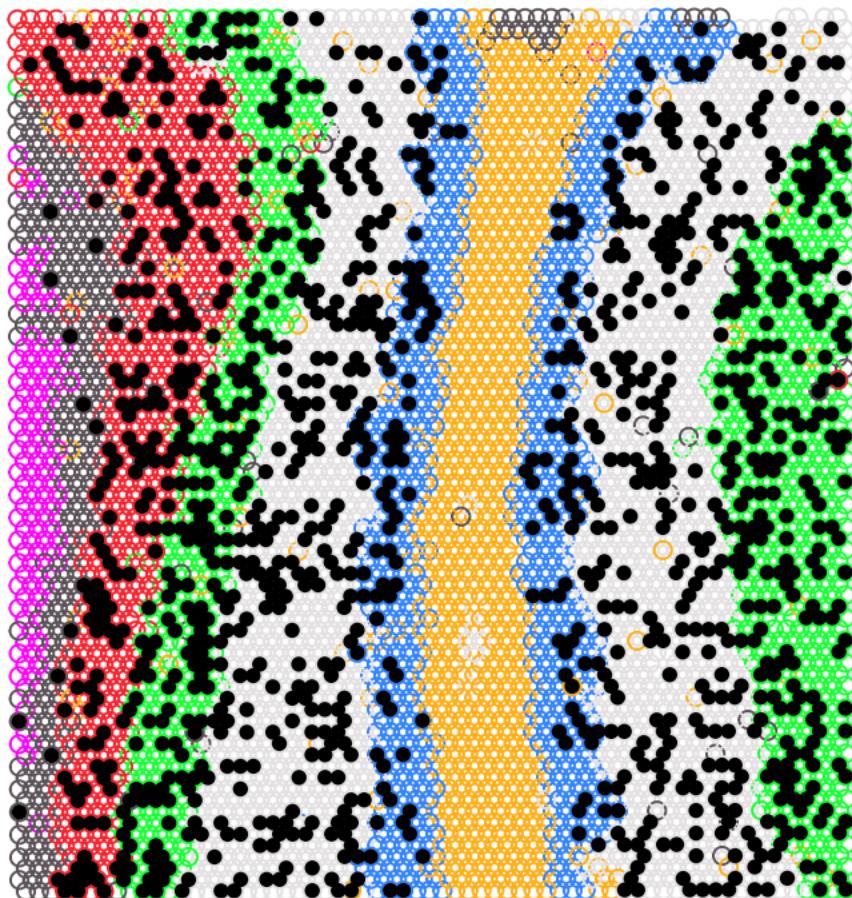
# V13M06-343\_A1



# V13M06-343\_B1



# V13M06-343\_C1



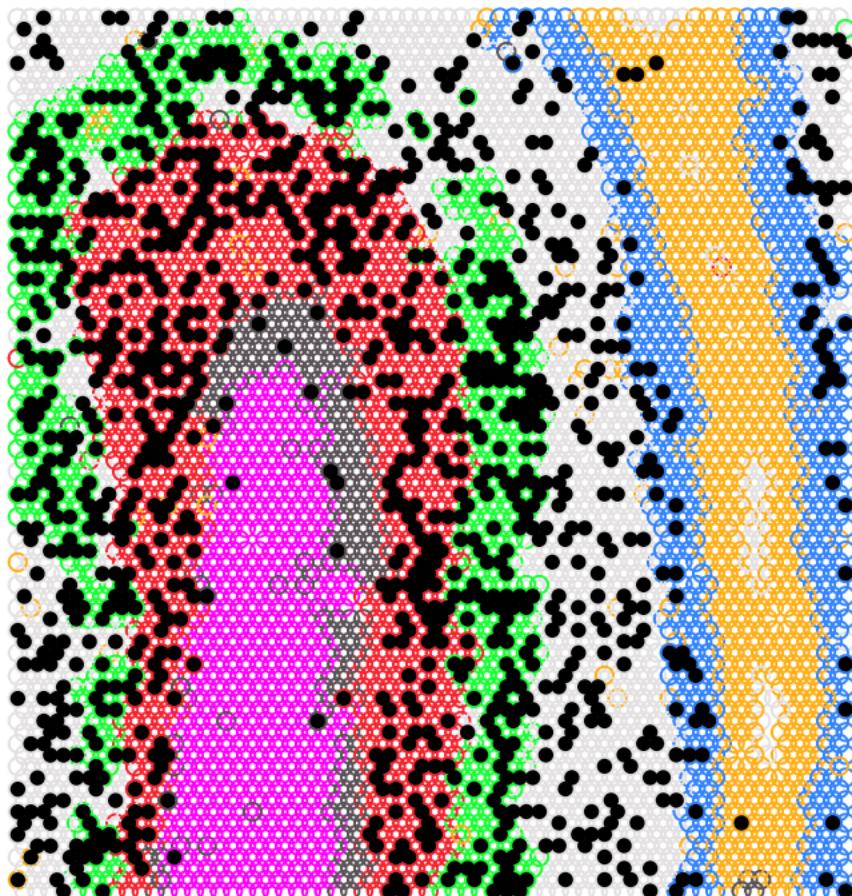
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13M06-343\_D1



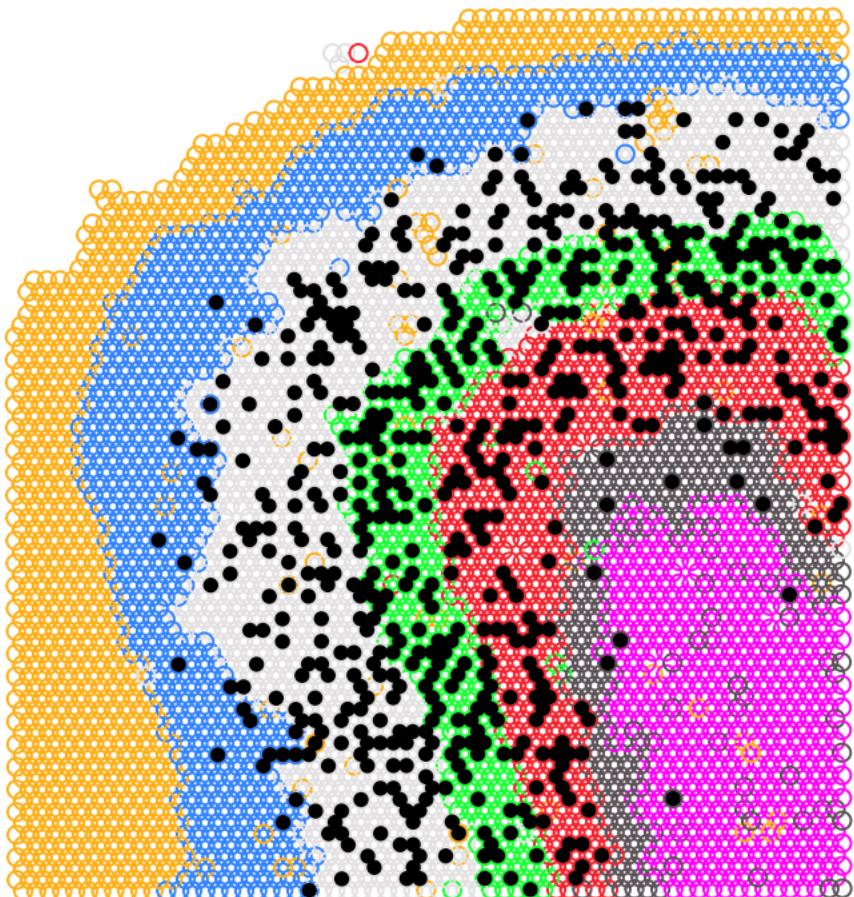
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13M06-344\_A1



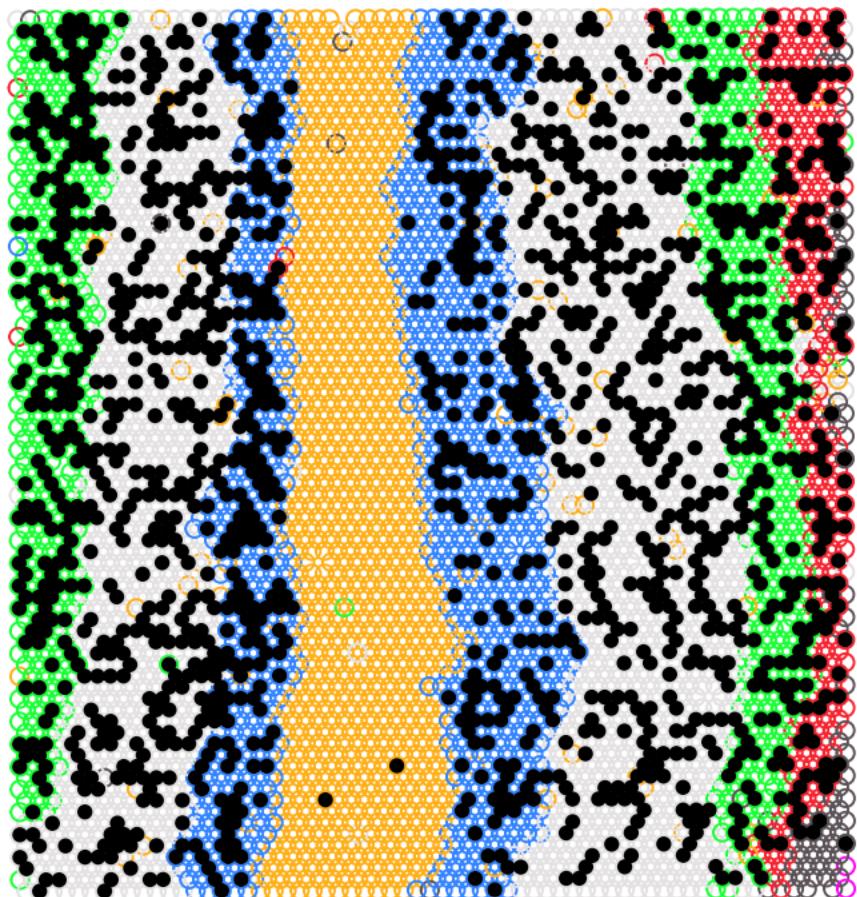
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13M06-344\_B1



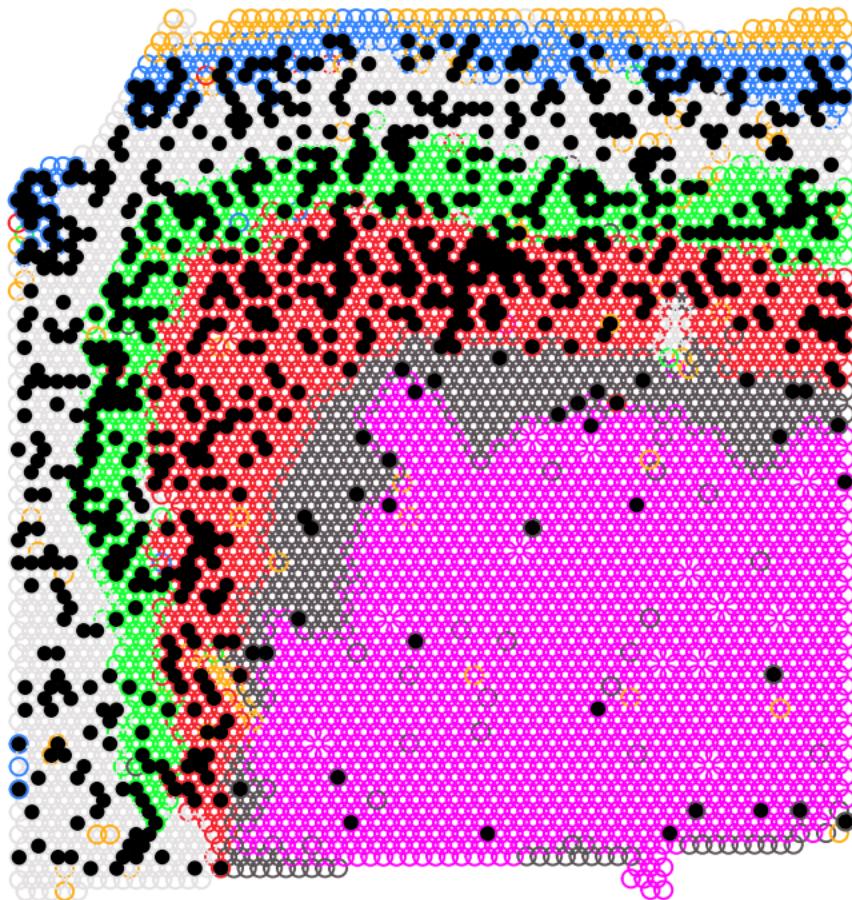
`neun_pos`

- FALSE
- TRUE

`PRECAST_07`

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13M06-344\_C1



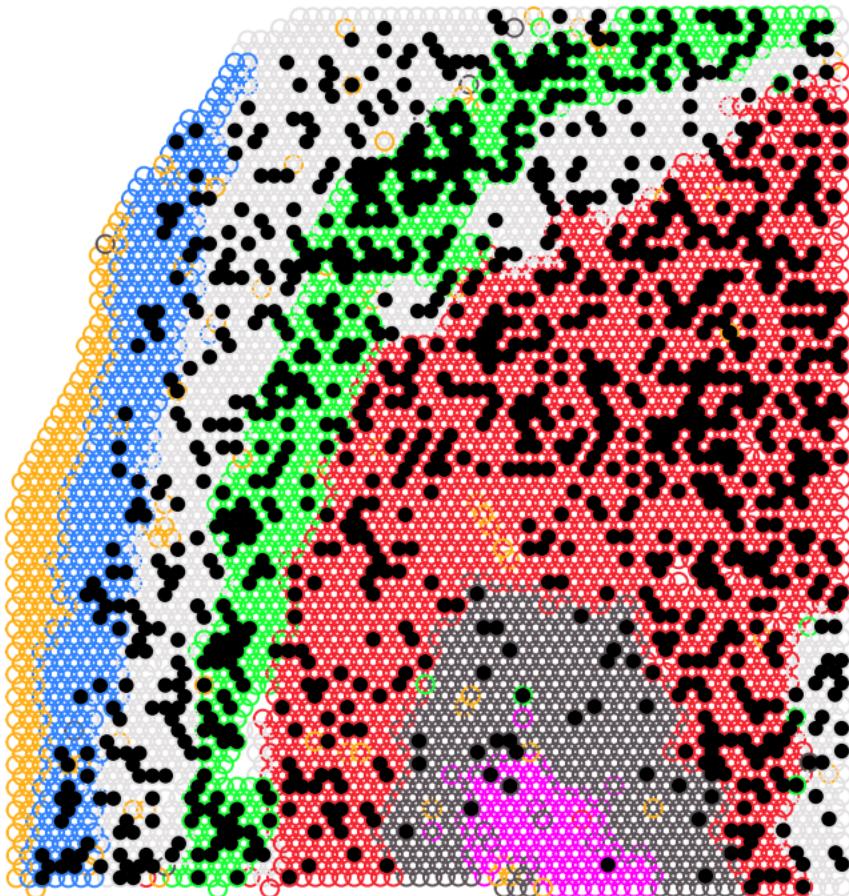
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13M06-344\_D1



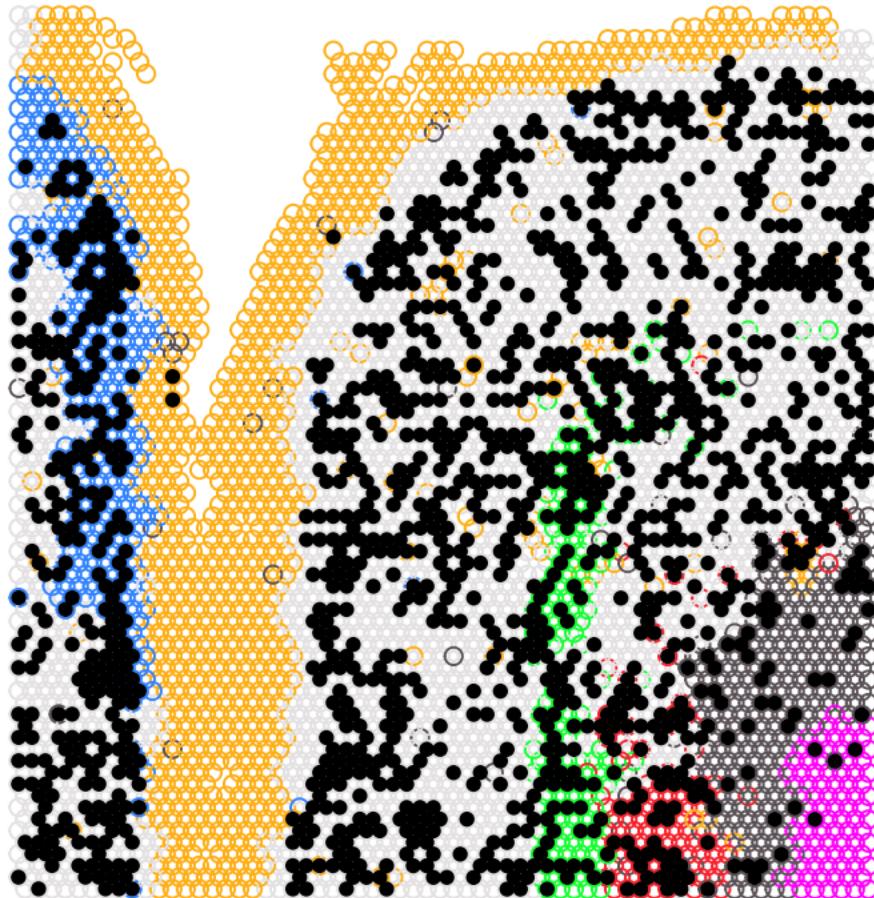
neun\_pos

- FALSE
- TRUE

PRECAST\_07

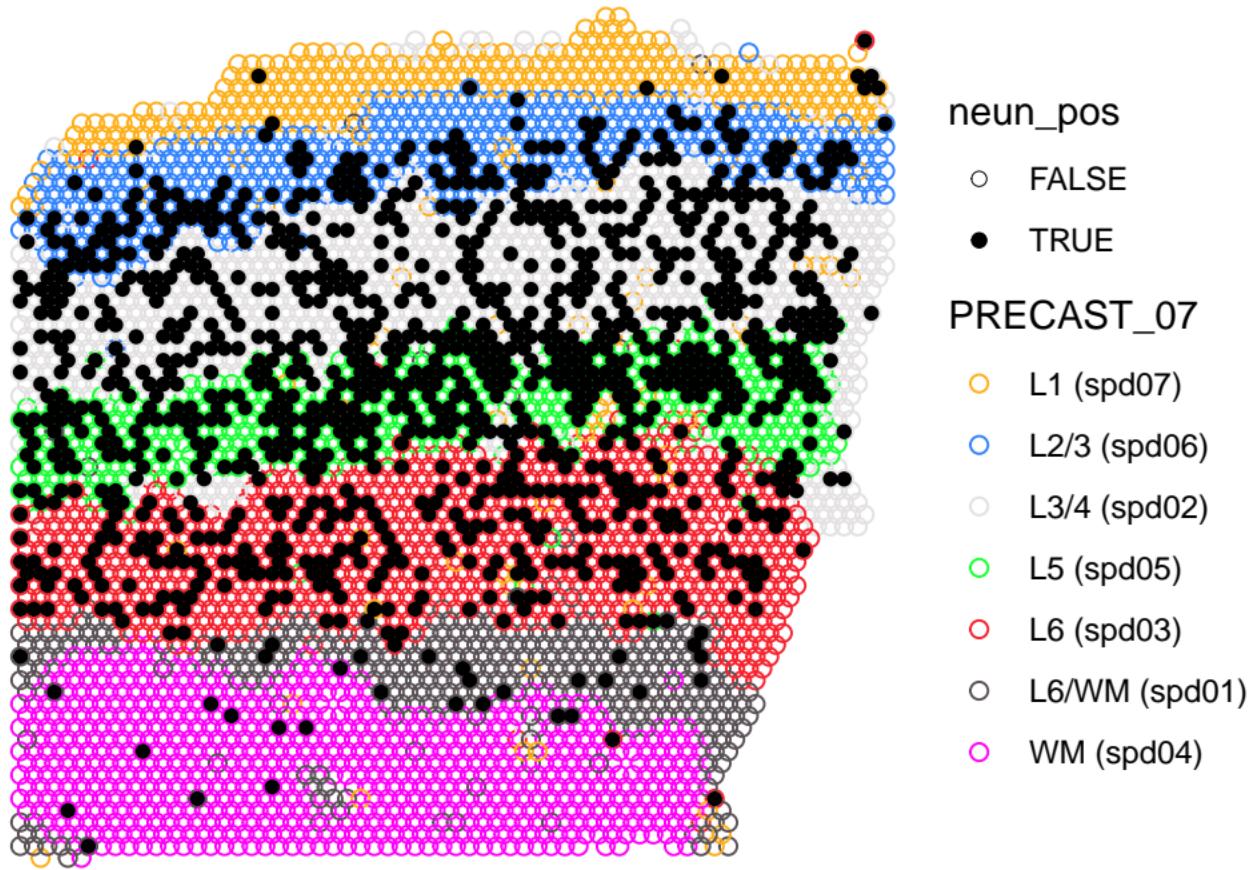
- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

V13F27-336\_A1

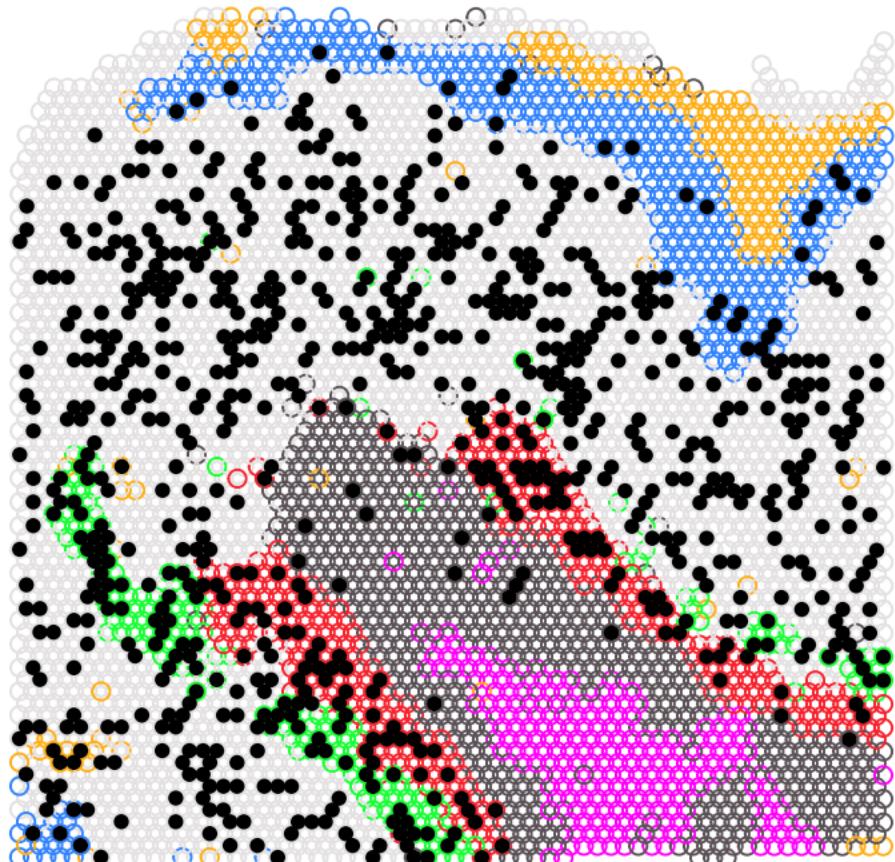


- neun\_pos**
  - FALSE
  - TRUE
- PRECAST\_07**
  - L1 (spd07)
  - L2/3 (spd06)
  - L3/4 (spd02)
  - L5 (spd05)
  - L6 (spd03)
  - L6/WM (spd01)
  - WM (spd04)

# V13F27-336\_B1



# V13F27-336\_C1



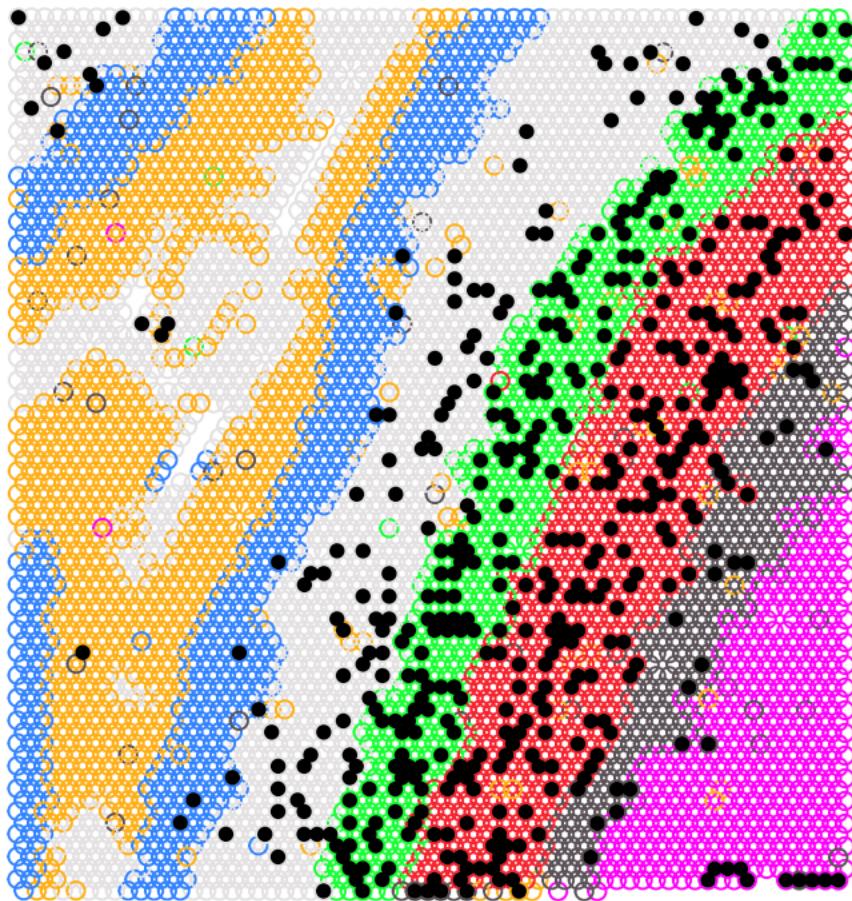
neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

# V13F27-336\_D1



neun\_pos

- FALSE
- TRUE

PRECAST\_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)