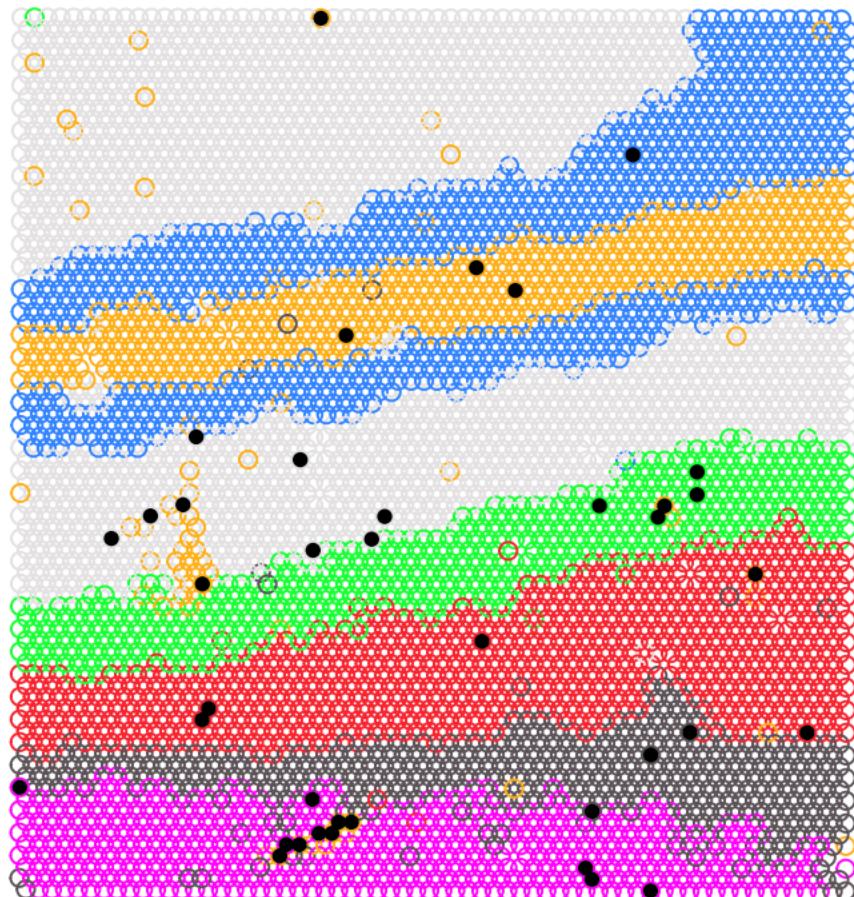


V12F14-053_A1



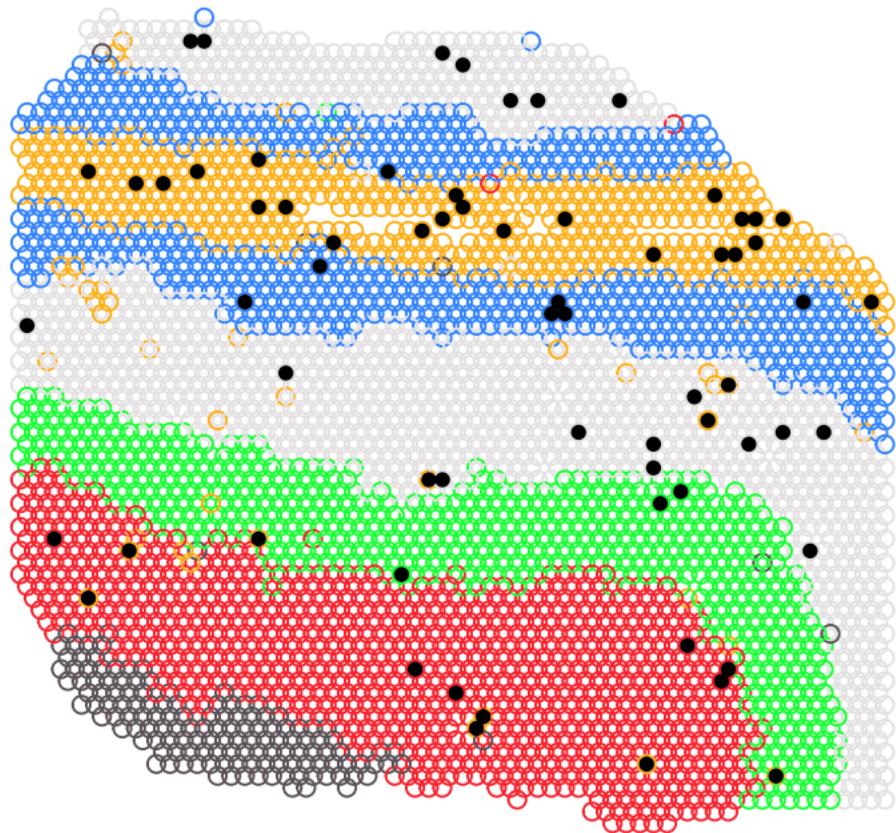
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V12F14-053_C1



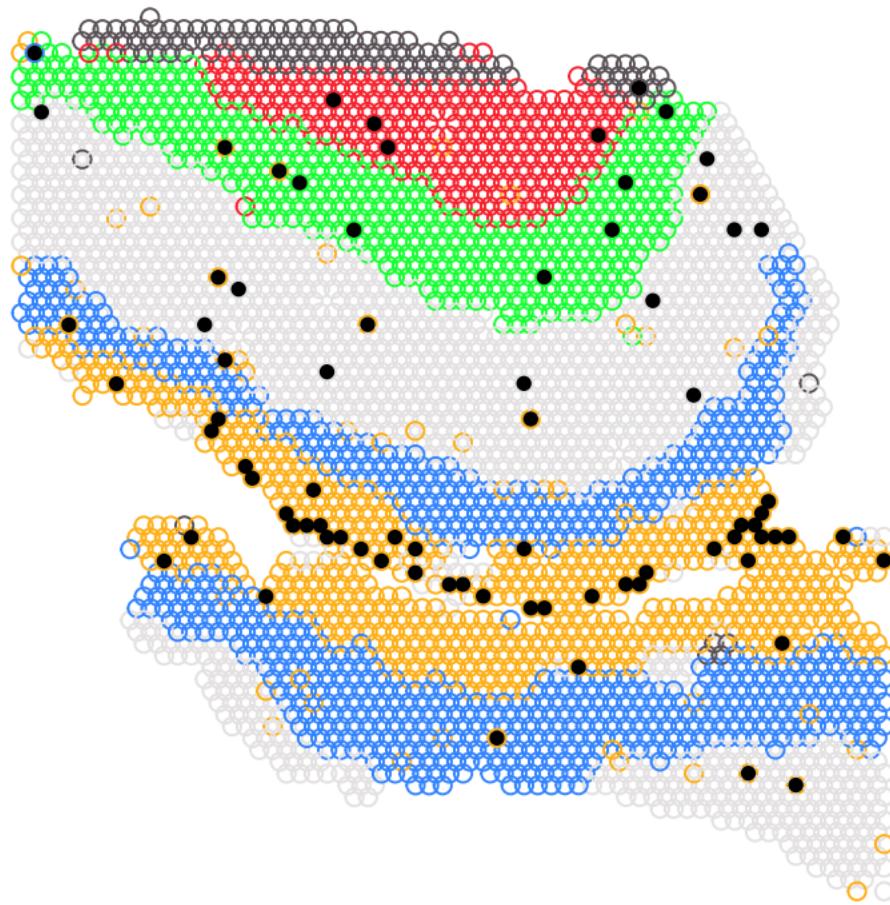
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V12F14-053_D1



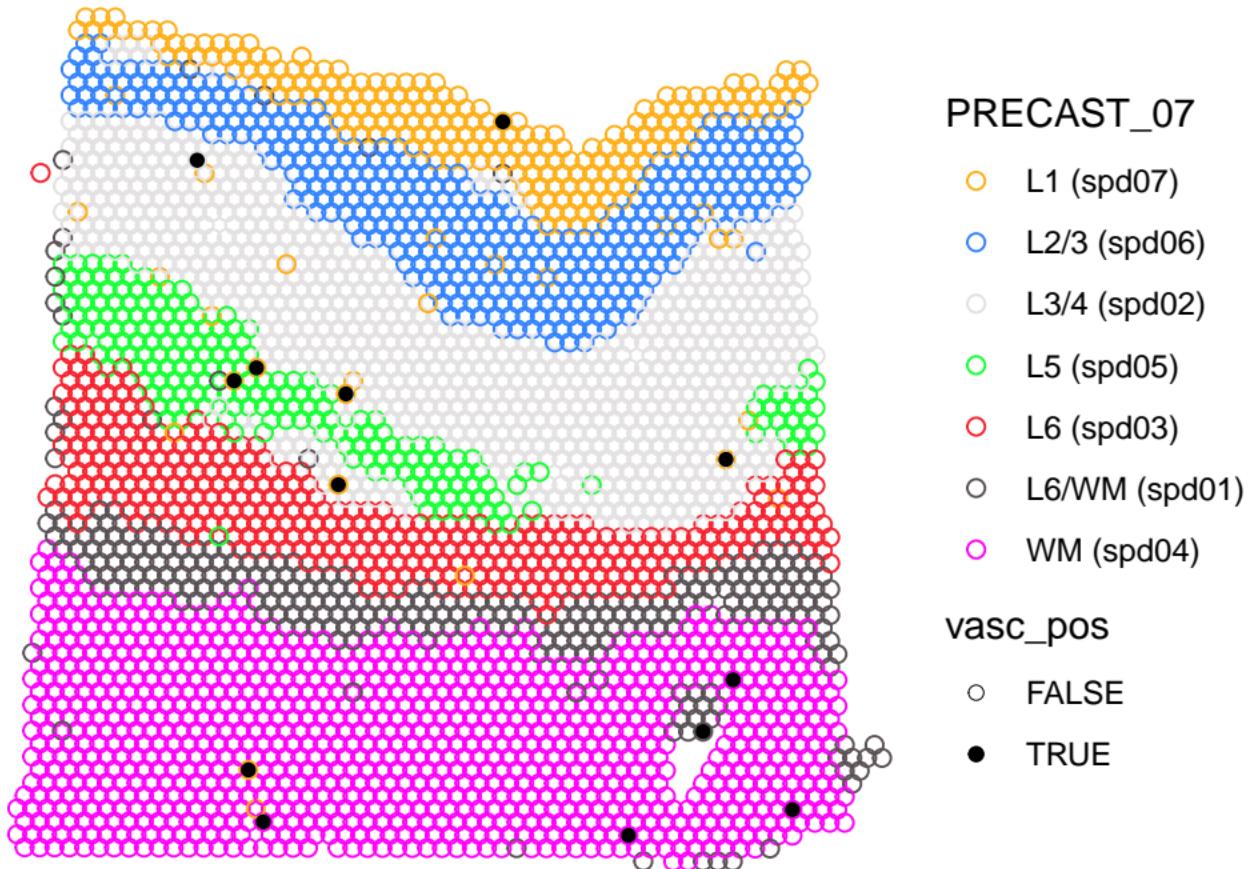
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

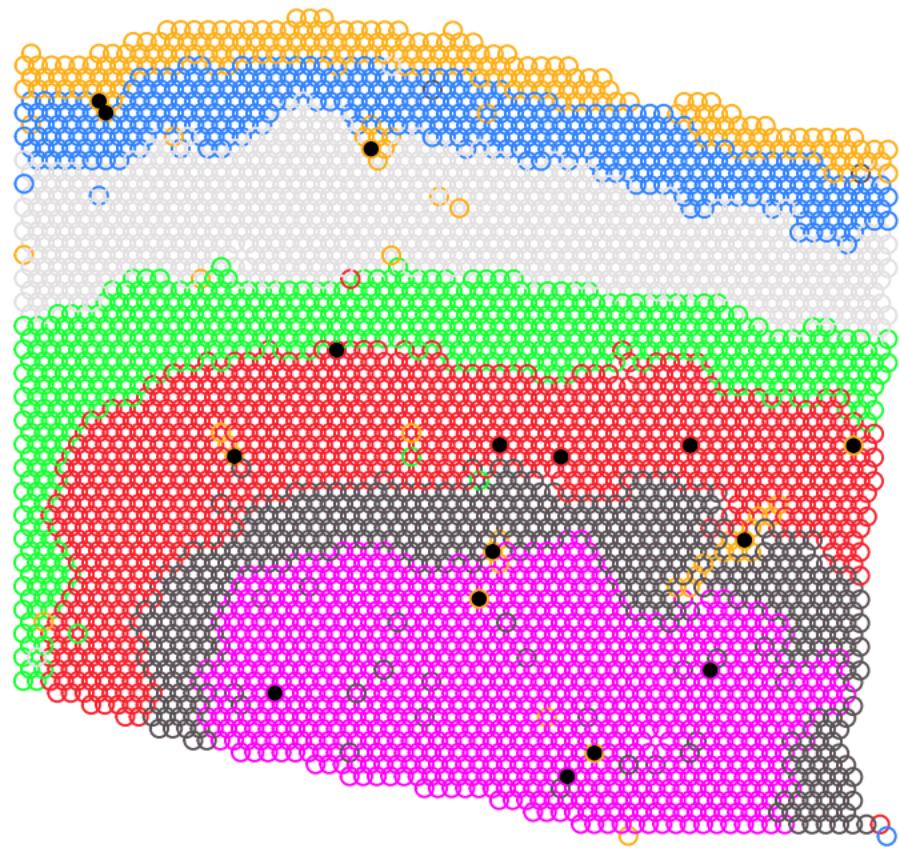
vasc_pos

- FALSE
- TRUE

V12F14-057_A1



V12F14-057_B1



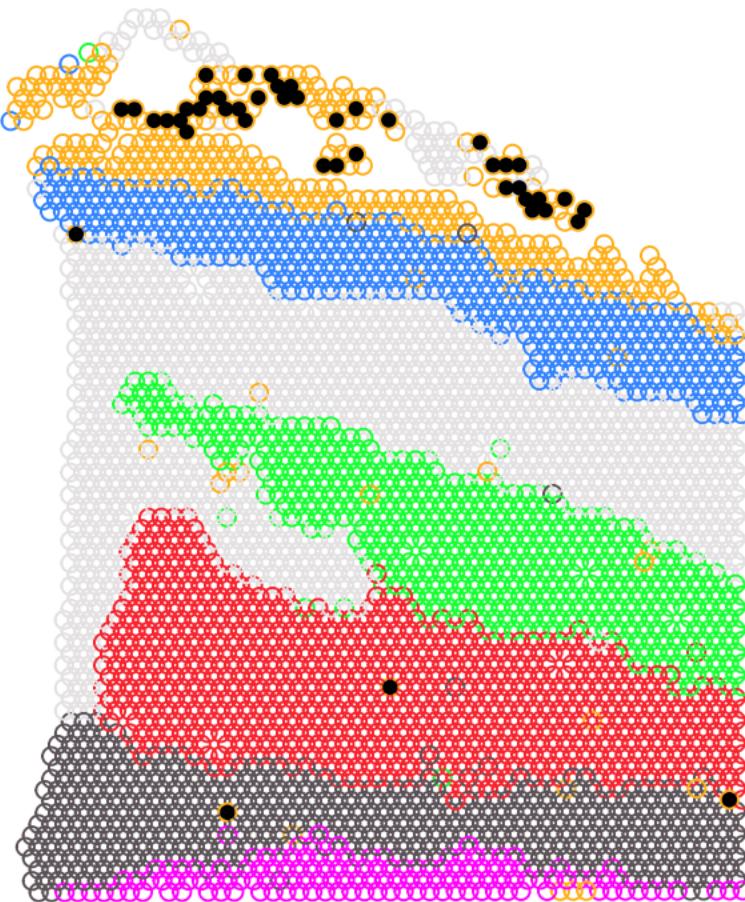
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V12F14-057_C1



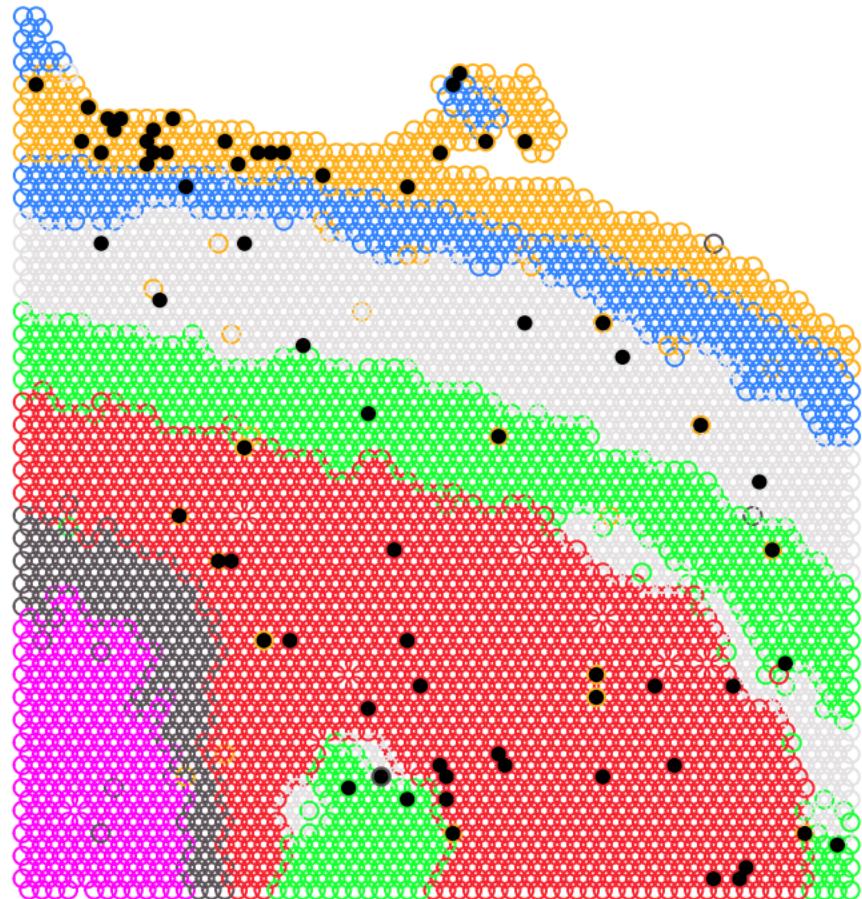
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V12F14-057_D1



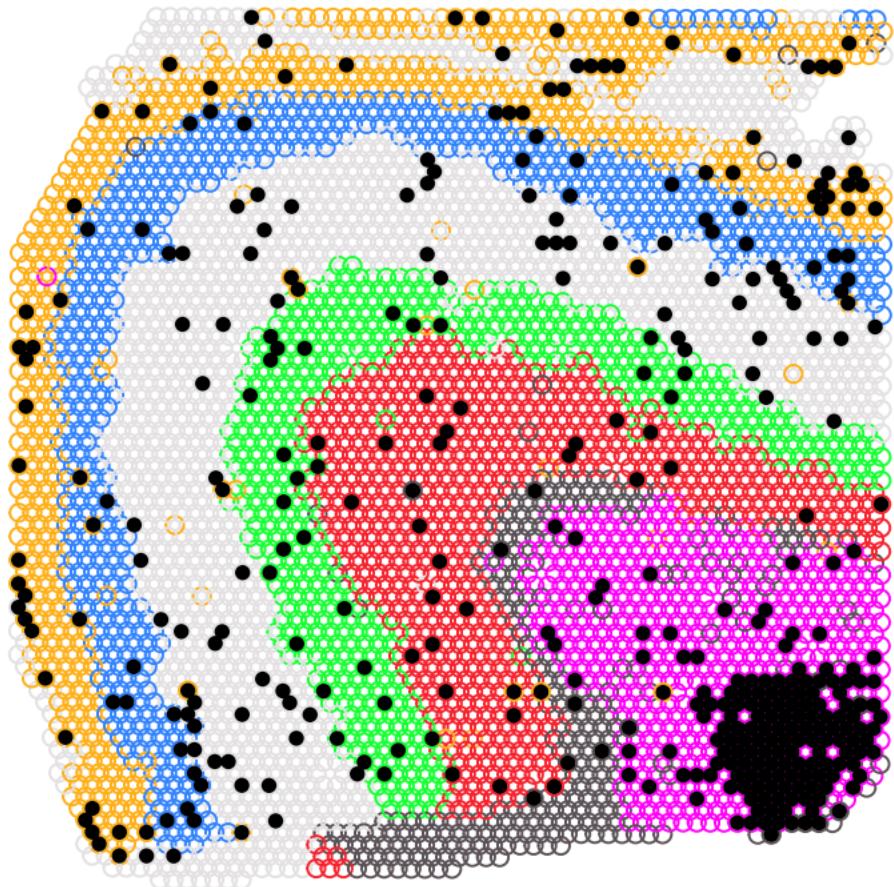
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V12D07-334_A1



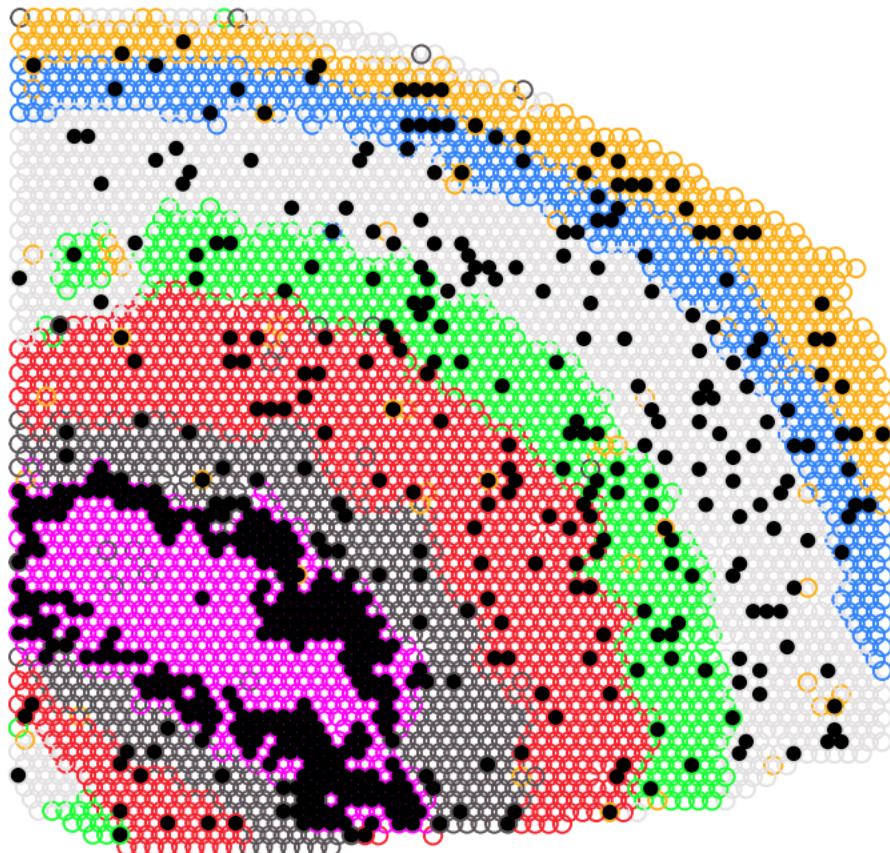
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V12D07-334_B1



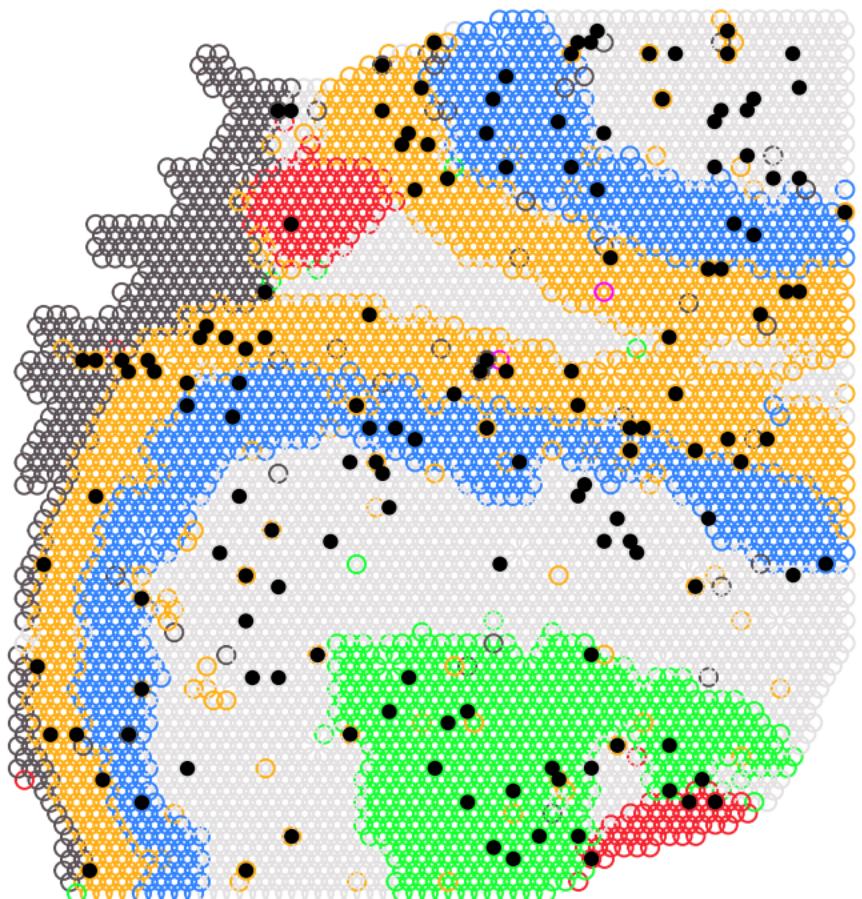
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V12D07-334_C1



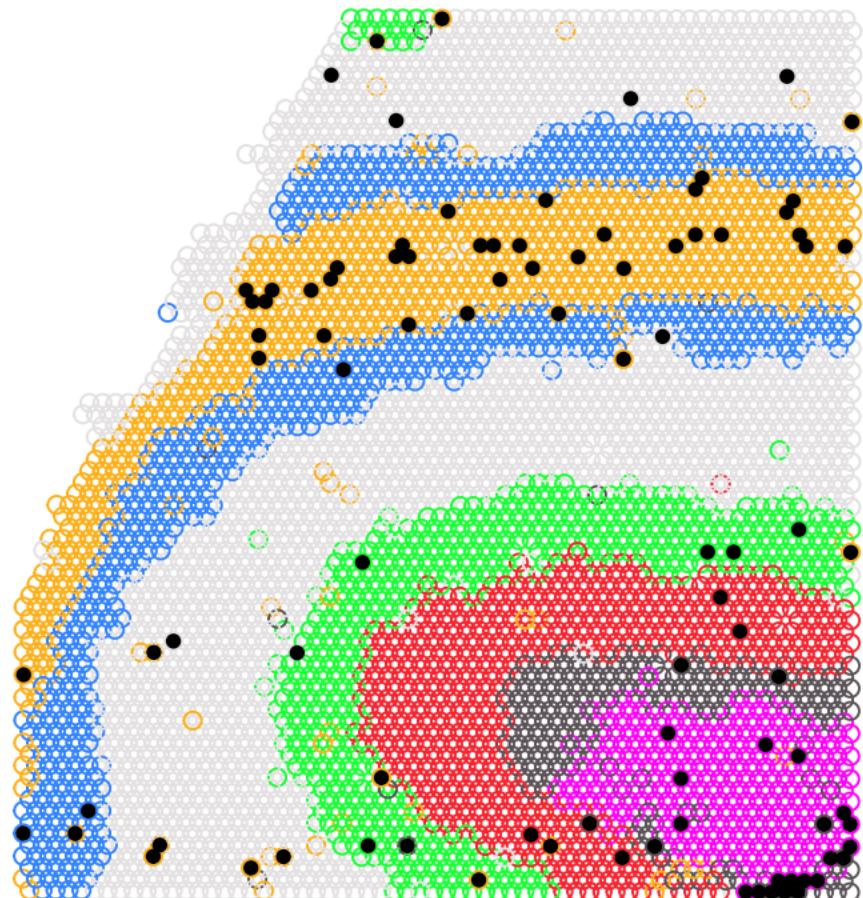
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V12D07-334_D1



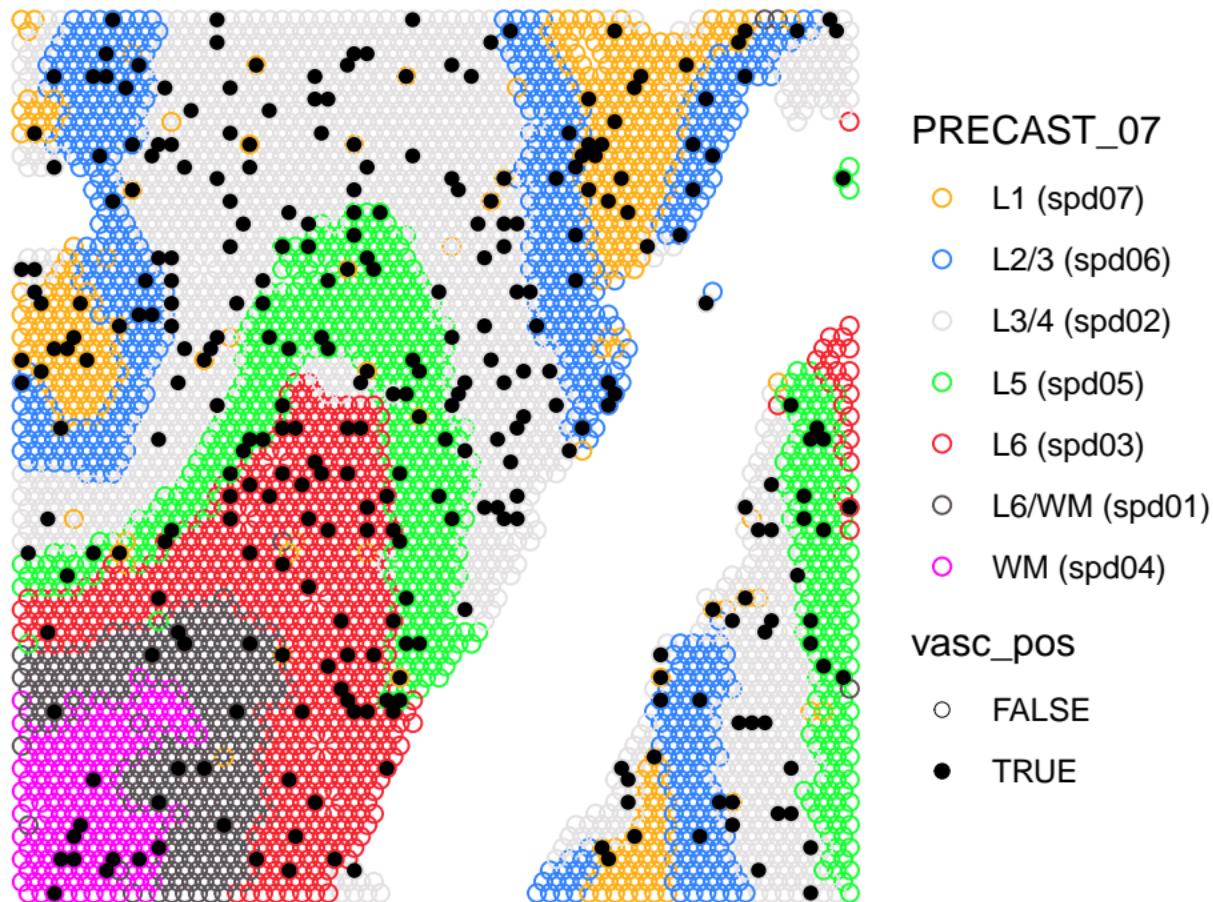
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

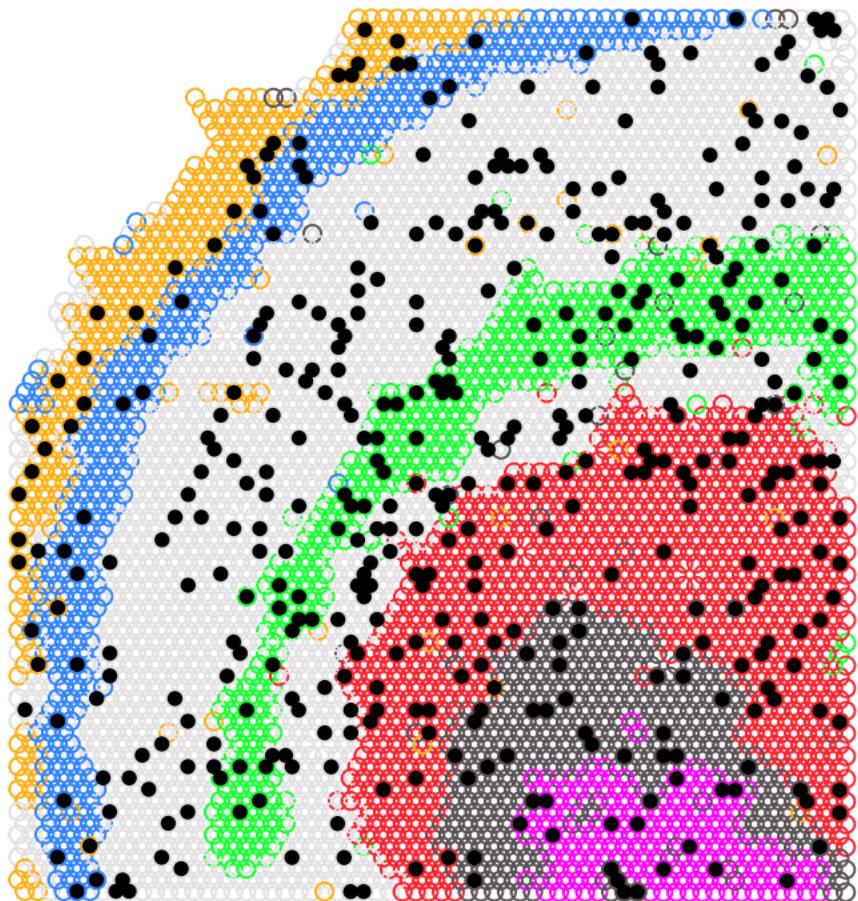
vasc_pos

- FALSE
- TRUE

V13M06-279_A1



V13M06-279_B1



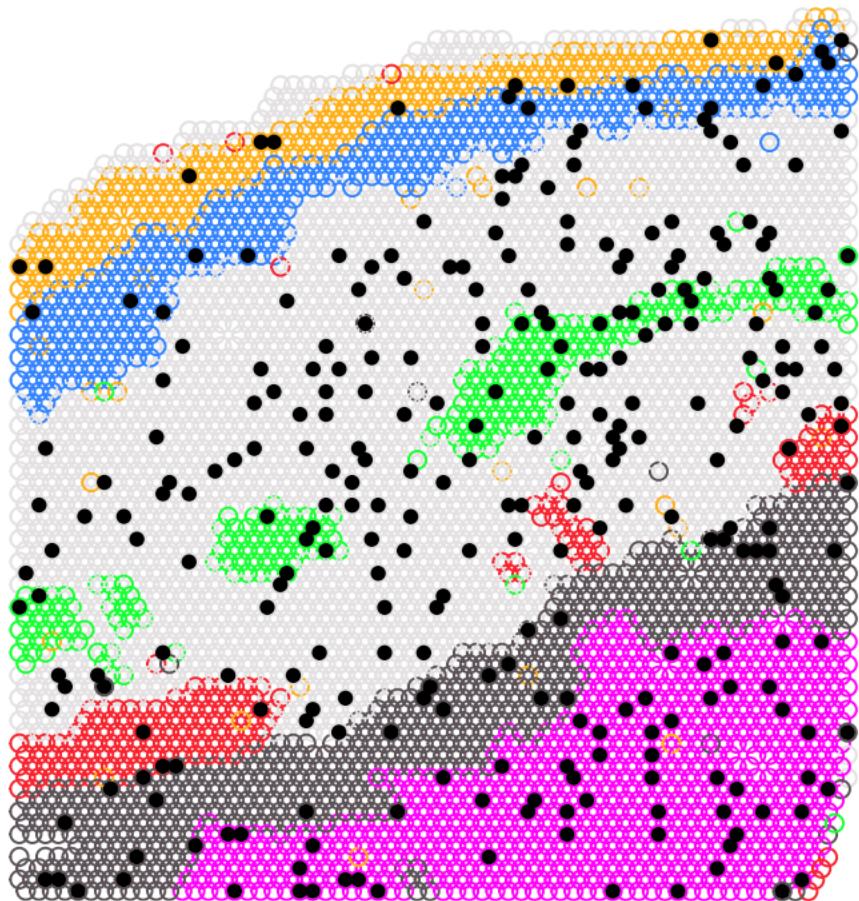
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06-279_C1



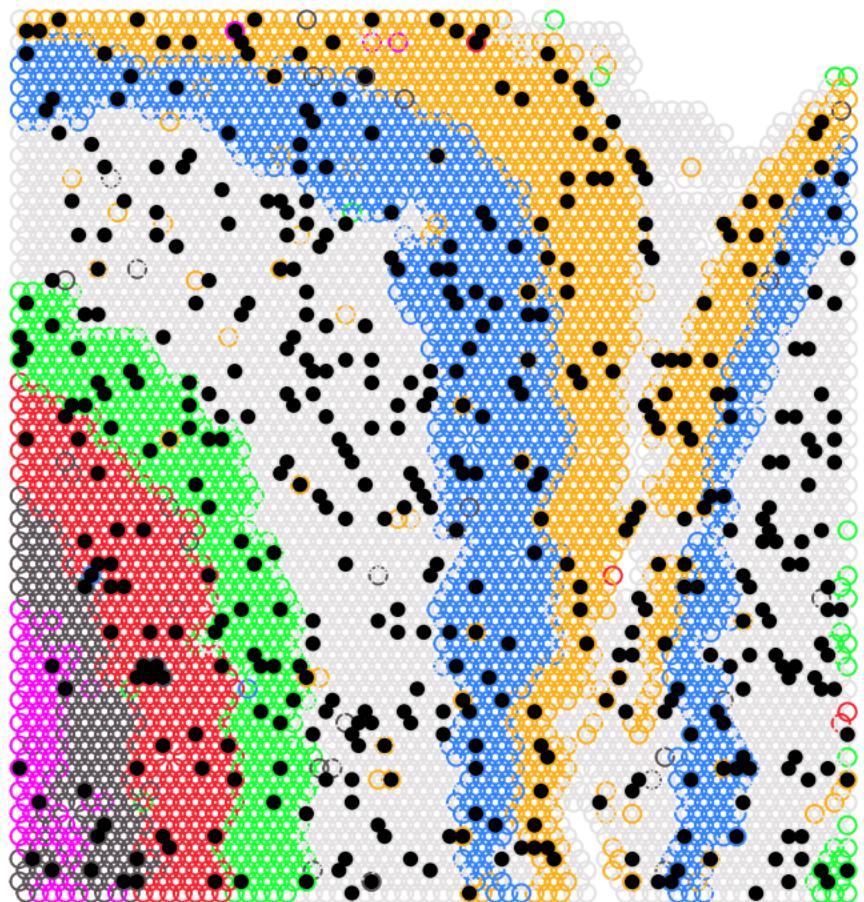
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06-279_D1



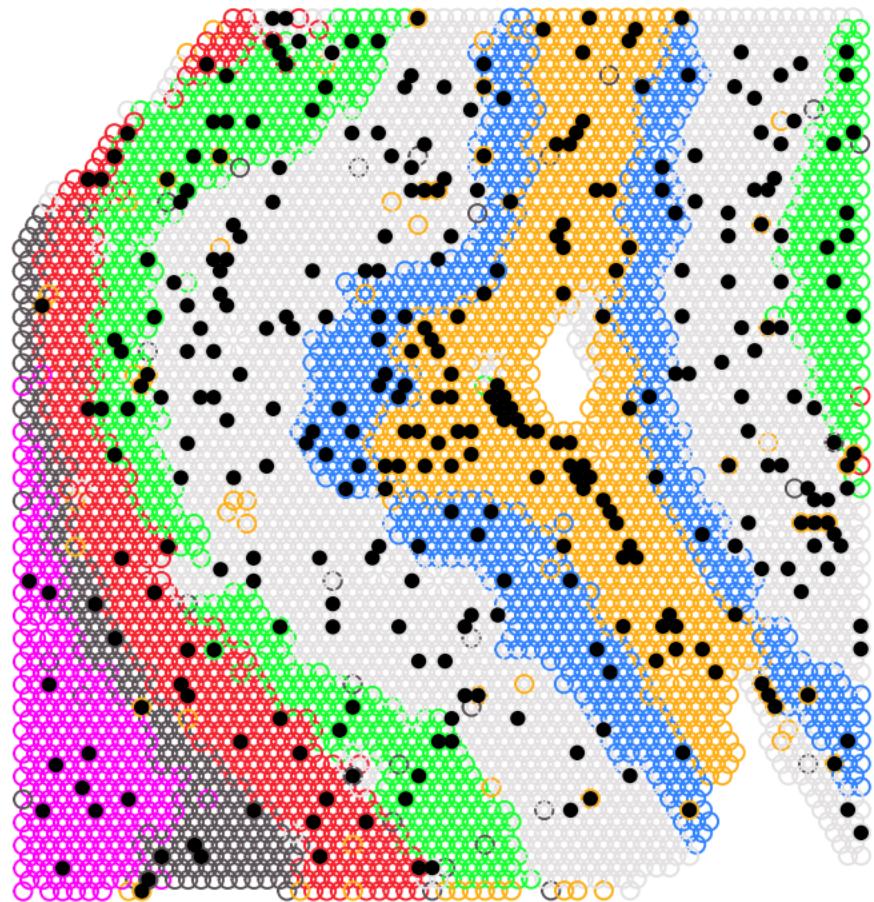
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06-280_A1



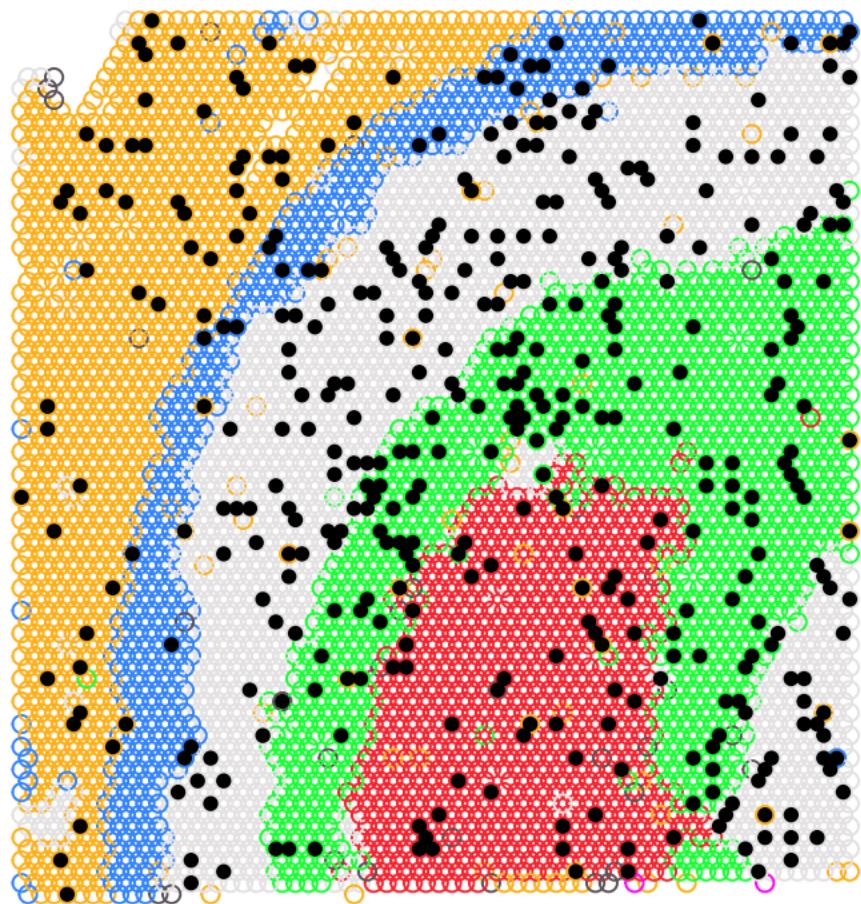
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06-280_B1



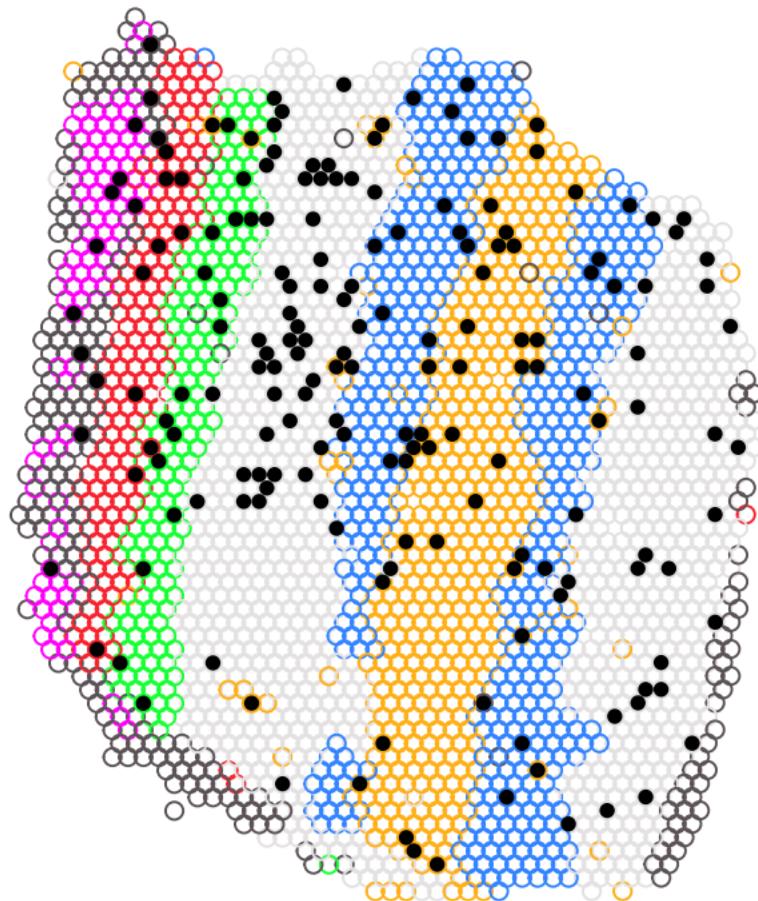
PRECAST_07

- L1 (spd07)**
- L2/3 (spd06)**
- L3/4 (spd02)**
- L5 (spd05)**
- L6 (spd03)**
- L6/WM (spd01)**
- WM (spd04)**

vasc_pos

- FALSE**
- TRUE**

V13M06-280_C1



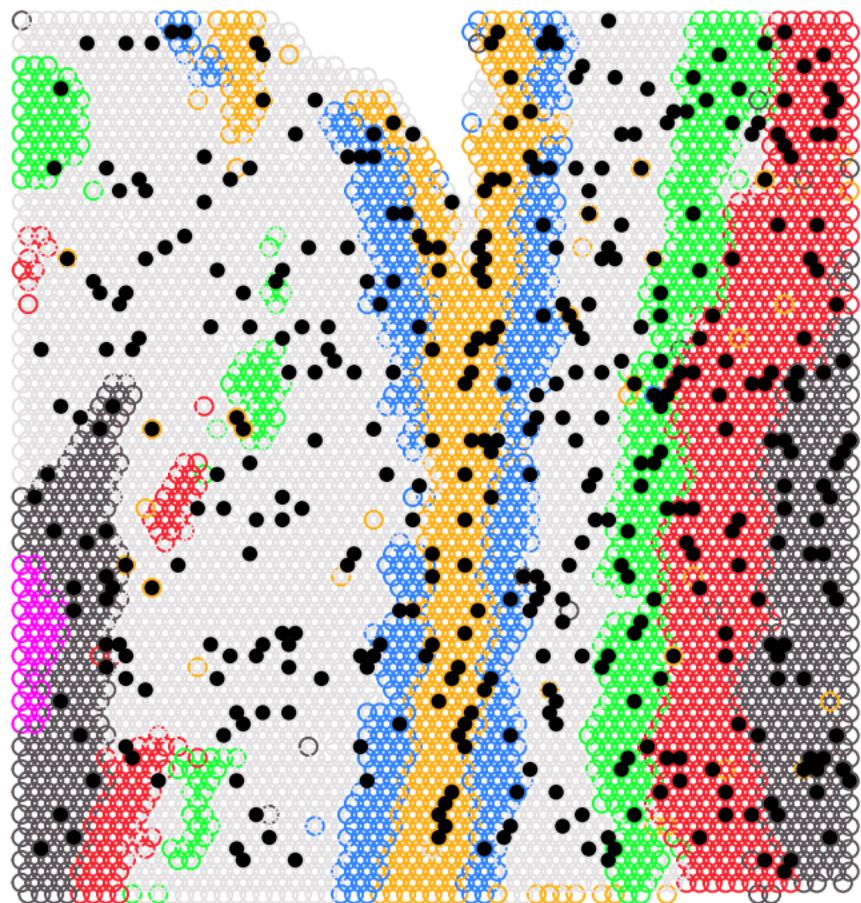
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06-280_D1



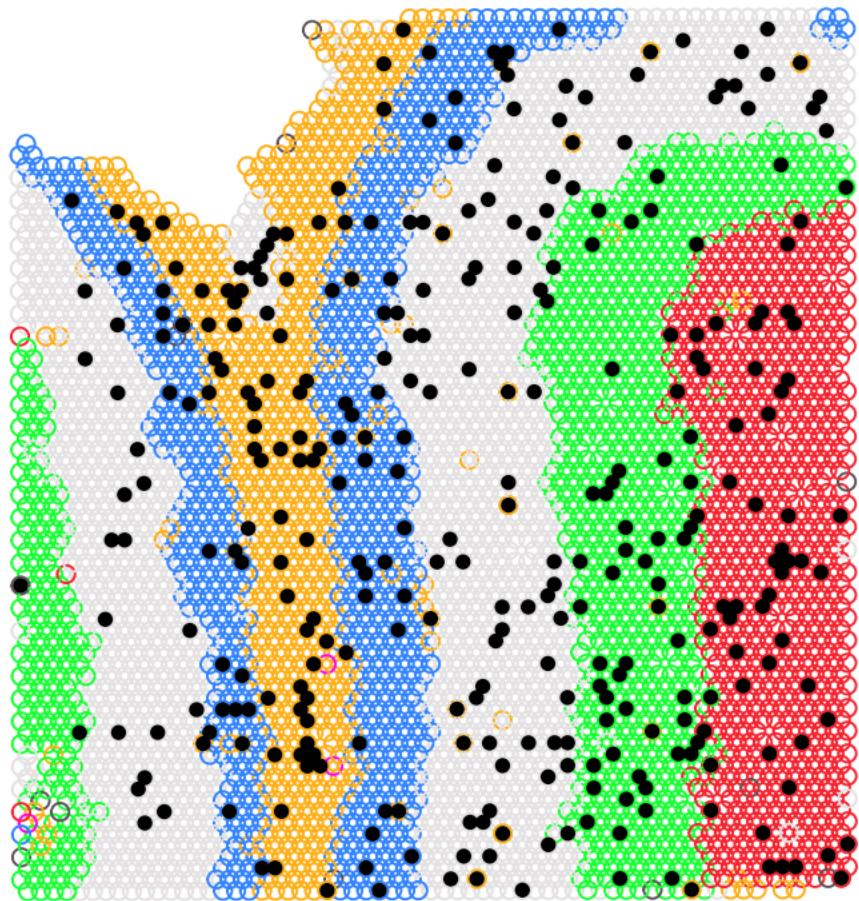
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06-281_A1



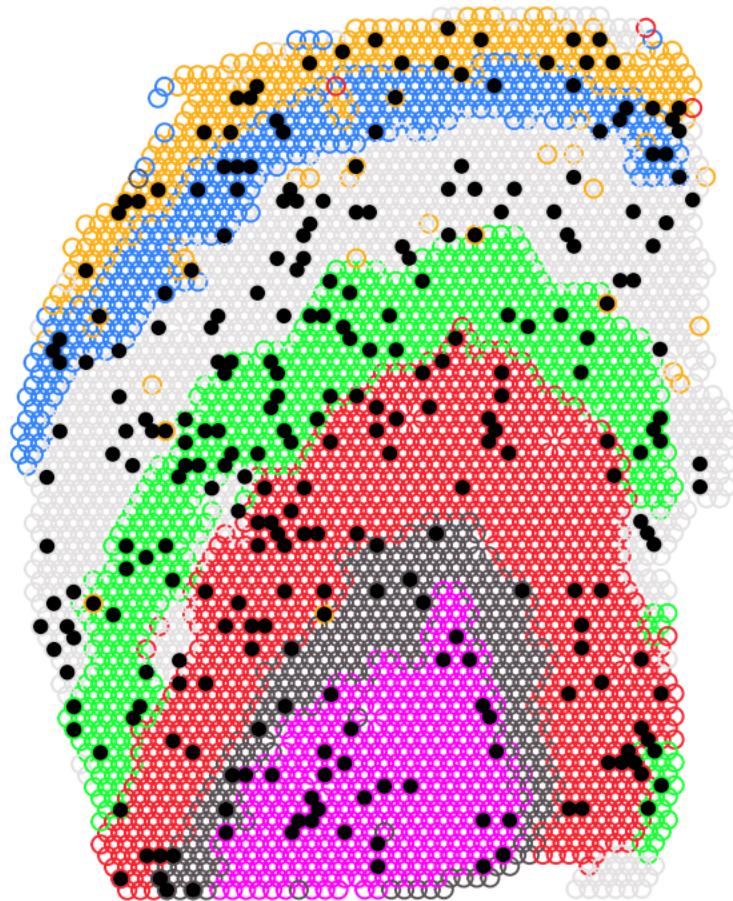
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06-281_B1



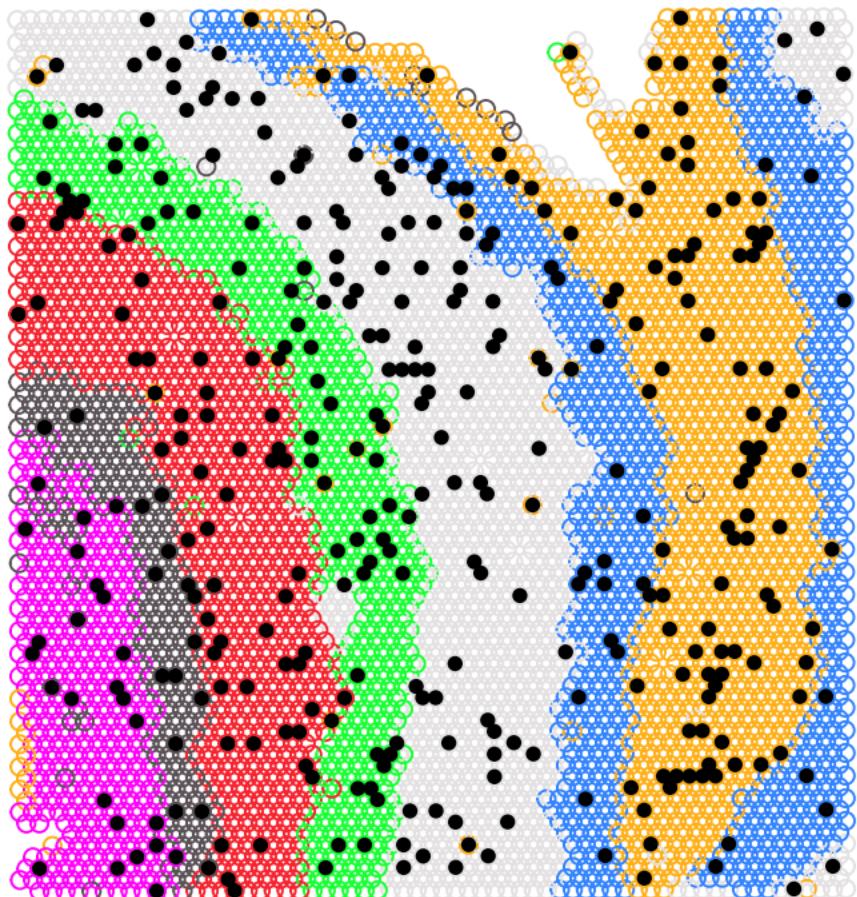
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06-281_C1



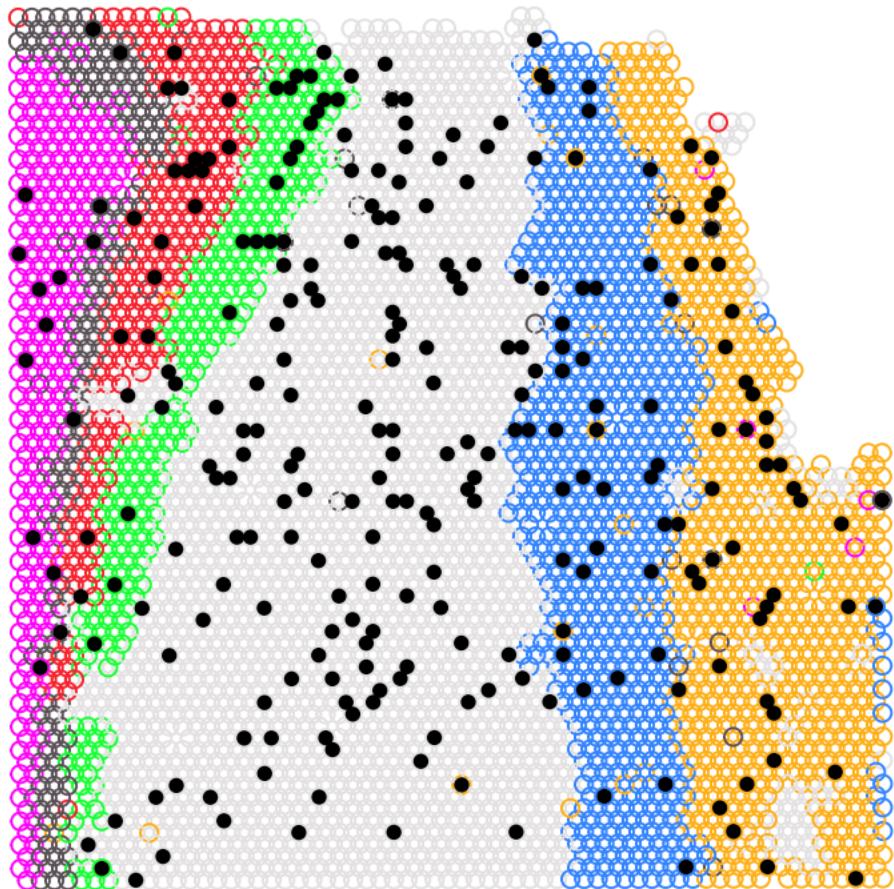
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06–281_D1



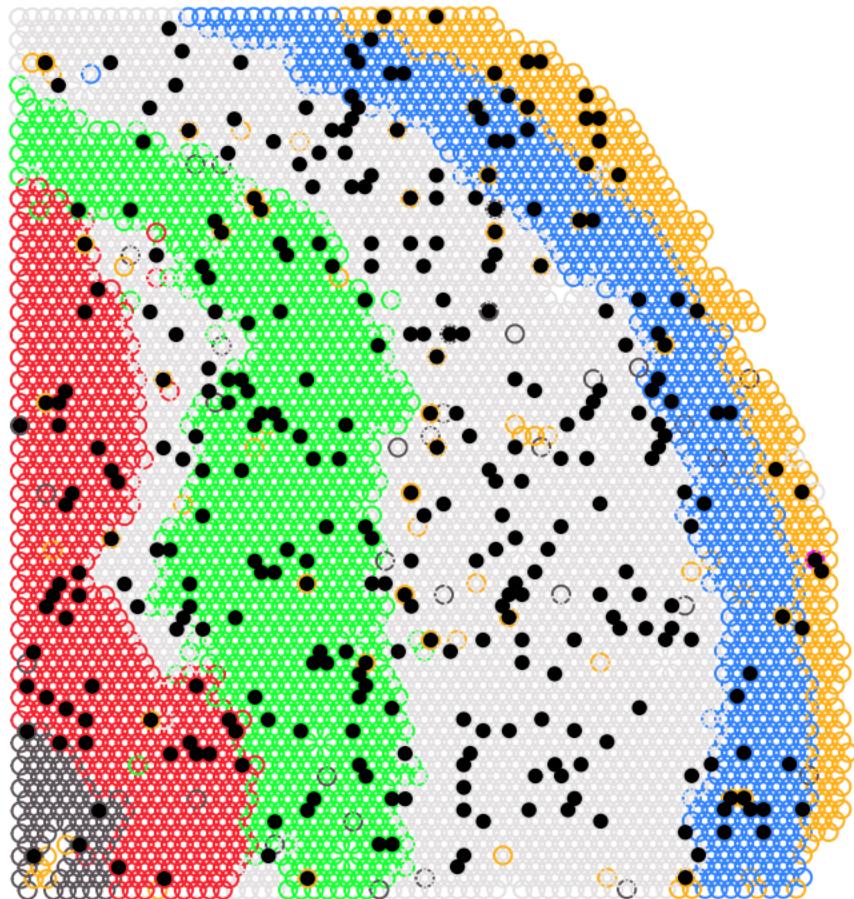
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06-282_A1



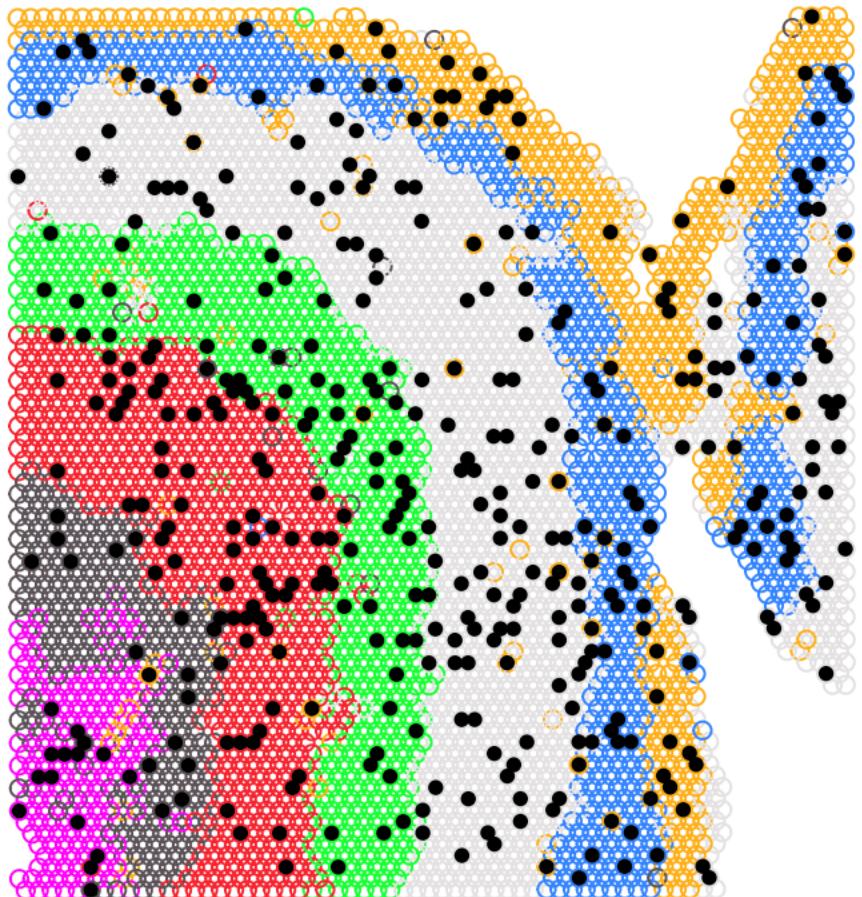
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06-282_B1



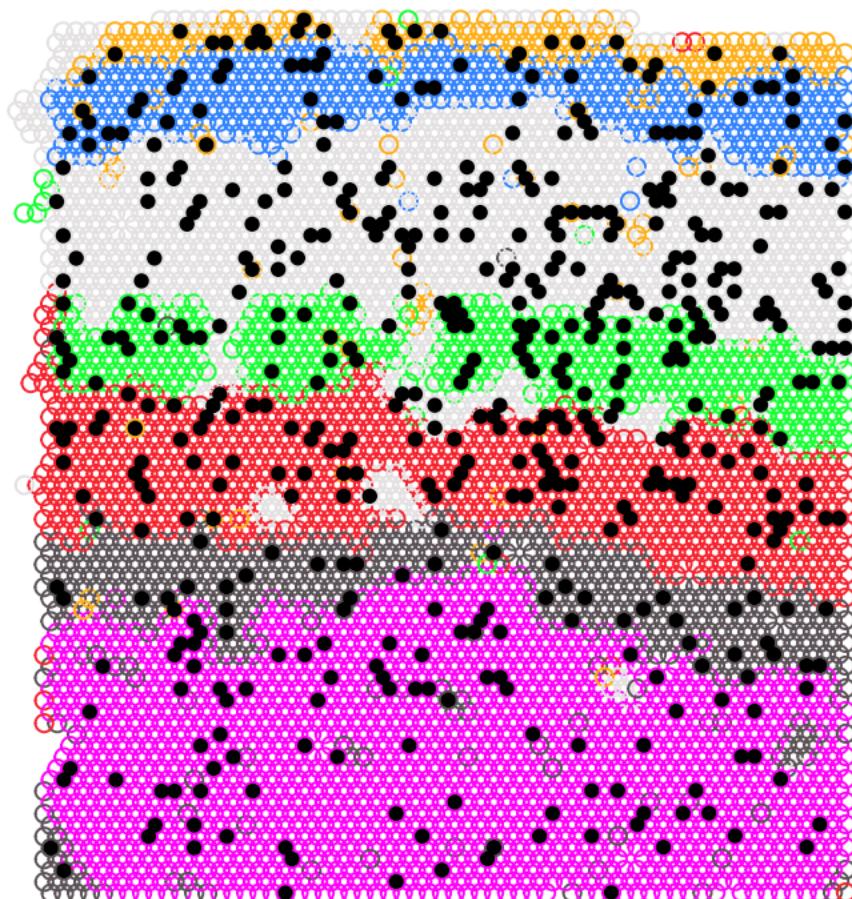
PRECAST_07

- L1 (spd07)**
- L2/3 (spd06)**
- L3/4 (spd02)**
- L5 (spd05)**
- L6 (spd03)**
- L6/WM (spd01)**
- WM (spd04)**

vasc_pos

- FALSE**
- TRUE**

V13M06-282_C1



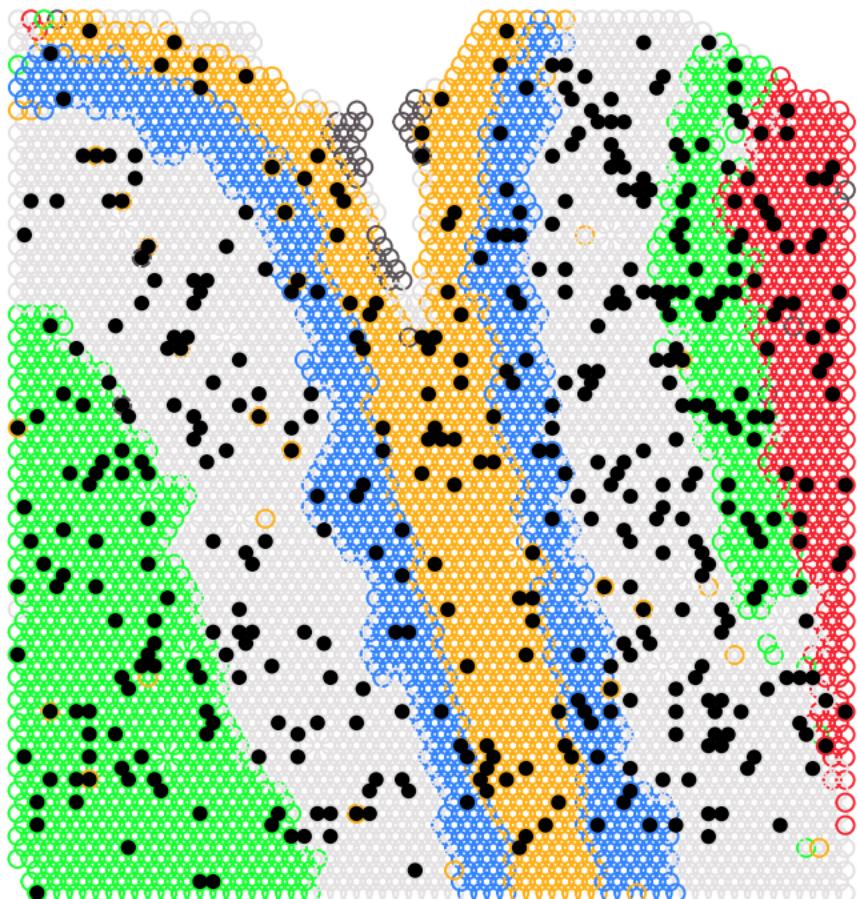
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06-282_D1



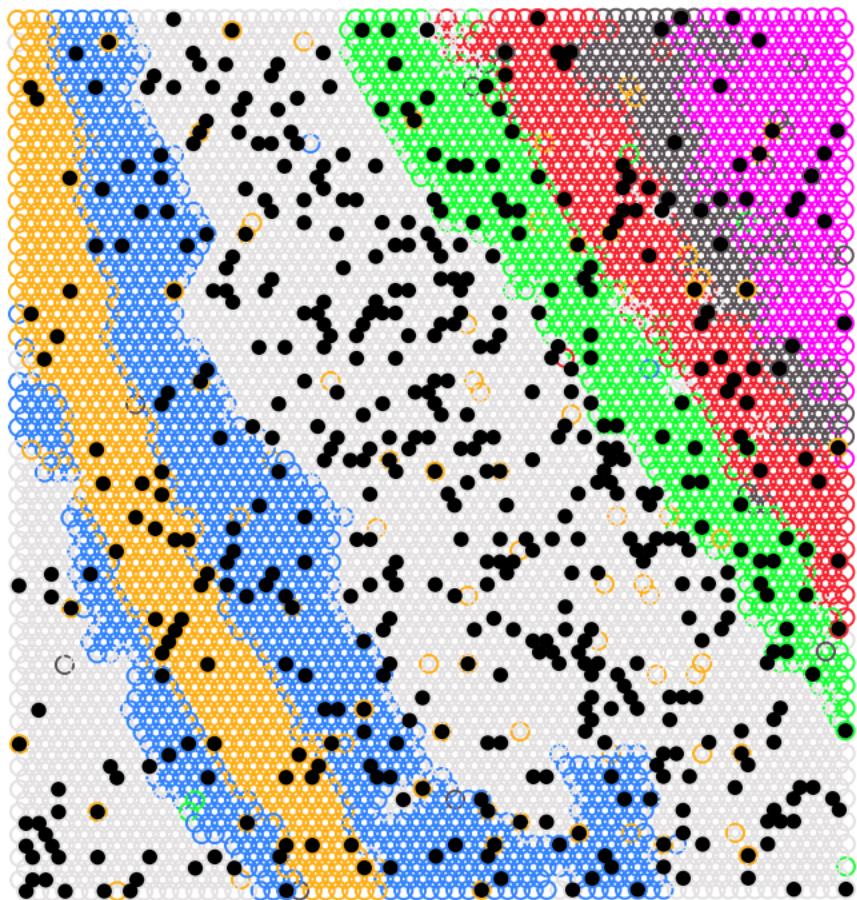
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13F27-293_A1



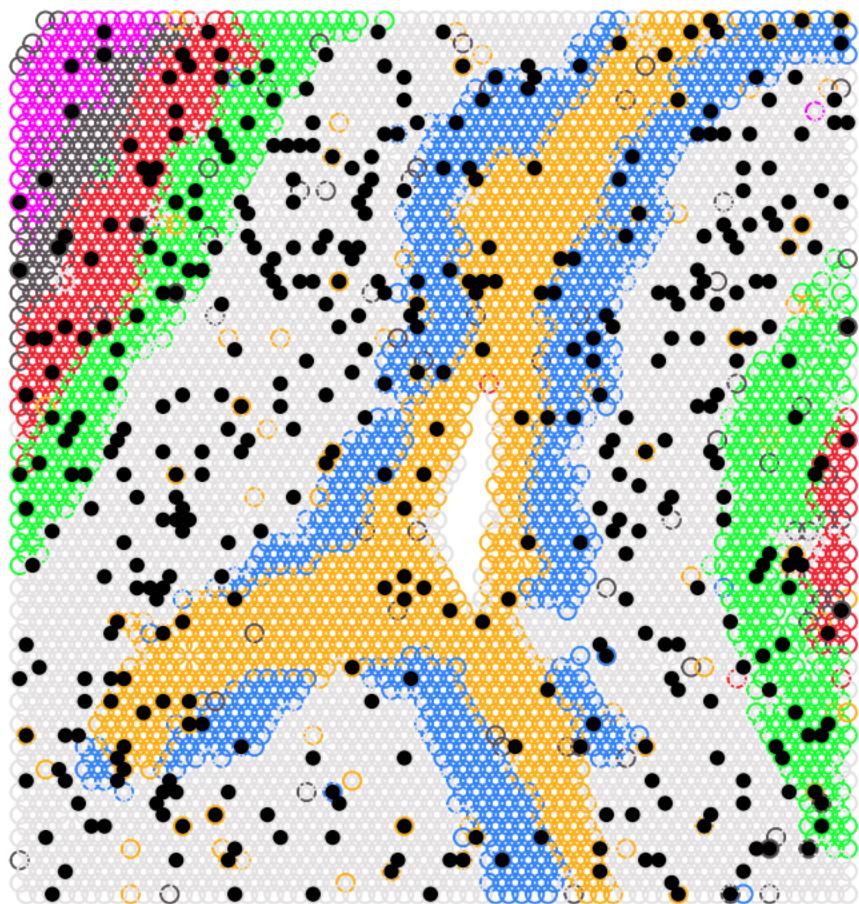
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13F27-293_B1



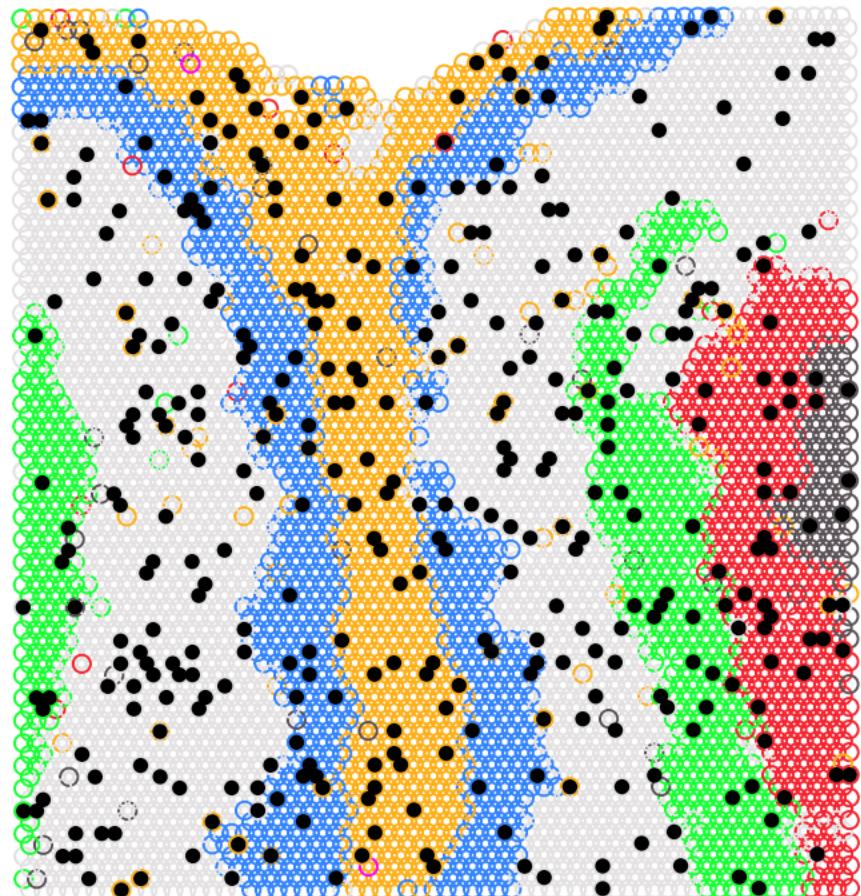
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13F27-293_C1



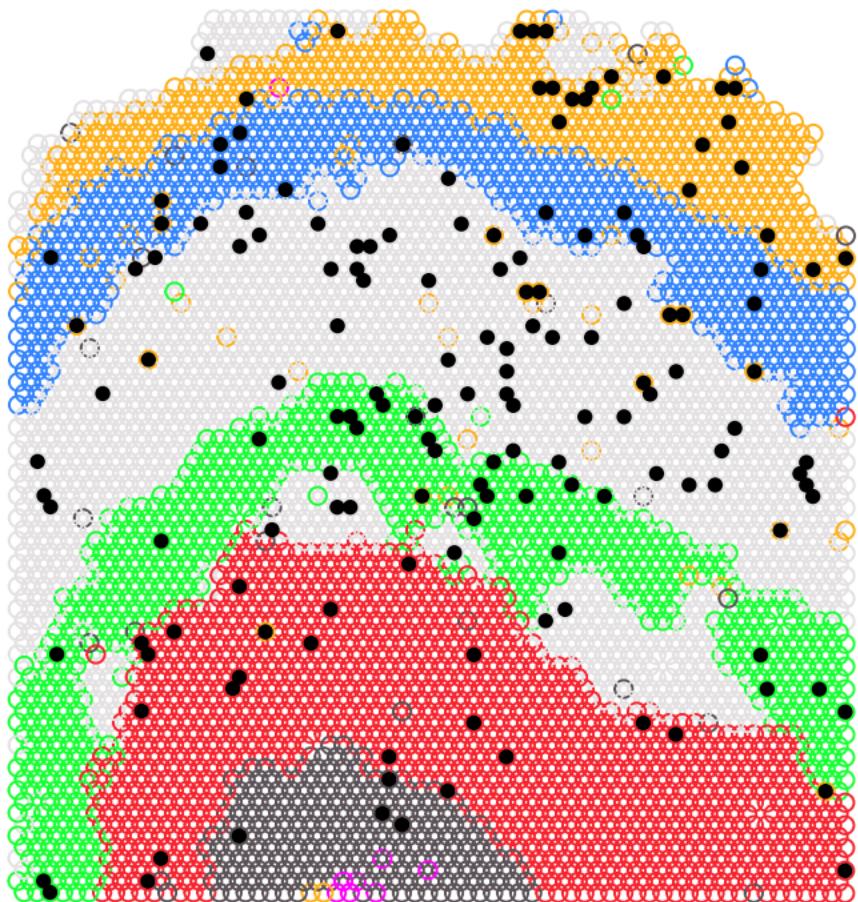
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13F27-293_D1



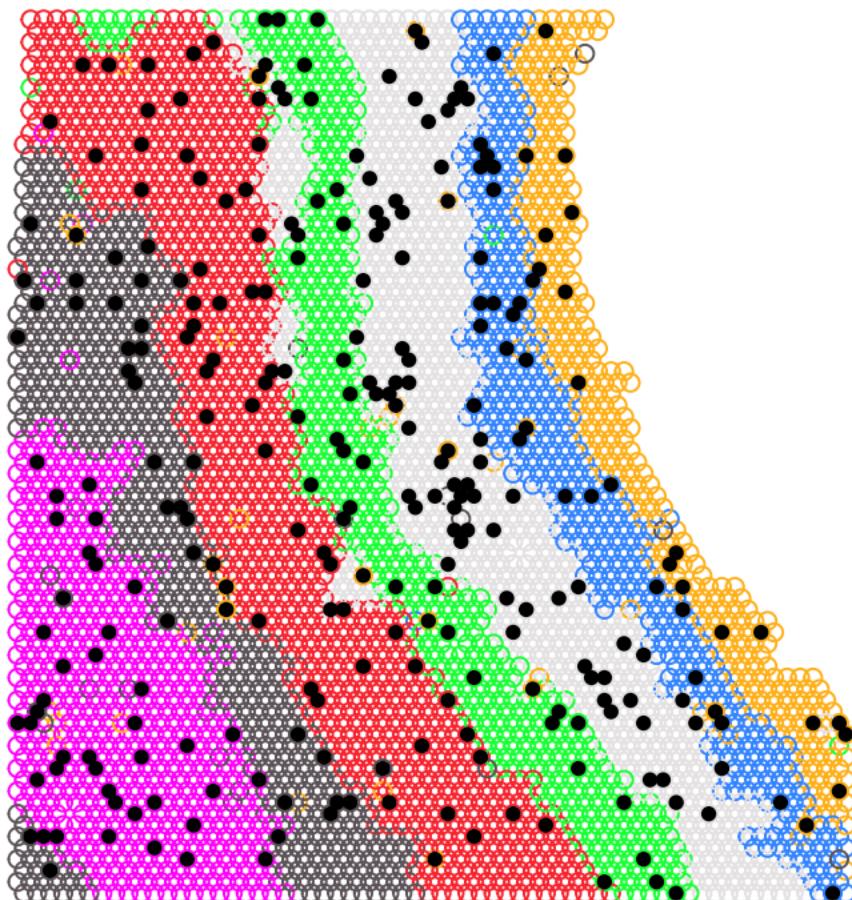
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13F27-294_A1



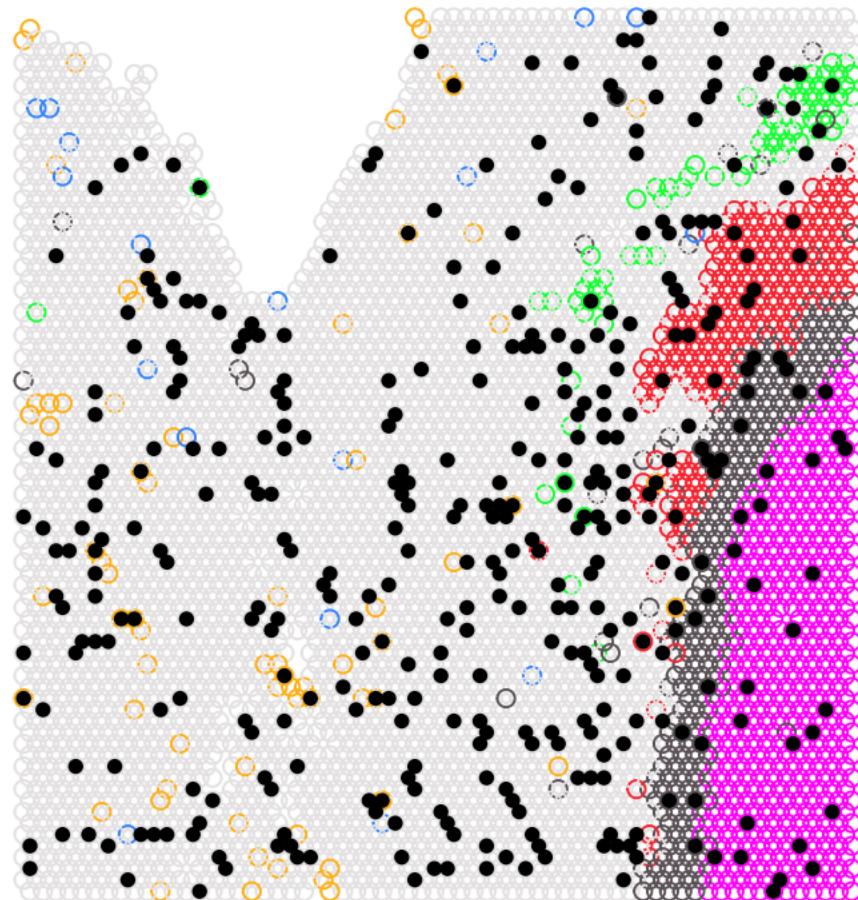
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13F27-294_B1



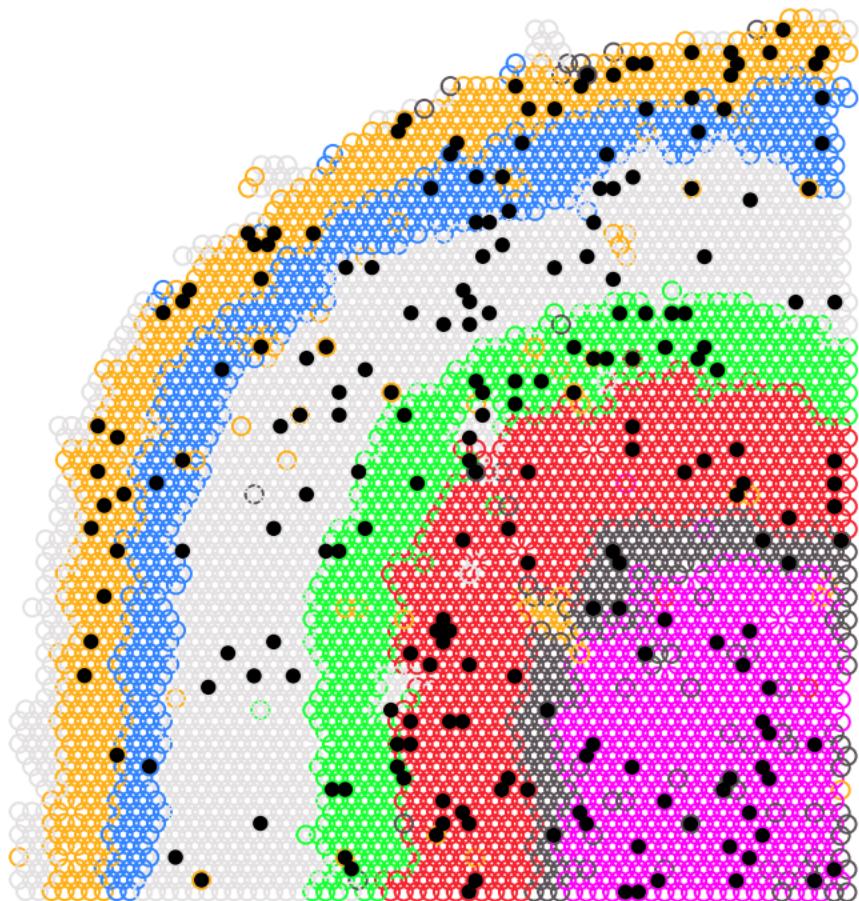
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13F27-294_C1



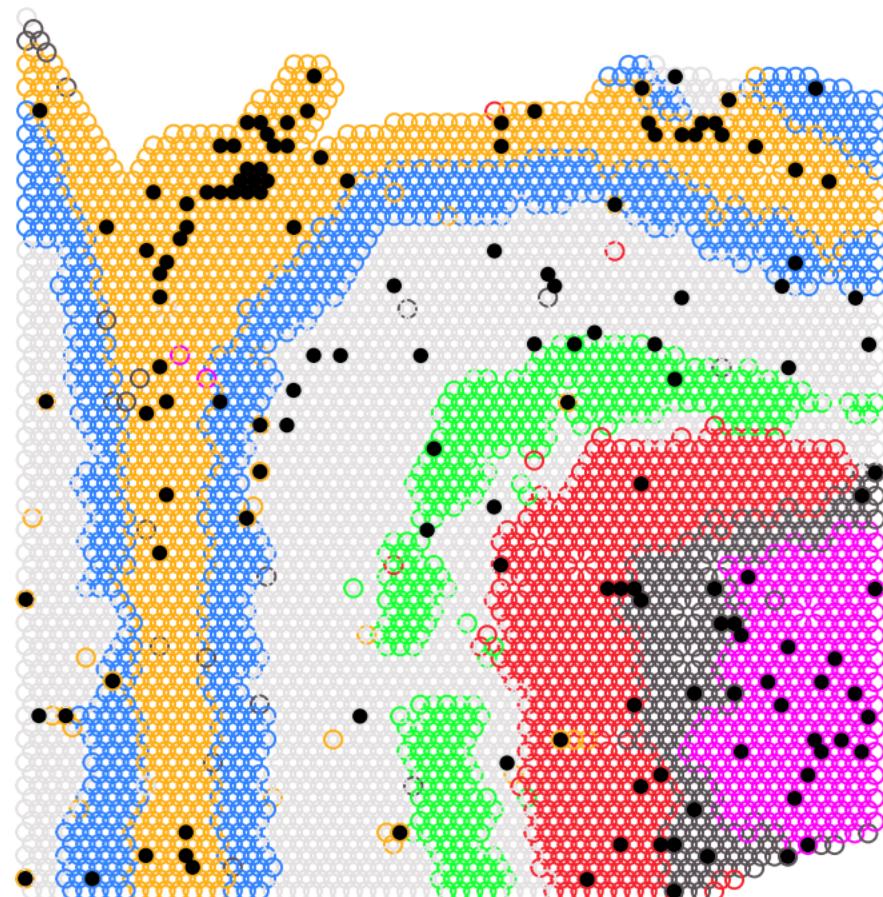
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13F27-294_D1



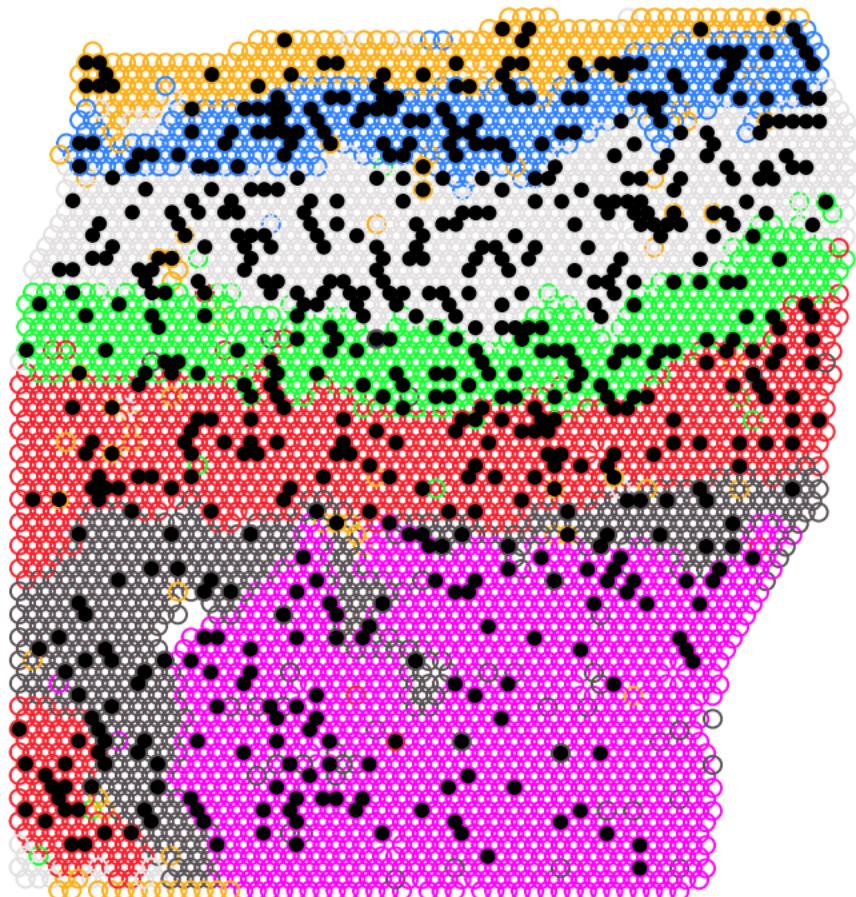
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13F27-295_A1



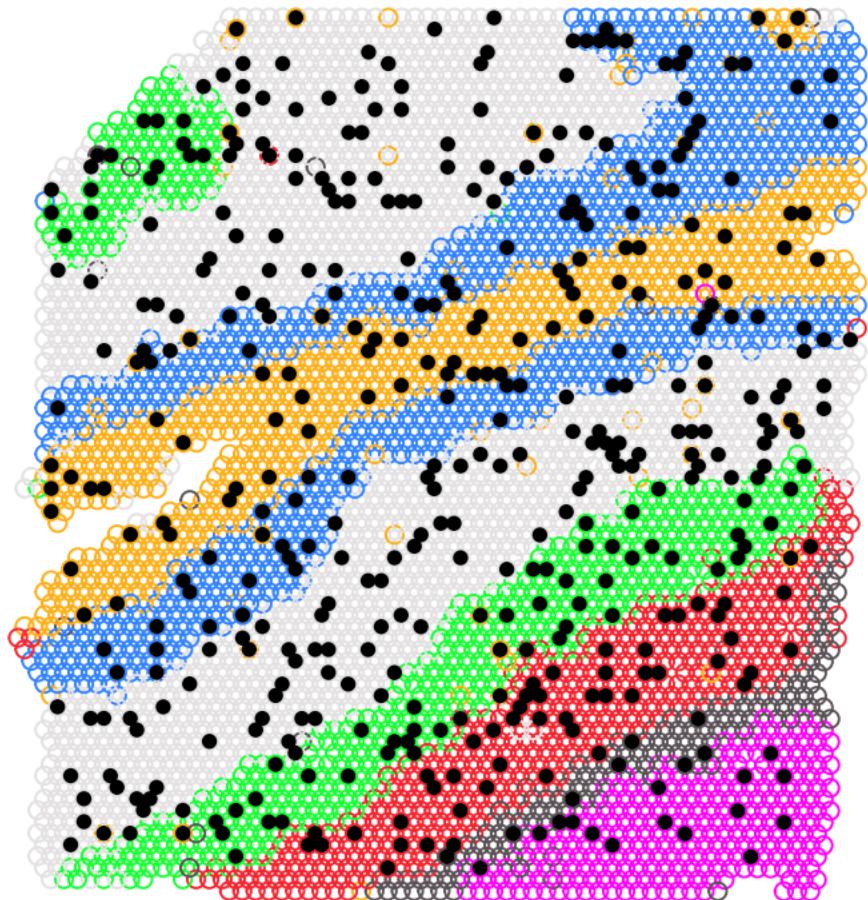
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13F27-295_B1



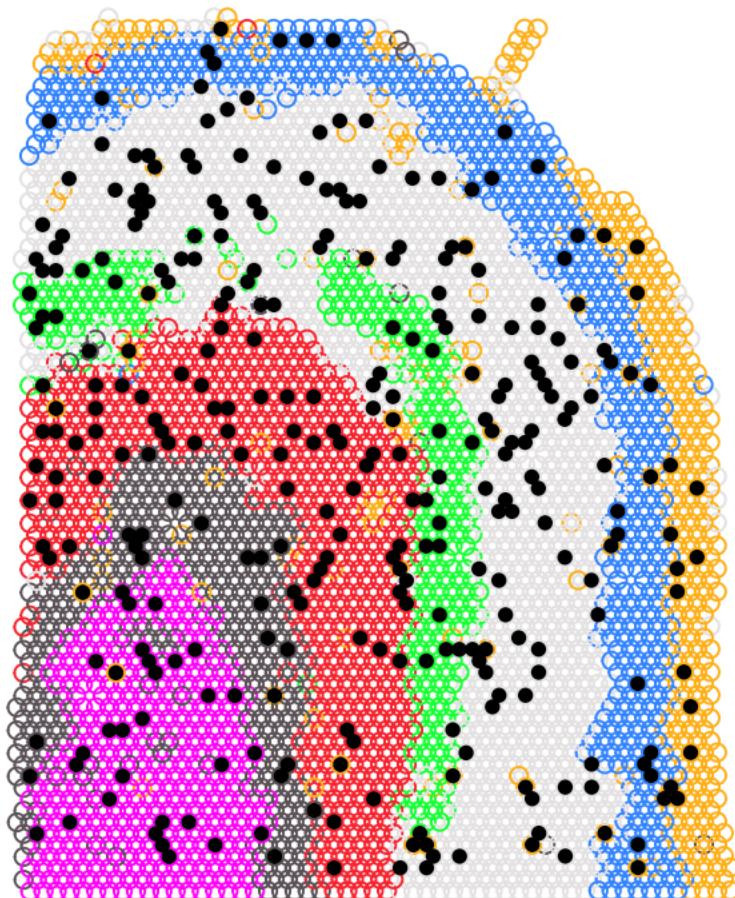
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13F27-295_C1



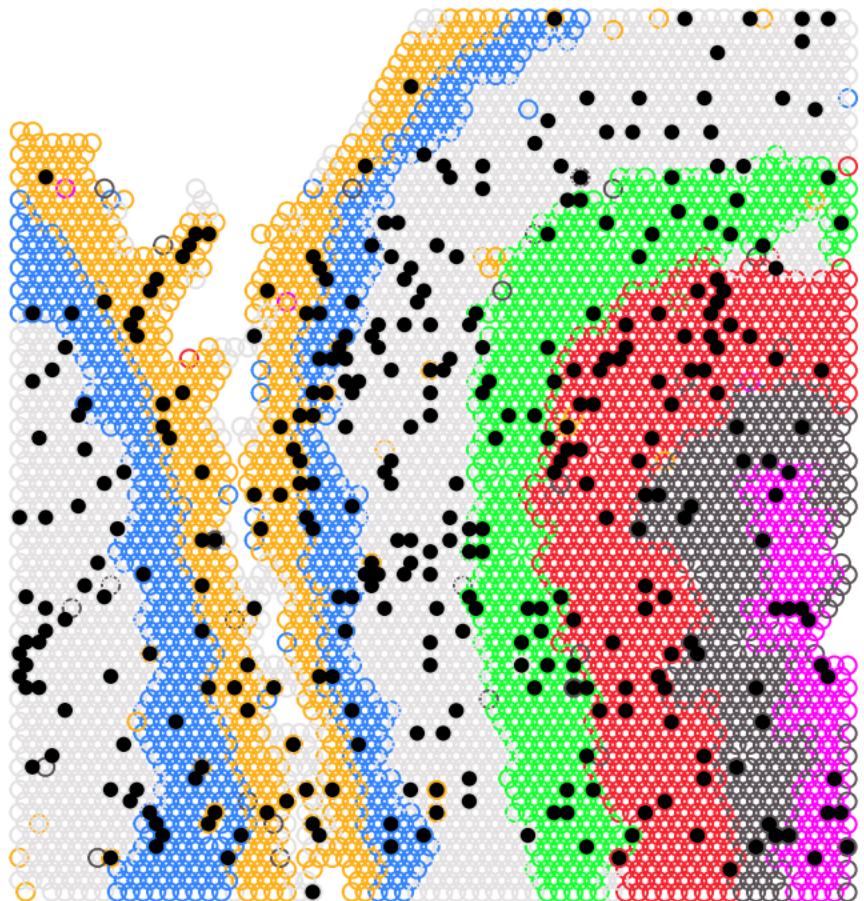
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13F27-295_D1



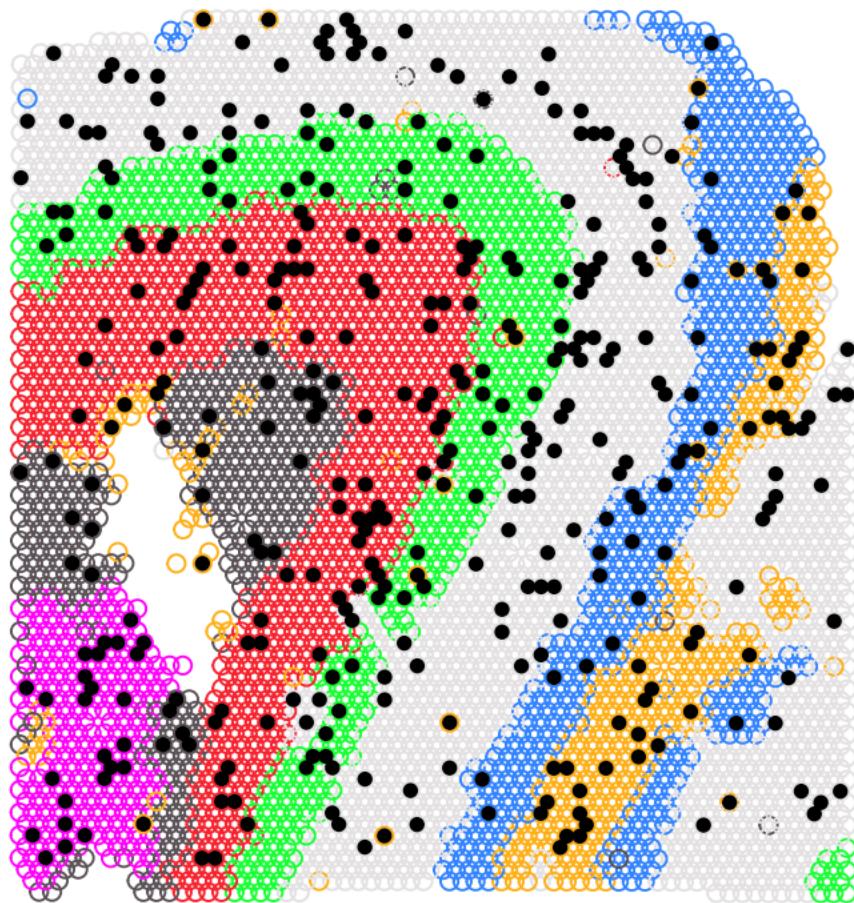
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13F27-296_A1



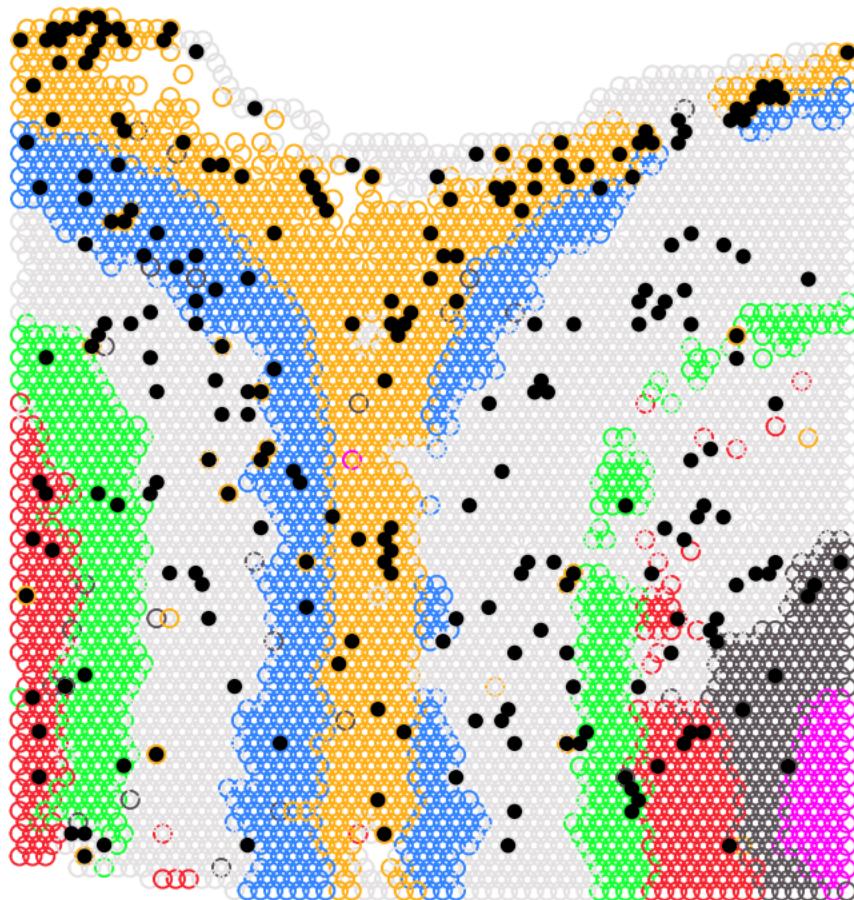
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13F27-296_B1



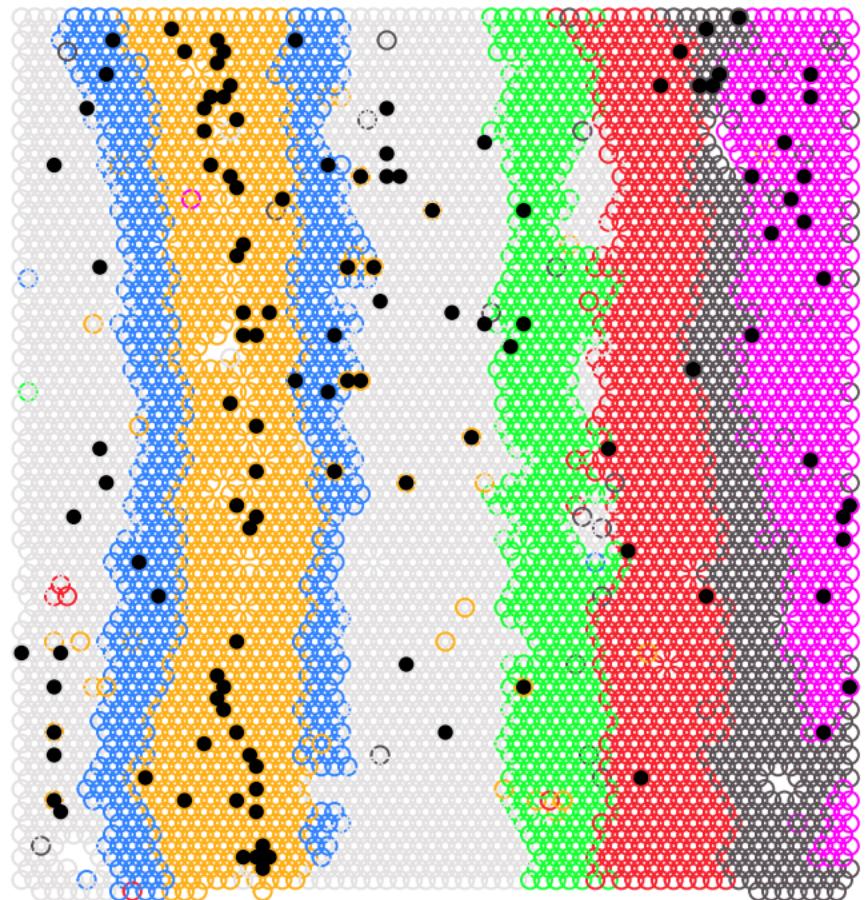
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13F27-296_C1



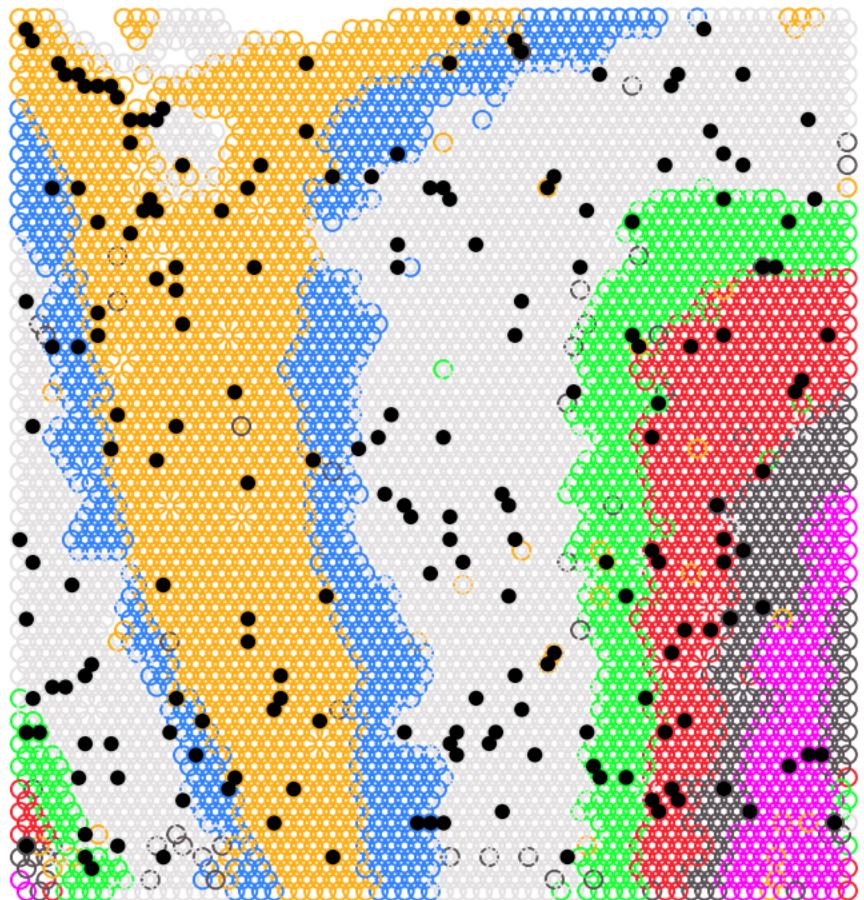
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13F27-296_D1



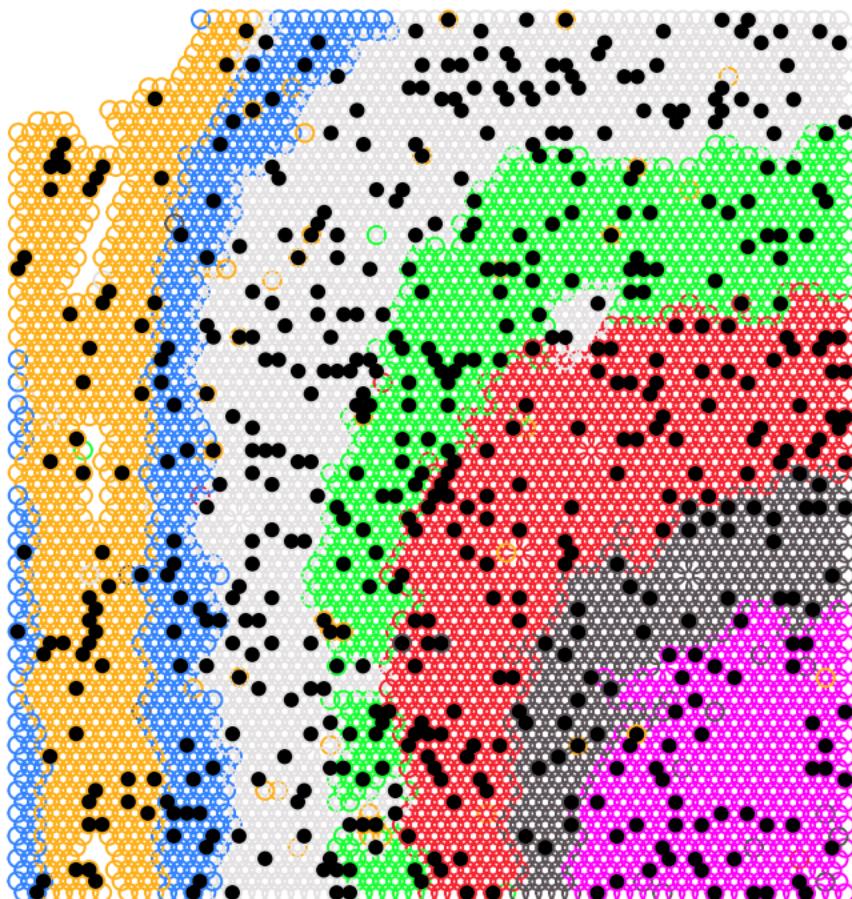
PRECAST_07

- L1 (spd07)**
- L2/3 (spd06)**
- L3/4 (spd02)**
- L5 (spd05)**
- L6 (spd03)**
- L6/WM (spd01)**
- WM (spd04)**

vasc_pos

- FALSE**
- TRUE**

V13M06-340_A1



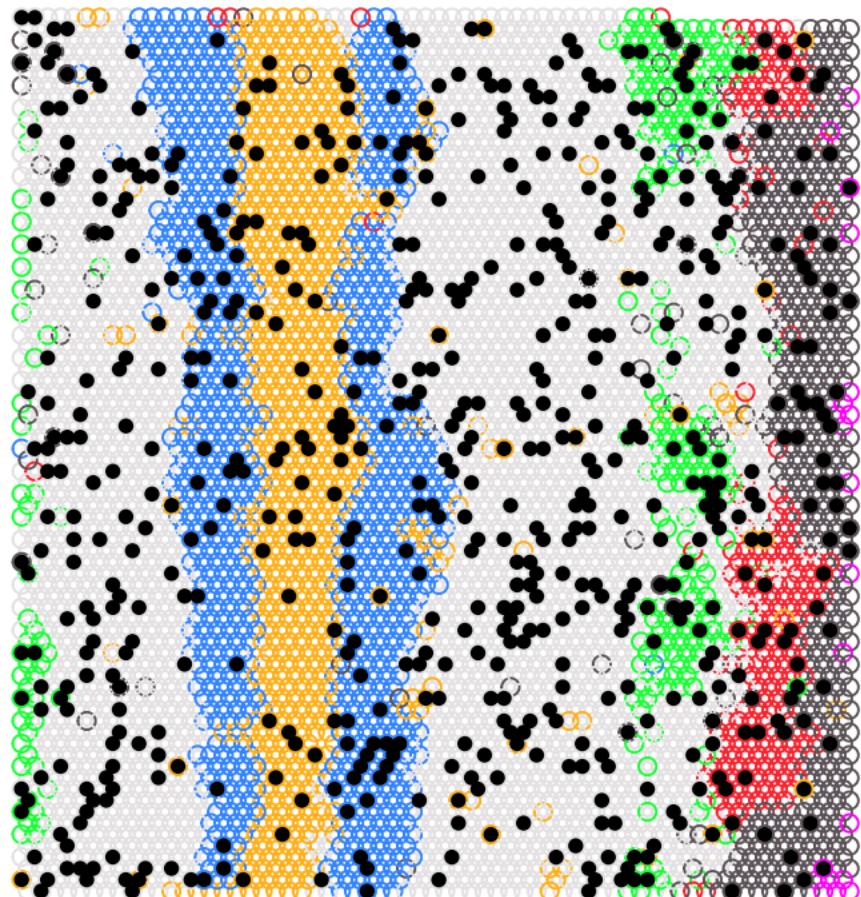
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06-340_B1



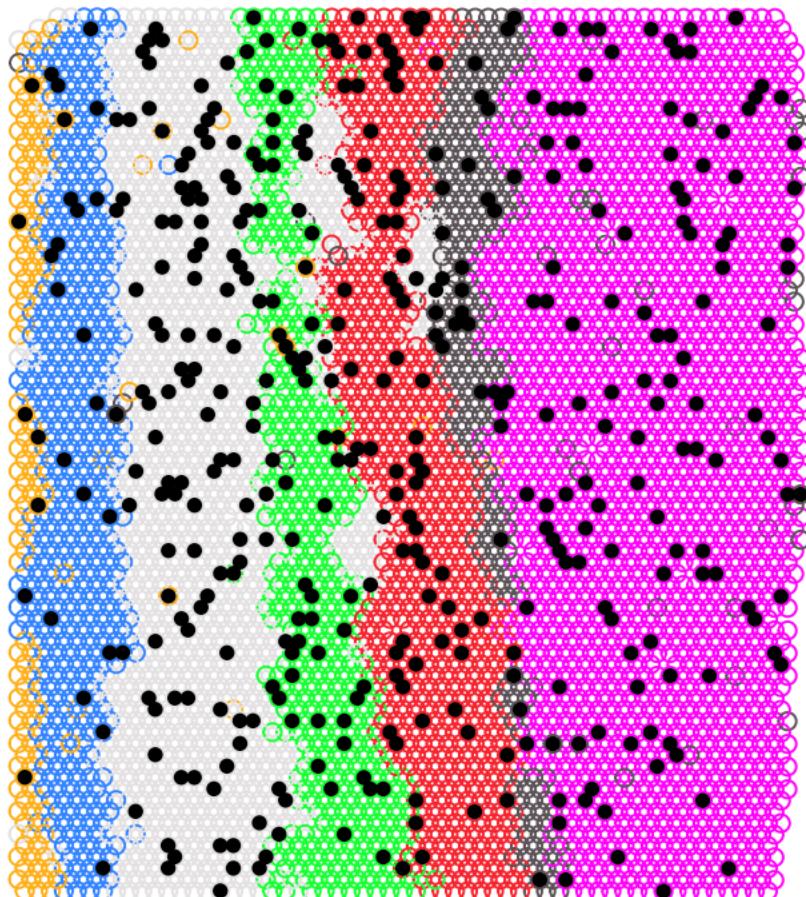
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06–340_C1



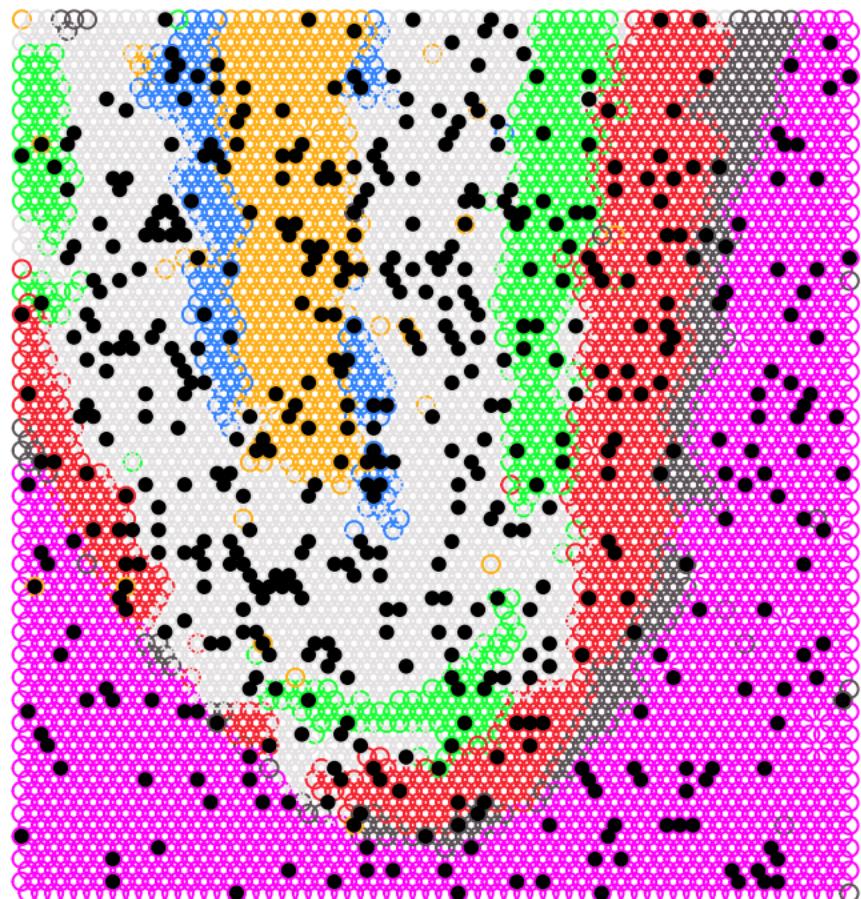
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06-340_D1



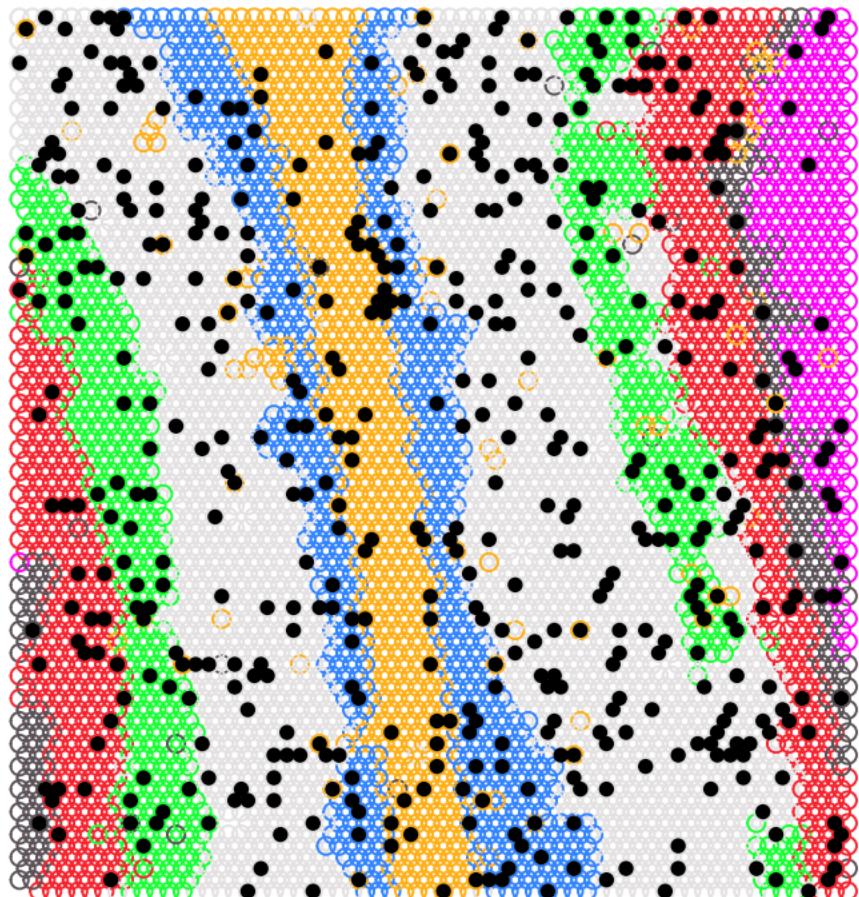
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06-342_A1



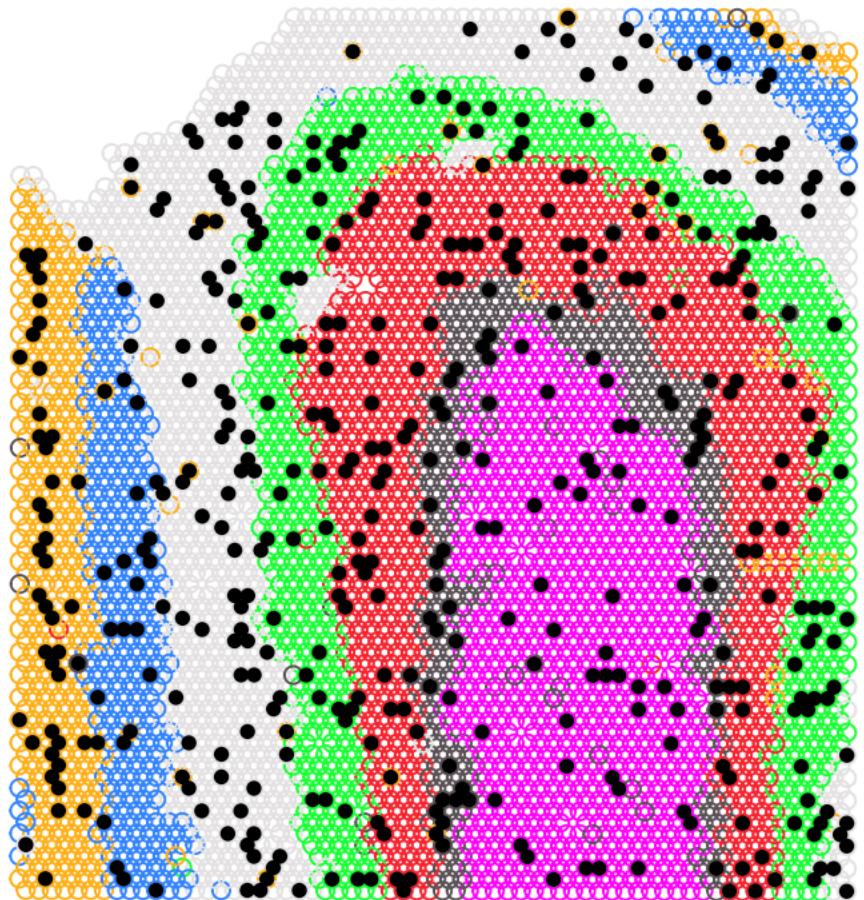
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06-342_B1



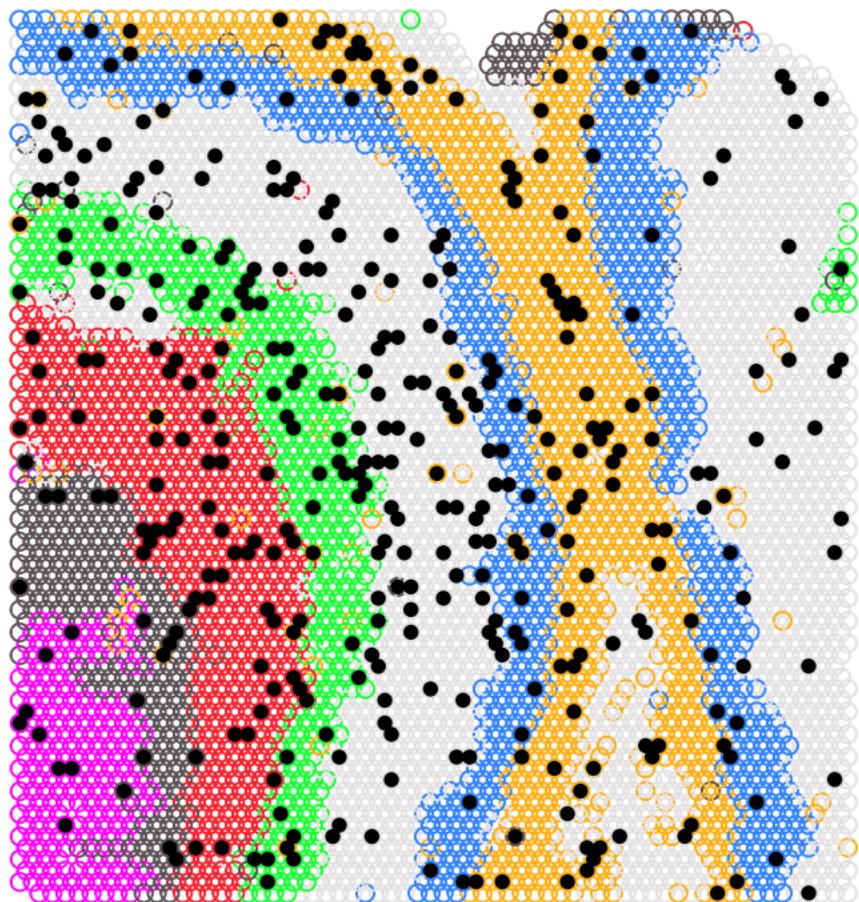
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06-342_C1



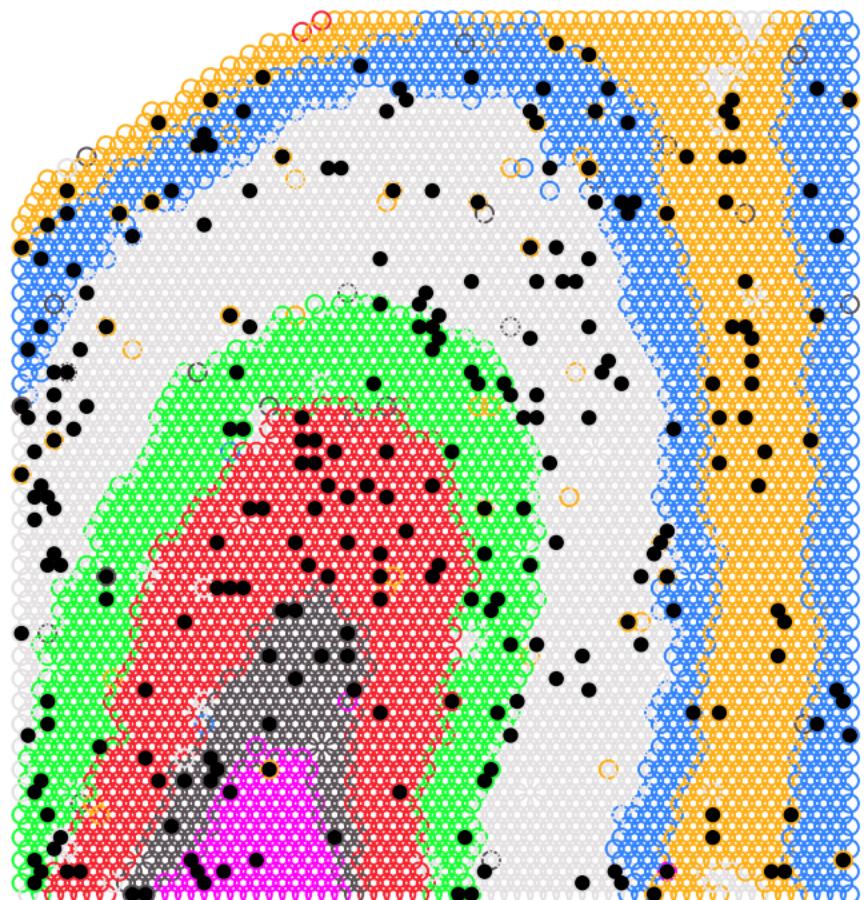
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06-342_D1



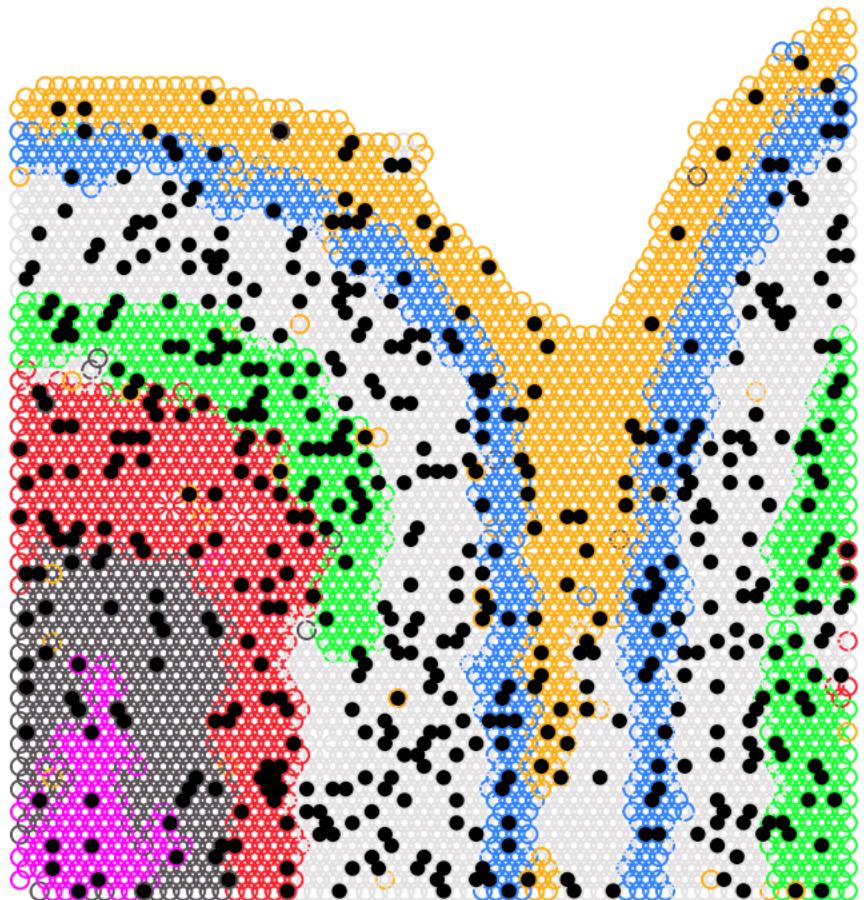
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06-343_A1



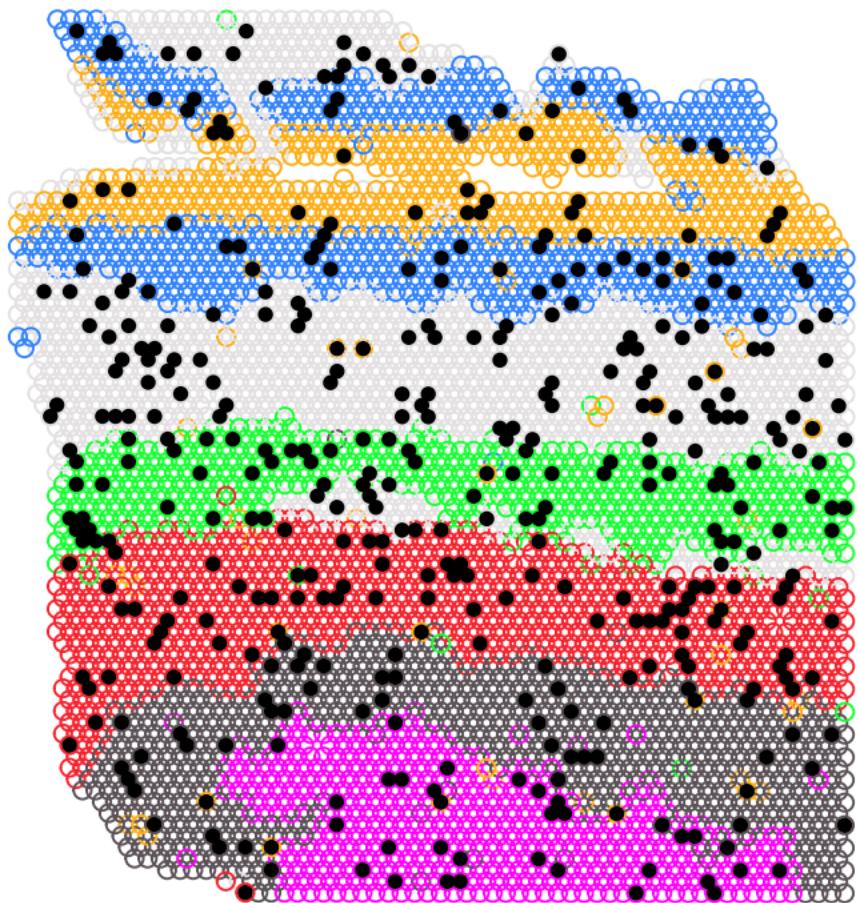
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06-343_B1



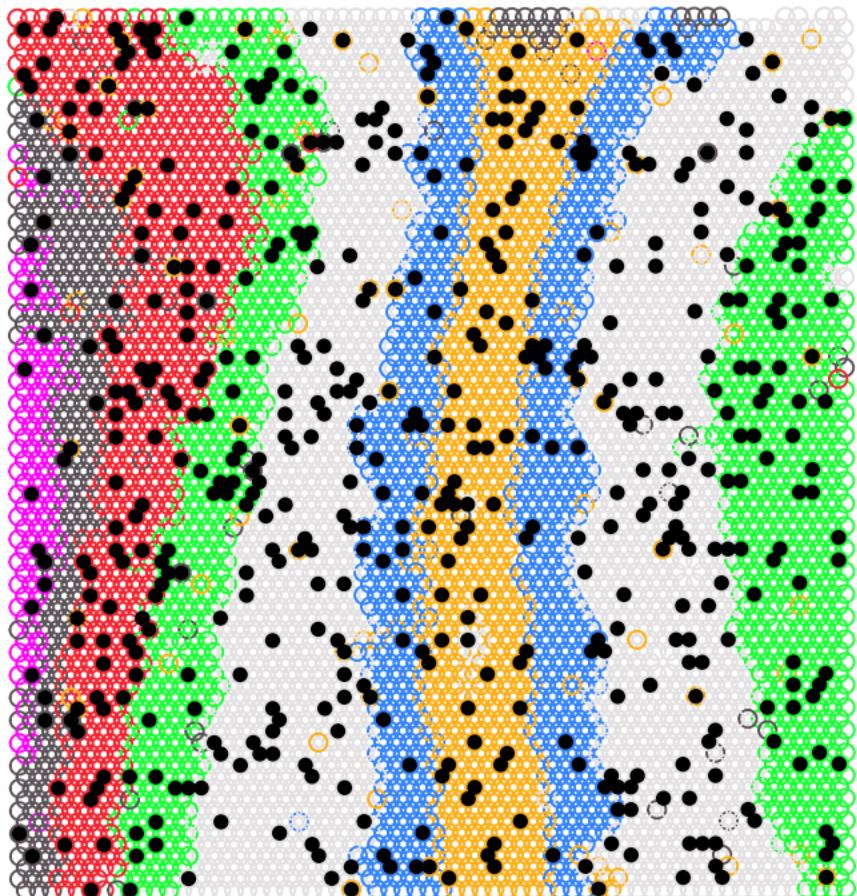
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06-343_C1



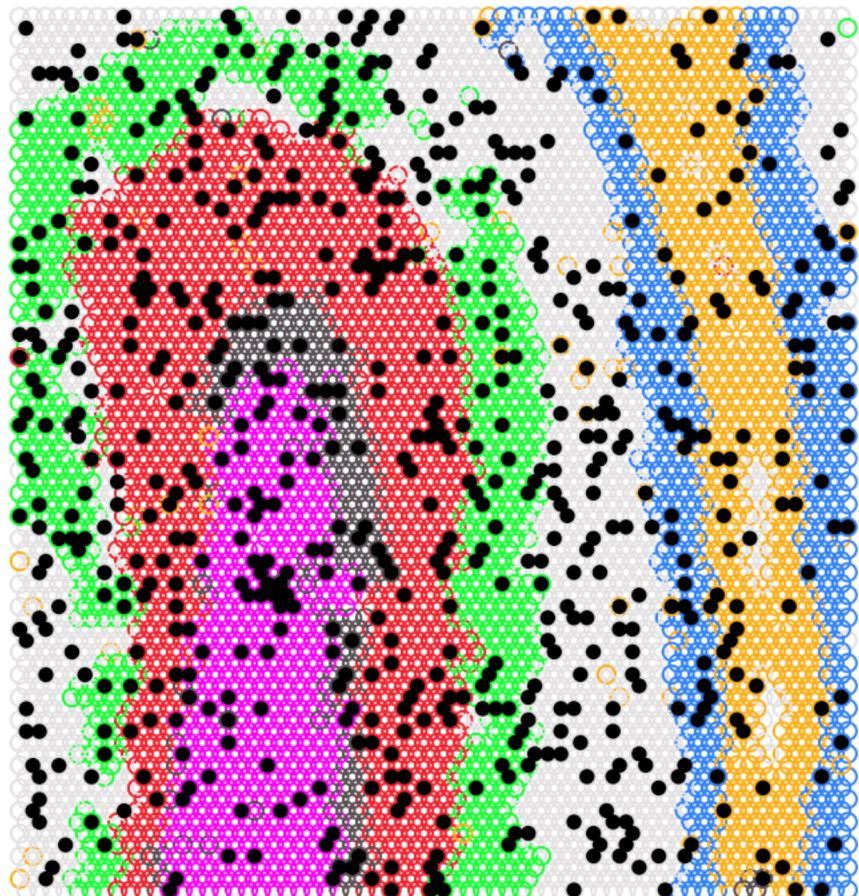
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06-343_D1



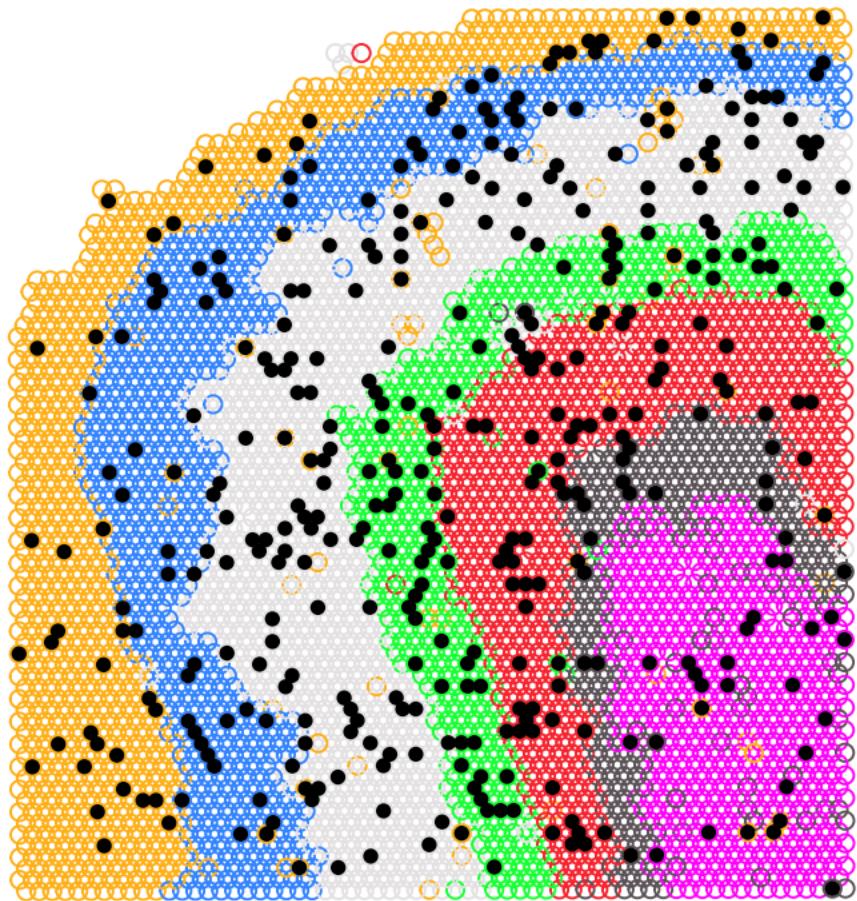
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06-344_A1



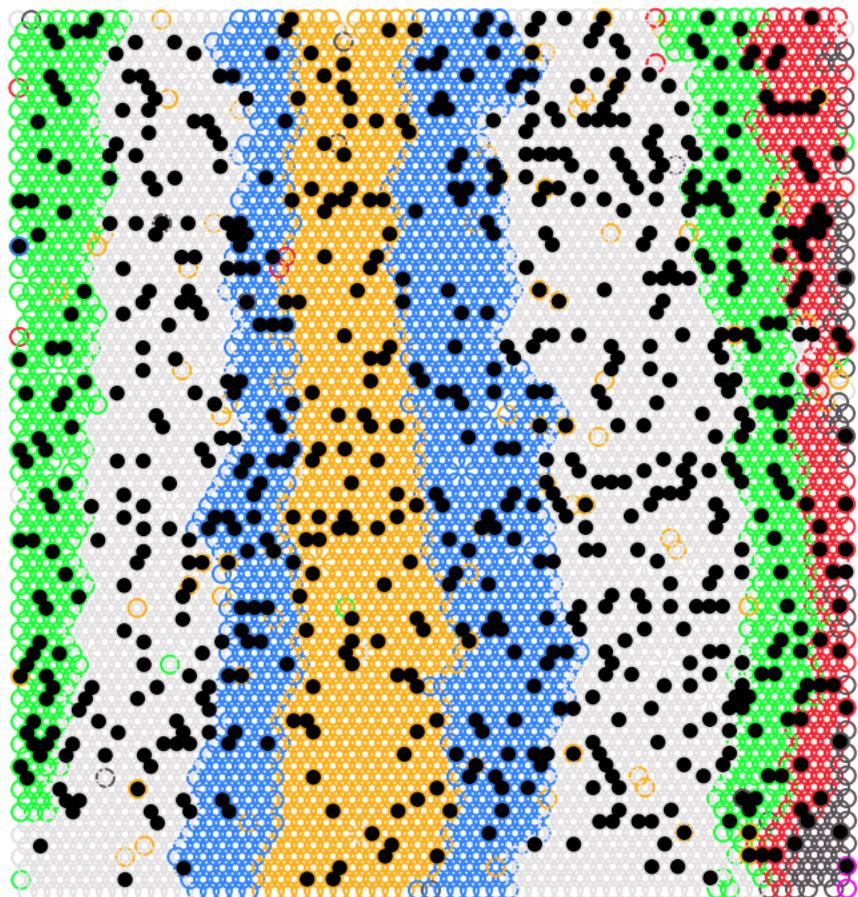
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06-344_B1



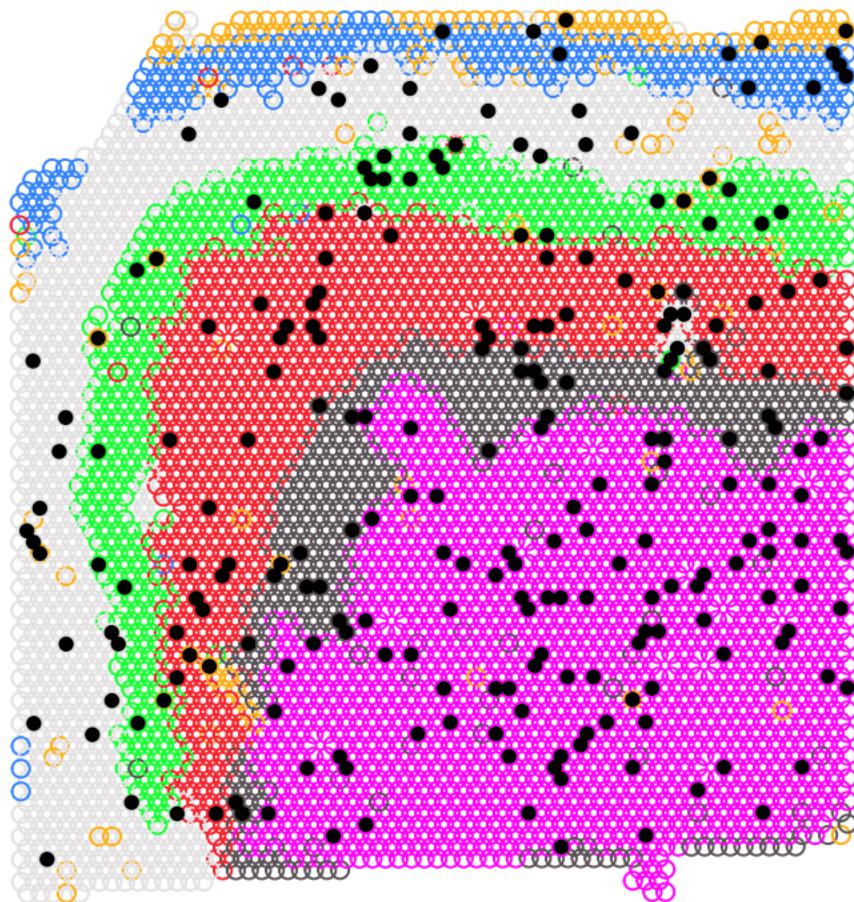
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06-344_C1



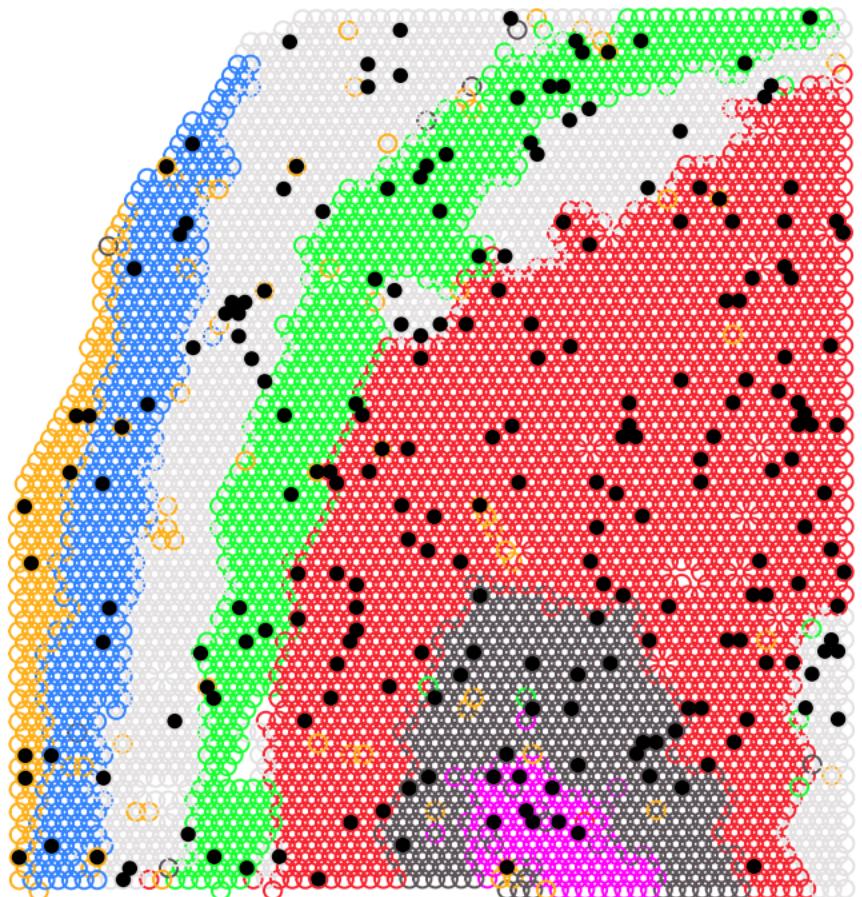
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13M06-344_D1



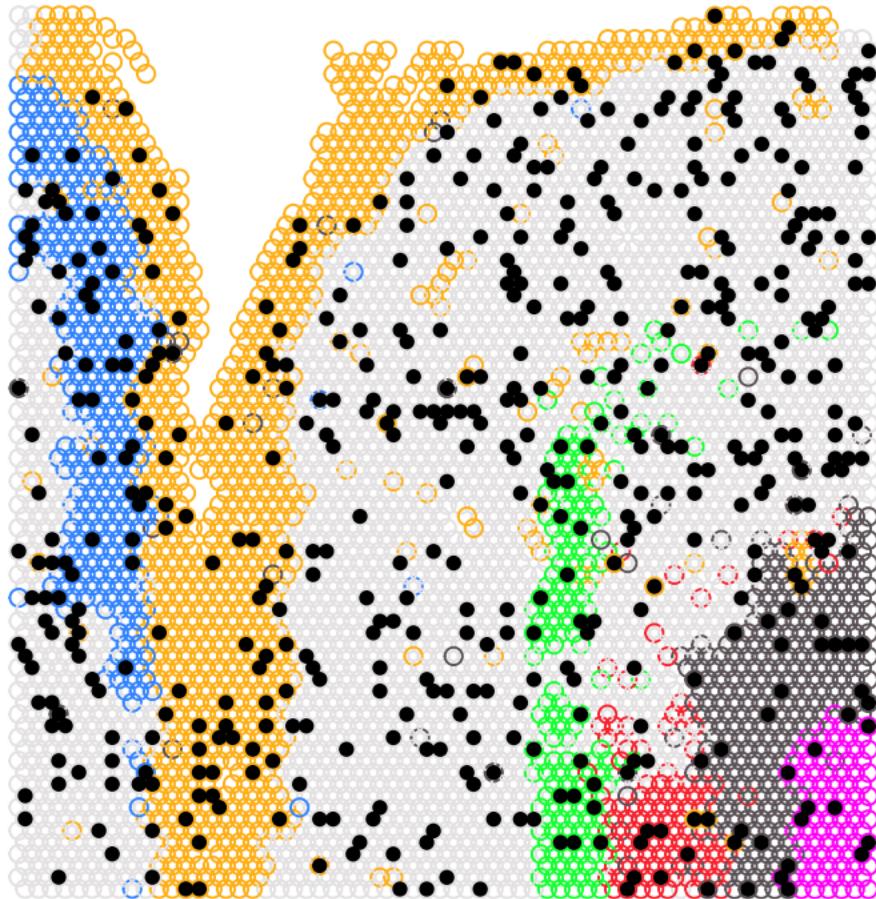
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

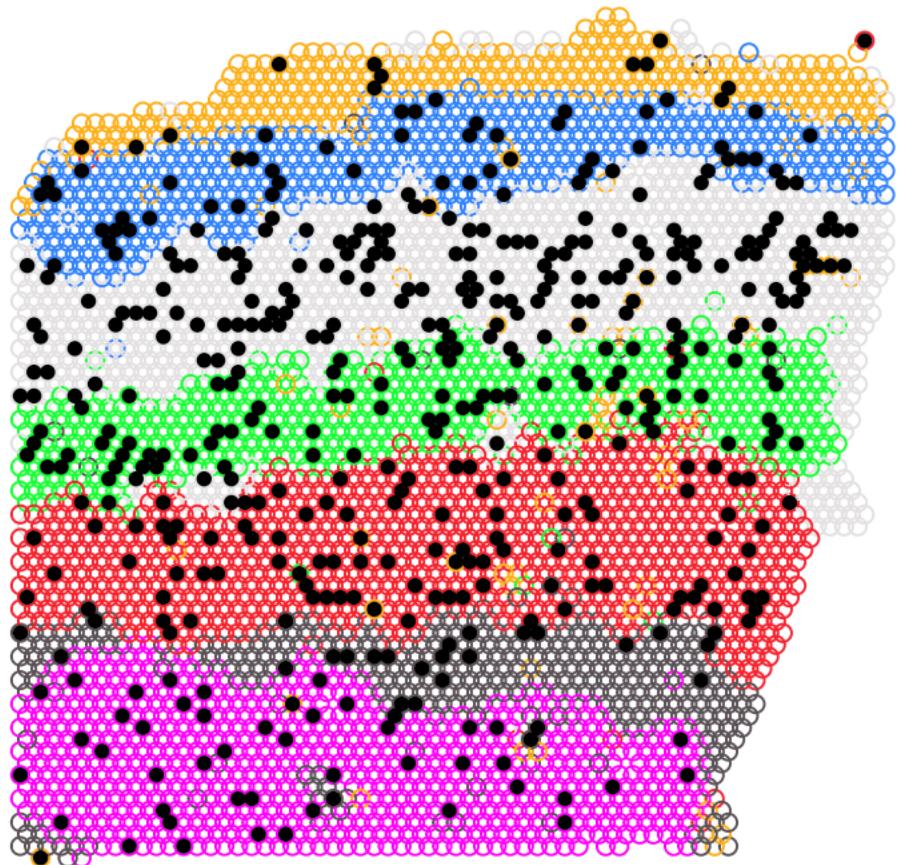
vasc_pos

- FALSE
- TRUE

V13F27-336_A1



V13F27-336_B1



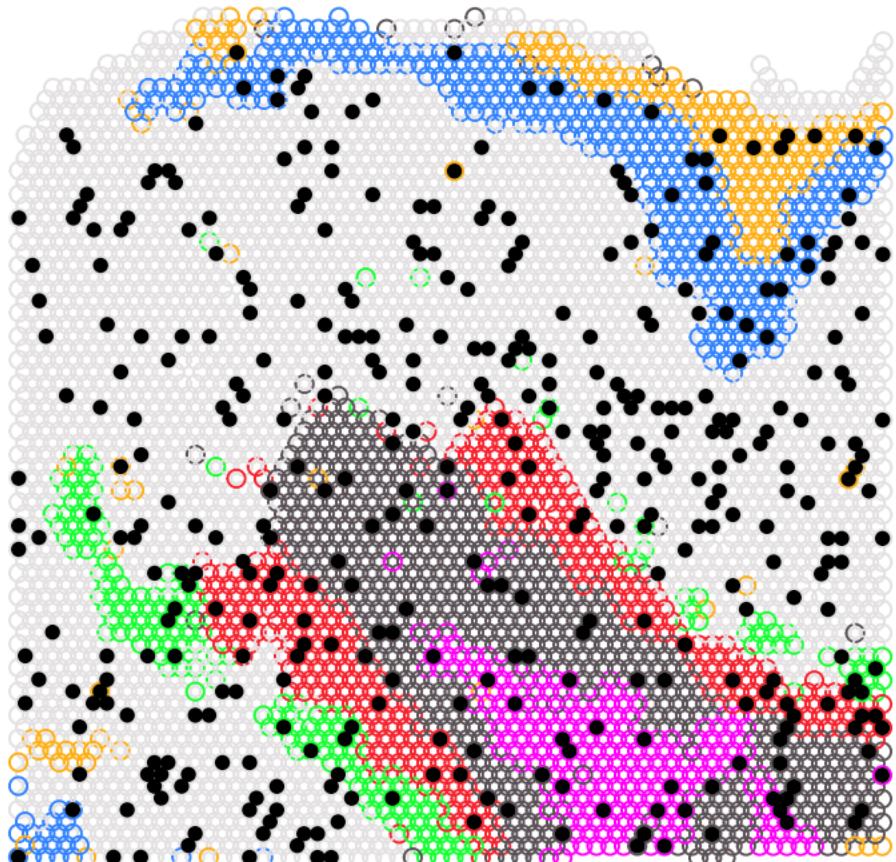
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13F27-336_C1



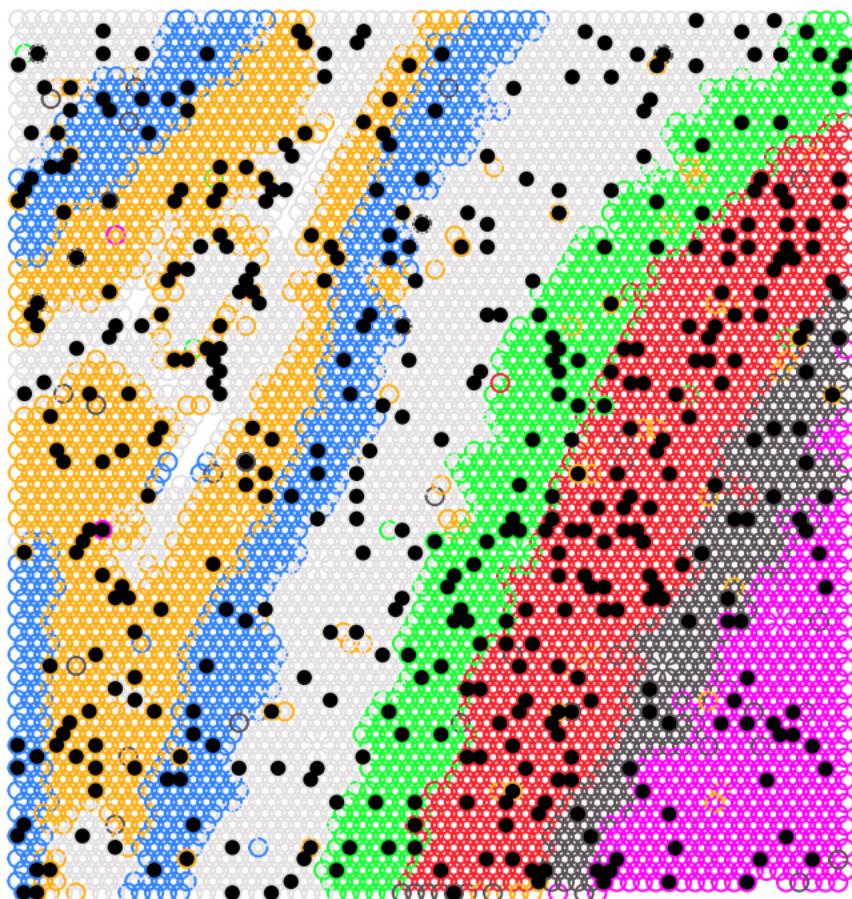
PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE

V13F27-336_D1



PRECAST_07

- L1 (spd07)
- L2/3 (spd06)
- L3/4 (spd02)
- L5 (spd05)
- L6 (spd03)
- L6/WM (spd01)
- WM (spd04)

vasc_pos

- FALSE
- TRUE