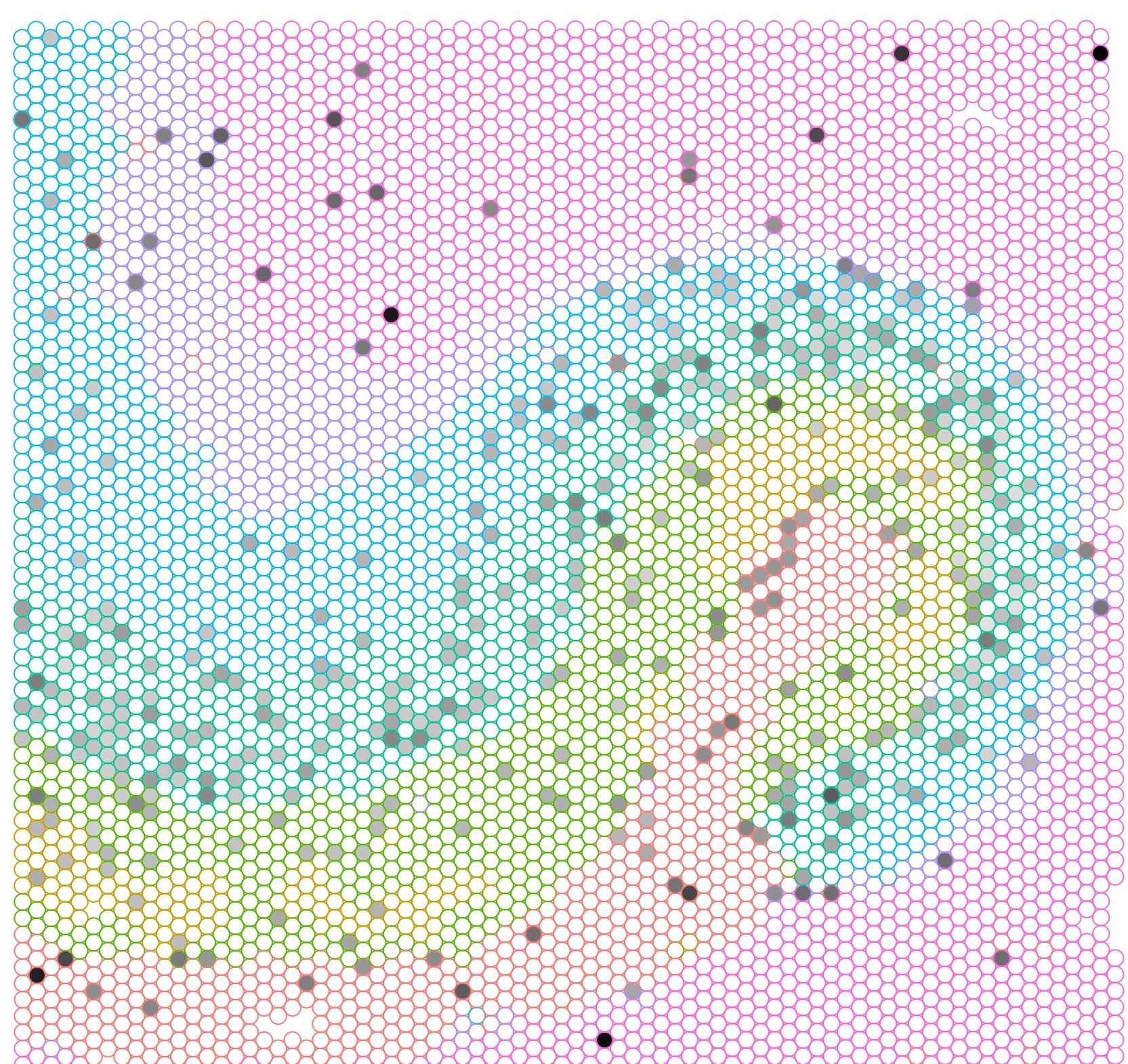
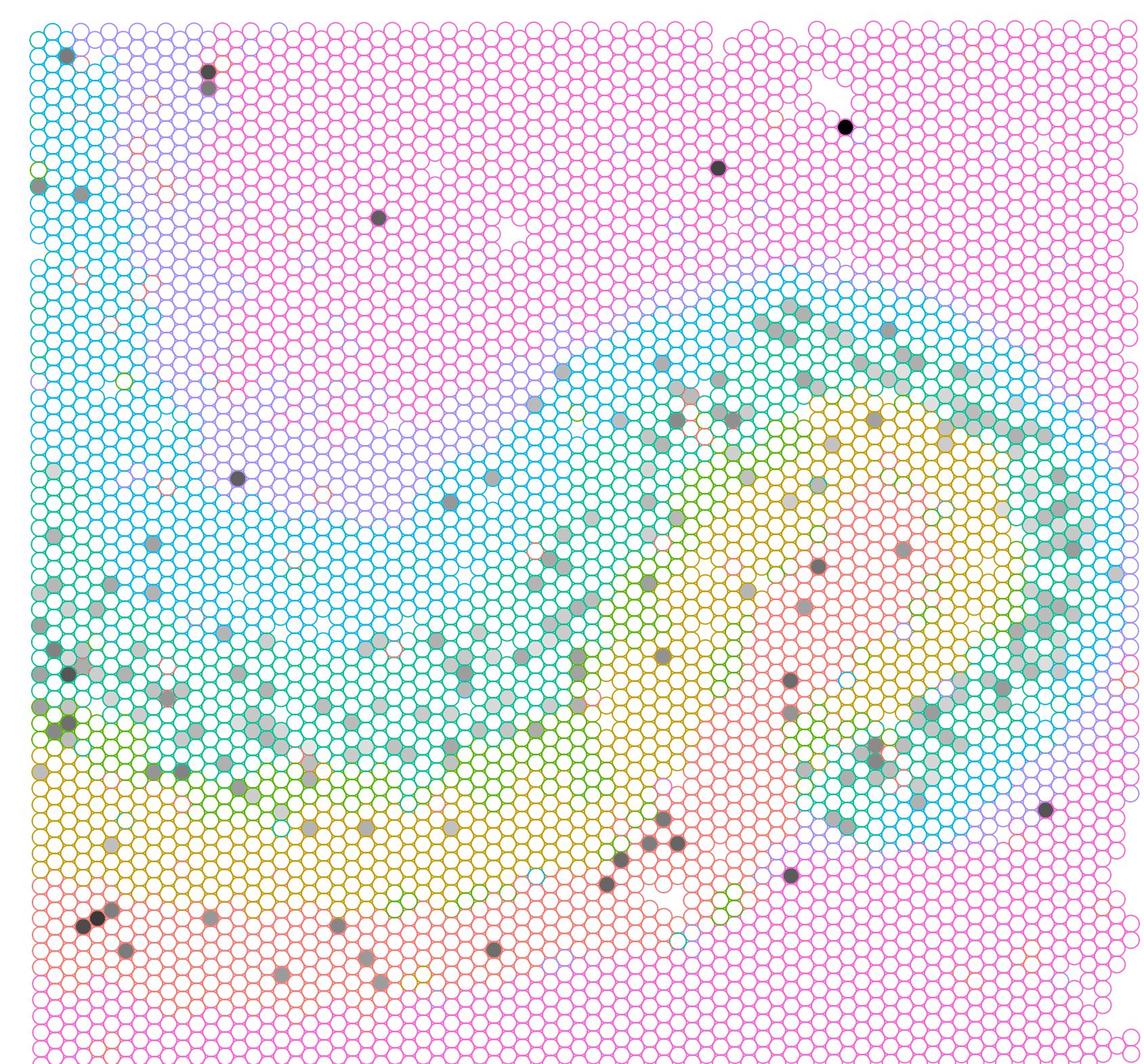


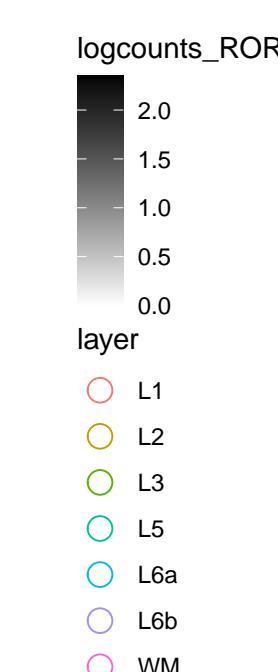
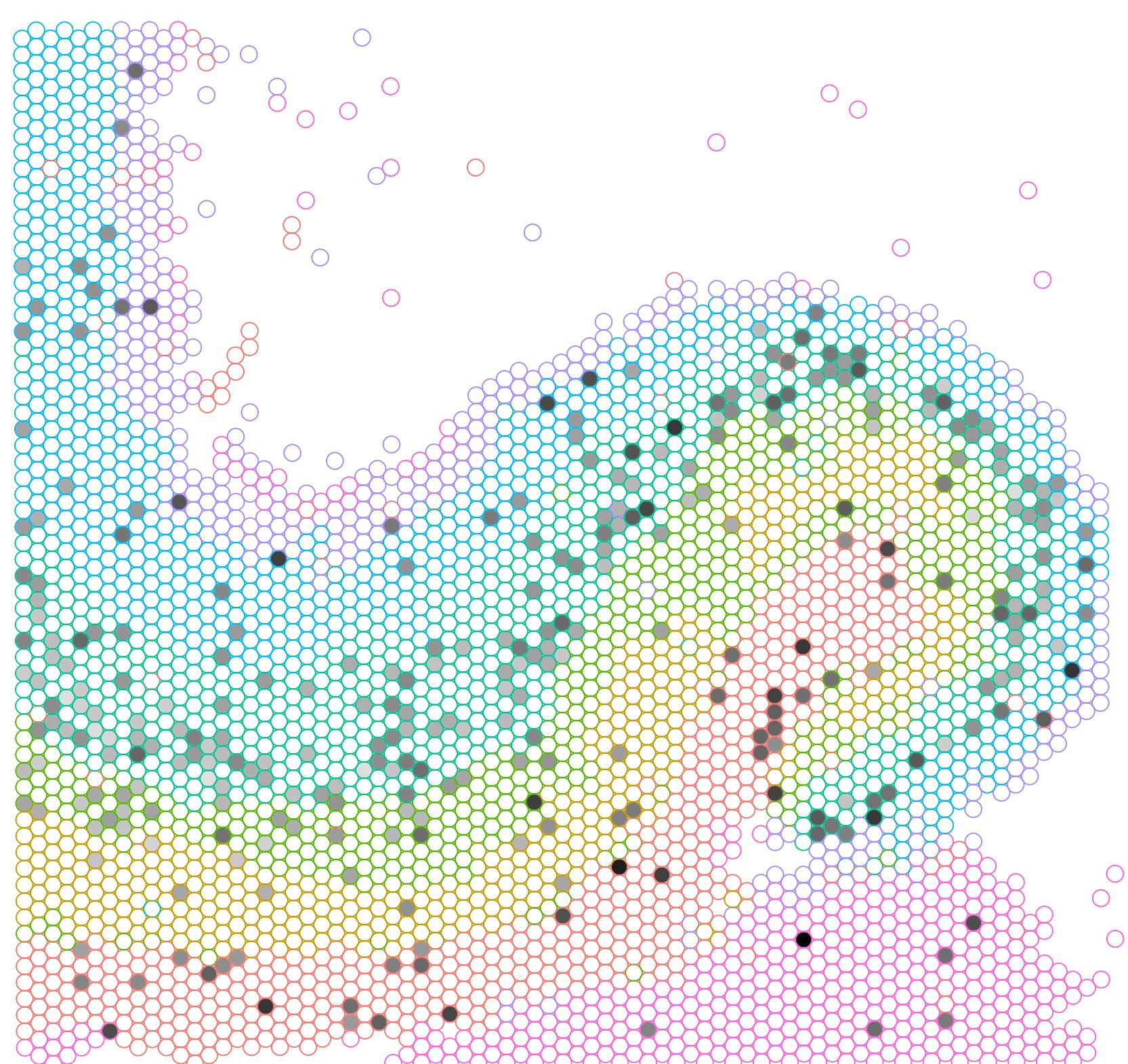
Sample V12J03–002_A1



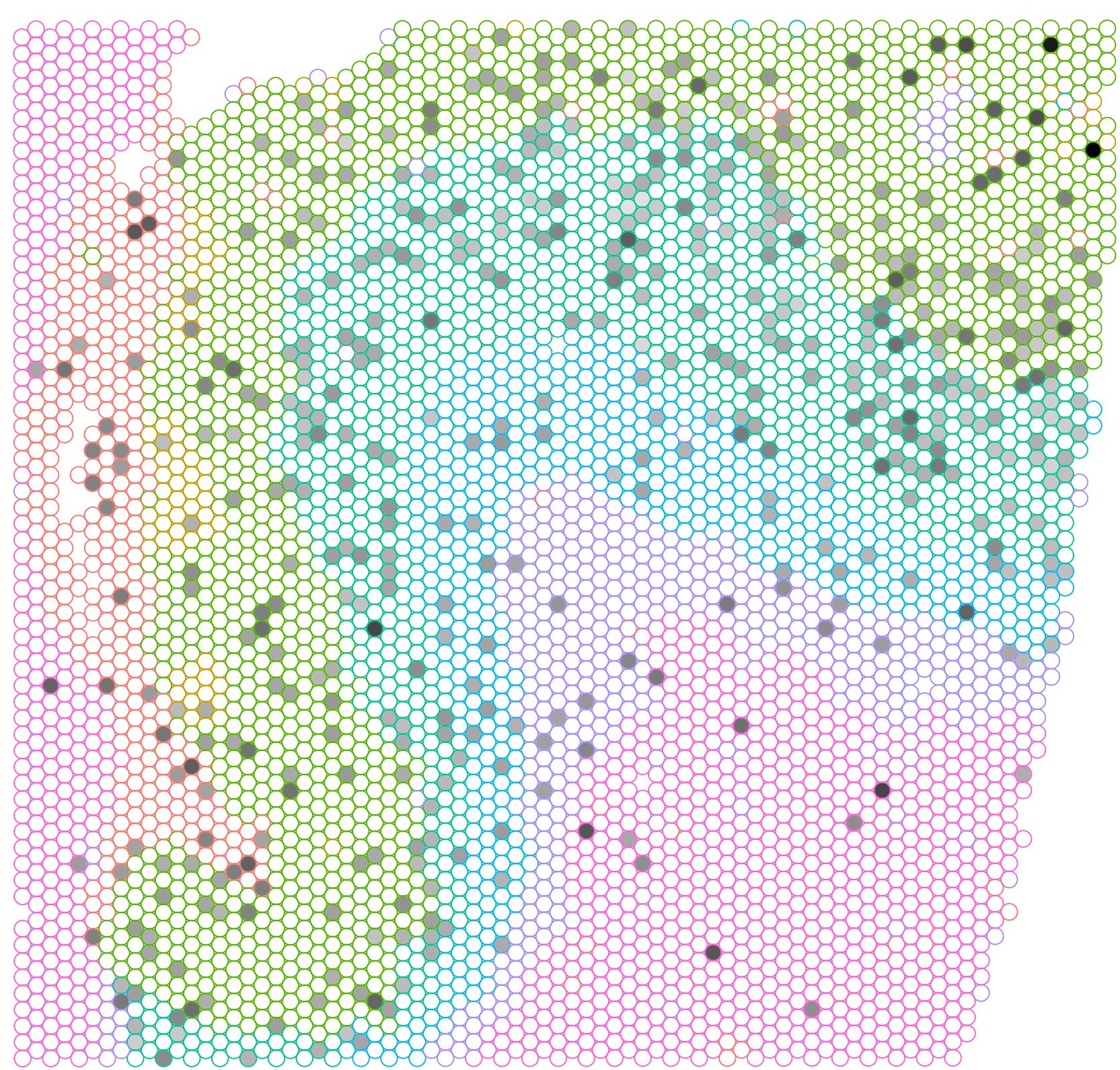
Sample V12N28–331_A1



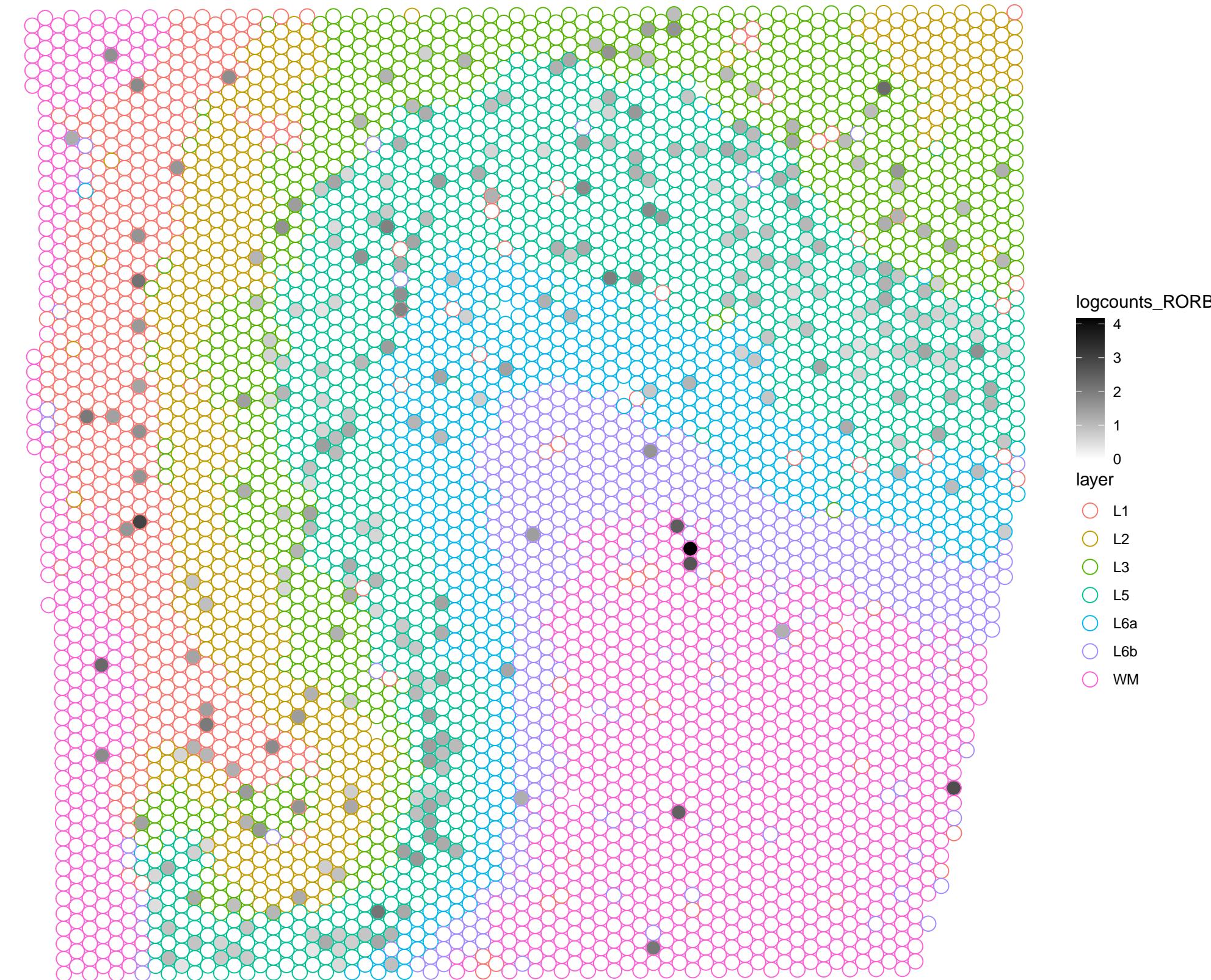
Sample V12N28–332_A1



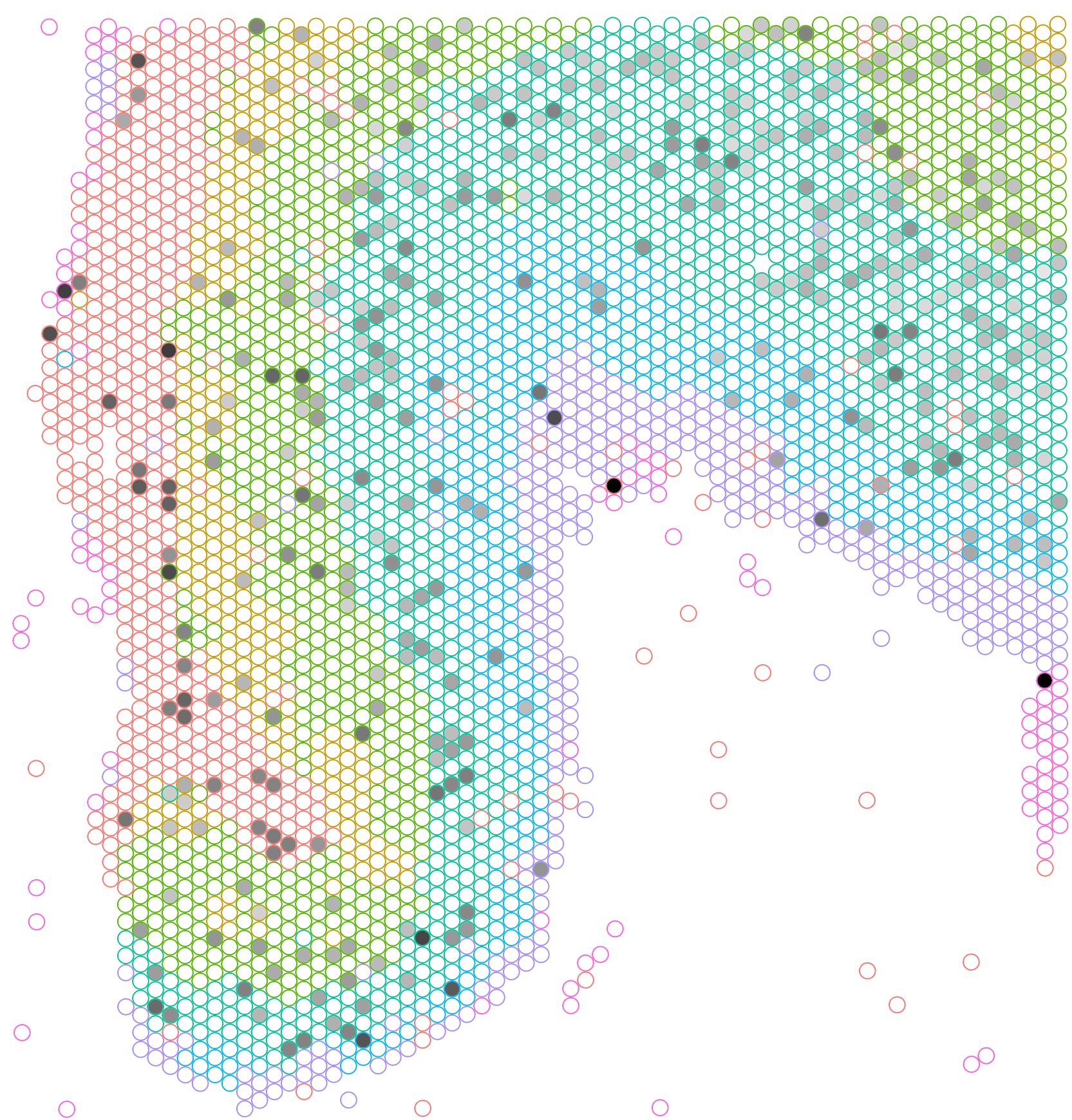
Sample V12J03–002_B1



Sample V12N28–331_B1



Sample V12N28–332_B1



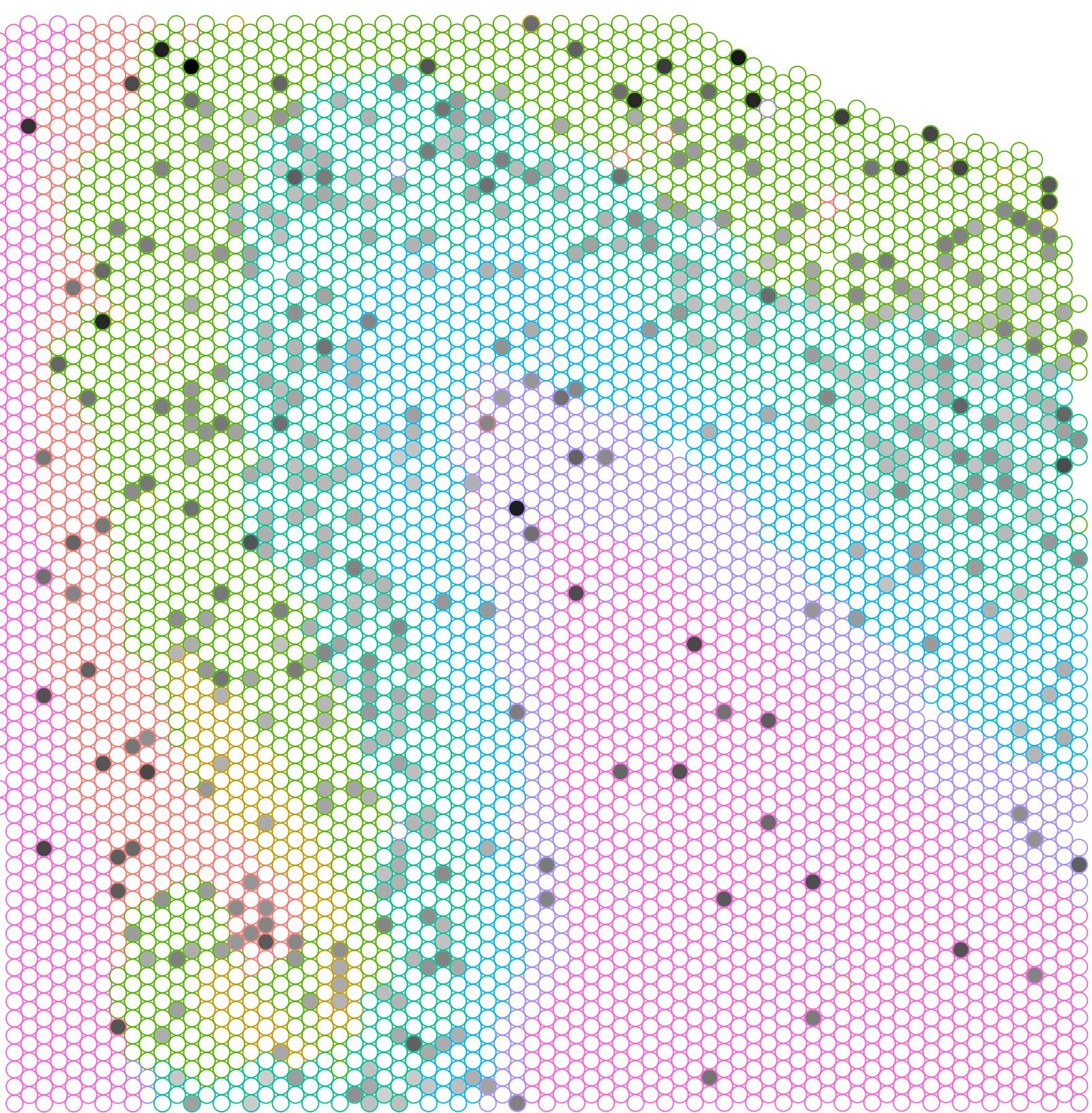
layer

- L1
- L2
- L3
- L5
- L6a
- L6b
- WM

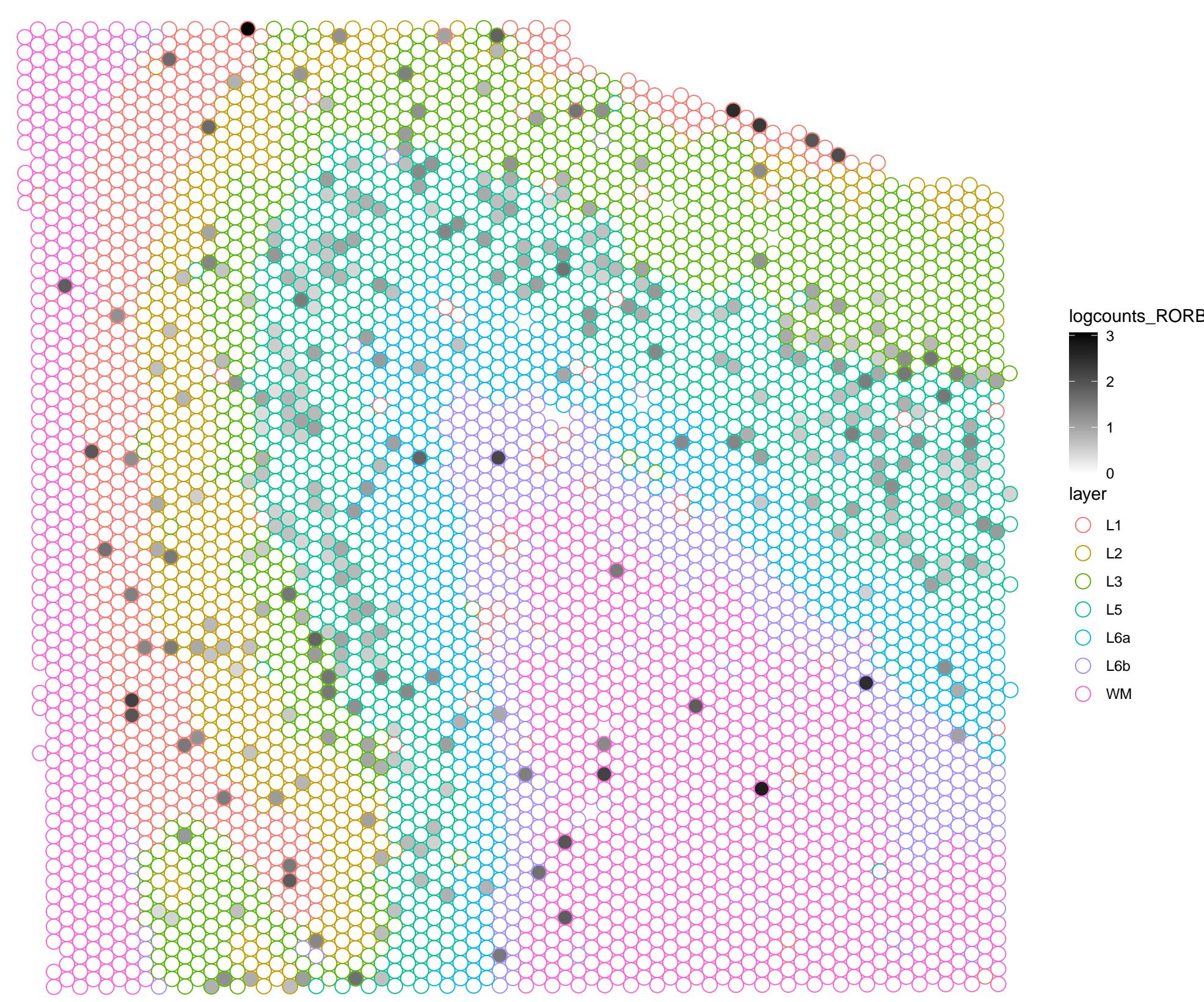
logcounts_RORB

- 3
- 2
- 1
- 0

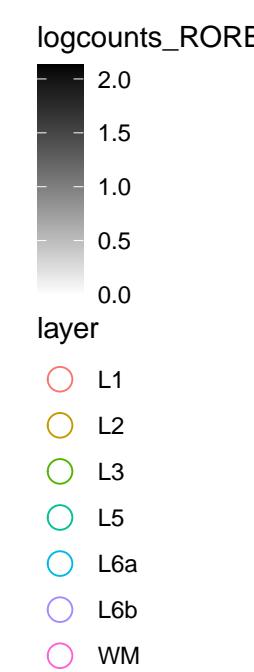
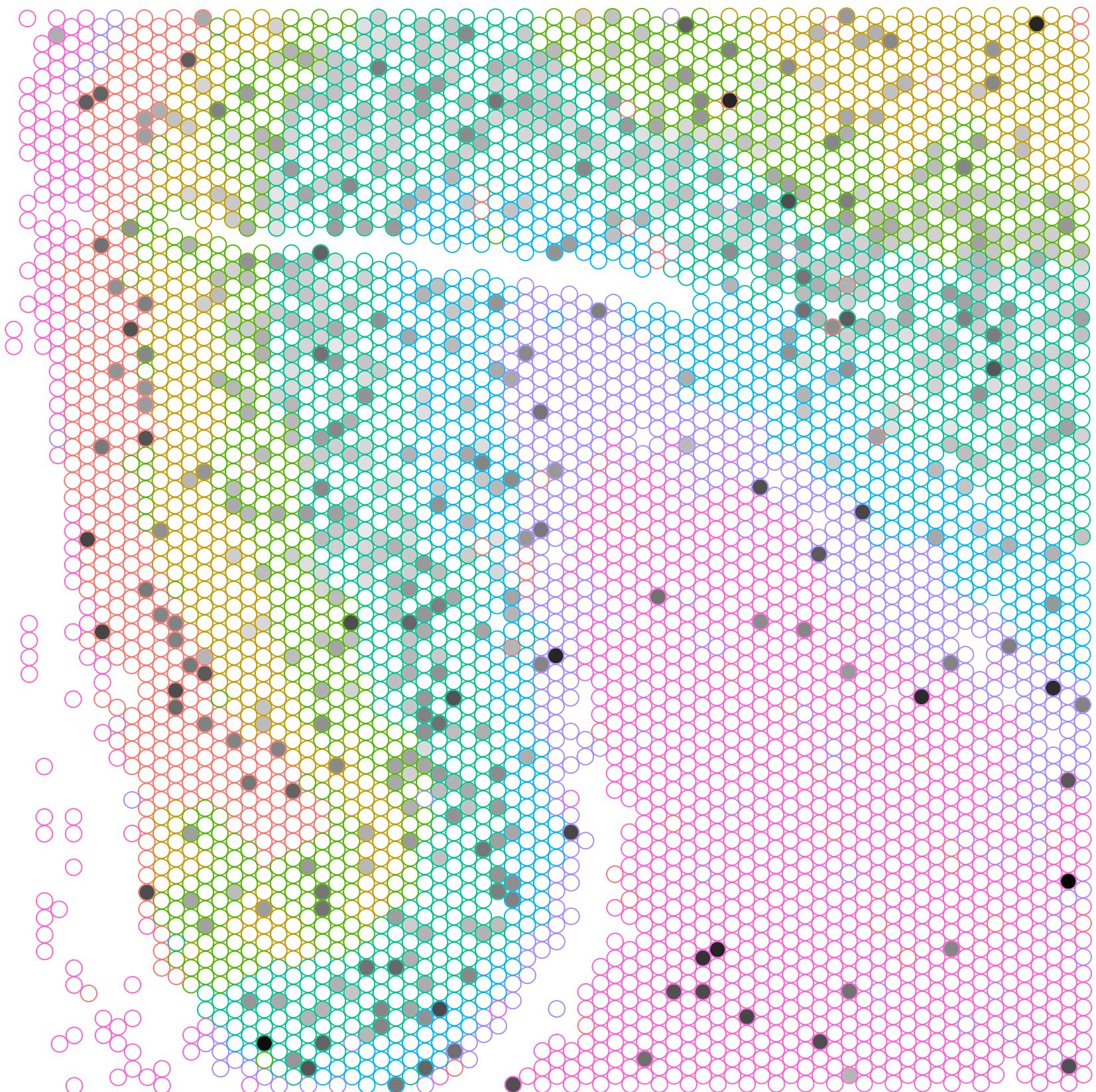
Sample V12J03-002_C1



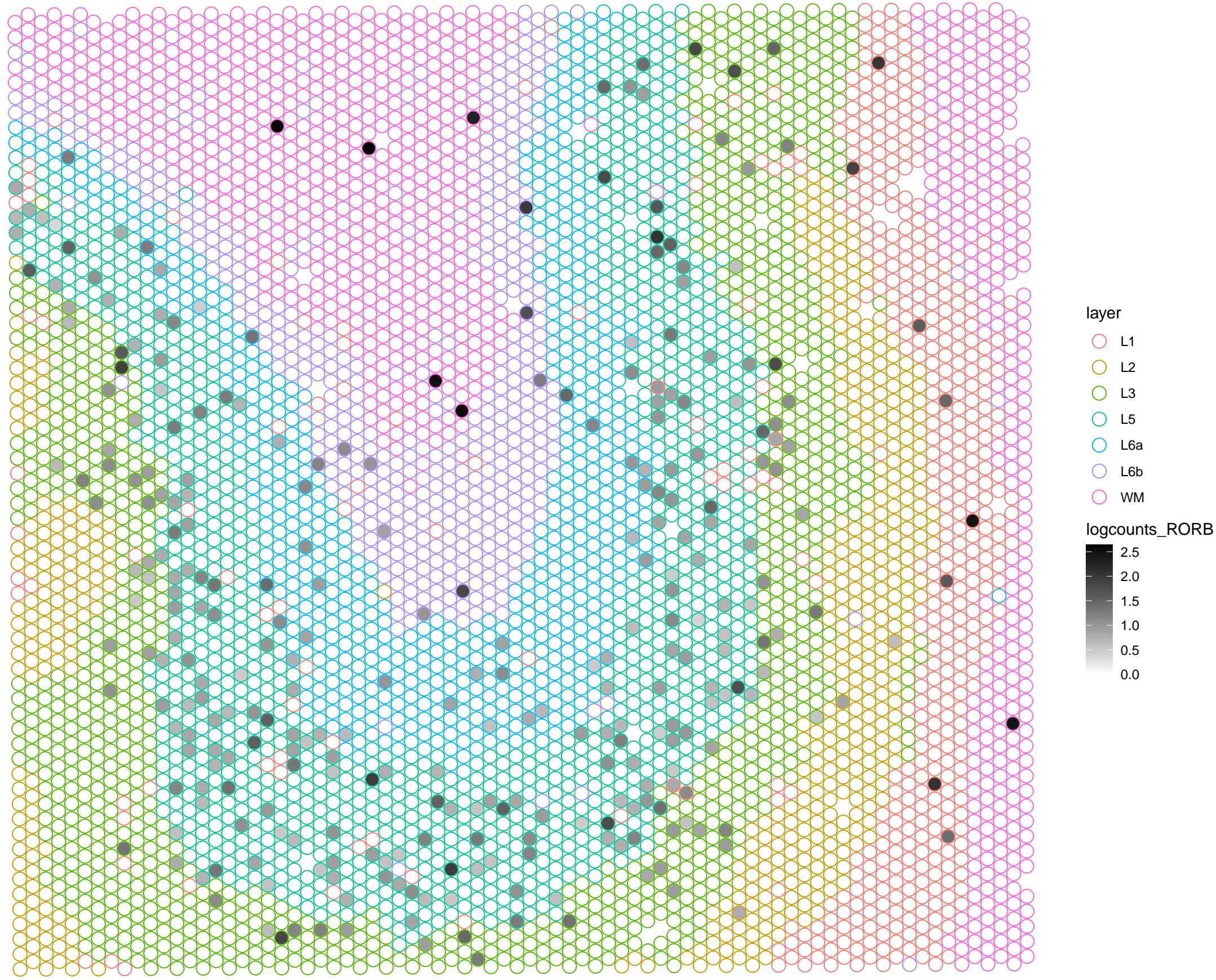
Sample V12N28-331_C1



Sample V12N28-332_C1



Sample V12N28-331_D1



Sample V12N28-332_D1

