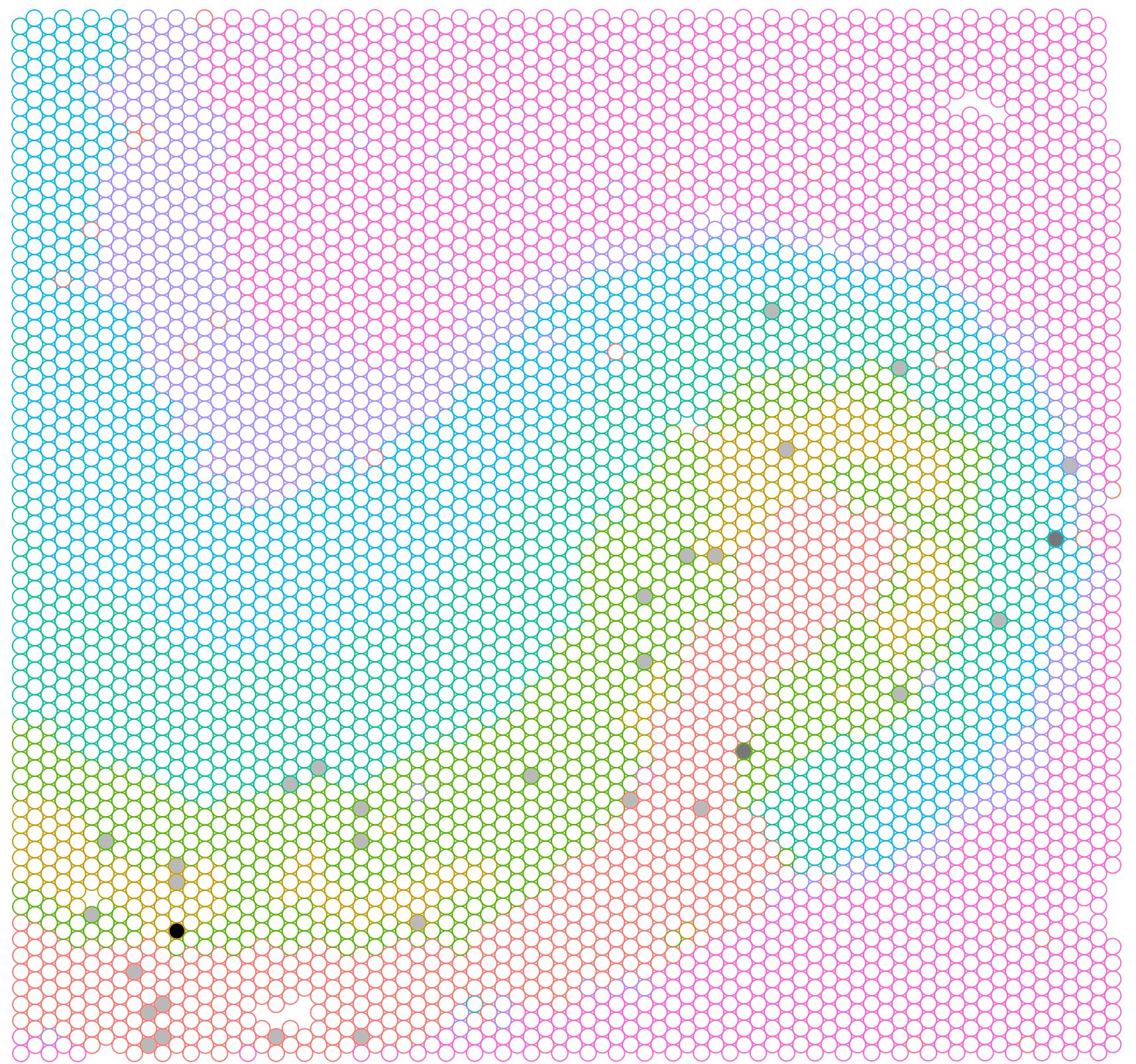
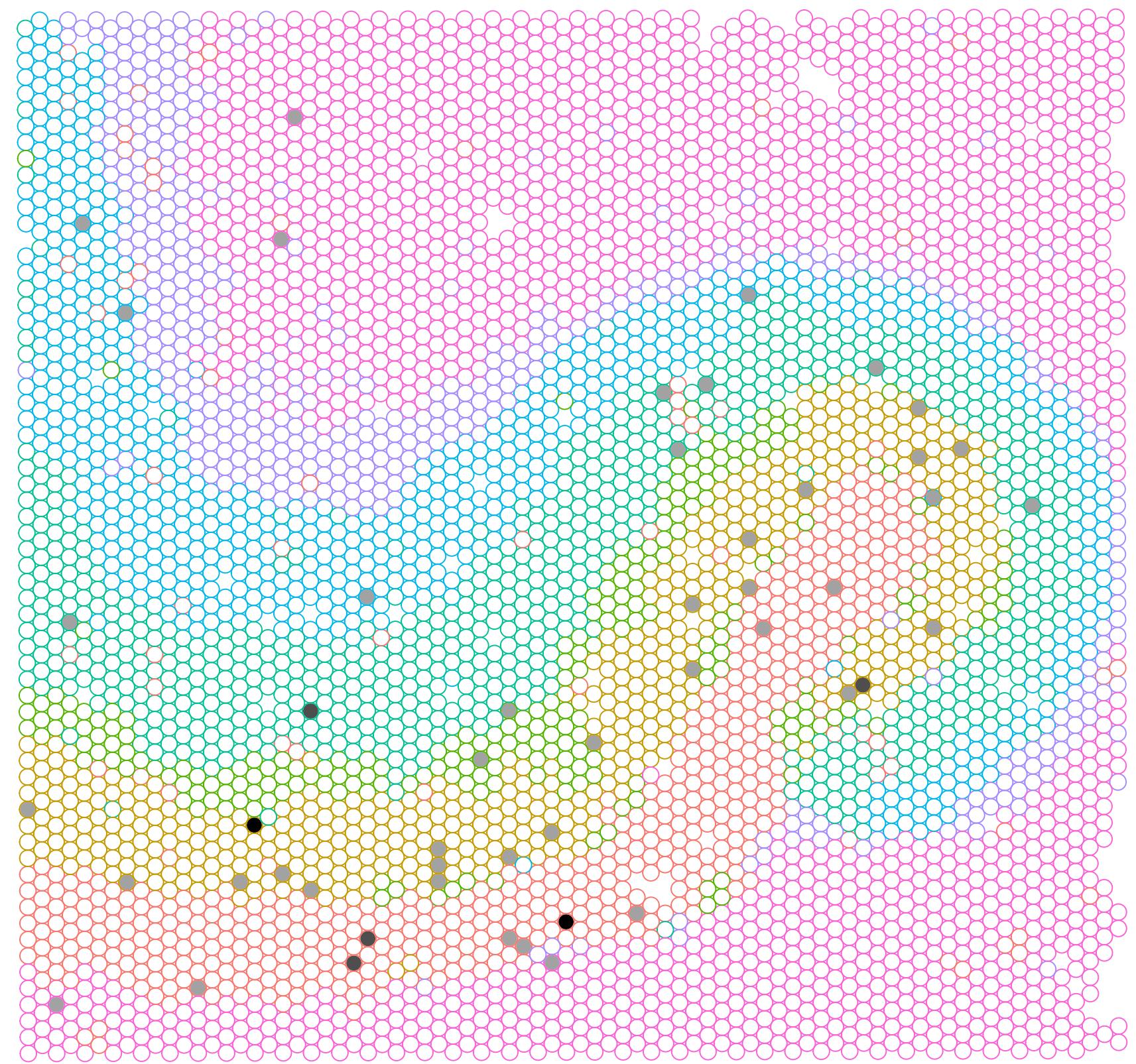


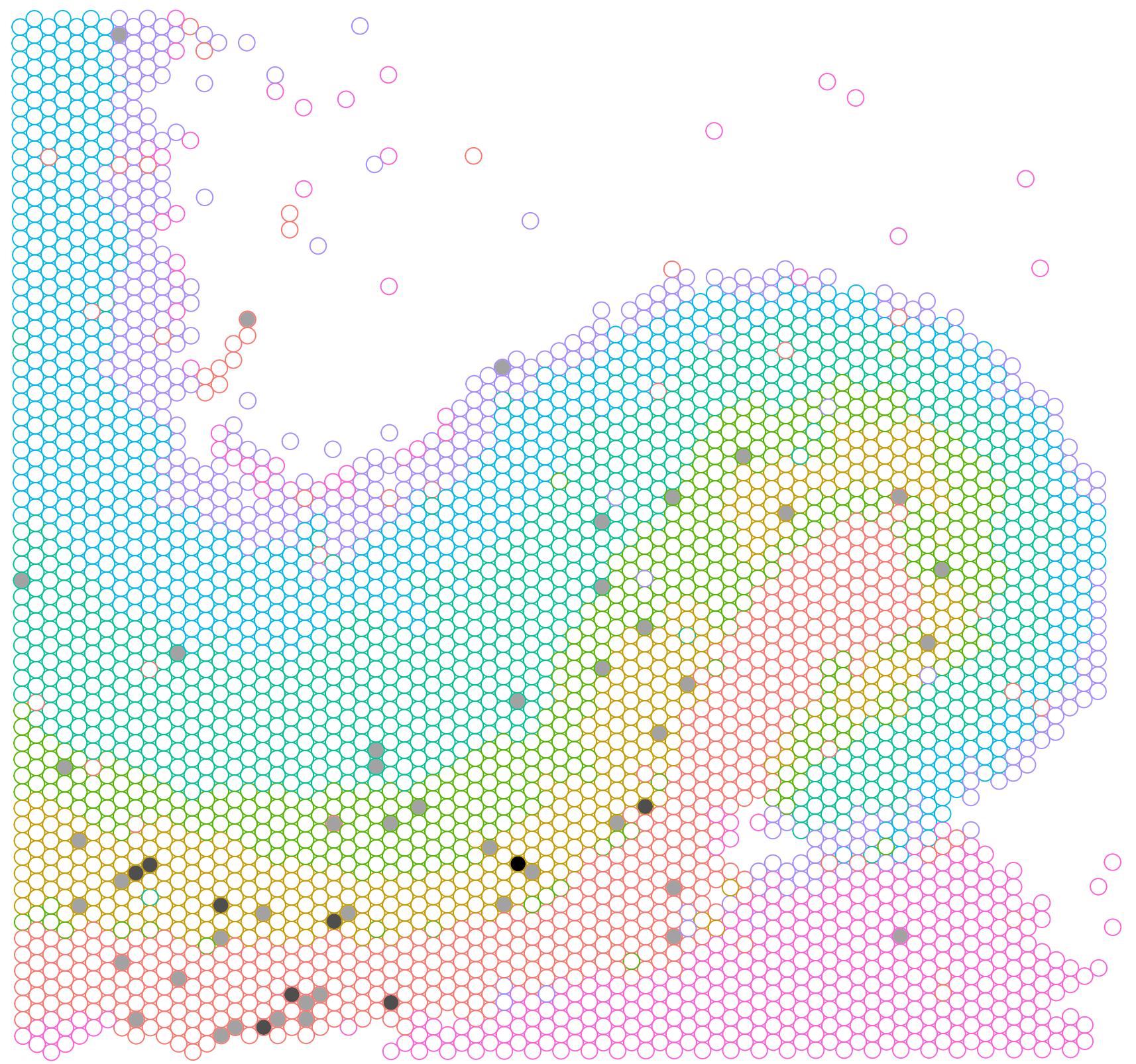
Sample V12J03–002_A1



Sample V12N28–331_A1



Sample V12N28–332_A1

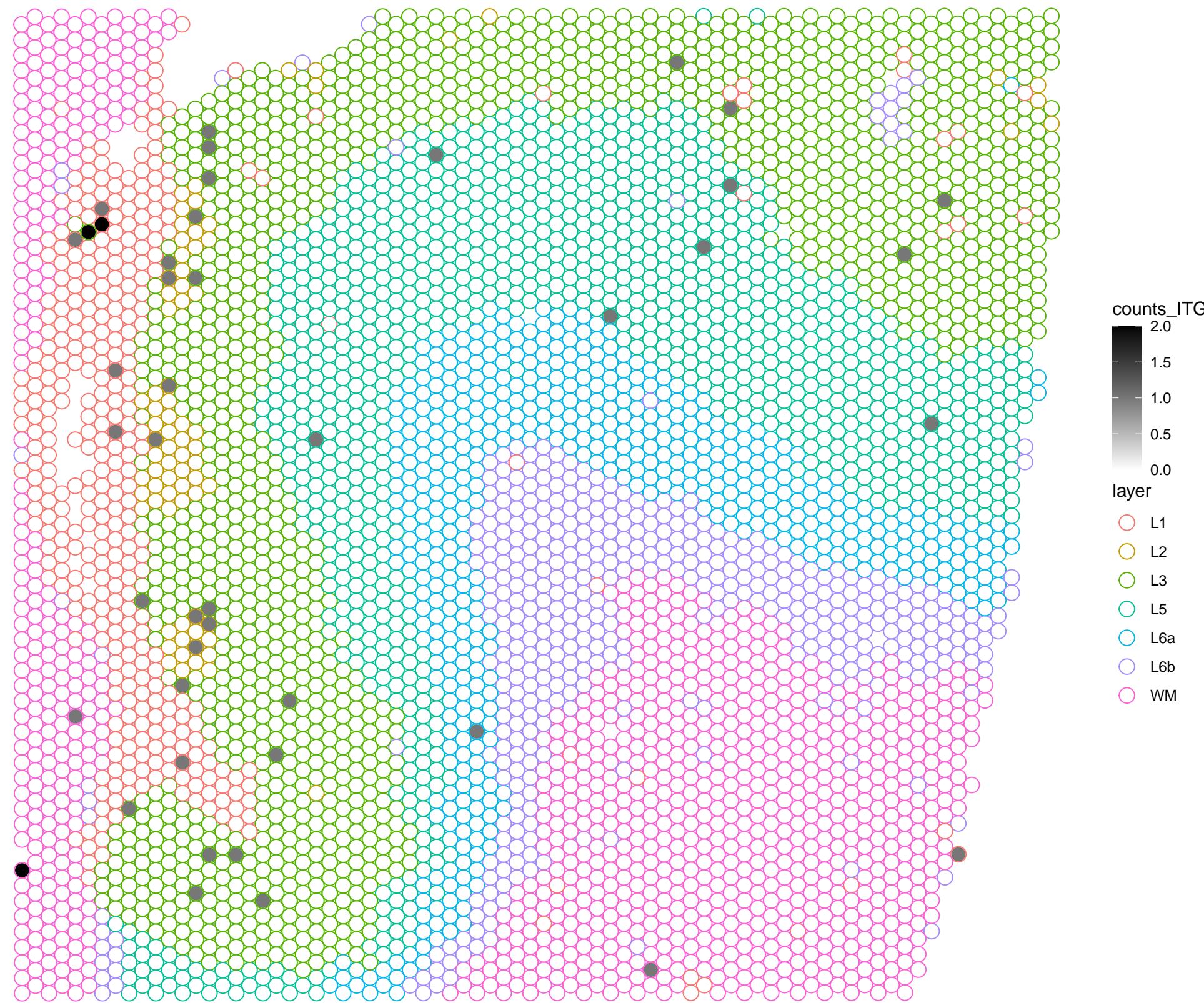


counts_ITGA4
layer
L1
L2
L3
L5
L6a
L6b
WM

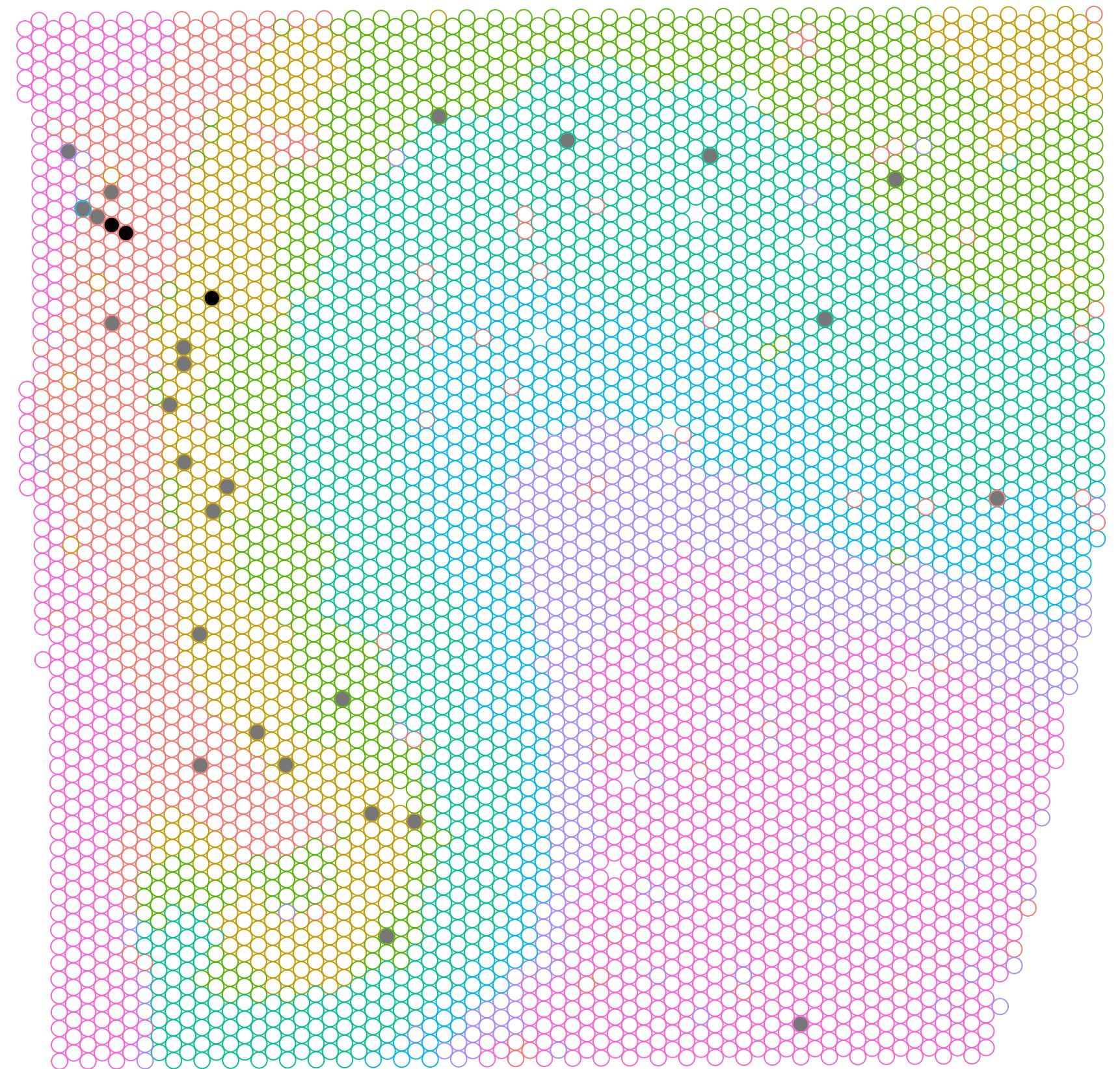
counts_ITGA4
layer
L1
L2
L3
L5
L6a
L6b
WM

counts_ITGA4
layer
L1
L2
L3
L5
L6a
L6b
WM

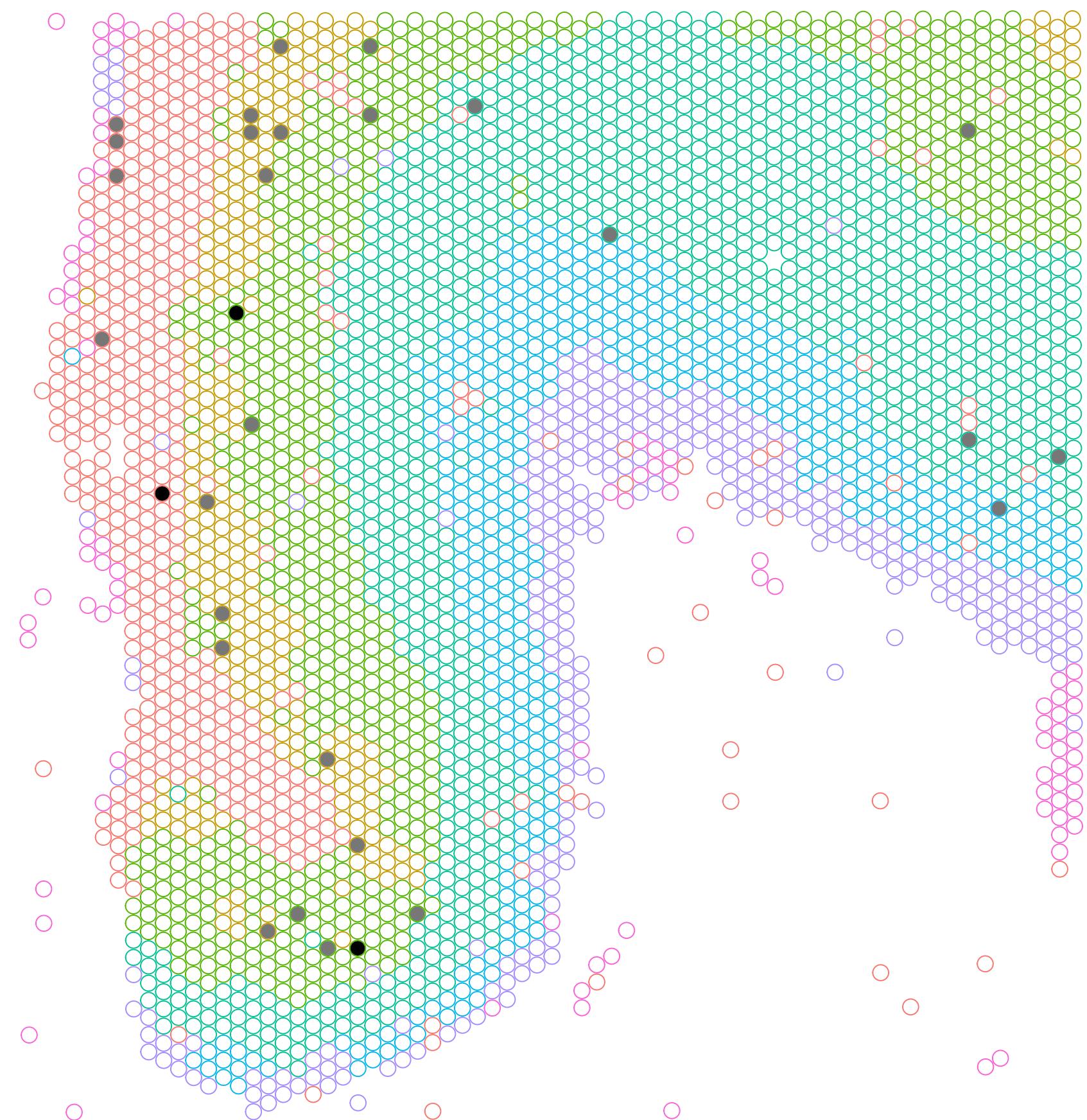
Sample V12J03-002_B1



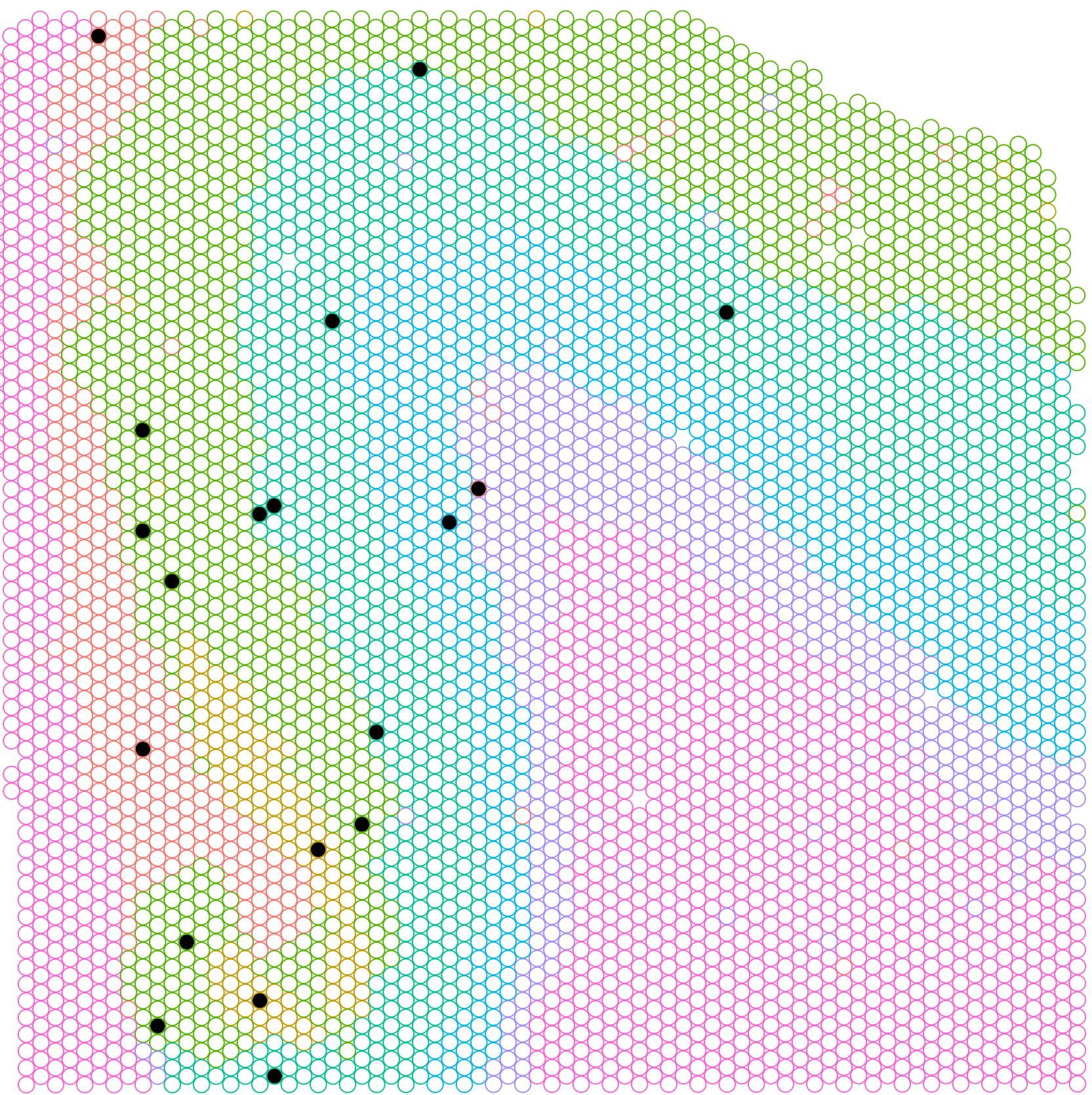
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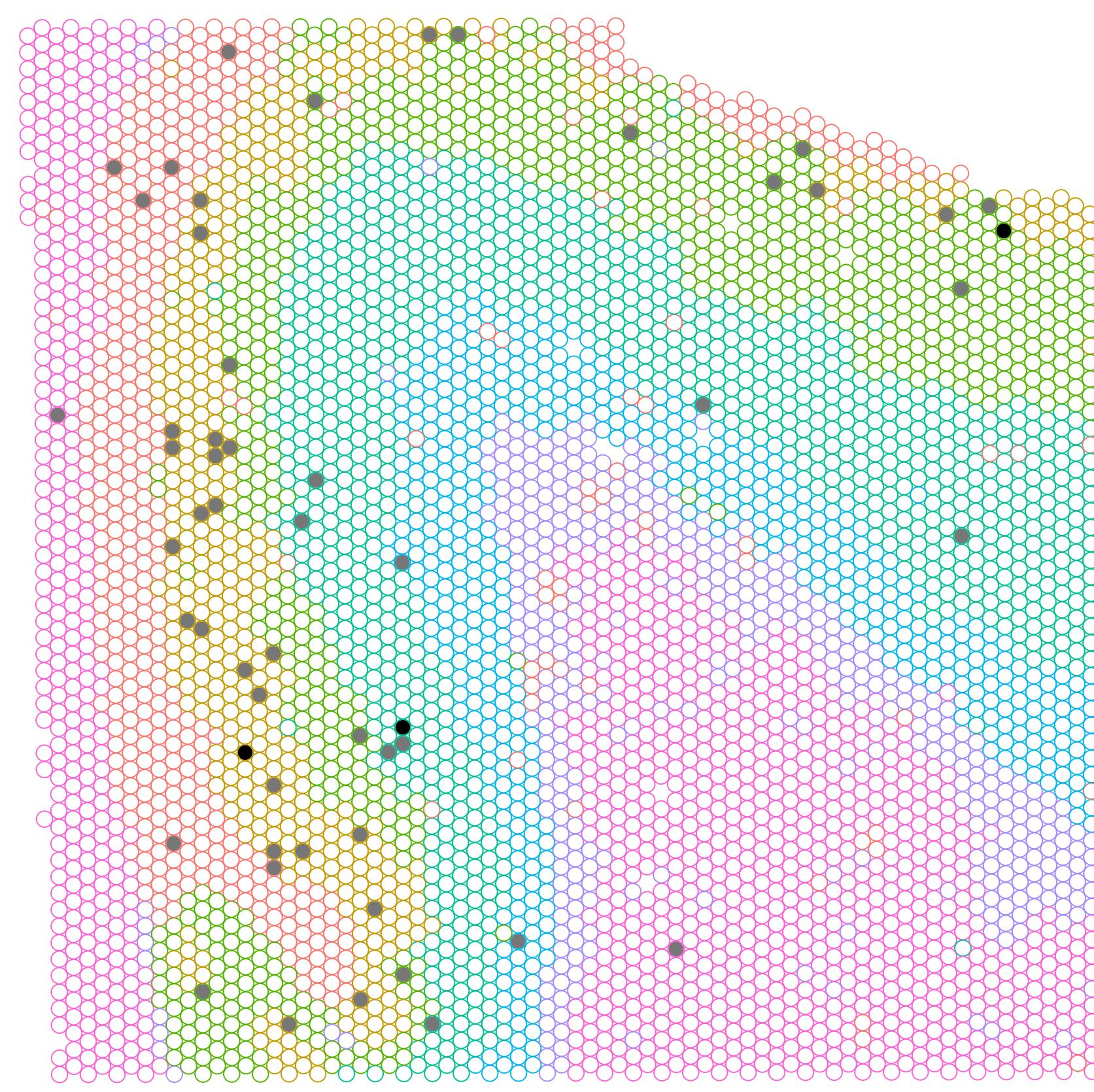
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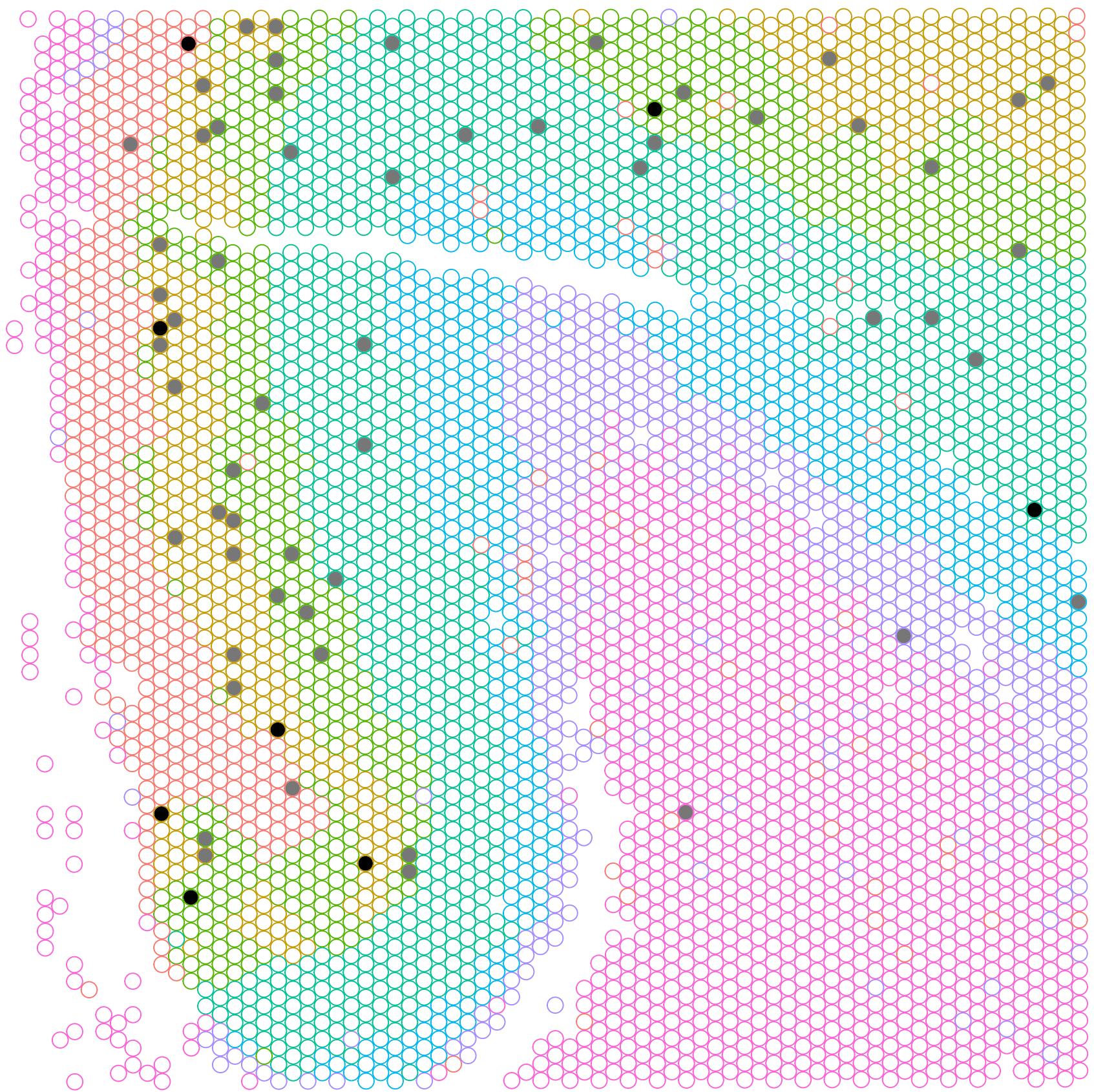
Sample V12J03–002_C1



Sample V12N28–331_C1



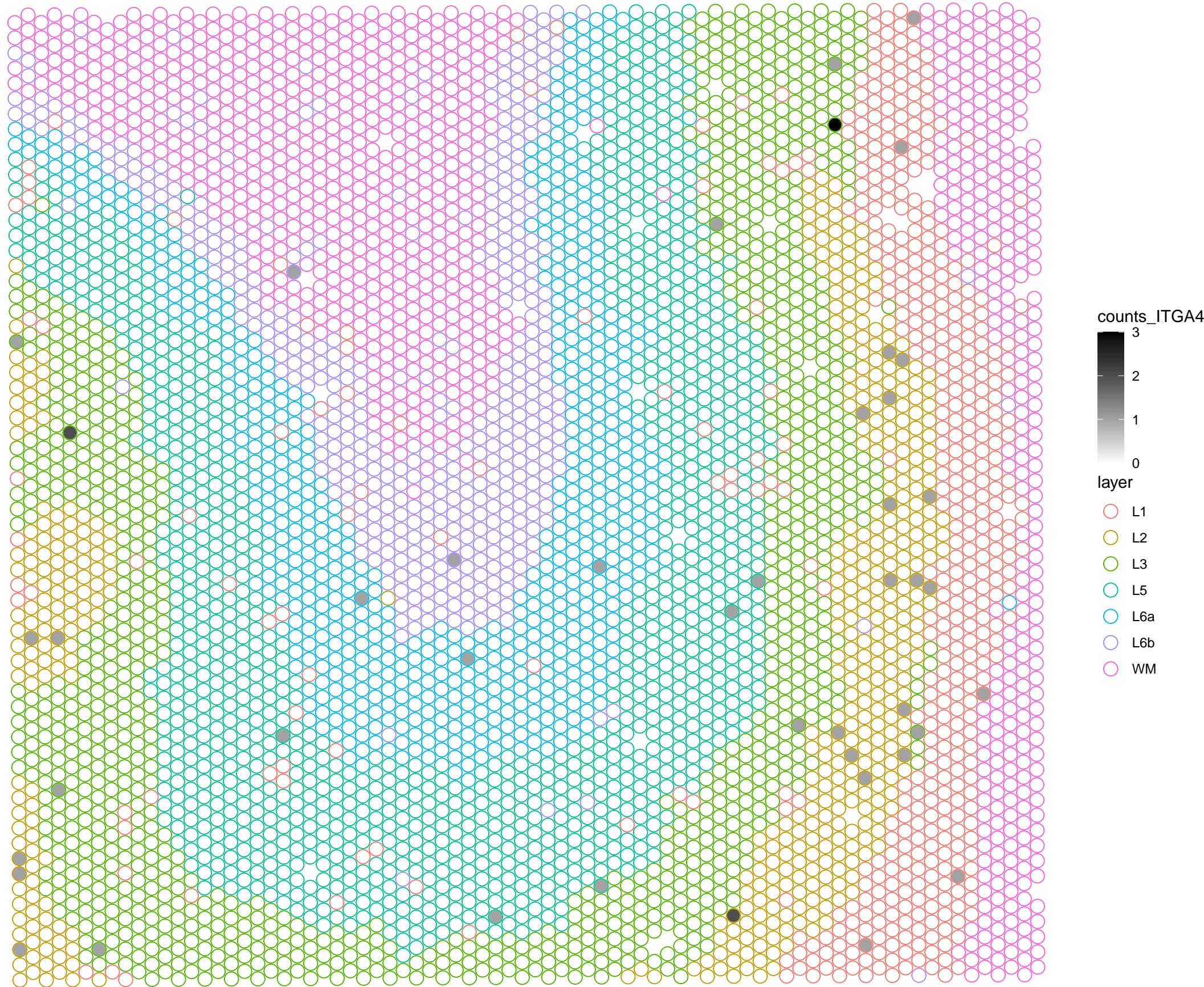
Sample V12N28–332_C1



counts_ITGA4
layer
L1
L2
L3
L5
L6a
L6b
WM

counts_ITGA4
layer
L1
L2
L3
L5
L6a
L6b
WM

Sample V12N28-331_D1



Sample V12N28-332_D1

