A Comprehensive Modeling Platform for Interconnect Technologies

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***Abstract*— With device scaling facing major physical and manufacturing challenges, many research efforts have been focused on the impact of device parameters and designs on circuit performance and power dissipation. However, similar research on the impact of Cu-low *k* interconnects at the advanced nodes and the potential benefits offered by novel wire and via material and process options is lacking. While studies based on smaller circuit blocks exist, the exploration of these benefits for the performance of larger processors is lacking although the limits imposed by interconnect resistances become more severe due to longer wires and increased complexity in larger circuits. In this article, we conduct a study to quantify the effect of back-end-of-the-line (BEOL) technology improvements on circuit power, performance, and area (PPA) of various circuits from small blocks up to a full commercial processor with L1-cache. We modified the interconnect technology (ICT) files for the ASAP7 process design kit (PDK) to reflect various BEOL options such as thinner barrier/liners, near barrierless vias, and alternative material options based on TCAD simulations. We show that these options can offer up to a 1.769× improvement in effective frequency or up to three metal-level savings.**

***Index Terms*— Back-end-of-the-line (BEOL), interconnects, place and route (PnR), power, performance, and area (PPA), Ru, transition-metal dichalcogenide (TMD) material.**

I. Introduction

CONTINUED device scaling has led to ultranarrow wire dimensions that significantly increase interconnect resistances. A major source of resistance increase comes from highly resistive barrier/liner layers as they take an ever increasing fraction of the interconnect trenches and add a large series resistance to the bottom of vias [1]. To address these challenges, researchers aim to reduce the thickness of these layers, remove or thin down barrier layers at the bottom of the vias [2], replace existing barriers with ultrathin 2-D materials [3], or use metals that need very thin or no barriers at all such as Ru. In many cases, these solutions may offer various trade-offs.

Present industry's methods and values for the barrier pitch and via resistances are presented in [4] and [5]. Based on these values, Huang et al. [1], [2] investigate the impact of metal barrier/liner (MB) thickness on circuit power, performance, and area (PPA), while Chen et al. [3] investigates the impact of replacing the TaN/Ta barrier/liner with transition-metal dichalcogenide (TMD) material. Research on interconnect *RC* parasitics based on a 3-nm gate-all-around FET has also been conducted [6]. While these works initiate the research on interconnect and process options at advanced nodes, they are limited to ring oscillators or relatively small circuits. In a modern processor, there are many critical paths with vastly different compositions of logic gates, interconnects and vias at various metal levels. Hence, the potential impact of various interconnect options can be evaluated only after place and route (PnR) at the chip level.

In this article, the resistances of wires and vias made of various materials and dimensions are calculated based on a uniform set of assumptions in wire dimensions and aspect ratio (AR), using TCAD tool SEMulator3D from coventor [8] for Cu + Ru/TaN and COMSOL simulations for Cu + TMD. To ensure consistency, COMSOL simulations for Cu + Ru/TaN are also conducted and compared with those from Coventor. The results are then used in an register-transfer level (RTL)-to-graphic data stream (GDS) design flow with commercial EDA tools for a variety of circuits from small blocks all the way to a commercial processor with L1 cache (ARM's Cortex[1]-A53) to evaluate the impact of each interconnect option on the circuit PPA. This contrasts with prior works [1], [2], [3], [6] that only used small circuit blocks to evaluate the impact of wire and via resistances. Uniform modeling of various options and their side by side evaluation at the processor level also provide important insights regarding the trade-offs offered. In addition, we also conduct a cost study

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[1]Registered trademark.

TABLE I
KEY LAYER PARAMETERS AND RESISTANCES FOR THE DIFFERENT BEOL OPTIONS. UNIFORM WIDTHS, PITCHES, AND AR (=2) WERE USED

Metal/Via	Width/Pitch (nm)	CuBKM	M13 Thin	CuThin	ImpVia	Ru [7]	TMD 0.5x	TMD	TMD 2x
M1	18/36	306 $\Omega/\mu m$	212 $\Omega/\mu m$	212 $\Omega/\mu m$	306 $\Omega/\mu m$	200 $\Omega/\mu m$	149 $\Omega/\mu m$	149 $\Omega/\mu m$	149 $\Omega/\mu m$
M2-M3	18/36	306 $\Omega/\mu m$	212 $\Omega/\mu m$	212 $\Omega/\mu m$	306 $\Omega/\mu m$	200 $\Omega/\mu m$	149 $\Omega/\mu m$	149 $\Omega/\mu m$	149 $\Omega/\mu m$
V1-V3	18/36	104 Ω	56 Ω	56 Ω	52 Ω	20 Ω	55 Ω	88 Ω	158 Ω
M4-M5	24/48	121 $\Omega/\mu m$	121 $\Omega/\mu m$	91 $\Omega/\mu m$	121 $\Omega/\mu m$	121 $\Omega/\mu m$	62 $\Omega/\mu m$	62 $\Omega/\mu m$	62 $\Omega/\mu m$
V4-V5	24/48	54 Ω	54 Ω	31 Ω	27 Ω	54 Ω	31Ω	50.6 Ω	89 Ω
M6-M7	32/64	47 $\Omega/\mu m$	47 $\Omega/\mu m$	38 $\Omega/\mu m$	47 $\Omega/\mu m$	47 $\Omega/\mu m$	26$\Omega/\mu m$	26 $\Omega/\mu m$	26 $\Omega/\mu m$
V6-V7	32/64	30 Ω	30 Ω	18 Ω	15 Ω	30 Ω	18 Ω	28 Ω	50 Ω
M8-M9	40/80	23 $\Omega/\mu m$	23 $\Omega/\mu m$	19 $\Omega/\mu m$	23 $\Omega/\mu m$	23 $\Omega/\mu m$	14 $\Omega/\mu m$	14 $\Omega/\mu m$	14 $\Omega/\mu m$
V8	40/80	19 Ω	19 Ω	12 Ω	9 Ω	19 Ω	11 Ω	18 Ω	32 Ω

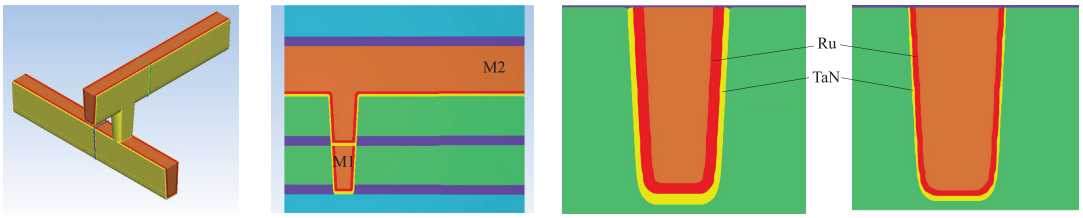

Fig. 1. Via and MB modeling for V1 and M1 and M2 through SEMulator3D (Coventor) tool. (a) 3D model and (b) cross section of M1, M2, and V1. Cross sections of (c) CuBKM and (d) CuThin interconnect models.

on how many metal levels we can save by improving the back-end-of-the-line (BEOL) options using an industry standard processor circuit.

The rest of this article is organized as follows. We first describe the BEOL options we model and the design flow for our TCAD and circuit simulations in detail in Sections II and III, respectively. These sections are followed by Sections IV and V, where we show our circuit simulation results and analysis, respectively.

II. WIRE AND VIA RESISTANCE MODELING

With advanced nodes, the interconnect cross-sectional dimensions are scaled down to 18 nm and smaller meaning that the diffusion barrier can take up more than 40% of the interconnect trenches [1]. With these highly resistive diffusion barriers, interconnect resistance almost doubles from one node to the next. The main challenge in improving this issue lies in the TaN/Ta or TaN/Ru's 3-D nature as it is extremely difficult to make these diffusion barriers thinner with the commonly used sputtering method without causing major reliability and yield challenges [9].

In this section, various interconnect technology options to improve BEOL resistances are discussed, starting with industry's best-known method (CuBKM) which is used as a baseline. The resistance values for each BEOL option are shown in Table I.

A. Cu With Ru/TaN Liner/Barrier

The Cu wire and via resistances for the BEOL stack are modeled using process emulation tool SEMulator3D with assumptions from [10] (see Fig. 1). The process assumptions include self-aligned vias [11] and calibrated Cu resistance models [5]. In addition, physical vapor deposition (PVD) TaN with 50% sidewall coverage compared with the bottom and chemical vapor deposition (CVD) Ru with conformal coverage are assumed for the Cu MB. As this baseline option is based on current industry's best-known method [4], it will be referred to as CuBKM.

B. Thinning the Barrier Liner

The first two case studies are on the impact of thinning the MB bottom thickness from 4 to 2 nm (1-nm TaN/1-nm Ru) and are based on [4]. For the first case (M13Thin), only the MB for the local interconnects (M1–M3) are thinned down. In the second case (CuThin), the MB for all metal levels (M1–M9) are thinned down to 2 nm. These case studies represent one of the projected limits of MB engineering.

C. Near Barrierless Via

The third case study investigates the impact of improving only the vias (ImpVia). In this case, the line resistances are the same as the CuBKM case, and only the via resistances are improved. This could be achieved either through near barrierless via fills or via prefills [10].

D. Ruthenium Interconnects

While ruthenium has a higher bulk resistivity compared to copper, it requires only a thin adhesion layer unlike copper, which also requires an additional MB [7]. Furthermore, ruthenium is less sensitive to size effects, and its resistivity does not increase as fast as Cu when wire dimensions are scaled aggressively. Ru therefore is considered a promising Cu replacement for low metal levels where diffusion barriers can take a large fraction of the cross-sectional area of Cu interconnects and size effects are quite prominent. In upper metal levels, however, Cu is still a better option (M4-M9 in this work).

E. TMD Interconnects

While it is challenging to reduce the interconnect resistance with conventional barrier materials due to their 3-D

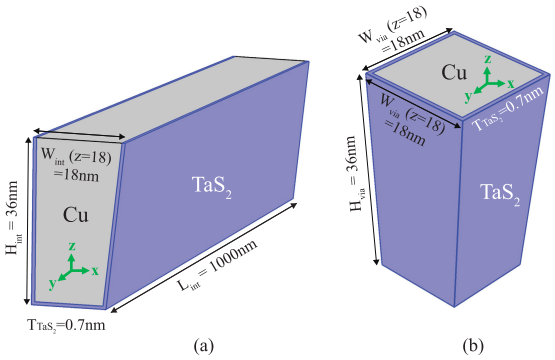

Fig. 2. TMD interconnect and via modeling. (a) 3-D model structure for TMD-augmented interconnect. (b) 3-D model structure for TMD-augmented via. The resistance for the TMD-augmented via is modulated to be 0.5× (TMD 0.5×) and 2× (TMD 2×).

nature, many 2-D materials are being studied as possible solutions. Cu + graphene hybrid interconnects have been of particular interest due to the good diffusion barrier property of graphene [12] and its ability to lower electron scattering at the surface [13]. However, graphene lacks good adhesion and wettability properties [9], [14]. Moreover, the growth temperature for CVD-based graphene is 1000 °C, which makes it incompatible with the BEOL process. CVD-grown TMD materials such as TaS_x, on the other hand, have growth temperatures as low as 400 °C [9] and are a more BEOL compatible class of 2-D materials as recent experiments have indicated good wettability and adhesion properties [9], [15].

For TMD-augmented interconnects, 3-D models are created using COMSOL Multiphysics employing 0.7-nm monolayer TaS_2 as the liner/barrier [3] (see Fig. 2). While the line metal resistance is significantly reduced due to larger Cu conduction area, the via resistance increases [15] due to a 10× higher vertical resistivity of TaS_x (compared to Ta/TaN). To better understand the effect of increased vertical resistivity, Z-directional resistivity is modulated to be 0.5× (TMD 0.5×) and 2× (TMD 2×) of the original vertical resistivity of TaS_x while the xy plane direction resistivity stays the same.

III. Design Flow

ASAP7, an open-source predictive 7-nm FinFET technology node developed by Arizona State University (ASU), along with a standard GDS-to-RTL design flow similar to that of [2] was used for the purpose of the study. The modeling of the baseline BEOL and the memory components are also based on the ASAP7 process design kit (PDK) dimensions.

The via and wire resistances are first modeled using the TCAD tool SEMulator3D from Coventor [8] similar to those modeled in [11]. The via resistance is sensitive to the bottom contact area to the lower metal level as shown in Fig. 1(a). Based on the TCAD modeling results for various BEOL options and the original ASAP7 PDK, the interconnect technology (ICT) files, which are used for capacitance parasitic calculations during QRC extraction, were developed. Due to the lack of a 7-nm memory compiler, the macros were created by a 14/16-nm node memory compiler and scaled down for both geometries and timing/power values for benchmarks with on-chip memory. The scaling factors were found by modeling SRAM memory for 16- and 7-nm technology nodes with NVSim [16].

The benchmark netlists were synthesized using the Synopsys Design Compiler with the ASAP7 standard cell library and the newly modified BEOL files. With the resulting netlist and the ICT files, PnR was performed using the commercial EDA tool Innovus from Cadence. Once PnR is completed, timing and power analysis were done using the Tempus Signoff Solution from Cadence. In addition, analysis on the wire and via resistance composition of the top critical paths and the buffer usage was performed to better understand the impact of various forms of BEOL improvement on system-level performance.

TABLE II
Benchmark Characteristics. For Cortex-A53, Only the Percentage for Pin and Wire Capacitance Values Are Shown Due to Nondisclosure Agreement

	AES	LDPC	Rocket core	Cortex-A53
pin cap	148.1 (68.6%)	69.6 (46.8%)	142.6 (59.9%)	45.8 %
wire cap	67.9 (31.4%)	79.2 (53.2%)	95.4 (40.1%)	54.2 %
FF %	7.5%	3.4%	20.0%	8.7%

IV. Circuit Simulations

A. Simulation Setup

For circuit-level analysis, we used Advanced Encryption Standard (AES), a cell-dominant circuit, low-density parity check (LDPC), a wire-dominant circuit, Rocket core, a small RISC-V-based CPU core design, and ARM's Cortex[1]-A53, a relatively large industry standard CPU core design. Some benchmark characteristics including flip-flop percentage are provided in Table II. Based on these values, we categorize AES and Rocket core as more cell-dominant circuits and LDPC and Cortex-A53 as wire-dominant circuits. The flip-flop percentage will be used later in the power analysis in Section V-D.

B. Circuit Results

The layouts of the designs are shown in Fig. 3, and the effective frequencies that can be achieved for each benchmark are shown in Fig. 4. Tables III–V show the detailed post PnR results for the Rocket core and Cortex-A53 benchmarks.

AES and LDPC are both relatively small circuits with no memory components, but AES is cell-dominant while LDPC is more wire-dominant. Although improved BEOL has the least impact on the performance of the AES circuit, we still observe an 18.1% performance improvement in the TMD 0.5× case. In the case of LDPC, the performance is slightly more affected by the BEOL changes with a performance gain of 20.0%. In both cases, we observe that improving the metal levels without any material replacements (CuThin cases) still gives 12.2% and 17.1% improvements. As the LDPC benchmark is wire-dominant, it is affected more by the changes in the BEOL resistances compared with AES. Due to their small floorplan size, these two benchmarks show relatively smaller improvements in performance compared to Rocketcore and Cortex-A53, as shown in Fig. 4.

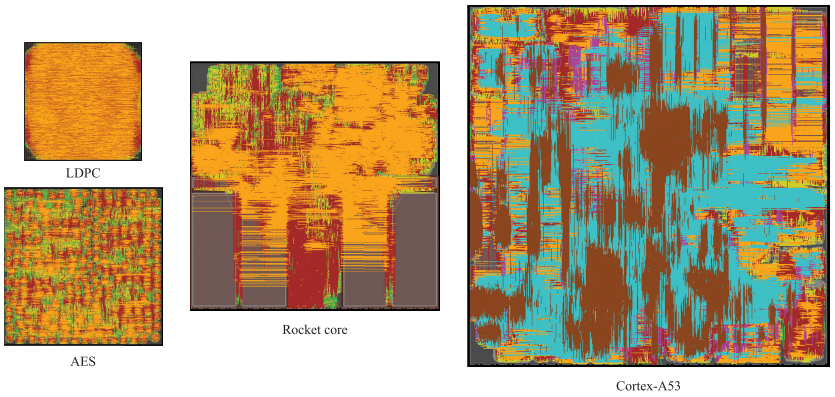

Fig. 3. Layouts of our benchmark designs. Note that the figure is not to scale.

TABLE III
IMPACT OF BEOL IMPROVEMENT ON CIRCUIT PPA FOR ROCKET CORE. SW. PWR, INT. PWR, LKG. PWR, SEQ. PWR, CLK. PWR, AND COMB. PWR EACH STAND FOR SWITCHING, INTERNAL, LEAKAGE, SEQUENTIAL, CLOCK, AND COMBINATIONAL POWER, RESPECTIVELY

	CuBKM	M13Thin	CuThin	ImpVia	Ru	TMD0.5x	TMD	TMD2x
Rocket core								
Eff. Freq. (MHz)	1544	1806 (17.0%)	2006 (29.9%)	1796 (16.3%)	1923 (24.5%)	2062 (33.5%)	1995 (29.2%)	1760 (14.0%)
Footprint (um)	210x211							
Cell Area (um^2)	21614	21791	21930	21810	21857	21829	21921	21686
WL (m)	0.791	0.795	0.795	0.805	0.794	0.786	0.787	0.784
Power Breakdown 1								
Sw. Pwr (mW)	25.16	30.39	33.99	30.62	32.13	33.60	33.94	28.56
Int. Pwr (mW)	34.78	42.09	47.39	42.13	44.55	46.81	47.45	39.82
Lkg. Pwr (mW)	11.11	11.18	11.25	11.18	11.21	11.22	11.25	11.16
Power Breakdown 2								
Seq. Pwr (mW)	22.38	26.60	29.66	26.61	27.97	29.42	29.52	25.14
Clk. Pwr (mW)	2.90	3.62	3.67	3.71	3.84	3.54	3.61	3.00
Comb. Pwr (mW)	27.12	33.45	38.41	33.62	35.63	37.81	38.67	31.88
Macro Pwr (mW)	18.64	19.99	20.89	19.99	20.44	20.85	20.84	19.51
Total Pwr (mW)	71.04	83.66	92.62	83.93	87.89	91.63	92.64	79.54
Cell and Buffer Count Analysis								
Cell Count	161278	162569	163717	162875	162870	162128	163279	161416
Buffer Count	24765	25977	26665	25932	26164	25765	26000	25155
Buffer Pwr (mW)	9.14	12.10	13.87	11.92	12.96	13.51	13.76	11.01

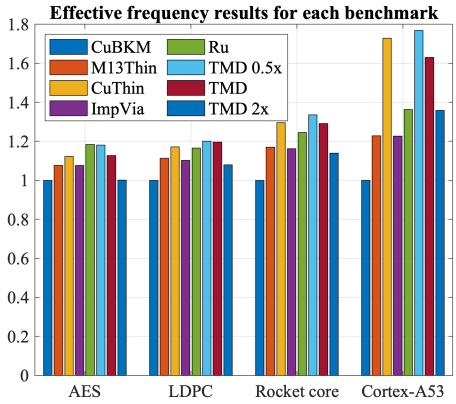

Fig. 4. Summary of performance results.

The single core variants were used for both the Rocket core and Cortex-A53 benchmarks. With memory components and more functionality on the chip, both circuits are considerably larger compared to AES and LDPC. Although Rocket core is a cell-dominant circuit, the achievable performance improves by a greater amount with improved BEOL compared to the relatively smaller circuits as shown in Table III. The larger circuit size causes it to contain higher number of longer wires compared to the smaller benchmarks, and thus Rocket core benefits more showing a performance improvement of 33.5% with the TMD 0.5× case.

Cortex-A53 has the highest performance gain from all the benchmarks with the TMD 0.5× case showing a 76.9% improvement with nine metal-level designs (see Table IV). Unlike Rocket core, Cortex-A53 is wire-dominant. In general, all hypothetical BEOL improvements have a larger impact on the effective frequency compared to other circuit benchmarks. In the case of this benchmark, the ImpVia and M13Thin cases offer the smallest improvements but still provide about 22.7% performance improvement. This highlights the impact of the long interconnects that connect the logic to L1 cache which are often routed in intermediate or upper metal levels. In addition, we observe that improving the local vias significantly is more impactful than improving both wires and vias moderately from the Ruthenium and M13Thin cases. Also, the very low wire resistances offered by TMD interconnects can result in

TABLE IV

IMPACT OF BEOL IMPROVEMENT ON CIRCUIT PPA FOR CORTEX-A53 DESIGNS WITH NINE METAL LEVELS (BASELINE FOR COMPARISON IS THE CUBKM BEOL OPTION). ALL RESULTS ARE NORMALIZED WITH RESPECT TO THE BASELINE DUE TO NONDISCLOSURE AGREEMENT

Cortex-A53 9 metal layers								
	CuBKM	M13Thin	CuThin	ImpVia	Ru	TMD0.5x	TMD	TMD2x
Eff. Freq. (normalized)	1.000	1.229	1.729	1.227	1.363	1.769	1.630	1.359
Footprint (normalized)				1x1				
Cell Area (normalized)	1.000	1.020	1.066	1.018	1.029	1.037	1.031	1.019
WL (normalized)	1.000	1.024	1.051	1.028	1.031	0.928	0.942	0.929
Power Breakdown 1								
Sw. Pwr (normalized)	1.000	1.275	1.933	1.287	1.446	1.922	1.765	1.404
Int. Pwr (normalized)	1.000	1.294	2.111	1.294	1.478	2.142	1.907	1.471
Lkg Pwr (normalized)	1.000	1.596	3.714	1.520	1.857	3.824	3.061	1.906
Power Breakdown 2								
Seq. Pwr (normalized)	1.000	1.198	1.674	1.207	1.331	1.795	1.672	1.374
Clk. Pwr (normalized)	1.000	1.199	2.331	1.640	1.392	2.349	2.197	1.289
Comb. Pwr (normalized)	1.000	1.322	2.134	1.313	1.516	2.092	1.875	1.460
Macro Pwr (normalized)	1.000	1.213	1.704	1.212	1.354	1.782	1.642	1.363
Total Pwr (normalized)	1.000	1.283	2.002	1.290	1.459	2.009	1.820	1.430
Cell and Buffer Count Analysis								
Cell Count (normalized)	1.000	1.020	1.055	1.016	1.027	1.022	1.020	1.013
Buffer Count (normalized)	1.000	1.124	1.312	1.098	1.174	1.177	1.162	1.111
Buffer Pwr (normalized)	1.000	1.555	2.878	1.509	1.871	2.726	2.390	1.713

TABLE V

IMPACT OF BEOL ON COST-PERFORMANCE OF CORTEX-A53. ALL ALTERNATIVE BEOL DESIGNS WITH SIX METAL LEVELS ARE COMPARED TO CUBKM DESIGNS WITH SIX AND NINE METAL LEVELS. THE RELATIVE IMPROVEMENT IS SHOWN

	Eff. freq		Total Pwr	
	CuBKM-6	CuBKM-9	CuBKM-6	CuBKM-9
M13Thin-6	+32.877%	-12.293 %	+34.270 %	-9.910 %
CuThin-6	+45.344 %	-4.064 %	+42.652 %	-4.286 %
ImpVia-6	+11.439 %	-26.443 %	+9.411 %	-26.589 %
Ru-6	+31.449 %	-13.236 %	+34.953 %	-9.452 %
TMD0.5x-6	+79.375 %	+18.398 %	+85.355 %	+24.366 %
TMD-6	+77.605 %	+17.230 %	+84.613 %	+23.868 %
TMD2x-6	+22.345 %	-19.245 %	+23.010 %	-17.465 %

substantial circuit performance gains despite their larger via resistances. Overall, the Cortex-A53 results show that BEOL resistances are more critical in large wire-dominant circuits.

V. ANALYSIS

A. Number of Metal Levels

In addition to the BEOL impact study with the same number of metal levels, a metal-level cost-performance study using Cortex-A53 has been conducted. In the previous sections, Cortex-A53 designs used nine metal levels. In this case study, we explore the impact of using various BEOL options on metal-level/cost savings. The results are summarized in Tables IV and V. We observe that the Cortex-A53 design done with the CuThin BEOL and six metal levels can achieve a similar effective frequency as the design done with the CuBKM BEOL and nine metal levels. When using the TMD 0.5× BEOL option, we can outperform the nine metal-level baseline design by 18.4%. We also observe that the improvement in performance is larger for designs done with six metal levels. This is due to the fact that the six metal-level circuit designs have more restrictions and less routing resources. Nine metal-level designs have access to low-resistance upper metal levels (M7–M9) which can be used to route longer connections.

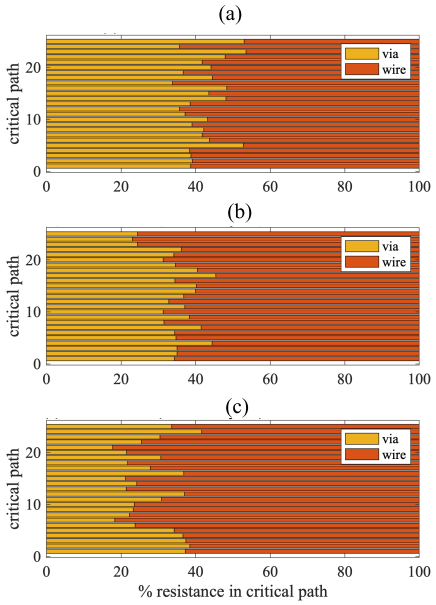

Fig. 5. Via and wire resistance composition in the top 25 critical paths for (a) Rocketcore and (b) Cortex-A53 with six metal levels and (c) Cortex-A53 with nine metal levels.

B. Resistance Sensitivity Analysis

We have also conducted a study on critical path resistance composition. Fig. 5 shows how much via and wire resistances contribute to the total interconnect resistances in the top 25 critical paths for Rocket core and Cortex-A53 designs. In average, vias contribute much more to the total interconnect resistances when comparing Rocketcore to Cortex-A53. Vias contribute 42.4% to the total interconnect resistances in the case of Rocketcore, while they only contribute 28.7% in the case of the nine metal-level Cortex-A53 design. This explains the reason why the TMD 2× design outperforms

TABLE VI
POWER BREAKDOWN FOR ROCKET CORE

Freq. (MHz)	1,544
Sw P. (mW)	25.16
Int P. (mW)	34.78 (49.0%)
Lkg P. (mW)	11.11
Total P. (mW)	71.04
# of cells	161278

→

Item	Power (mW)
FF	19.38 (55.7%)
Clk Buffer	0.97 (2.8%)
Memory	7.34 (21.1%)
Comb.	7.09 (20.4%)

both M13Thin and ImpVia designs for Cortex-A53 with nine metal levels but not for Rocketcore. Improving vias is much more important in the case of Rocketcore due to the critical path composition. Similarly, in the case of six metal-level Cortex-A53 design, the contribution of via resistance is higher compared to the nine metal-level case which causes the TMD 2× case to perform worse than the M13Thin case.

C. Buffer Savings

It is easier to close timing with lower interconnect resistances, which can reduce the number of buffers necessary. Through our simulations, we observed that all BEOL options tend to use fewer buffers with both low and high drive strength compared with the baseline option.

D. Other Observations

We also conducted a study on the impact of BEOL improvements on circuit power. The BEOL improvements have a minimal impact on circuit power as we are only improving the resistances for our cases. With continued node scaling, the portion that the internal power takes up out of the total power of a chip increases. Table VI shows the power breakdown of the Rocketcore design using the CuBKM BEOL. From Table VI, we observe that the internal power contributes 49.0% out of the total power consumption of the design. About 76.8% of this internal power draw is attributed to flip flops and memory, which cannot be reduced by BEOL improvement.

With only the resistance improvements, the main method of saving power is to save on cell power with less usage of buffers. However, buffers make up a relatively small portion of the total standard cells, and the number of buffers saved is trivial. Thus, the BEOL improvement options are not as effective in saving circuit power. Lowering the voltage is possible and could be helpful for power reduction, but that is beyond the scope of this article.

VI. CONCLUSION

In this article, we started from TCAD simulations of MB and vias and went all the way up to placement and routing to investigate the impact of BEOL technology options on circuit performance. With SEMulator-3D and COMSOL simulations, we established a more accurate and uniform modeling for various options. We performed PnR with four benchmarks, each with different size and characteristics to cover a wide range of circuit options. We show that improving the interconnect resistances are more effective in larger and wire-dominant circuits. In the case of Cortex-A53, improving the upper metal levels along with lower metal levels showed significantly higher improvements compared to just improving the lower metal levels, highlighting the impact of improving longer wires connecting to memory blocks in the intermediate to upper metal levels. With TMD interconnects we can substantially lower wire resistances and improve the effective frequency of Cortex-A53 by 76.9% despite their higher via resistances. These BEOL options can also provide up to three metal-level savings in the case of Cortex-A53 as the six metal layer design using TMD interconnects outperforms the baseline nine metal layer design by 18.5%.

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