



# Introduction to Intel® FPGAS and the Quartus® Prime Software Using Remote Hands-Free Labsland

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## 1 HINTS AND TRICKS

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*Some helpful things to keep in mind. Refer to these if you have problems!*

- You should use the Lite version of the Intel Quartus Prime software. This version requires no license. The standard version is fine as well, but that version needs a license that is not provided through this lab work. The Intel® Quartus® Prime Pro Edition software will not work as it does not support the target hardware.
- When Intel Quartus Prime software runs for the very first time, it might ask you about purchasing a license. Select **Run Quartus**. All licenses are free for this lab.
- If something fails to compile, check **Top Level Entity Setting** → **Setting** → **Top Level Entity** and make sure that the module **<design>** matches your top level entity. This includes Verilog file names that don't match module names with case-sensitivity.
- If Programmer fails to program on the first try, hit **Start** twice.
- The errors in the Knight Rider Lab code are intentionally designed to give you an opportunity to practice debugging. Study the code carefully to fix errors.
- If the Knight Rider LEDR[0] is the only LED that turns on, you have not assigned the CLOCK\_50 pin properly in your assignments.
- Check the LEDR[0] and LEDR[9] pins carefully in the Knight Rider Lab and see if they sequence properly. If not, study the code carefully!
- Sometimes copying and pasting from text files into Quartus's TCL console can have carriage return formatting errors. Links are provided with the code to help you solve this problem. If you see run-on lines with no carriage returns, you need to either copy code over line by line or add the appropriate file to your project. This is not specifically documented in the lab flow.

## 2 Installing the Quartus Prime Lite Design Tools

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### 2.1 Background

A field-programmable gate array, or FPGA, is a digital semiconductor that can be used to build a wide variety of electronic functions. These data center accelerators, wireless base stations and industrial motor controllers to name but a few common applications. This is because FPGAs can be infinitely reconfigured to perform different digital hardware functions, which also makes for an excellent learning platform.

To configure an FPGA, first you describe your digital electronics with either a Hardware Description Language (HDL), such as Verilog or VHDL, or a schematic. Then you assign the “pins” of your FPGA based on how the Printed Circuit Board (PCB) connects the FPGA to various peripheral components on your board. Some examples of peripherals are switches, LEDs, memory devices and various connectors. Finally, you “compile” your design and program the FPGA to perform the function you have specified in the HDL or schematic.

This training class assumes you have some prerequisite knowledge of how computers and digital electronics work, but by no means do you need an electrical engineering degree to follow along this introductory course.

### 2.2 Installation

Quartus Prime is Intel FPGA's design tool suite. It serves a number of functions:

- Design creation through the use of HDL or schematics
- System creation through the Platform Designer (formerly Qsys) graphical interface
- Generation and editing of constraints (timing, pin locations, physical location on die, I/O voltage levels)
- Synthesis of high level language into an FPGA netlist, formally known as mapping

- FPGA place and route, formally known as fitting
- Generation of design image used to program an FPGA, formally known as assembly
- Timing Analysis
- Download of design image into FPGA hardware, formally known as programming
- Debugging by insertion of debug logic (in-chip logic analyzer)
- Interfacing to third party tools such as simulators
- Launching of Software Build Tools (Eclipse) for Nios II To download Quartus

Prime Lite, follow these instructions:

Visit this site: <http://fpgasoftware.intel.com/?edition=lite>.

Select version 18.1 and your PC's operating system.

For the smallest installation and quickest download time, select only the fields shown below in Figure 1.

Follow the instructions to activate the Quartus tools on your PC.

## Download Center for FPGAs

Design Software

Embedded Software

Archives

Licensing

Programming Software

Drivers

Board System Design

Board Layout and Test

Legacy Software

Quartus Prime Lite Edition

Release date: September, 2018  
Latest Release: v20.1.1

Select edition: 

Lite

Select release: 

18.1

Operating System: 

Windows

Linux

Intel Quartus Prime

Design Software

A newer version of the Quartus Prime Design Software is available. Users should upgrade to the latest version of the [Quartus Prime Design Software](#). This version does not include the latest functional and security updates. If you must use this version of software, follow the [technical recommendations](#) to help improve security. For critical support requests, please contact our [support team](#).

The Quartus Prime Lite Edition Design Software, Version 18.1 is subject to removal from the web when support for all devices in this release are available in a newer version, or all devices supported by this version are obsolete. If you would like to receive customer notifications by e-mail, please subscribe to our [subscribe to our customer notification mailing list](#).

The Quartus Prime Lite Edition Design Software, Version 18.1 supports the following device families: Arria II, Cyclone 10 LP, Cyclone IV, Cyclone V, MAX II, MAX V, and MAX 10 FPGA. [View](#)

Combined Files Individual Files Additional Software Updates

Download and Install Instructions: [More](#)

[Read Intel FPGA Software v18.1 Installation FAQ](#)

[Quick Start Guide](#)

LinkTypes Available

Quartus Prime Lite Edition (Free)

Quartus Prime (Includes Nios II EDS)  
Size: 1.7 GB MD5: F0D752D67B18C88F8C0043CEE676896D

ModelSim-Intel FPGA Edition (Includes Starter Edition)  
Size: 1.1 GB MD5: 7FD6E889A8929AEDD617F410079AA38

Devices

You must install device support for at least one device family to use the Quartus Prime software.

Arria II device support  
Size: 499.6 MB MD5: D87CA20C91596BC6C78CE64283D956B7

Cyclone IV device support  
Size: 466.6 MB MD5: 9E32B86F83A4408041848D729B143D8C

Cyclone 10 LP device support  
Size: 496.1 MB MD5: 7274C819D935FF6B6E42849B8F0FDD0

Cyclone V device support  
Size: 1.1 GB MD5: 79F5029A9058F64F969486B016EE19D4

MAX II, MAX V device support  
Size: 11.4 MB MD5: ED980776F79C86D308877F27A30B7666

MAX 10 FPGA device support  
Size: 330.9 MB MD5: E87E36DAB144529EFC818C2482F1B1FE

Note: The Quartus Prime software is a full-featured EDA product. Depending on your download speed, download times may be lengthy.

Figure 1: Quartus Prime Lite Minimum Required Files to Download

## 3 New Project Wizard


### 3.1 Summary

This is a short lab that completes the basic project setup. At the end of this lab, you will be able to start a new project using New Project Wizard in Quartus Prime

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Software. There are other related tutorial links provided for you to learn more about the software.

## 3.2 Navigation of Quartus Prime Lite

Open the tools by double clicking the Quartus Prime icon: . You should now see something similar to Figure 2. The first time you launch Quartus, it might ask you about acquiring a license, you just need to use the run Quartus option.

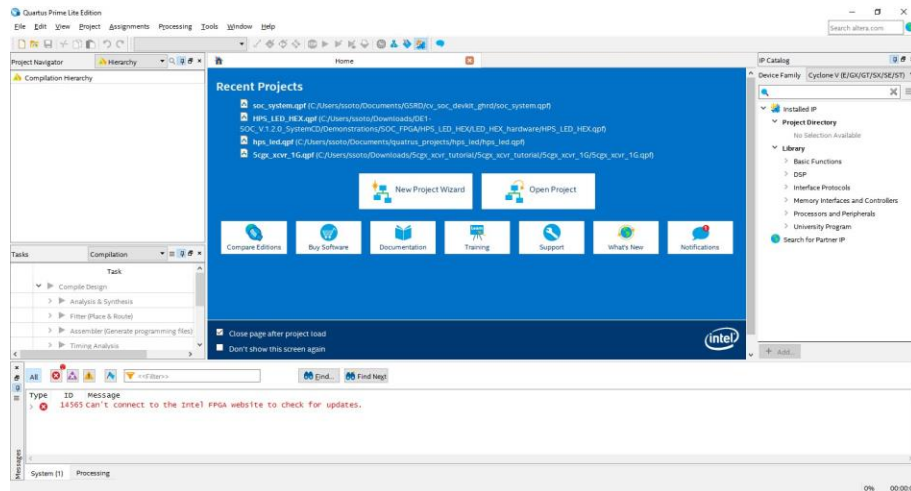


Figure 2: Quartus Prime main window

## 3.3 New Project Wizard

In the main toolbar of Quartus, navigate to the **File** drop down menu and **New Project Wizard**.

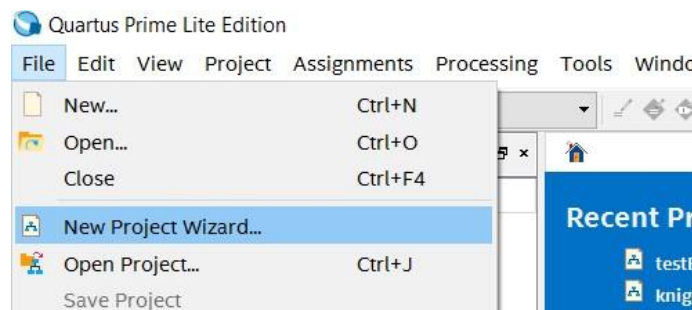


Figure 3: Quartus Prime file menu

**Pane 1: Introduction.** There is nothing to configure on this pane. Click **Next** to continue.

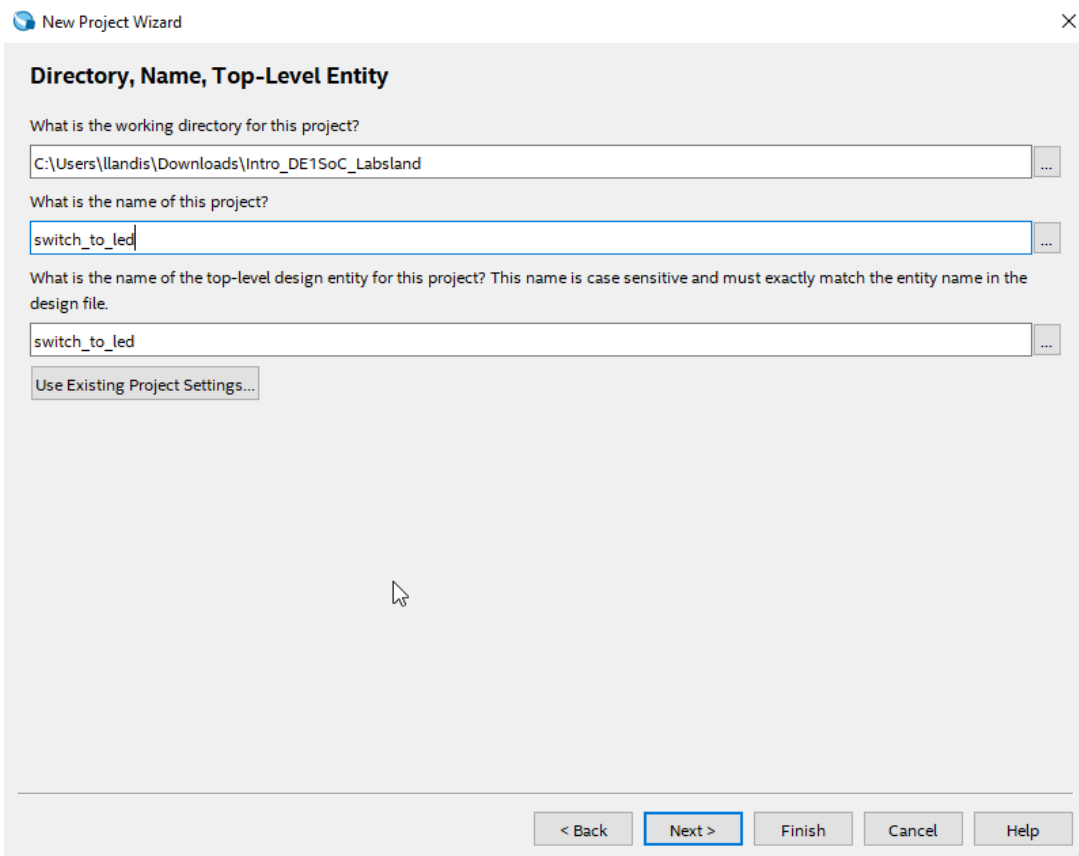
## **Pane 2: Directory, Name, Top-Level Entity.**

Fill in with a directory of your choice. It is recommended to be a personal directory, and not a directory under Quartus installation which is the default.

Call the project **switch\_to\_led** and the top level entity **switch\_to\_led**.

*The name of the top-level design entity is **case-sensitive** so ensure that you type the name in all lower-case. See Figure 4 below for a completed Pane 2.*

*Note: the screen shots will have a different directory than what you will use for your project. This is fine!*



The screenshot shows the 'New Project Wizard' window, specifically the 'Directory, Name, Top-Level Entity' pane. The window has a title bar with a blue icon and the text 'New Project Wizard'. The main area contains three text input fields, each with a '...' button to its right. The first field is labeled 'What is the working directory for this project?' and contains the text 'C:\Users\l\landis\Downloads\Intro\_DE1SoC\_Labsland'. The second field is labeled 'What is the name of this project?' and contains the text 'switch\_to\_led'. The third field is labeled 'What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.' and contains the text 'switch\_to\_led'. Below these fields is a button labeled 'Use Existing Project Settings...'. At the bottom of the window is a row of five buttons: '< Back', 'Next >', 'Finish', 'Cancel', and 'Help'. The 'Next >' button is highlighted with a blue border.

*Figure 4: Pane 2 of the New Project Wizard*

**Pane 3: Project Type.** Select **Empty project**. Click **Next**.

**Pane 4: Add Files.** Click **Next**. We will add project source files later.

**Pane 5: Family, Device, and Board Settings.**

Family should be set to Cyclone V. Make sure the tab is set to Device.

The part number for the FPGA chip you will use is 5CSEMA5F31C6. You need to type this number in the search bar.

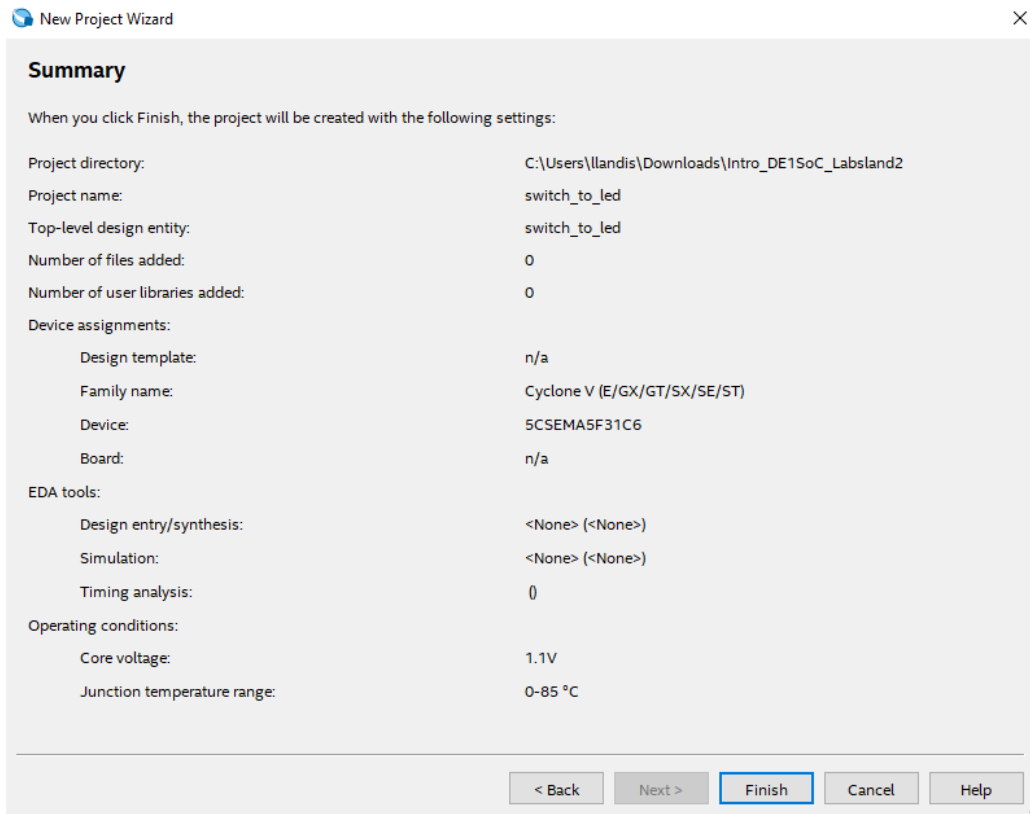
**Pane 6: EDA Tool Settings.** Skip this section and click **Next**. This section is only needed if you are using other development software besides Quartus Prime.

**Pane 7: Summary.** Pane 7 should look similar to the image seen in Figure 5.

*Note: you now have a project called **Lab**, and top-level entity called **switch\_to\_led**, no files selected (yet) and are using a Cyclone III device.*

Click **Finish**.





*Figure 5: Summary page generated by the New Project Wizard*

You should now see something similar to Figure 6 (The **Tool View Window** may just have a gray Quartus Prime screen. This is fine.)

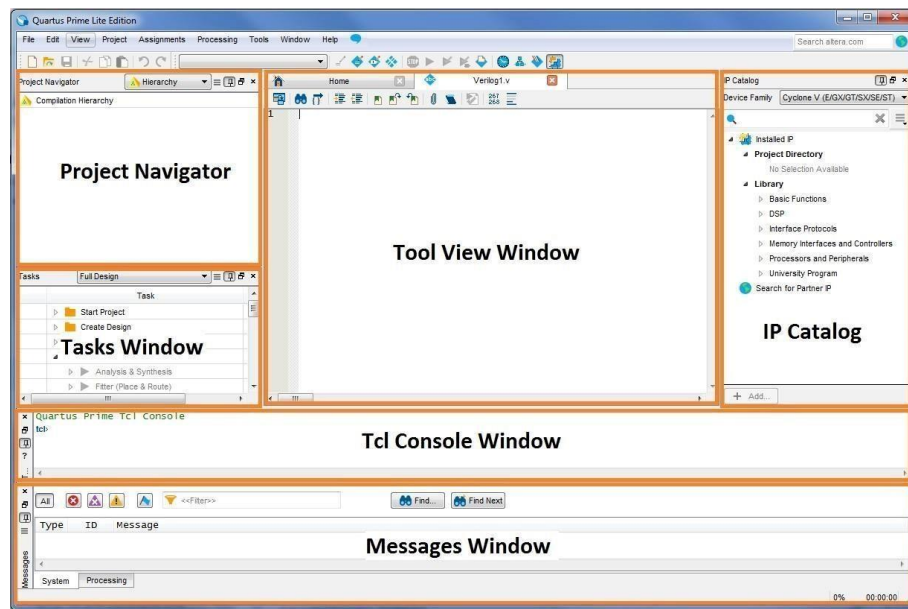


Figure 6: Quartus Prime project window

Some windows may not be shown by default. To customize what windows are shown, click on the **View** tab and look under the **Utility Windows** drop down as seen in Figure 7.



*Figure 7: Utility Windows dropdown*

If you navigate in Windows Explorer to your project directory, you will see some files and directories created by the New Project Wizard as part of the setup process.

## 4 Switch to LED

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### 4.1 Summary

This lab will step you through the process of a simple design from generating your first Verilog file to synthesize and compile. Synthesis converts your Verilog language file to an FPGA specific “netlist” that programs the programmable FPGA lookup tables into your desired function. Compilation figures out the location of the lookup table cells used in the FPGA and generates a programming image that is downloaded to your Intel FPGA Development kit. At the end of this lab, you will be able to test the functionality of the example digital electronic circuits by toggling the switches and observing the LEDs for proper circuit operation.

### 4.2 Creating a New File

Create a Verilog HDL file. Go the File dropdown menu and select New.

A window, shown in Figure 8, should pop up. Click on Verilog HDL File and then Ok.

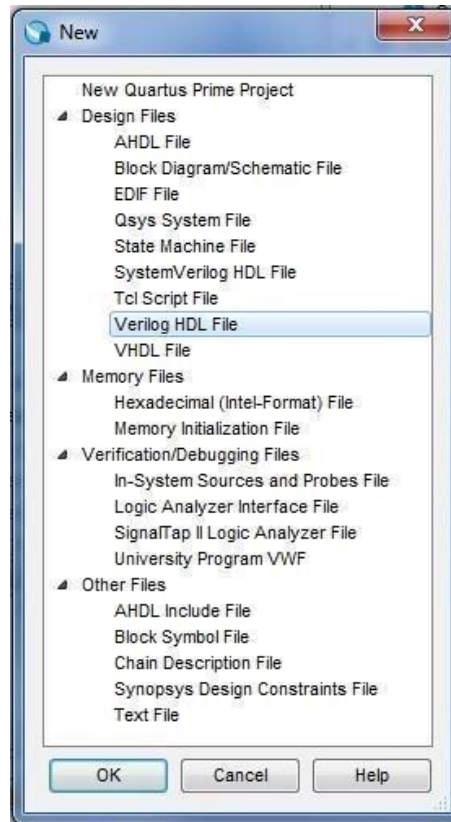


Figure 8: New File Window

### 4.3 Adding Verilog Code

Create a simple module in your Verilog HDL file copying/pasting this code from the file [switch\\_to\\_led.v](#).

The code you will use is displayed below. **Do not** cut and paste from here as sometimes cut and paste from a github pdf or downloaded pdf introduces some illegal characters.

```
module switch_to_led(SW, LEDR); //create module switch_to_led
input [9:0] SW; // input declarations: 10 switches
output [9:0] LEDR; // output declarations: 10 red LEDs
assign LEDR = SW; // connect switches to LEDs
endmodule
```

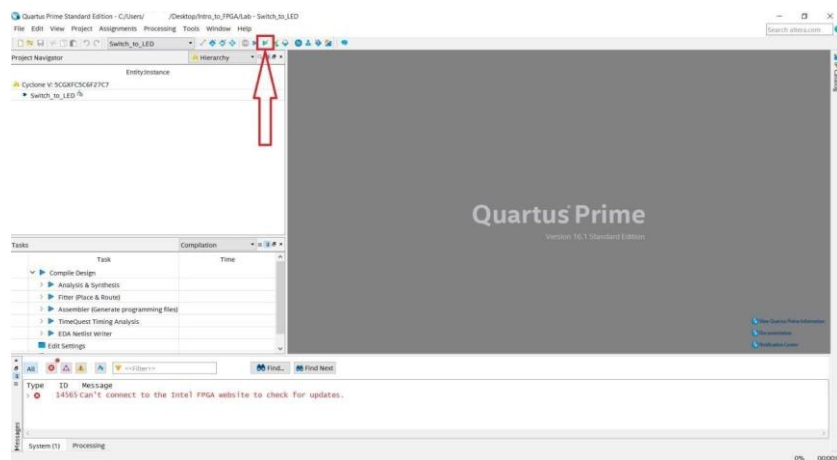
Make sure carriage returns and new lines are in the right location or your code will not compile properly! Verilog treats all blank space (spaces or tabs) the same.

**BRAIN EXERCISE** : Check your syntax carefully! Can you explain what this circuit does?

Click on File, name the file as switch\_to\_led (ensuring case-sensitivity), and click Save As... to save your Verilog file.

Next you will run Analysis and Elaboration. Analysis and Elaboration checks the syntax of your Verilog code, resolves references to other modules and maps to FPGA logic. If you see any errors during the Analysis and Elaboration step, carefully review your Verilog code for syntax errors and re-run this step.

To run Analysis and Elaboration, click the Play button with a green check mark, shown in Figure 9 below.



*Figure 9: Analysis and Elaboration check mark*

#### 4.4 Assigning Pins

By default, Quartus Prime does not know how the FPGA pins on the DE1-SoC development board are connected to the switches and LEDs used in this circuit. Because our FPGA is already on a PCB, we need to tell Quartus what pins to use. Although Quartus allows you to select a development board with a predefined pinout, this lab shows you how to define your own pinout as an exercise.

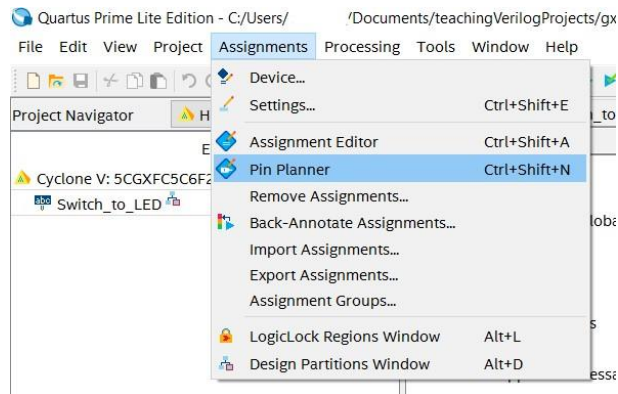


Figure 10: Quartus Assignments menu

The next steps will assign the switches and LED signals in your code to the appropriate pins.

Using the main toolbar at the top of the Quartus window, navigate to the Assignments dropdown menu as shown above in Figure 10. Click on Pin Planner and a window similar to the image in Figure 11 should open.

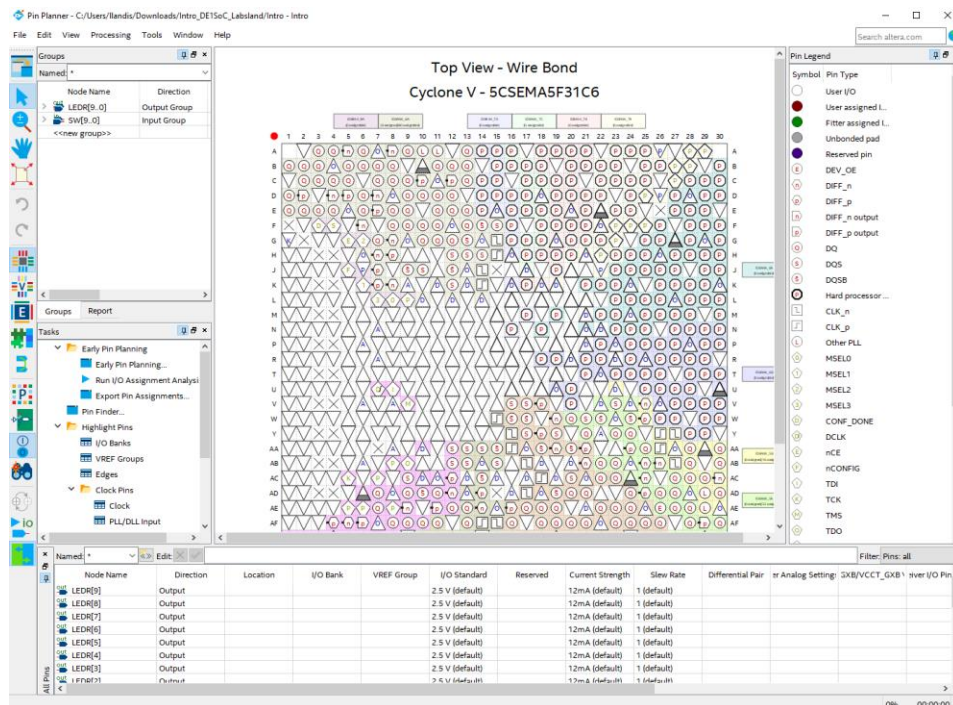


Figure 11: Pin Planner Assignment window

We can see the I/O pins have not been assigned to any locations yet. To make the right pin assignments, refer to the table below.

*Note: The switch\_to\_led lab does not require the CLOCK\_50 signal but it will be used in the final lab and will resolve when you run that lab.*

LEDR[9]	PIN_Y21
LEDR[8]	PIN_W21
LEDR[7]	PIN_W20
LEDR[6]	PIN_Y19
LEDR[5]	PIN_W19
LEDR[4]	PIN_W17
LEDR[3]	PIN_V18
LEDR[2]	PIN_V17
LEDR[1]	PIN_W16
LEDR[0]	PIN_V16
SW[9]	PIN_AF16
SW[8]	PIN_AE16
SW[7]	PIN_AG16
SW[6]	PIN_AH17
SW[5]	PIN_AH18
SW[4]	PIN_AJ16
SW[3]	PIN_AJ17
SW[2]	PIN_AJ19
SW[1]	PIN_AK19
SW[0]	PIN_AK18
CLOCK_50	PIN_AF14

## TO ASSIGN PINS

Match the Signal Name (1st column) with the FPGA Pin # (2nd column) in the table above. Assign LEDR[9] to PIN\_Y21 by typing PIN\_Y21 in the location column in the Pin Planner.

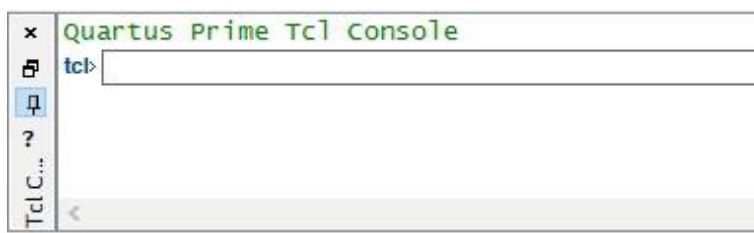
*Note: the signal names in your code and names in the manual don't have to match. As long as you connect the names in your design to the proper pin location, your design will be connected properly. In this lab, we have named the signals as a vector so pin names are of the form LEDR[0], LEDR[1] and so on.*



An alternate method is to left click on the Node Name in the Pin Planner and drag the pin on top of the ball grid map location assigned in the table. Release the pin on the proper location. Hit the escape key and move to the next pin. Assign LEDR[8] to PIN\_W21 using this method.

When you finish, you can just close the window – the Pin Planner does not have a Save button, but it will save anyways. This switch\_to\_led lab does not require the CLOCK\_50 signals so you can ignore these for the time being. The clock signal is required for the Knight Rider lab, so you will need to assign it prior to compiling that lab.

Last, we will assign the remaining pins using a TCL commands. In Quartus, proceed to View → Utility Windows → TCL Console. You should see a window across the bottom of your Quartus window as shown in Figure 12. If it doesn't show up, try the command again as this toggles the window on and off.



*Figure 12: TCL Console window*

Open this file that contains the TCL pin placement commands: [DE1\\_SOC\\_pins.tcl](#).

Copy the commands from the file and enter them in the TCL Console window. Note that if you reassign pins that have already been assigned in the pin planner, this will not cause a problem, as long as the pin locations are correct. Make sure that carriage returns are properly copied over from these TCL commands into the TCL utility window. If all the lines in the DE1SOC\_pins.tcl show up on one line, try another editor (eg vi seems to merge all the lines and notepad includes the carriage returns). If all 21 TCL commands show up as a single continuous line, you will need to copy and paste each command one at a time, or copy from a different editor. The beginning of each line starts with set\_location\_assignment. **Note:** Make sure you enter the last carriage return


entered in the TCL command window to pick up the last line CLOCK\_50 pin location.

Now the remaining pins have been assigned for you by the script. To check what has been assigned, you can return to the Pin Planner application or alternatively open the Assignment Editor Window (Assignments → Assignment Editor) to check that the TCL commands have properly set the pinout for your Switch to LED design. Try both methods to familiarize yourself with different techniques to manage and observe pin constraints. Note the direction of the ports since they match your switch\_to\_led design. CLOCK\_50 port is indicated with a question mark since it doesn't exist in your design, but will be used in a subsequent lab.

	tatu	From	To	Assignment Name	Value	Enabled	Entity	Comment	Tag
1	✓		out LEDR[9]	Location	PIN_Y21	Yes			
2	✓		out LEDR[8]	Location	PIN_W21	Yes			
3	✓		out LEDR[6]	Location	PIN_Y19	Yes			
4	✓		out LEDR[7]	Location	PIN_W20	Yes			
5	✓		out LEDR[5]	Location	PIN_W19	Yes			
6	✓		out LEDR[4]	Location	PIN_W17	Yes			
7	✓		out LEDR[3]	Location	PIN_V18	Yes			
8	✓		out LEDR[2]	Location	PIN_V17	Yes			
9	✓		out LEDR[1]	Location	PIN_W16	Yes			
10	✓		out LEDR[0]	Location	PIN_V16	Yes			
11	✓		in SW[9]	Location	PIN_AF16	Yes			
12	✓		in SW[8]	Location	PIN_AE16	Yes			
13	✓		in SW[7]	Location	PIN_AG16	Yes			
14	✓		in SW[6]	Location	PIN_AH17	Yes			
15	✓		in SW[5]	Location	PIN_AH18	Yes			
16	✓		in SW[4]	Location	PIN_AJ16	Yes			
17	✓		in SW[3]	Location	PIN_AJ17	Yes			
18	✓		in SW[2]	Location	PIN_AJ19	Yes			
19	✓		in SW[1]	Location	PIN_AK19	Yes			
20	✓		in SW[0]	Location	PIN_AK18	Yes			
21	?		CLOCK_50	Location	PIN_AF14	Yes			
22		<<new>>	<<new>>	<<new>>					

Figure 13: Pin Assignments

#### 4.5 Compiling Your Code

Click , located at the top of the main Quartus window, to start the full compilation of your code. You can also go to: **Processing → Start Compilation**.

After roughly 1 to 2 minutes depending on your machine type and amount of RAM, the compilation should complete and there should be 0 errors. (You can ignore warnings.)

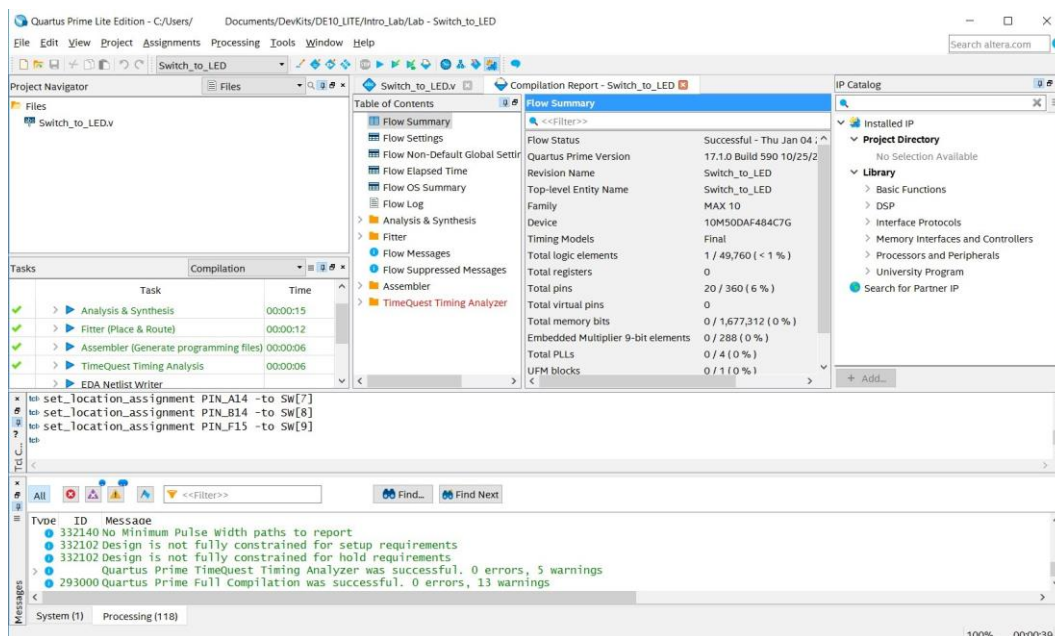


Figure 14: Quartus window showing successful compilation

#### 4.6 Programming Your FPGA Design using labsland remote board access

Labsland is a company that specializes in hosting remote labs. Click on this [link](#) and you will be instructed to create a student account. Enter your credentials.

Labsland offers two methods of connectivity to development boards. The first is what is called IDE mode. IDE mode is an overlay on top of Quartus that allows a user to add files, compile and program in a simplified GUI. It doesn't offer the flexibility of Quartus but is great for first time users of FPGAs. The second mode is called no-IDE mode which supports programming the FPGA development kit only. All design and development work is run on a locally installed version of Quartus. You will be using the no IDE mode for this lab.

At this point you should be in the No-IDE mode window. If you are not, click on this [link](#) to run the DE1-SoC development kit in "no-IDE" mode. To allow others access and make sure boards are not always occupied, you get two minutes to access your FPGA development kit. **Note:** Do not log out of the Labsland window for the duration of the workshop or your credentials might expire! Work efficiently so you don't need to

continually login to connect to a board. Click Access. Next click Choose File and navigate to your programming image called switch\_to\_led.sof which is usually located in the output\_files directory of your project. If you have used Quartus before it might have a setting to place in the project directory.

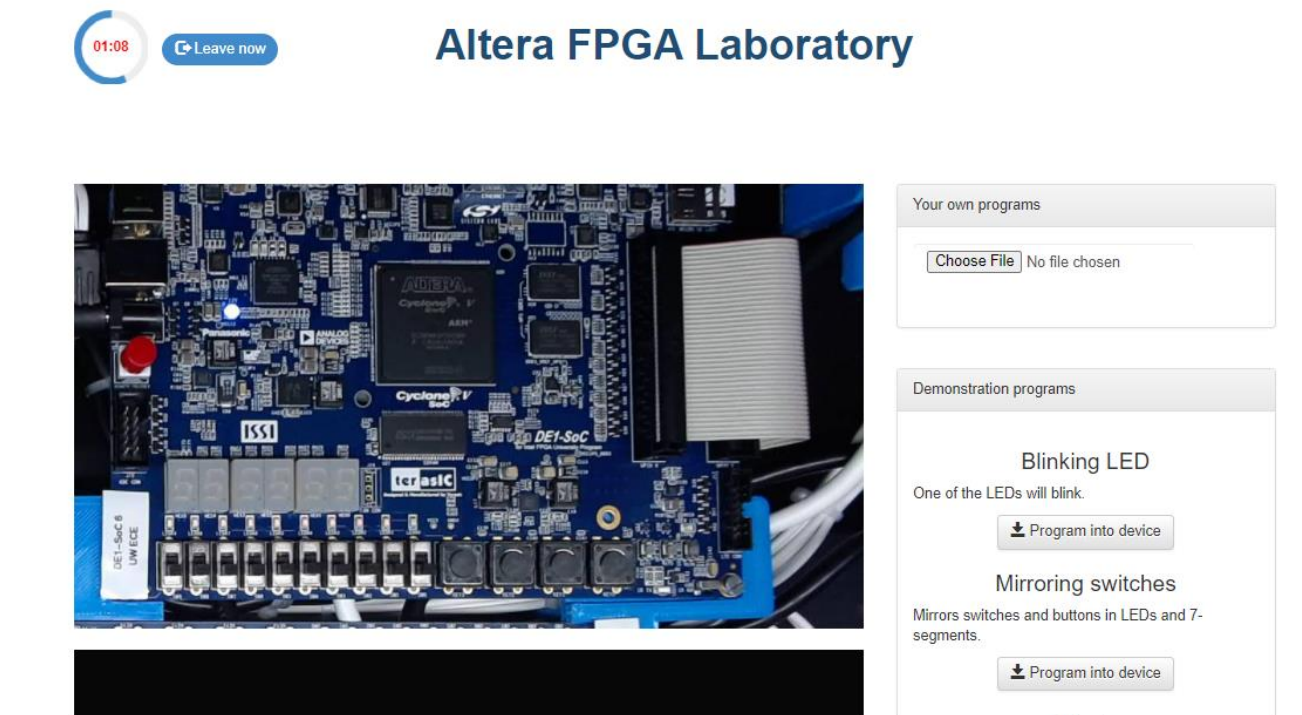


Figure 15: Labsland FPGA labratory

Upload the .sof file. Next, click on the virtualized switch buttons and observe the associated LEDs illuminate on the board through the camera view. Congratulations! You have just completed the switch\_to\_led lab using the DE1-SoC Development Board.

## 5 LAB 4: 2 TO 1 MULTIPLEXER

### 5.1 Summary

Follow the steps from last lab and implement a 3 bit wide 2-to-1 multiplexer. A 2-1 multiplexer selects one of 2 data inputs. If the “S” pin is logic 0, M gets the

value X, else (if S is logic 1) M gets the value Y. Note this lab uses arrays. To define an array, refer back to the `switch_to_led.v` code in Section 3.1 where we used syntax such as `input [9:0] SW` to define the input signal.

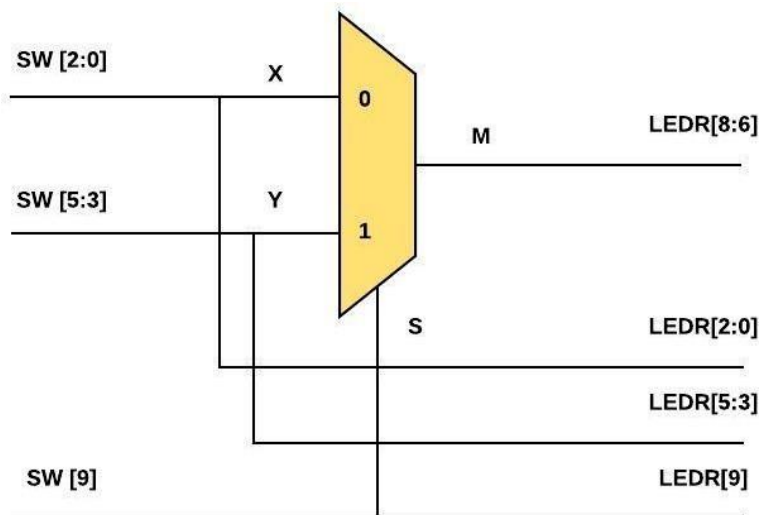


Figure 16: Logic Flow for a 2 to 1 Mux

## 5.2 Creating a Revision

In this lab, we are going to use a handy feature in Quartus called revisions. Using revisions will save you time since you can reuse the pin settings you made in the Pin Planner tool and carry them over to other projects. The revision will create a copy of your design with device and pin settings, and Verilog source code used in the prior lab.

Launch the Revision tool by navigating to **Project** → **Revisions**.

Add a new revision by doubling clicking on the **New Revision** selection and make the revision name **mux\_2\_to\_1**. *Ensure that the revision name is entered with case-sensitivity to avoid compilation errors.* On the following page, continue by clicking **OK**.

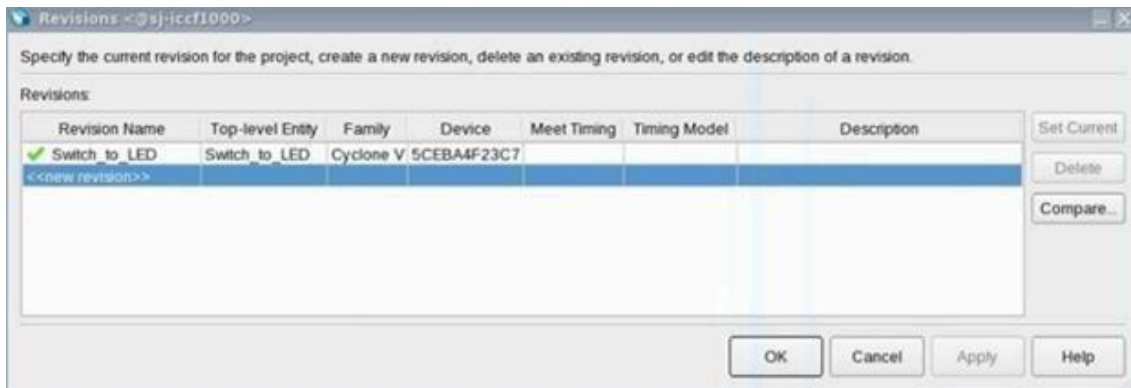


Figure 17: Quartus revisions window

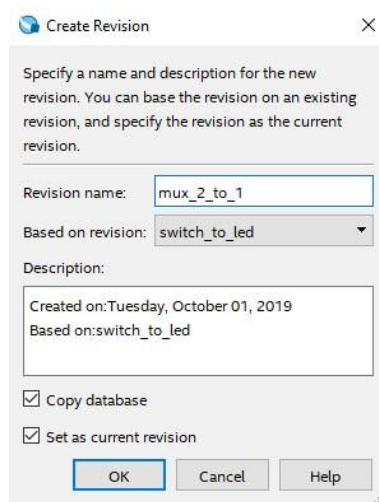


Figure 18: Final Revision Creation window

### 5.3 2 to 1 Mux Verilog Code

There are several approaches to this lab. If you are brand new to coding in Verilog you may copy and paste the code from Section 4.5 (not the code snippets below). Should you choose this option, once you copy the code and save the Verilog file to the name **mux\_2\_to\_1.v**. You can also download the code [here](#).

The other option is to create a Verilog file from scratch for the 3-bit wide 2-to-1 multiplexer in your project. Take a look at the code from switch\_to\_led on how to declare the ports on your module. This means to include the module statement and inputs/output definitions.

## CHECKLIST:

Use switch **SW[9]** as the **S** input (the selection bit of the multiplexer), switches **SW[2:0]** as the **X** input and switches **SW[5:3]** as the **Y** input.

With assign statements, display the value of the input **S** on **LEDR[9]**, input **X** on **LEDR[2:0]**, input **Y** on **LEDR[5:3]**.

Assign **M** to **LEDR[8:6]**.

There are several ways to define a multiplexer in Verilog. Pick one of the three styles shown below. If you have time, try a couple of different coding styles for practice. Place these lines after the module definition and before the end module statement.

## CONTINUOUS ASSIGNMENT:

```
assign M = (S==1) ? Y : X; // If S then M = Y else M = X //  
    All signals are of type wire.
```

## PROCEDURAL ASSIGNMENT "IF" STATEMENT:

```
always @ (S or X or Y) begin // If any of the signals S, X or Y //  
    change state, execute this code.  
    // Note that signals to the left of an  
    // equal sign in an always block // need  
    to be declared of type reg so // declare  
    M as:  
    // reg [2:0] M;  
  
    if(S == 1)  
        M <= Y;          // Note the non-blocking operator "<="
```

```
    else  
        M <= X;  
end
```

## PROCEDURAL ASSIGNMENT "CASE" STATEMENT:

```

always @ (S or X or Y) begin case (S)
'1b0: M <= X;
'1b1: M <= Y; endcase
end

```

Also note that variables that are assigned to the left of an equal sign (= or <=) in an always block must be defined as reg. Other variables are defined as wire. If undeclared, variables default to a 1 bit wire.

With the above port and signal assignments, we will see the output X when the select input S is low and we will see Y when S is high.

The completed code is here:

```

module mux_2_to_1 (SW, LEDR);          //Create module mux_2_to_1
input [9:0]SW; //Input Declarations: 10 slide switches
output[9:0]LEDR; //Output Declarations: 10 red LED lights

wire S; //Declare the Select signal
wire [2:0] X, Y, M; //Declare the inputs and outputs to the MUX

assign S = SW[9]; //Assigning input switches to internal signals
assign X = SW[2:0];
assign Y = SW[5:3];
assign LEDR[8:6] = M; //Assigning internal signals to output LEDs
assign LEDR[9] = SW[9];
assign LEDR[2:0] = SW[2:0];
assign LEDR[5:3] = SW[5:3];
assign M = (S == 0) ? X : Y; //MuxSelect Function

endmodule

```

## 5.4 Revision Control

Now you need to make sure you have the proper files included in your project.



To the right of the Project Navigator Window, change Hierarchy to Files. You will only be operating on the mux\_2\_to\_1.v so you will need to remove switch\_to\_led.v from your project.

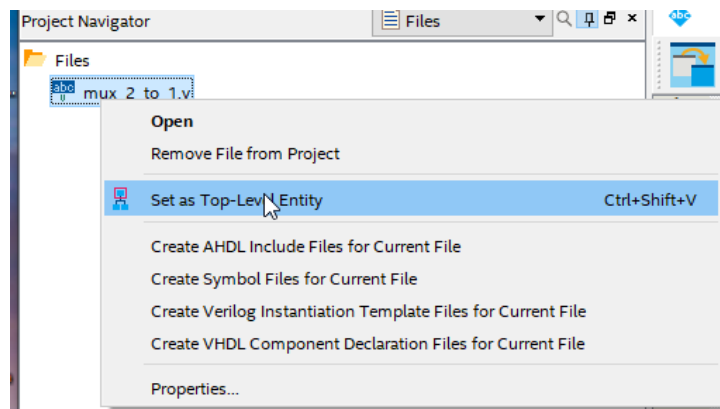


Figure 19: Changing Top Level Entity

Right click **switch\_to\_led.v** and remove this source file from your project.

Next you need to change your top-level entity from switch\_to\_led to mux\_2\_to\_1. Right click mux\_2\_to\_1.v and **Set as Top-Level Entity**. Now your revision and your top level entity is mux\_2\_to\_1.

*It is important to note the difference between a project, revision, top level entity, and top level Verilog file of your overall project. A single project can have multiple revisions. The project name does not have to match the name of the top level entity of your design. Similarly, the Verilog file name might not have the same name as the top level entity and can indeed contain many modules (entities).*

A common compilation error is a mismatch between what the top level module in your code is versus the one assigned in the Quartus settings. If you have a compilation error of this nature, check: Assignments → Setting → General and make sure the top level entity (in this case mux\_2\_to\_1) is indeed set to the one you think you are compiling your Verilog source code. Ensure that top level entity names match with their corresponding Verilog file names as they are case-sensitive.

Compile your design by pressing  along the top of the Quartus window.

## 5.5 Checking Pin Locations and Editing (If Necessary)

In your project, the required pin assignments for your DE1-SoC Development board will have carried over from the previous lab since the pin names are the same.

Open up the Assignment Editor to make sure the pin names are indeed assigned to the appropriate pin locations. Assignments → Pin Planner. (Note: pin assignments can also be seen through Assignments → Assignment Editor.)

## 5.6 Downloading Your Design to Your Device

Once you have successfully compiled the project, download the resulting .sof file onto the FPGA chip as you did in section 3.5.

Test the functionality of the 3-bit wide 2-to-1 multiplexer by toggling the switches and observing the LEDs. Remember that we want the lights LEDR[2:0] to display input X, LEDR[5:3] to display Y, LEDR [8:6] to display the multiplexed result, LEDR[9] to display the switch SW[9] result (selection bit).

## 5.7 Viewing Design Schematic

When you compile Verilog, or any HDL (Hardware Description Language), Quartus synthesizes your code into hardware. This hardware can be viewed through the RTL Viewer (Register Transfer Level Viewer).

The RTL Viewer can be found under task on the left-hand side by looking into the Analysis & Synthesis dropdown and then the Netlist Viewers dropdown, as shown in Figure 22. Once opened, you should see a 2-to-1 mux similar to what is seen in Figure 23.

	Task	Time
✓	▼ ▶ Compile Design	00:02:24
✓	▼ ▶ Analysis & Synthesis	00:01:11
	■ Edit Settings	
	■ View Report	
✓	▶ Analysis & Elaboration	
	> ▶ Partition Merge	
	▼ 📁 Netlist Viewers	
	🔍 RTL Viewer	
	🌐 State Machine Viewer	
	🗺️ Technology Map Viewer (Post-Mapping)	

Figure 20: RTL Viewer selection

	Task	Time
✓	▼ ▶ Compile Design	00:02:24
✓	▼ ▶ Analysis & Synthesis	00:01:11
	■ Edit Settings	
	■ View Report	
✓	▶ Analysis & Elaboration	
	> ▶ Partition Merge	
	▼ 📁 Netlist Viewers	
	🔍 RTL Viewer	
	🌐 State Machine Viewer	
	🗺️ Technology Map Viewer (Post-Mapping)	

Figure 21: RTL Viewer of a 2 to 1 Mux

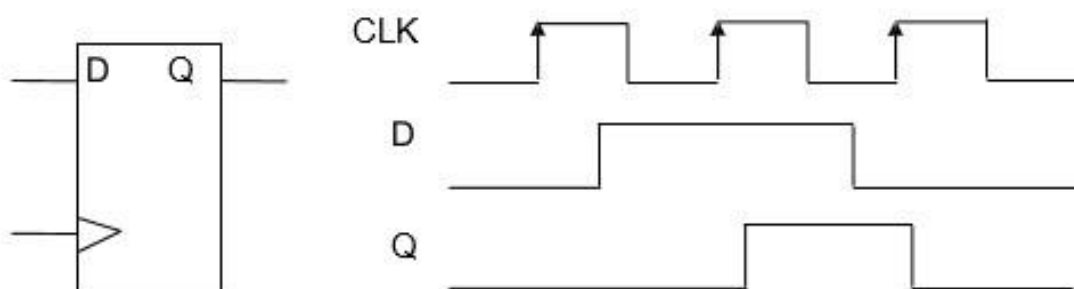
## 6 Knight Rider

### 6.1 Summary

Perhaps some of you have heard of or watched a TV show called Knight Rider that aired from 1982 to 1986 and starred David Hasselhoff. The premise of the show was David Hasselhoff was a high-tech crime fighter (at least high

technology for 1982) and drove around an intelligent car named “KITT”. The KITT car was a 1982 Pontiac Trans-Am sports car with all sorts of cool gadgets. The interesting gadget of interest for this lab were the headlights of KITT which consisted of a horizontal bar of lights that sequenced one at a time from left to right and back again at the rate of about 1/10th of a second per light. Check out this short [YouTube<sup>1</sup> video](#) for crime fighting and automotive lighting technology’s finest moment. This lab will teach you a thing or two about sequential logic and flip-flops. Let’s quickly review how flip-flops work.

Flip-flops are basic storage elements in digital electronics. In their simplest form, they have 3 pins: D, Q, and Clock. The diagram of voltage versus time (often referred to as a waveform) for a flip-flop is shown below. Flip-flops capture the value of the “D” pin when the clock pin (the one with the triangle at its input transitions from low to high). This value of D then shows up at the Q output of the flip-flop a very short time later.



*Figure 22: Flip-flop diagram*

When you connect several flip-flops together serially you get what is known as a shift register. That circuit serves as the basis for the Knight Rider LED circuit that we will study in this lab. Note how we clock in a 1 for a single cycle and it “shifts” through the circuit. If that “1” is driving an LED each successive LED will light up for 1/10 of a second.

## 6.2 Knight Rider Verilog Code

The following Verilog code is the starting point for your Knight Rider design, but there are some bugs. Start a new revision of the project “switch\_to\_led” as you did in section 4.0 and call it knight\_rider with similar settings as the previous labs.

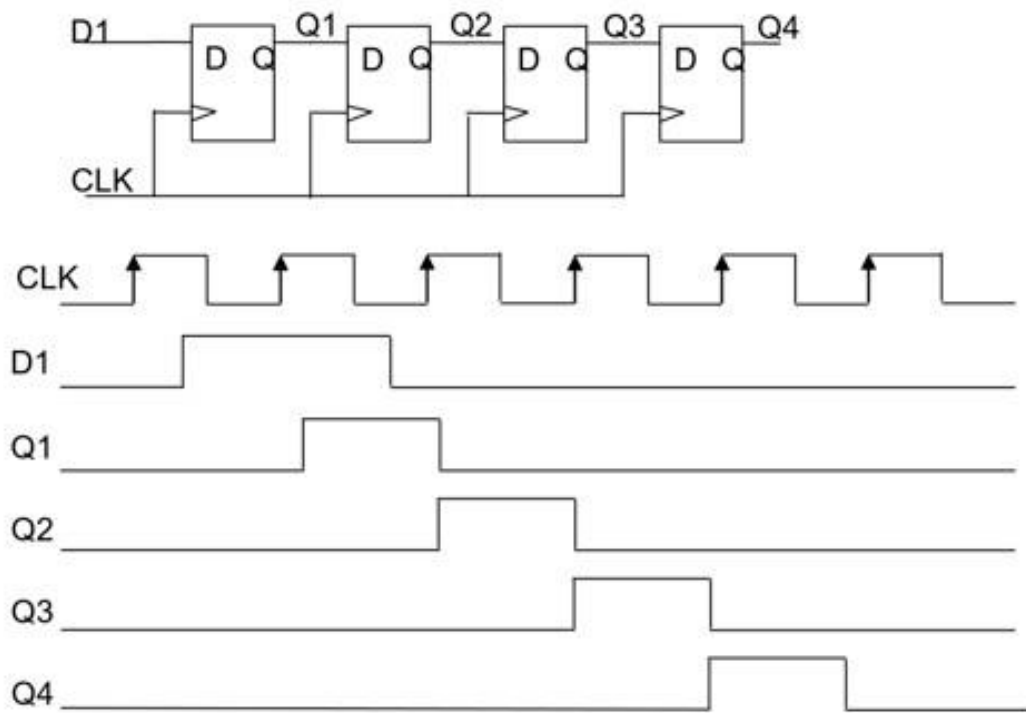


Figure 23: Shift Register diagram

The code given **intentionally** has errors. See if you can find them all. You can find this in design file [knight\\_rider.v](#)

### 6.3 Creating “knight\_rider.v”

Open a new Verilog file and which will you later save as **knight\_rider.v**. Copy and paste the code above into knight\_rider.v in Quartus.

Make sure your top level entity is called knight\_rider and the source file is knight\_rider.v.

Delete any other Verilog files in the current project – eg right click and remove from mux\_2\_to\_1.v from your project.

In the upper left Project Navigator window, you should see something similar to this:

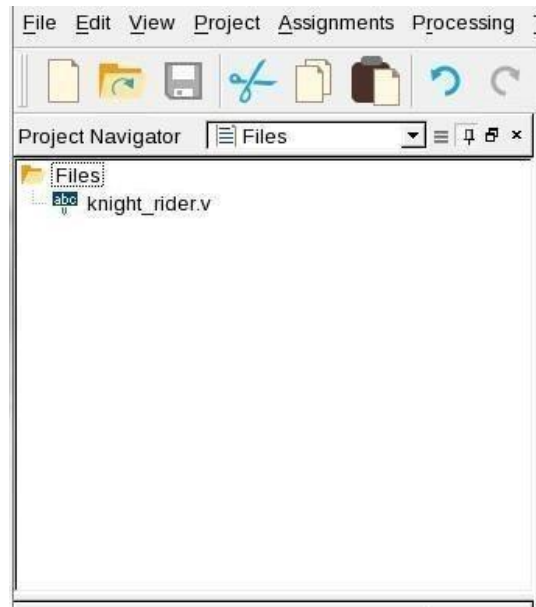





Figure 24: Example of *knight\_rider.v* in Quartus Window

## 6.4 Debugging Code

Click on the **Play**  button and run **Analysis & Elaboration**. This source code has several syntax bugs. Look at the transcript window on the bottom and observe the errors that are flagged with  symbol. Carefully look at the source code and fix the errors and continue to recompile until the compilation steps run to completion.

## 6.5 Assigning Pins with the Pin Planner Tool

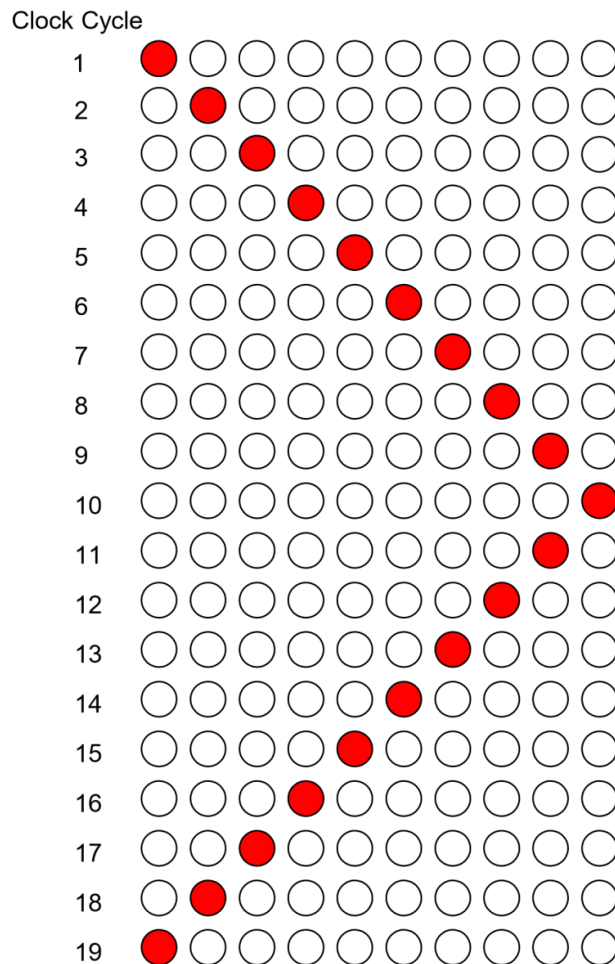
Next you need to make sure the pins are in the right place. Open up the **Pin Planner** as done in previous section. You can also click this icon  along the top of the Quartus window.

Check the pins and make sure the LEDs are assigned to the same locations as the first lab. Note that there is an additional pin name called `CLOCK_50` in this design that needs to be assigned. The clock should be connected to `PIN_AF14` (50 MHz). There should be no question marks in the port direction icon.

Hit compile after observing the pinout.

## 6.6 Downloading Your Code to Your Device

By now you should have the hang of how to program the FPGA image into the DE1-SoC development kit. Go ahead and try it out. Do you see the infamous Knight Rider pattern? When working properly, you should see something like the following:



*Figure 25: Example of Knight Rider sequence*

What do you see? **(If it does not work look at the next section.)**

## 6.7 More Debugging

You knew we weren't going to make it that easy, did you? How come the lights don't sequence? Here is a portion of the explanation. The selected clock frequency of the DE1-SoC Board is 50 MHz. That means the clock changes 50 million times per second. If you change the LEDs at that rate, you cannot view them with the naked eye.

When you go through the code you will see a module in your code called **clock\_divider**. You want the output clock to toggle at around 10 Hz (10x per second). This **clock\_divider** module takes the 50 MHz clock and divides down the clock to a slower frequency. Your lab instructor goofed and did not calculate the right divide ratio to slow the 50 MHz clock down to 10 Hz.

You need to do a bit of math (including the log function!) to determine how to derive the proper size of the counter to divide 50 MHz to roughly 10 Hz.

Basically, think about a divide ratio that is  $2^N$  where N is the width of the counter. Adjust the parameter to **COUNTER\_SIZE** to the appropriate ratio and recompile and reprogram the FPGA.

Work out N based on the following equation:  $10 = 50,000,000 / 2^N$ . Round N up to the nearest integer to discover the proper **WIDTH** parameter setting.

Recompile and program the DE-SoC development board.

### 6.8 Even More Debugging!

Is the Knight Rider sequence working properly? Does each LED stay on for about 1/10 second? If not, redo your math to find the right **WIDTH** parameter. Look at the sequencing carefully. Does each LED illuminate once and proceed to its neighboring LED? As you will observe **LED[0]** and **LED[9]** will blink twice.

Dang! That lab instructor created another error in the design! Look at the source code in the **knight\_rider.v** code and see if you can find the error.

Change the code, recompile and reprogram your DE0 development kit until your Knight Rider LEDs are sequencing properly.

Try viewing your knight rider hardware through the RTL Viewer (Register Transfer Level Viewer) like you did for the mux 2 to 1 design!

Note: The **COUNTER\_SIZE** looks good when set to 23 or 24.

### 6.9 Correcting the double blink problem



The simulation shown below in figure below illustrates the problem. Note how count increases past 9 to 10 and causes the erroneous double blink problem.

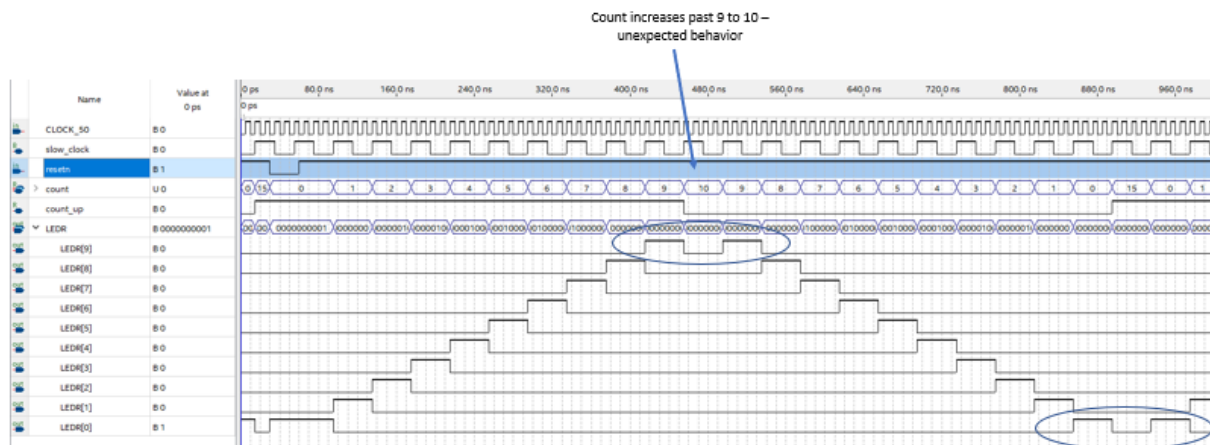


Figure 26: Incorrect sequencing waveform

Changing the count\_up trigger clock to the fast\_clock allows count\_up to change state at the appropriate time allowing proper behavior. Keep the trigger clock as slow\_clock and changing the limits between 9 and 0 to 8 and 1 also will correct the problem.

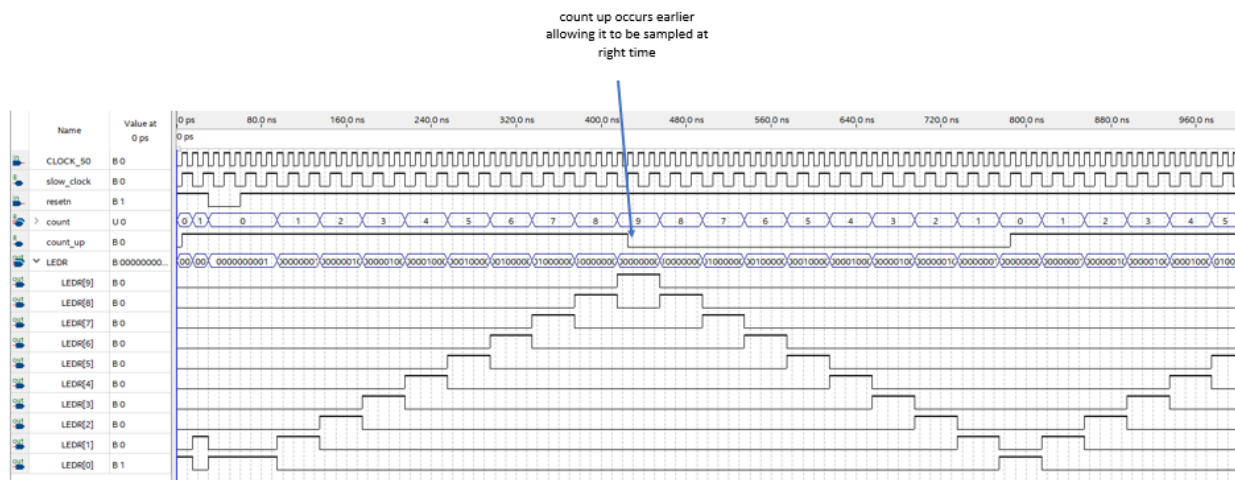


Figure 27: Corrected sequencing waveform

Thanks for taking time learning how to develop Intel FPGA products. We hope you found this lab informative.

**LINKS:**

1. <https://youtu.be/oNyXYPhnUIs?t=8s>
2. <https://youtu.be/PJQV1VHsFF8>

## Revision History

DATE	NAME	DESCRIPTION
03/21/2016	L. Landis	Initial Release
04/13/2016	L. Landis	Remove Modelsim from download package
05/24/2016	P. Mayer	Fixed broken links, updated for Quartus 16.0, added a few extra assignments
06/03/2016	L. Landis	Added solution to 2:1 Mux lab
06/07/2016	L. Landis	Added revision for copying pin assignments
07/20/2016	L. Landis	Clarify Mux_2_to_1 copy and paste code
10/03/2016	L. Landis	Clarify no driver image; typos
03/16/2017	A. Weinstein	Added USB Blaster driver installation instruction. Added table of figures and figure numbers. Made instructions clearer w.r.t. revision control and when writing Verilog code for labs. Added a solution for the 3-1 MUX lab.
10/10/2017	D. Henderson	General document formatting and clean up. Additionally, updated wiki links and some screen shots. Last, added TCL script instructions for assigning pins.
11/15/2017	D. Henderson	Cleaned up naming from previous port of the documentation
12/01/2017	S. Girisankar	Updated from 4-bit to 3-bit 2 to 1 Mux
01/04/2018	L. Landis	Changed TCL from file download to tcl console
04/10/2018	A. Joshipura	Changed from .pdf to .word format.
07/10/2018	S. Soto	General document formatting and clean up. Updated cross references. Created download links for all tcl scripts and Verilog code. Updated screenshots. Added Test Your Knowledge Lab. RTL Viewer of Mux 2-to-1 added.
07/24/2018	H. Martinez	Updated format to fit Intel Branding Guidelines. Changed formatting from Microsoft Word to L <sup>A</sup> T <sub>E</sub> X

08/08/2019	R. Nevin	Removed all references to Altera links and correct some trademark names
10/01/2019	S. Cabanday	Updated Verilog file names from upper-case to lower-case and screenshots to include new, all lower-cased file names
01/29/2020	S. Cabanday	Minor grammar revisions, updated screenshots, emphasis on case-sensitivity
3/17/2021	L. Landis	Modified for DE0 Cyclone III board
4/13/2021	L. Landis	Modified for DE1-SoC board and labsland
4/15/2021	L. Landis	Fix a few typos and errors.

Table 3: Revision Control History