

# TEACHING WITH INTEL® FPGAS

## TRAINING AID CATALOG



Intel Programmable Solutions Group

# Welcome to Intel Programmable Solutions Group Academic Program

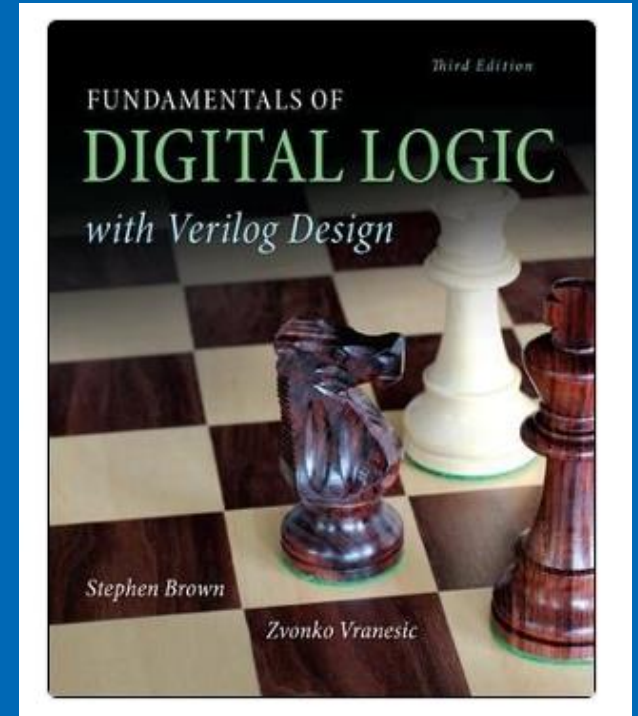
*Our Intel PSG Academic Program is here to support all aspects of Intel FPGA education utilizing our SW & HW tools. The next 40 slides will introduce you to:*

- 1) Program History
- 2) Undergraduate EE Coursework
- 3) Graduate EE Coursework
- 4) Dev Kits & HW available (donation & reduce price)
- 5) New Remote Learning Framework
- 6) FPGA Cloud – Free
- 7) Workshops / Training – Host a Workshop

Please visit our website: [Intel® FPGA Academic Program](#)

# 1) HISTORY OF INTEL® FPGA UNIVERSITY PROGRAM

- Program started @ Altera 2006
- Launched by Professor Stephen Brown from University of Toronto; Over 1800 university labs
- Developed coursework for Digital Logic, followed by Computer Organization and Embedded Systems
- Partner with Terasic Corporation to develop Altera based FPGA development kits for training and research
- Web page offers coursework and board and license purchase and donations



# INTEL® FPGA ACADEMIC ECOSYSTEM



- Train the next generation of FPGA Designers
- Increase Intel® FPGA presence in academia



- Academic access to the latest generation of Intel FPGAs



- Nurture the talent pipeline for Intel and our customers
- Engage research on Intel FPGAs

## 2) UNDERGRADUATE EE COURSEWORK





# ELECTRONICS COURSEWORK DELIVERY TECHNIQUES



1 week!



## Traditional:

- University: In-person semester long
- Industry: In-person workshops 1-8 hours
- Handout hardware per person or per group

## Online/Virtual for the CV19 world we live in:

- Instructor led: Zoom/GotoMeeting/Webex/Team/Google Hangout/Skype/Jupyter
- Recorded Lectures
- MooC (Massively Open Online Course): Coursera, Udemy, Khan Academy)
- Remote labs with no on-premise hardware

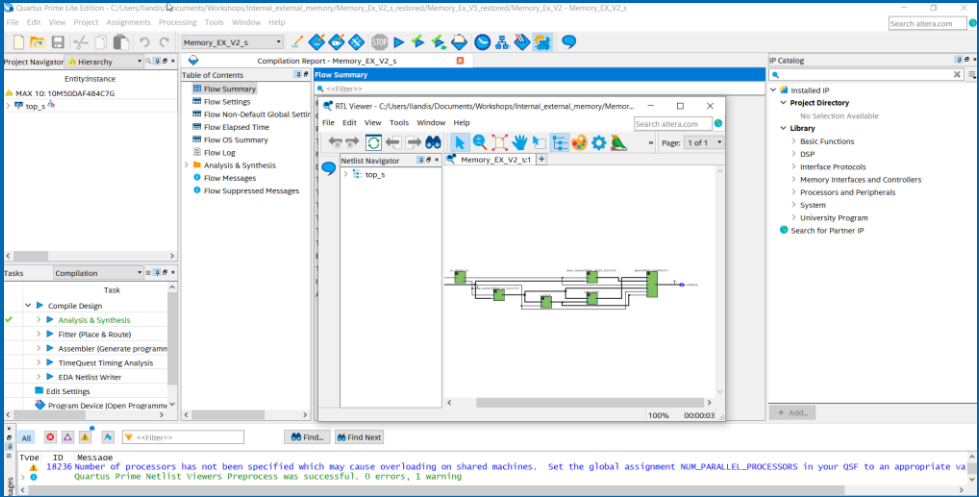
# INTEL® FPGA COURSEWORK OFFERINGS

## Undergraduate

- Digital Logic
- Digital Systems
- Computer Organization
- Embedded Systems



# INTEL® QUARTUS® DEVELOPMENT TOOL SUITE



Everything you need to develop Intel® FPGAs!

Free software for academia with Intel® MAX® 10 and Cyclone® V low cost FPGA families

Includes Modelsim\* Simulator from Mentor\*

Includes Eclipse\* IDE for use with NIOS® “Soft” Processor



Create Design

Constrain Design

Compile Design

Close Timing

Configure Design on Board



# TUTORIALS: HARDWARE DESIGN (STEP BY STEP HOW-TO)

LEARN THE BASICS OF INTEL® QUARTUS PRIME SOFTWARE AND HOW TO USE IT WITH THE TERASIC DE-SERIES DEVELOPMENT KITS

<b>Get Started with the Terasic DE-Series Boards</b>	<a href="#">Verilog &amp; VHDL PDF</a>
<b>Introduction to Intel® Quartus® Prime Pro Edition Software</b>	<a href="#">Verilog PDF</a> <a href="#">VHDL PDF</a>
<b>Introduction to Intel® Quartus® Prime Software (standard or lite)</b>	<a href="#">Verilog PDF</a> <a href="#">VHDL PDF</a>
<b>Use Schematic Designs in Intel® Quartus® Software</b>	<a href="#">Verilog PDF</a> <a href="#">VHDL PDF</a>
<b>Use the Library of Parameterized Modules (LPM)</b>	<a href="#">Verilog PDF</a> <a href="#">VHDL PDF</a>

# TUTORIALS

## TIMING, SIMULATION AND DEBUGGING

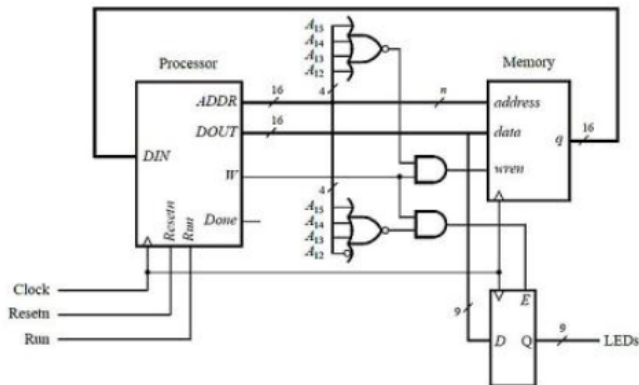
<b>Timing Analyzer in Intel® Quartus® Prime Software</b>	<a href="#">Verilog PDF</a> <a href="#">VHDL PDF</a>	<a href="#">Verilog Design Files</a> <a href="#">VHDL Design Files</a>
<b>Use ModelSim* with Testbenches</b>	<a href="#">Verilog PDF</a> <a href="#">VHDL PDF</a>	<a href="#">Verilog Design Files</a> <a href="#">VHDL Design Files</a>
<b>Use ModelSim* by Drawing Waveforms</b>	<a href="#">Verilog PDF</a>	<a href="#">VHDL PDF</a>
<b>Signal Tap II Logic Analyzer</b>	<a href="#">Verilog PDF</a>	<a href="#">VHDL PDF</a>
<b>Debug Hardware Designs</b>	<a href="#">Verilog PDF</a>	<a href="#">VHDL PDF</a>

# TUTORIALS: SYSTEM DESIGN

Tutorials	Downloads
Introduction to the Platform Designer System Integration Tool	<a href="#">PDF</a>
Make Platform Designer Components	<a href="#">PDF</a>
Introduction to the Arm* Processor	<a href="#">Arm* Toolchain PDF</a> <a href="#">Toolchain from Intel® PDF</a>
Introduction to the Nios® II Processor	<a href="#">PDF</a>
Debug Application Programs	<a href="#">PDF</a>
Use the Arm Generic Interrupt Controller	<a href="#">PDF</a>
Monitor Program Tutorial for the Arm Processor	<a href="#">PDF</a>
Monitor Program Tutorial for the Nios II Processor	<a href="#">PDF</a>
Hardware Abstraction Layer (HAL) Device Drivers with the Monitor Program	<a href="#">PDF</a>
Terminals with Terasic DE-Series Boards	<a href="#">PDF</a>

# DIGITAL LOGIC/SYSTEMS – 12 LABS

1. Switches, Lights and Multiplexers
2. Numbers and Displays
3. Latches, Flip-Flops and Registers
4. Counters
5. Timers and Real Time Clock
6. Adders, Subtractors and Multipliers
7. Finite State Machines
8. Memory Blocks
9. A Simple Processor
10. An Enhanced Processor
11. Implement Algorithms in Hardware
12. Basic Digital Signal Processing



## Lab 10: An Enhanced Processor

Implement an enhanced processor using the skills learned from Lab 9.

- Add functionality so that your processor can perform read and write operations using memory or other devices.
- Create an output module for your processor to drive seven-segment displays.
- Connect an input module for your processor to read and store the state of switches on the board.

[Download Verilog](#)[Download VHDL](#)



# COMPUTER ORGANIZATION – 8 LABS: ARM® OR NIOS®

1. Use a Hard or Soft Processor System on Intel® FPGAs
2. Logic Instructions
3. Subroutines and Stacks
4. Input and Output in an Embedded System
5. Use Interrupts with Assembly Code
6. Use C Code with an Intel FPGA Processor
7. Use Interrupts with C Code
8. Introduction to Graphics and Animation

Address	31	30	...	4	3	2	1	0	
0xFF200050	Unused						KEY <sub>1-0</sub>		Data register
Unused	Unused								
0xFF200058	Unused						Mask bits		Interruptmask register
0xFF20005C	Unused						Edge bits		Edgecapture register

**Lab 4: Input and Output in an Embedded System**

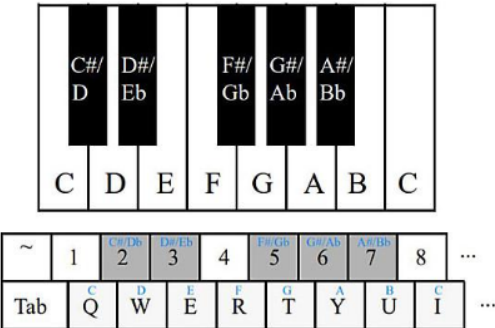
Investigate the use of devices that provide input and output capabilities for a processor.

- Program a two-digit decimal counter on the seven-segment display.
- Implement polling to stop and start the counter when any push-button key is pressed.
- Add a hardware timer to the program.

[Download \(Arm\)](#)[Download \(Nios II\)](#)

# EMBEDDED SYSTEMS – 8 LABS: ARM® A9 SOC FPGA RUNNING LINUX

1. Get Started with Linux\*
2. Develop Linux Programs that Communicate with FPGAs
3. Character Device Drivers
4. Using Character Device Drivers
5. Use ASCII Graphics for Animation
6. Introduction to Graphics and Animation
7. Use the ADXL345 Accelerometer
8. Introduction to Audio and Multithreaded Applications



The diagram shows a piano keyboard layout with notes C, D, E, F, G, A, B, C. Above the notes are sharps and flats: C# (D), D# (Eb), F# (Gb), G# (Ab), A# (Bb). Below the notes is a MIDI controller layout with buttons labeled 1 through 8, and a 'Tab' button. The buttons are color-coded: 1 (blue), 2 (green), 3 (yellow), 4 (orange), 5 (red), 6 (purple), 7 (pink), 8 (light blue). The MIDI controller layout also includes a 'Tab' button and a 'C' button.

**Lab 8: Introduction to Audio and Multithreaded Applications**

Create user-level Linux programs that produce audio output on the Terasic DE1-SoC board.

- Write a multithreaded program to implement a digital piano using an audio port.
- Visualize sound as wave forms on a VGA display.
- Record and play back songs.

[Download](#)

# REFERENCE DESIGN REPOSITORY

- Intel FPGA “Design Store” catalogs reference designs by product family, development kit, tool release and function
- Great starting point for student projects

The screenshot shows the Intel Design Store website. The top navigation bar includes links for PRODUCTS, SUPPORT, SOLUTIONS, DEVELOPERS, and PARTNERS. The user is logged in as 'llandis'. The main content area is titled 'Design Store' and shows 'Design Examples' as the active tab. A search bar is present in the top right corner. Below the navigation, there are filters for Family (MAX 10), Category (Any), Quartus Prime Version (Any), Development Kit (MAX 10 DE10 - Lite), and IP Core (Any). A table of design examples is displayed below the filters.

Name	Category	Development Kit	Family	Quartus Prime Version	Vendor
Adapting Digilent PmodCLP LCD Display to DE10 Lite Development Kit Arduino Shield Header	Design Example	MAX 10 DE10 - Lite	MAX 10	16.0.0	Intel
Adapting Digilent PmodCLP LCD Display to DE10 Lite Development Kit Arduino Shield Header	Design Example	MAX 10 DE10 - Lite	MAX 10	16.1.0	Intel
ADC RTL - MAX10 DE10 Lite	Design Example	MAX 10 DE10 - Lite	MAX 10	15.1.0	Intel
Baseline Pinout - MAX10 DE10 Lite	Design Example	MAX 10 DE10 - Lite	MAX 10	16.1.0	Intel

# HOW-TO VIDEOS

- Engineer to Engineer youtube video repository – short 3 to 5 minute videos on 100's of topics

The screenshot displays the Intel FPGA YouTube channel interface. At the top, the channel name 'Intel FPGA' is shown with 29.6K subscribers. Navigation tabs include HOME, VIDEOS, PLAYLISTS (selected), COMMUNITY, CHANNELS, and ABOUT. A search icon is also present. Below the navigation, a dropdown menu shows 'Engineer to Engineer: How-to and Training Videos'. The main content area features several video playlists, each with a thumbnail, title, video count, and a 'VIEW FULL PLAYLIST' link. The playlists are: High Level Design (45 videos), Acceleration (11 videos), Configuration (47 videos), Enpirion Power (7 videos), FPGA Design (180 videos), Embedded (69 videos), Interfaces (120 videos), and Intel FPGA Technical Training (156 videos).

Playlist Name	Video Count	Channel	Action
High Level Design	45	Intel FPGA	<a href="#">VIEW FULL PLAYLIST</a>
Acceleration	11	Intel FPGA	<a href="#">VIEW FULL PLAYLIST</a>
Configuration	47	Intel FPGA	<a href="#">VIEW FULL PLAYLIST</a>
Enpirion Power	7	Intel FPGA	<a href="#">VIEW FULL PLAYLIST</a>
FPGA Design	180	Intel FPGA	<a href="#">VIEW FULL PLAYLIST</a>
Embedded	69	Intel FPGA	<a href="#">VIEW FULL PLAYLIST</a>
Interfaces	120	Intel FPGA	<a href="#">VIEW FULL PLAYLIST</a>
Intel FPGA Technical Training	156	Intel FPGA	<a href="#">VIEW FULL PLAYLIST</a>



- Post your questions and answers – moderated by Intel FPGA experts

The screenshot displays the Intel FPGA University Program forum interface. At the top, there's a navigation bar with links for PRODUCTS, SUPPORT, SOLUTIONS, DEVELOPERS, and PARTNERS. Below this, a 'Community' section features the 'Intel® FPGA University Program' title and a search bar. The main content area is titled 'University Program Material, Education Boards, and Laboratory Exercises'. It contains a 'Discussions' section with a 'Post a question' button and a list of four discussion threads. Each thread shows the topic, author, date, and number of replies. To the right, there's an 'Announcements' section with support hours and a link to FPGA Knowledge Articles, and a 'Latest articles' section which currently shows 'No posts to display'.

Intel Community / FPGAs and Programmable Solutions / Intel® FPGA University Program

Option ▾

### University Program Material, Education Boards, and Laboratory Exercises

Discussions

Post a question

**What are the scripting languages needed for chip design engineer**  
 by Ashokraj on 07-16-2021 12:55 AM Latest post on 07-20-2021 06:13 PM by NurinaW

0 3 ✓

**nCONFIG pin abnormal**  
 by rMa1 on 06-09-2021 10:46 PM Latest post on 07-02-2021 03:45 AM by NurAiman\_M\_Intel

0 2

**WORKING: DE2-115 Simple Socket Server**  
 by Altera\_Forum on 04-04-2011 10:01 AM Latest post on 06-25-2021 12:09 PM by Apar

0 66

**Failed to initialize user clock?**  
 by davidwigley on 06-11-2021 08:48 AM Latest post on

0 6 ✓

Announcements

Intel Support hours are Monday-Fridays, 8am-5pm PST, except Holidays. Thanks to our community members who provide support during our down time or before we get to your questions. We appreciate you!

Need Forum Guidance? [Click here](#)  
 Search our FPGA Knowledge Articles [here](#).

Latest articles

No posts to display.

# TERASIC: FPGA DEVELOPMENT KIT

## PARTNER FOR INTEL®

1. Over 100,000 boards sold!
2. Special low cost academic pricing, free donations for professors
3. Many LED, switches and IO connectivity – perfect for learning hardware and embedded systems
4. FPGA only or FPGA with Arm\* A9 SoC HPS (Hard Processor Subsystem)
5. Board selector (add link here)

\$64



Terasic DE10-Lite Board with Intel® MAX® 10 FPGA

\$146



Terasic DE10-Nano Development Kit with Cyclone® V SoC FPGA

\$220



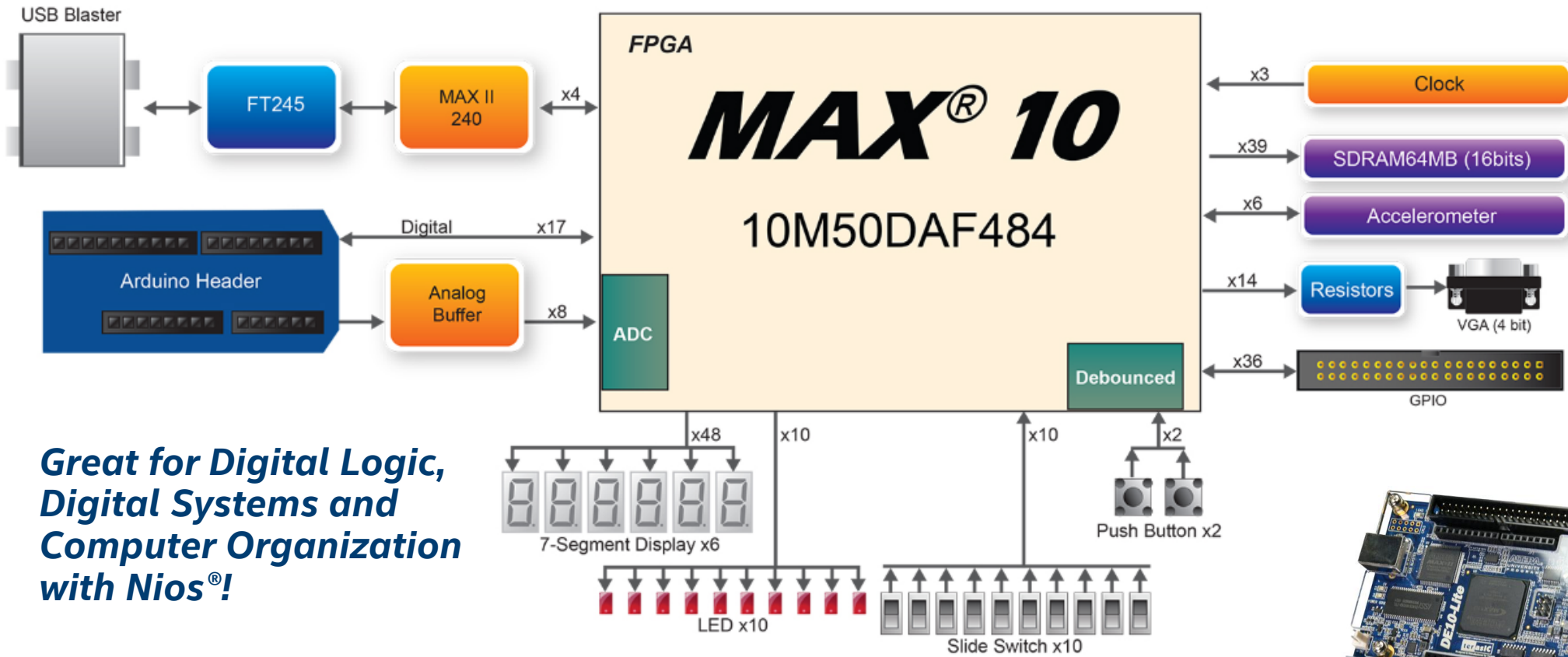
Terasic DE1-SoC Development Kit with Cyclone® V SoC FPGA

\$292

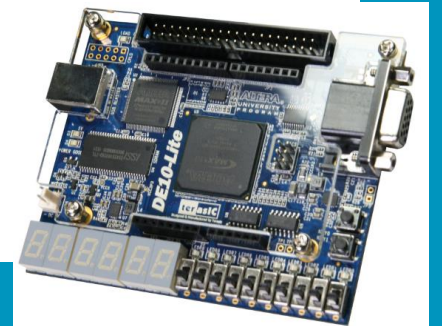


Terasic DE10-Standard Development Kit with Cyclone® V SoC FPGA

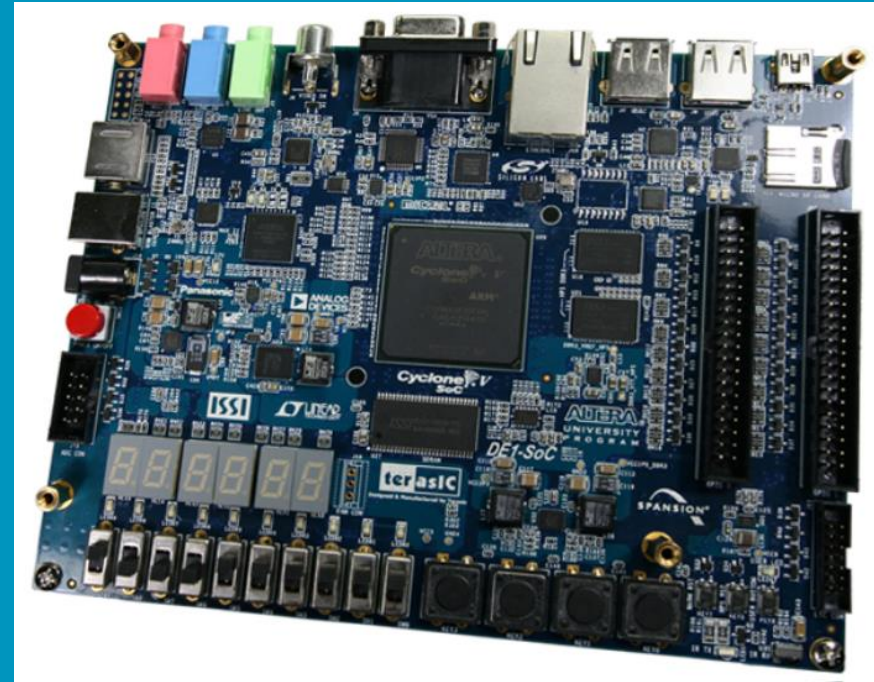
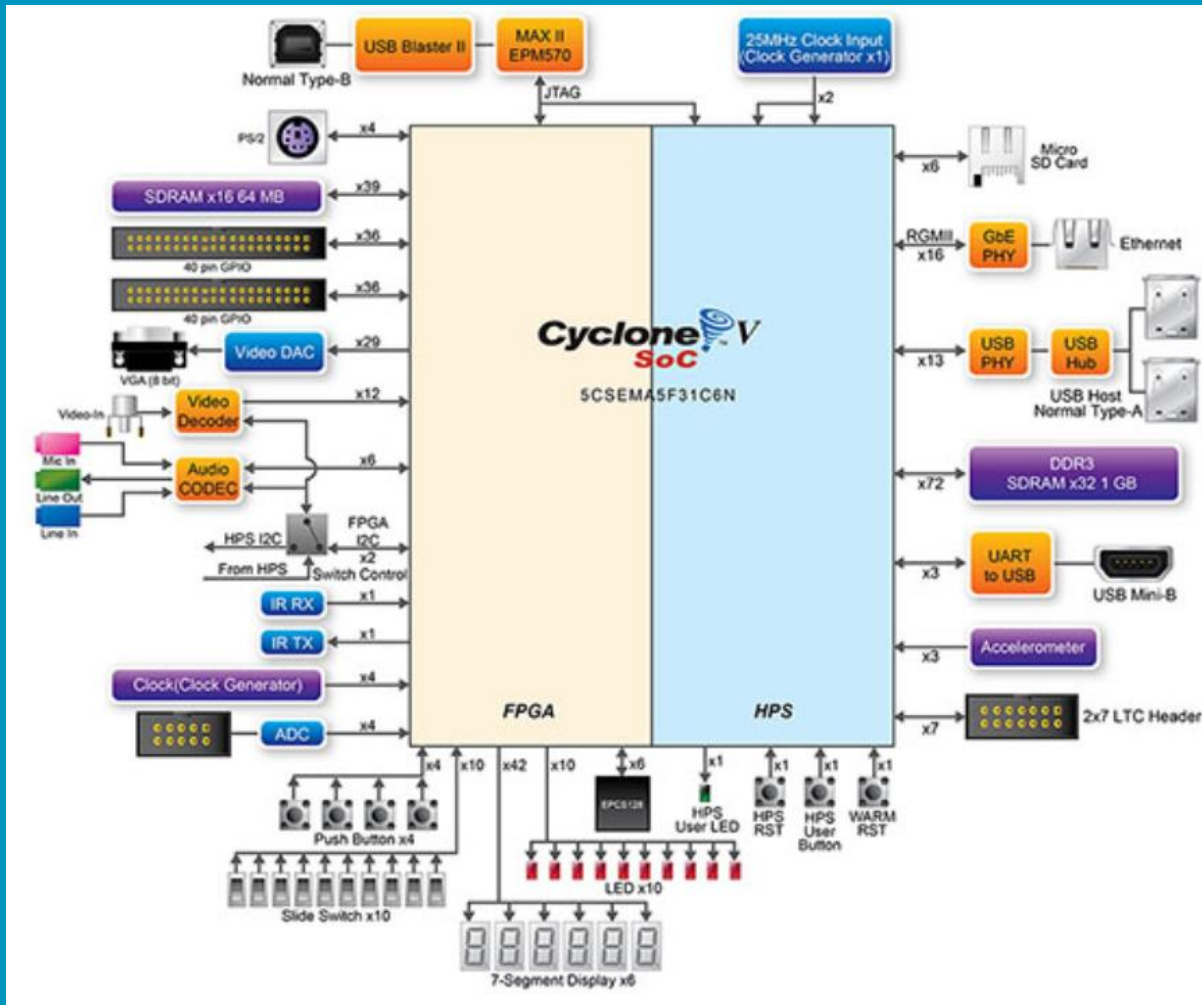
# DE10-LITE: \$64 USD



*Great for Digital Logic,  
Digital Systems and  
Computer Organization  
with Nios<sup>®</sup>!*



# DE1-SOC: \$220 USD



*Great for Embedded Systems with Arm\* A9 CPU*

*Includes Video, Audio, Ethernet and full Linux Support!*



# TERASIC: ROBOTIC KIT – SELF BALANCING ROBOT

\$305

Great kit to learn about embedded design, motor control and IO expansion with Intel® FPGA!

Perfect for senior projects – add Bluetooth, Wi-Fi, audio commands, etc.



# HANDS-FREE LABS INITIATIVE

- Provide a series of documentation, IP to facilitate hands free operation for as many features as possible for Intel® and Terasic FPGA development kits – change switches view LEDs fully virtualized
- Make adaption of existing in-person lab material easy for prof/TA to adapt to remote learning
- Host boards and compute on existing university premise
- Support common OS : Windows\*, Mac\*, Linux
- Opensource through [github](#) site

[Hardware based solution video](#)

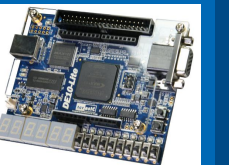
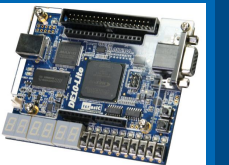
[Simulator based solution video](#)

Linux or Windows\*

Server



USB



**Method 1: Intel Quartus® Prime Software Hosted on Student's PC**

**Method 2: Intel Quartus® Prime Software Hosted on Server**

- Does not require 1 Devkit per Server – use USB port replicator
- Install setup at university engineering department cluster
- Host on Windows or Linux server running Intel Quartus Prime Programmer



Intel provides [guide](#) on how to setup and access remote board

# LABSLAND

- Labsland is a company with an installation of remotely hosted labs using video cameras on a variety of scientific topics, including Intel FPGAs
- Their business model is to utilize learning institutions to host the remote labs, and labsland collects a per student fee to access the remote learning setup.
- Host sites get free access to the remote labs. Please visit the [labsland.com](https://labsland.com) site for demonstrations of their remote FPGA board solution



**ELECTRICAL & COMPUTER  
ENGINEERING**  
UNIVERSITY of WASHINGTON



This FPGA is hosted at University of Washington.

01:31

Leave now

**Altera FPGA Laboratory**



98765

43210

KEY3KEY2KEY1KEY0



# INTEL® FPGA WORKSHOPS

1-4 hour hands-on workshops conducted by Intel® FPGA experts – material also available for professors to use in coursework. Available in person or virtual.  
Request here: [fpgauniversity@intel.com](mailto:fpgauniversity@intel.com)

1. Introduction to FPGA Design in Intel® Quartus® Prime Software
2. Embedded FPGA Design Using the Nios® II Processor
3. Introduction to Static Timing Analysis of Digital Circuits
4. Introduction to FPGA Simulation and Debug
5. Introduction to High-Speed I/O
6. Introduction to Video
7. Introduction to Memory
8. Introduction to High-Level Design
9. Introduction to FPGA Acceleration
10. How to Get Hired in Tech, An Insider's View
11. Semiconductor Industry Overview



# INTEL® FPGA TRAINING – *FREE FOR EDUCATORS!*



Hide Filter

Search

Course Type:  Language:  Price:  DeviceFamily:  Curriculum:

Share Result

Report  
Showing 1 - 8 / 8 Entries (Filtered From 399 total Entries)

Course Name	Type	Price	Language	Curriculum	Registration
Become an FPGA Designer in 4 Hours (ODSWBECOME) 4 Hours	Online	Free	English	FPGA Designers - Level 200	Register Now
Using the Nios® II Processor: Hardware Development (ONIIHW) 27 Minutes	Online	Free	English	FPGA Designers - Level 300	Register Now
Using the Nios II Processor: Software Development (ONIIISW) 10 Minutes	Online	Free	English	Embedded Hardware	Register Now
Using the MAX 10 User Flash Memory (OMAXUFM) 26 Minutes	Online	Free	English	Advanced Hardware	Register Now

1. 100s of courses: Self-directed, Virtual Teach and In-Person
2. Free for professors!
3. Every topic possible on FPGAs

# ACCESS TO COURSEWORK, LICENSES AND BOARDS

Signup for Intel® FPGA University Program

Gain access to coursework and solutions

Request board purchases and donations

Hardware Donations and Discount Purchases



Free Software and Intel® FPGA IP Licenses



Solutions and Source Files



# LICENSES, BOARD PURCHASE AND DONATIONS

## Hardware Donations and Discount Purchases

Submit your proposal to obtain free hardware for use in teaching or academic research.

[Recommended Teaching Hardware](#)

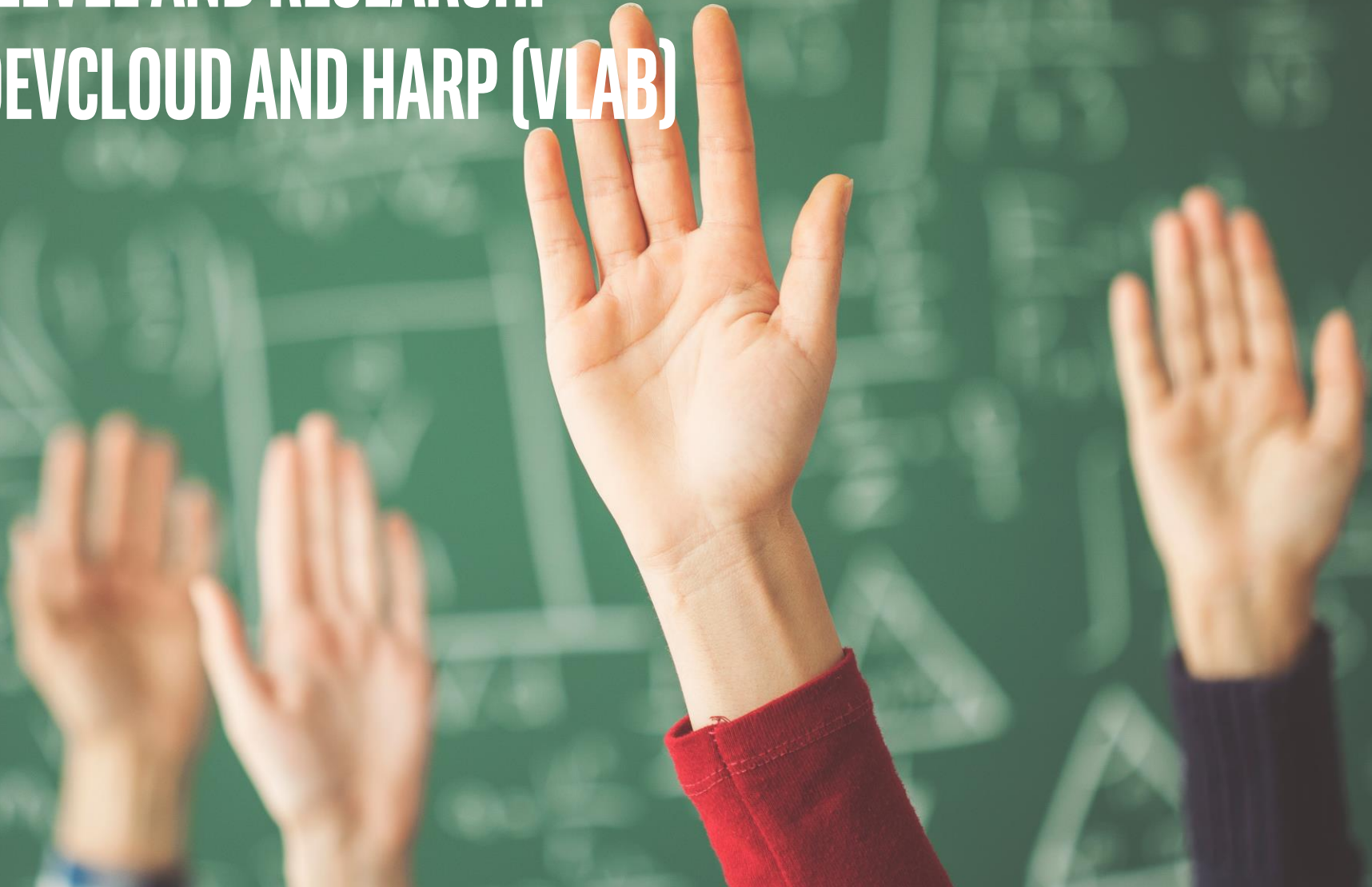
[Recommended Research Hardware](#)

[View All Intel FPGAs](#)

**Note** Hardware donations are limited and considered on a case-by-case basis. Discounted hardware options are available for students who are required to purchase their own hardware. Select this option when submitting your request.

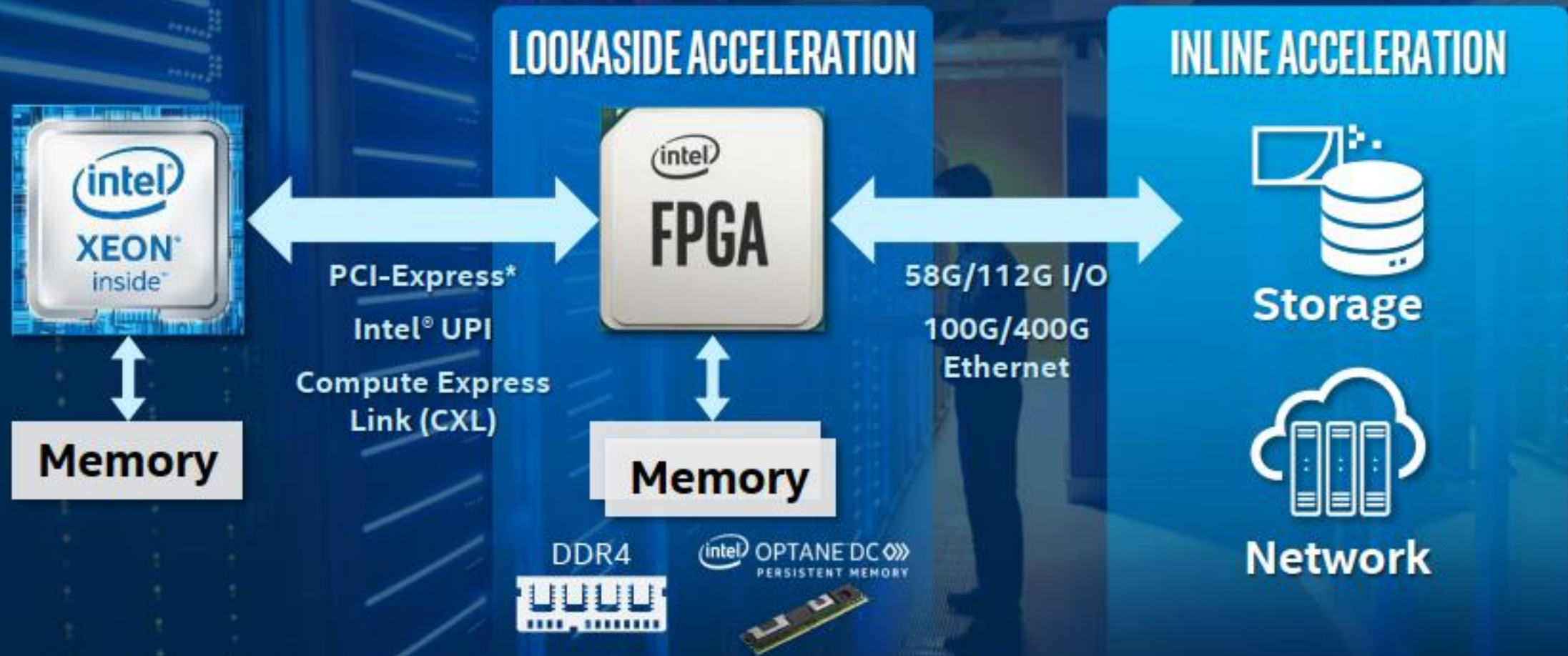
[Request Hardware](#)

### 3) GRADUATE LEVEL AND RESEARCH: INTEL® FPGA DEVCLOUD AND HARP (VLAB)





# INTEL® FPGAS ACCELERATING THE CLOUD & ENTERPRISE





# INTEL® FPGA UNIVERSITY GRADUATE LEVEL COURSEWORK

Graduate level FPGA coursework focuses on AI, Machine Learning, Heterogeneous Computing using C++ extension languages: HLS, OpenCL\*, DPC++

Many of these courses use high end FPGAs > \$1000 Boards

Complex PCIe\* plug-in cards with extensive software and drivers

Intel makes it easier by enabling access to our FPGA “Devcloud” or HARP free to academia

# INTEL FPGA RESEARCH

## Academics

**Intel academic research programs**  
(e.g., ISRAs, single PIs)

**Research programs Intel involved in**  
(e.g., SRC JUMP)

**Internship program**

**Access to FPGA technologies**  
(e.g., HARP, DevCloud)

## Internal Research

(PSG CTO, Intel Labs)

**DL workloads**

**Eval current FPGAs**

**Next-gen FPGAs**

**FPGA programmability**

**FPGAs in system**

...

## Broader Intel

**Engineering**  
(architecture, platform, tools, etc)

**Product planning**

**Marketing**

...

Transfers of innovations and technology

# INTEL® FPGA ACADEMIC CLOUDS

Cloud access to Intel servers with FPGAs for academics

*FPGAs/SW tools already installed. Just login remotely. Ready to use!*

## HARP (aka vlab) for Long-term Research

Hardware accelerator research program (HARP), originally offered cloud access to integrated (MCP) Intel® Xeon® + FPGA

Now expanded to offer servers with FPGAs cards in Intel® Labs Academic Compute Env.

Exclusively for long-term academic research (e.g., 1+ year PhD research)

## DevClouds for Teaching and Beyond

Offers servers with FPGA cards

Suitable for teaching (e.g., lab projects) and short-term research efforts. Move to HARP when research grows

And for short-term development projects in general (academic and industry)

# WHAT'S AVAILABLE TODAY

FPGA flows/framework	Devcloud	HARP
Traditional RTL flow	Y	Y
HLS Compiler	Y	Y
FPGA SDK for OpenCL*	Y	Y
DPC++ (part of oneAPI)	Y	Upon Request
OpenVINO* (AI framework)	Y	Upon Request

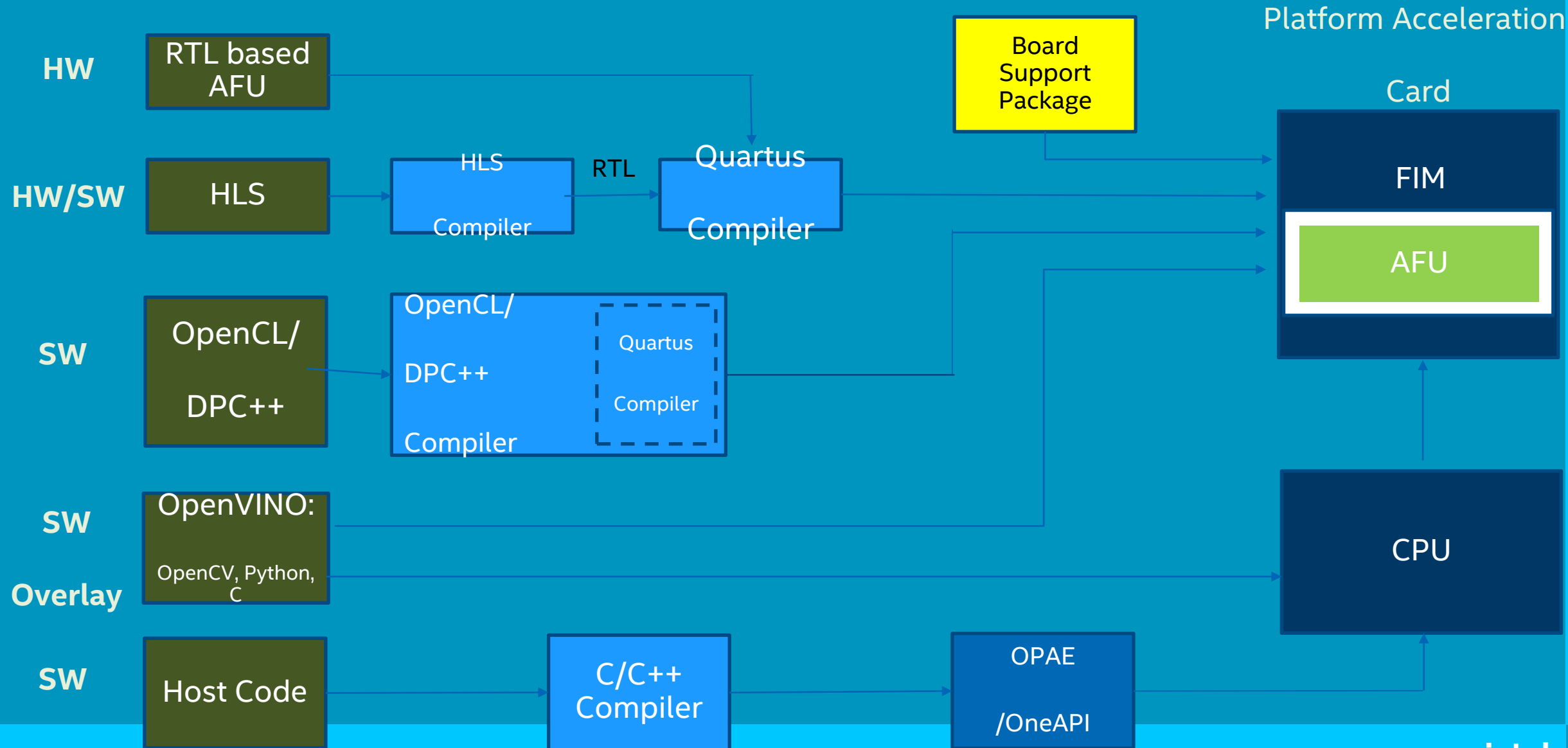
## FPGA Hardware

- Intel® Xeon® with Intel® Arria® 10 Programmable Acceleration Cards (PAC)
- Intel® Xeon with Intel® Stratix® 10 Programmable Acceleration Cards (PAC)
- Integrated Intel® Xeon + FPGA systems (HARP only)

Target

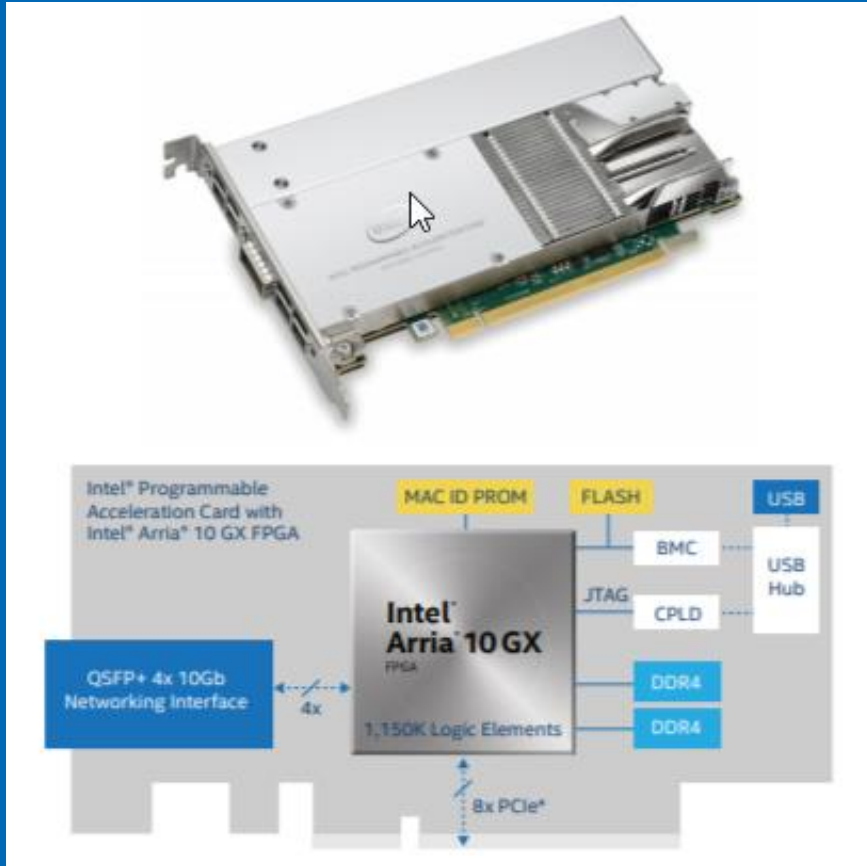
# WORKING IN THE FPGA CLOUDS

Developer





# ARRIA® 10 GX FPGA PROGRAMMABLE ACCELERATION CARD (PAC)



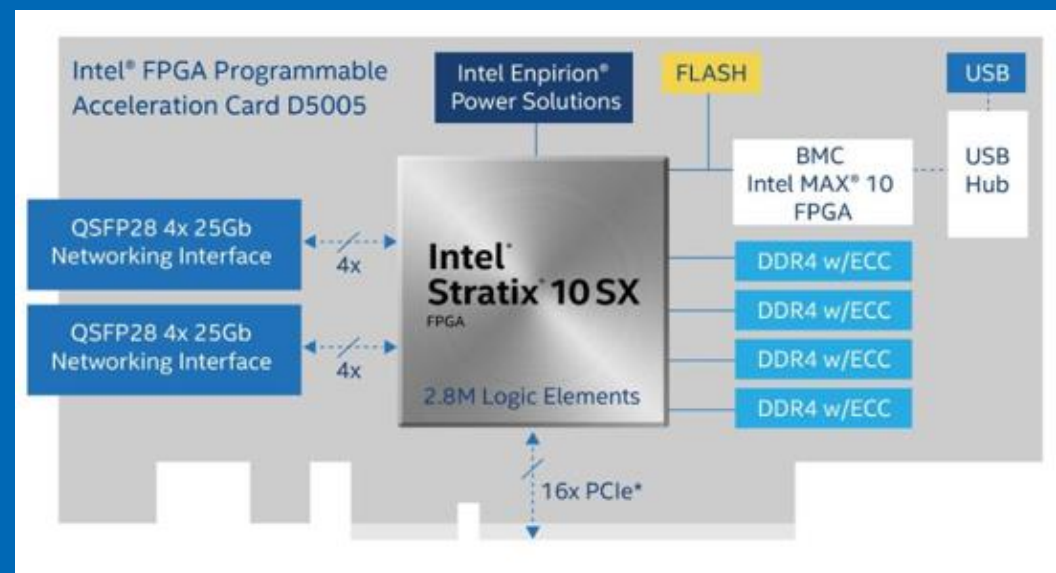
## Key Components and Interfaces

- Intel® Arria® 10 GX 20nm FPGA -1.15M LUTs
- 8 GB DDR4 memory banks (2 banks)
- 128 MB flash
- Quad small form factor pluggable (QSFP) interface speeds up to 40G
- PCI Express® (PCIe®) x8 Gen3 interface form factor
- Half-length card with standard (full height) and low profile (1/2 height) bracket options

# INTEL® STRATIX® 10 D5005 PAC


## Key Components and Interfaces

- Intel® Stratix 10 SX 14nm FPGA – 2.8M LUTs
- 32 GB DDR4 memory banks with error correction code (ECC) (4 banks, 2,400 Mbps)
- x2 quad small form factor pluggable (QSFP) with interface speeds up to 100G
- PCIe Gen3 x16 interface



# Website Access for the Intel® FPGA Devcloud

<https://software.intel.com/en-us/devcloud/FPGA>



The screenshot shows the Intel FPGA Devcloud website. At the top, there is a blue header with a hamburger menu icon and the text "Development Tools" on the left, and the Intel logo on the right. Below the header is a dark blue banner with the text "FPGA Design Development and Workloads for Hardware Acceleration" in white. Underneath this banner is a smaller blue box containing the text "Develop programmable solutions and validate your workloads on leading FPGA hardware with tools optimized for Intel® technology. Use this cloud solution in the classroom to support acceleration engineering curriculum." and a white button with the text "Sign Up →". Below the banner is a white section with the text "Overview | Intel® DevCloud for oneAPI | Edge" in the center. Further down is another white section with the text "What You Can Do" in the center. At the bottom of this section are three icons and their corresponding descriptions: a gear and chip icon for "Develop custom hardware IP and FPGA designs", a book and chip icon for "Teach advanced FPGA-based university courses", and a bar chart and chip icon for "Benchmark hardware acceleration performance".

Development Tools

intel


## FPGA Design Development and Workloads for Hardware Acceleration

Develop programmable solutions and validate your workloads on leading FPGA hardware with tools optimized for Intel® technology. Use this cloud solution in the classroom to support acceleration engineering curriculum.

Sign Up →

Overview | Intel® DevCloud for oneAPI | Edge

### What You Can Do

-  Develop custom hardware IP and FPGA designs
-  Teach advanced FPGA-based university courses
-  Benchmark hardware acceleration performance

# HARP: GETTING ACCESS

## To get access

- Send email to: IL\_Academic\_Res\_Env@intel.com
- Put email subject “[HARP] new account request”.
- Include a short (1 page max) research proposal
- Include the type of workloads you are planning to run

## More details

The following website offers information of available FPGA systems in HARP. It also provides detailed tutorials and examples on how to get started.

<https://wiki.intel-research.net/FPGA.html>

# TYPICAL EE/ECE CURRICULUM TIMELINE

Year	Grade Level	Fall Semester	Spring Semester
1	Freshman		
2	Sophomore		Digital Logic
3	Junior	Digital Systems	Computer Organization
4	Senior	Embedded Systems	Senior Project
5-6	Graduate Level	Heterogeneous Computing	



# Discussion Forums and Project Ideas

Contact Intel: [fpgauniversity@intel.com](mailto:fpgauniversity@intel.com)

Contact Terasic: [support@terasic.com](mailto:support@terasic.com)

[Intel FPGA University Forum \(FPGA Support\)](#)

[Intel FPGA reference design repository](#)

[Intel Developer Zone \(reference designs\)](#)

[Opencores.org \(repository of IP functions\)](#)

[Fun FPGA projects: fpga4fun](#)

[Digital logic university training: nandland](#)

Need ideas for capstones and senior designs? Contact us @ [fpgauniversity@intel.com](mailto:fpgauniversity@intel.com)

# SUMMARY

**Learning hasn't stopped and can't be stopped due to Covid-19**

**The Intel FPGA group is here to help!**

**Contact us: [fpgauniversity@intel.com](mailto:fpgauniversity@intel.com)**

# Legal Disclaimers/Acknowledgements

- Intel technologies may require enabled hardware, software or service activation
- No product or component can be absolutely secure
- Your costs and results may vary
- Intel, the Intel logo, and other Intel marks are trademarks of Intel Corporation or its subsidiaries. Other names and brands may be claimed as the property of others
- OpenCL and the OpenCL logo are trademarks of Apple Inc. used by permission by Khronos
- \*Other names and brands may be claimed as the property of others
- This document is intended for personal use only.
- Unauthorized distribution, modification, public performance, public display, or copying of this material via any medium is strictly prohibited.

