



# TEST YOUR KNOWLEDGE - CALCULATOR

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## 1.0 Introduction

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**This is a short lab to test your knowledge in assembling a small FPGA project on the DE10-Lite development kit. The circuit adds the values of two counters (0-98) that are enabled with push button switches. The two addends and the sum are displayed on the seven segment displays. Since the sum can overflow to a 3<sup>rd</sup> hundreds place digit and there are only 6 seven segment displays, the hundreds position should be represented by lighting up all 10 LEDs simultaneously.**

### 1.1 Prerequisites

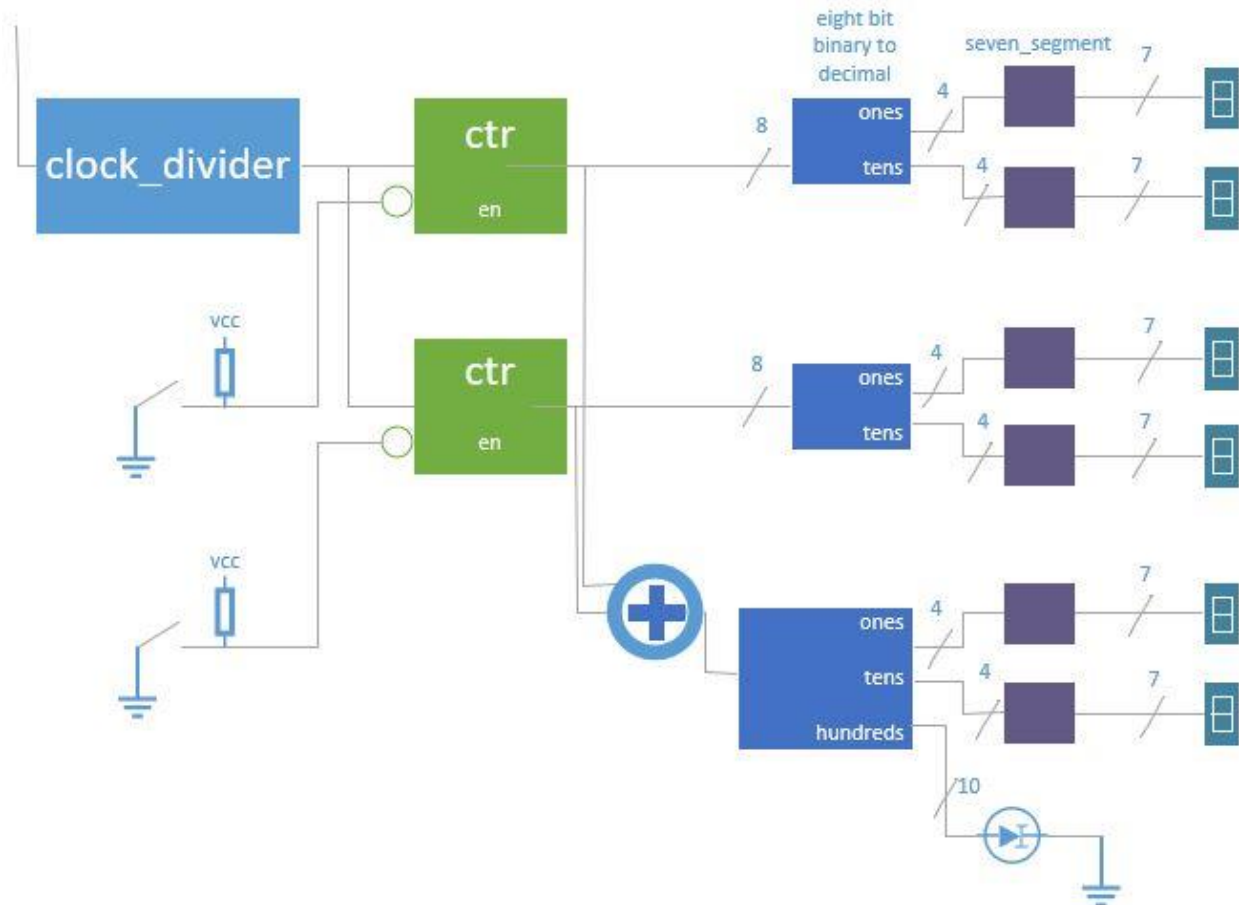
- Introduction to Intel FPGAs and Quartus Software course
  - Link to self-guided course: [OUWINTRO](#)
- Basic knowledge of Verilog and digital design

### 1.2 Reference Documents

**Table 1-1. Reference Documents**

Document	Document No./Location
QAR file for calculator	<a href="#">addit.qar</a>

## 2.0 Top Level Schematic



1. Create top module based on provided wrapper. This requires editing the Verilog file and wiring up the blocks.
2. Compile and program on board
3. Change ctr to count to 99
4. Now make the hundreds position light up 10 LEDs. Add LEDs to top level and check pin assignments
5. Bonus section (Go for it!) : Make ctr count up or down, by controlling its direction with switch 0.

## 3.0 Modules Provided

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### 3.1 Ctr 0-98 \*change to 0-99 (built from IP catalog)

Note that the counter is a parametrized IP. To edit the counter: Project Navigator Change to IP Components. Right click on LPM COUNTER and change to include updown input port. You will need to add the updown port to the top level and connect to appropriate SW[0] signal which is preassigned in the assignment editor.

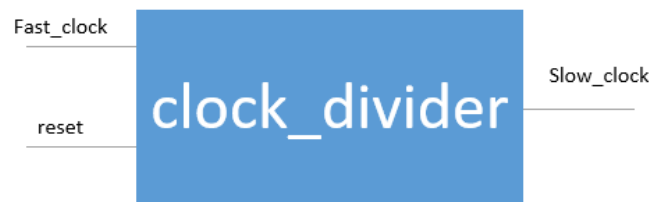
- Input a\_clr
- Input cnt\_en
- Input clk
- Output q



Counter counts up while cnt\_en is active at the rising edge of clk. A\_clr is used to reset the count which is output by q.

### 3.2 Clock divider 50 MHz to 2 MHz

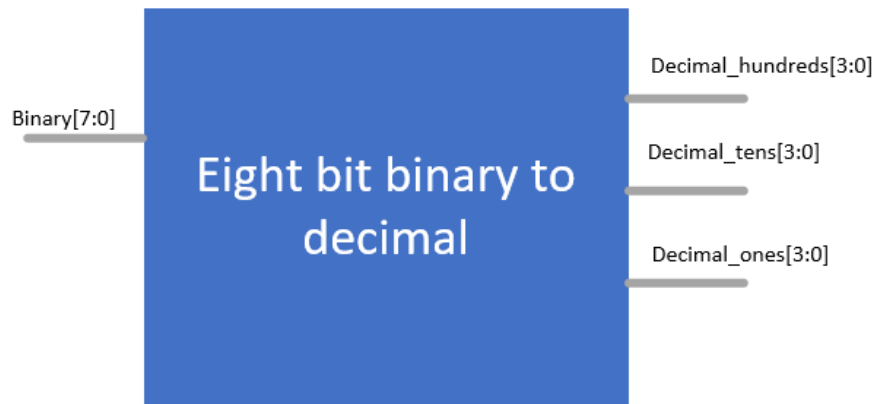
- Input fast\_clock
- Input reset
- Output slow\_clock



The clock divider takes the 50 MHz clock generated by the FPGA and outputs a slower clock signal which has a frequency dependent on the value of the size of the internal counter.

### 3.3 Eight bit binary to decimal

- Input [7:0] binary
- Output [3:0] decimal\_hundreds
- Output [3:0] decimal\_tens
- Output [3:0] decimal\_ones



Converts the binary output of the counter into values that represent ones, tens, and hundreds places in the decimal system.

### 3.4 Seven segment

- Input [3:0] led\_bcd
- Output reg [6:0] led\_out



Converts the value 0-9 from binary coded decimal to the decoded value needed to properly light up the 7-segment LED.

## **4.0 Document Revisions**

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Date	Author	Comments
6/25/2021	RK	Transferred TYK1 guide to common Word template and included diagrams for modules provided.