Intel FPGA Cloud Services

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- Larry Landis – University Outreach Senior Manager, Intel Programmable Solutions Group
- 31 years in semiconductor industry – design, sales, marketing, training for ASIC, FPGA
- Adjunct Lecturer for Digital Electronics Course – Santa Clara University

CSUN
CALIFORNIA STATE UNIVERSITY NORTHRIDGE

BSEE

LMU | LA
Loyola Marymount University

MSEE

SANTA CLARA BRONCOS

Adjunct Lecturer

Intel® FPGA Academic Ecosystem

- Train the next generation of FPGA Designers
- Increase Intel® FPGA presence in academia

- Academic access to the latest generation of Intel FPGAs

- Nurture the talent pipeline for Intel and our customers
- Engage research on Intel FPGAs

Undergraduate Teaching Resources for Computer Engineering Profs and TAs

INTEL® FPGA EE Undergrad Coursework Offerings

- **Undergraduate**
  - **Digital Logic**
  - **Digital Systems**
  - **Computer Organization**
  - **Embedded Systems**

What's included?

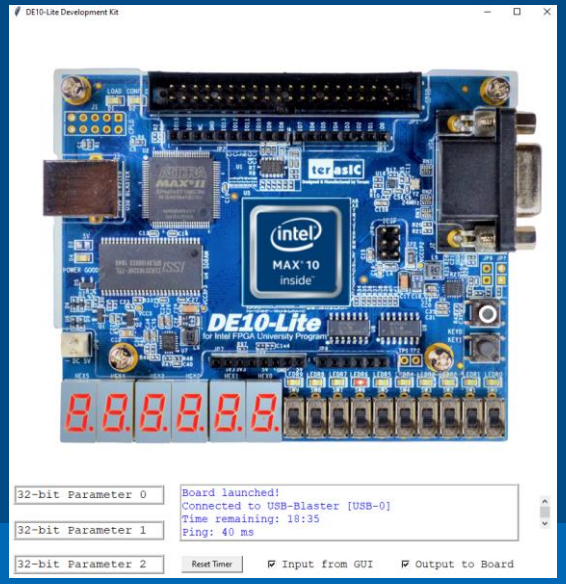
Tutorials on tool usage

Semester worth of labs

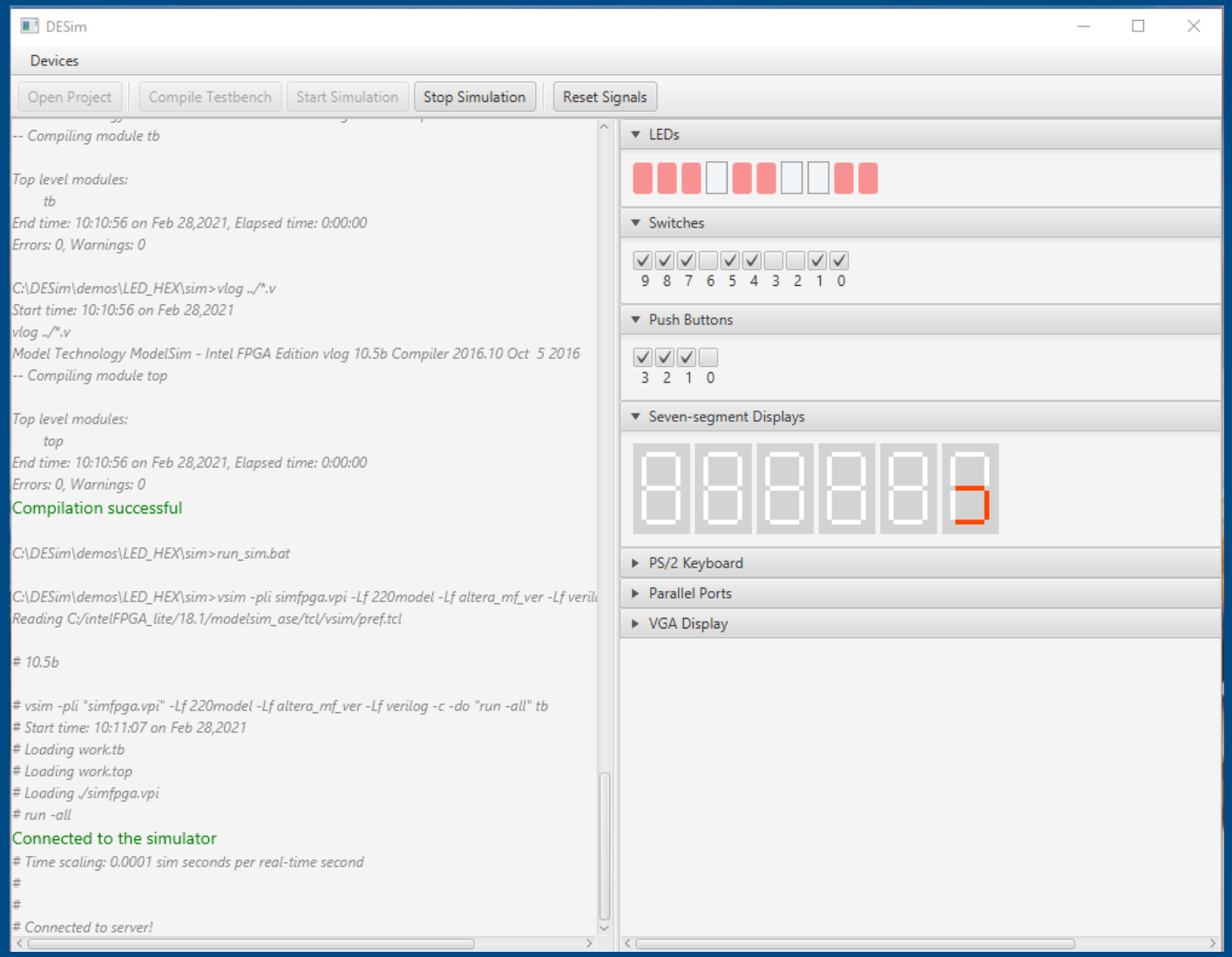
http://fpgauniversity.intel.com

Remote Learning Tools for Undergrad Coursework

- **DESim**
  - **Devkit like GUI that that runs Modelsim under the hood. Great for first time learners of Verilog/VHDL for stimulus/response type labs. No hardware required.**
- **Remote Console**
  - **“Video game” like GUI that connects to Terasic development kits**
  - **Enables remote hosting of boards – ideal for work from home environments**



DESim



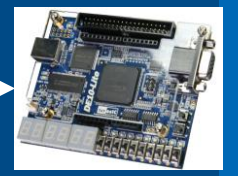
- **DESim**
  - **Student prepares Verilog/VHDL code**
  - **Prof provides testbench and student can observe behavior through GUI – great for new learners to visualize logic design behavior**

https://github.com/fpgacademy/DESim/releases/tag/v1.0.1

Remote Console

Linux or Windows*
Server

USB



Method 1: Intel Quartus® Prime Software Hosted on Server

-or-

Method 2: Intel Quartus® Prime Software Hosted on Student's PC

Does not require 1 Devkit per Server – use USB port replicator

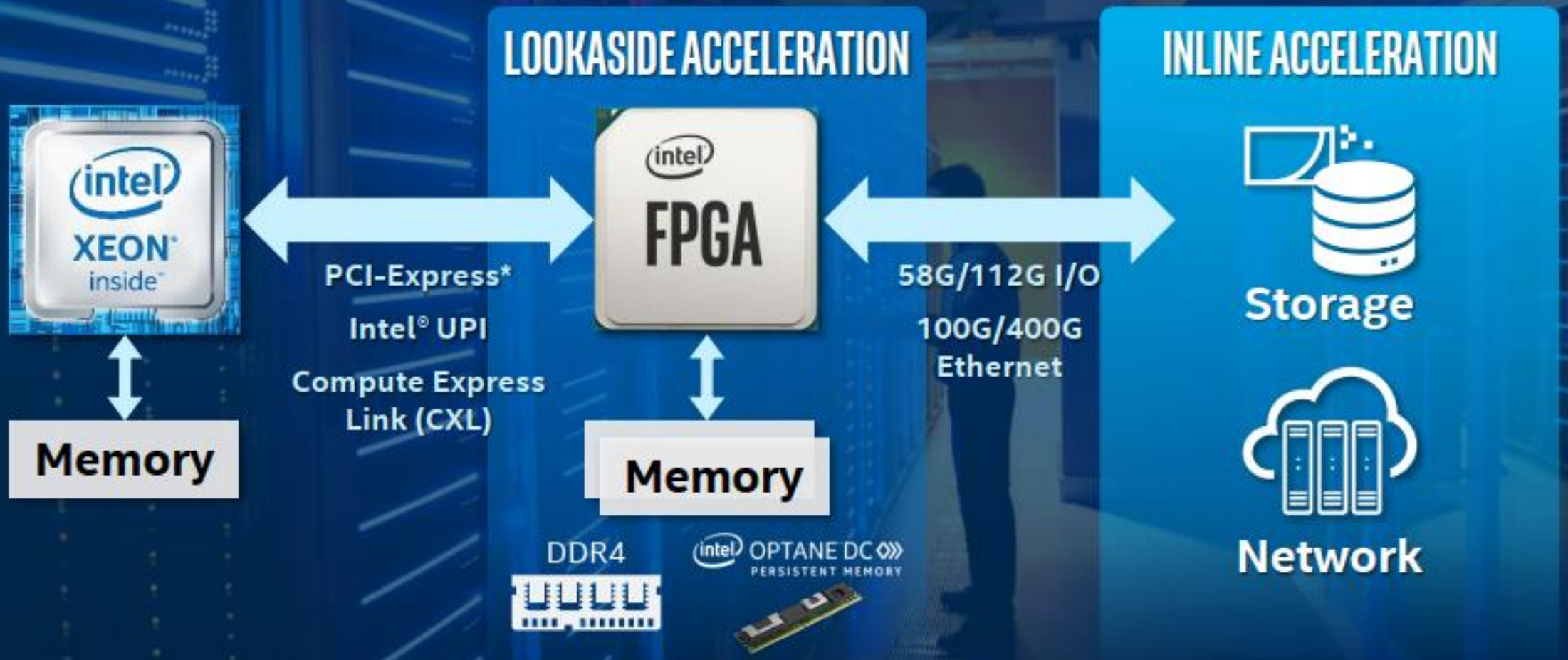
Install setup at university engineering department cluster

Host on Windows or Linux server running Intel Quartus Prime Programmer

https://github.com/intel/FPGA-Devcloud/tree/master/main/HandsFree

Graduate Level and Research: Intel Devclouds and HARP

INTEL® FPGAS ACCELERATING THE CLOUD & ENTERPRISE



Intel FPGA University Graduate Level Coursework

- Graduate level FPGA coursework focuses on AI, Machine Learning, Heterogeneous Computing using C++ extension languages: HLS, OpenCL, DPC++ and OpenVino for Visual Inferencing
- Run a web search on Intel FPGA Training for various topics
- Partner university links for FPGA devcloud coursework through Mindshare Grants:
  - U of Florida – RTL AFU
  - U Mass Lowell – OpenCL / OpenAPI
  - UC Davis - OneAPI
- Intel offers **free** FPGA HARP (aka vlab) for Research or Devcloud (Teaching) cloud services

Intel FPGA Academic Clouds

Cloud access to Intel servers with FPGAs for academics

FPGAs/SW tools already installed. Just login remotely. Ready to use!

HARP (vlab) for long-term research

Hardware accelerator research program (HARP), originally offered cloud access to integrated (MCP) Xeon+FPGA

Now expanded to offer servers with FPGAs cards, hosted in Intel's Academic Compute Env.

Exclusively for long-term academic research (e.g., 1+ year PhD research)

DevClouds for teaching and beyond

Offers servers with FPGA cards

Suitable for teaching (e.g., lab projects) and short-term research efforts. Move to HARP when research grows

And for short-term development projects in general (academic and industry)

What's available

FPGA flows/framework	Devcloud	HARP
Traditional RTL flow	Y	Y
HLS Compiler	Y	Y
FPGA SDK for OpenCL	Y	Y
DPC++ (part of OneAPI)	Y	Upon Request
OpenVino (AI framework)	Y	Upon Request

FPGA hardware

- Intel Xeon with Arria 10 Programmable Acceleration Cards (PAC)
- Intel Xeon with Stratix 10 Programmable Acceleration Cards (PAC)
- Integrated Xeon+FPGA systems (HARP only)

HARP: Getting access

To get access

Send email to: IL_Academic_Res_Env@intel.com
Put email subject “[HARP] new account request”.
Include a short (1 page max) research proposal
Include the type of workloads you are planning to run

More details

The following website offers information of available FPGA systems in HARP. It also provides detailed tutorials and examples on how to get started.
https://wiki.intel-research.net/FPGA.html

Intel Devclouds –Teaching and Short-term Research Focus

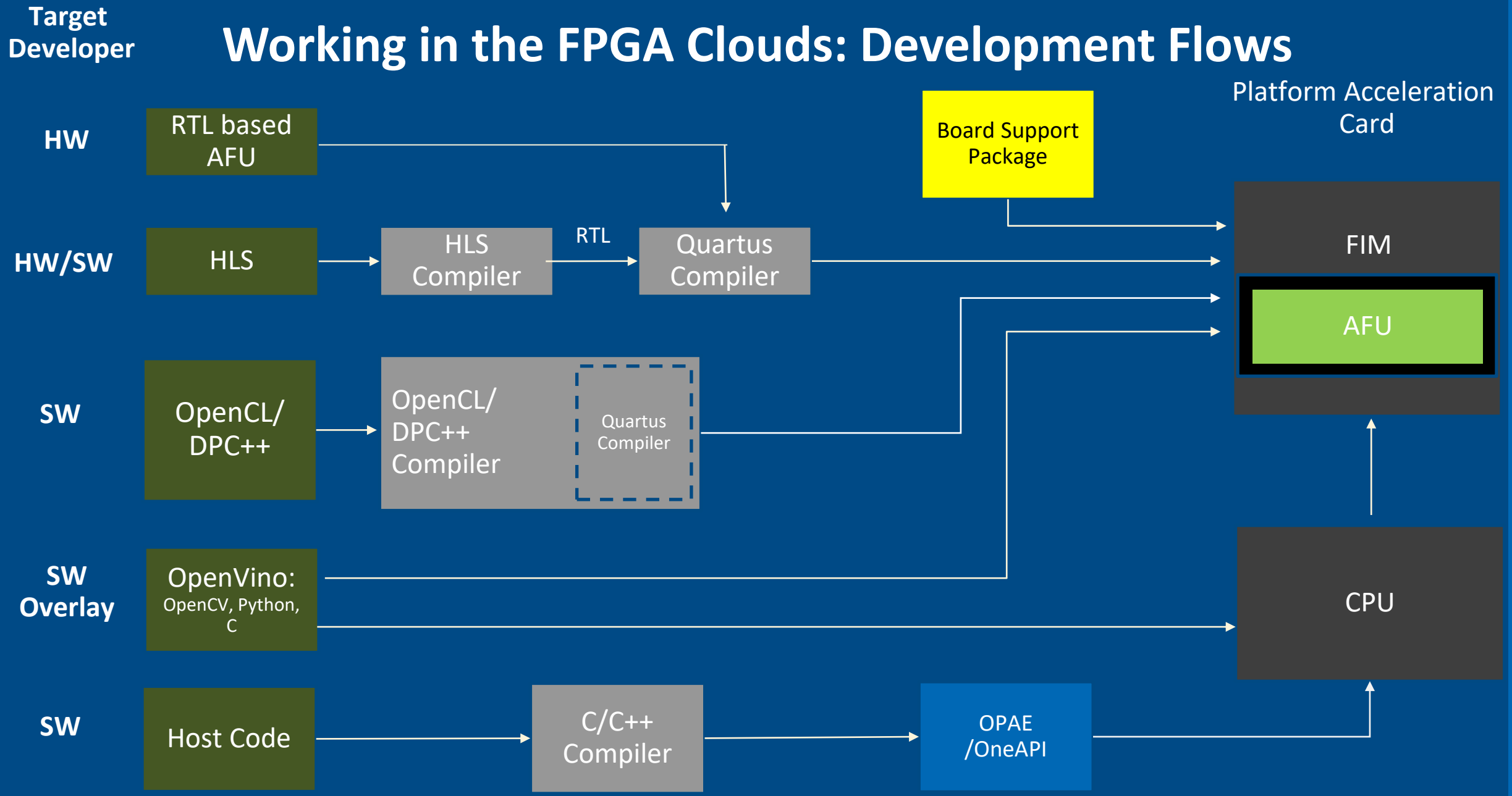
FPGA Instance:
RTL
OpenCL
CPU, FPGA

OneAPI Instance:
OneAPI (DPC++)
CPU, GPU, FPGA

Edge Instance:
OpenVino
CPU, GPU, VPU, FPGA

*Free Access!

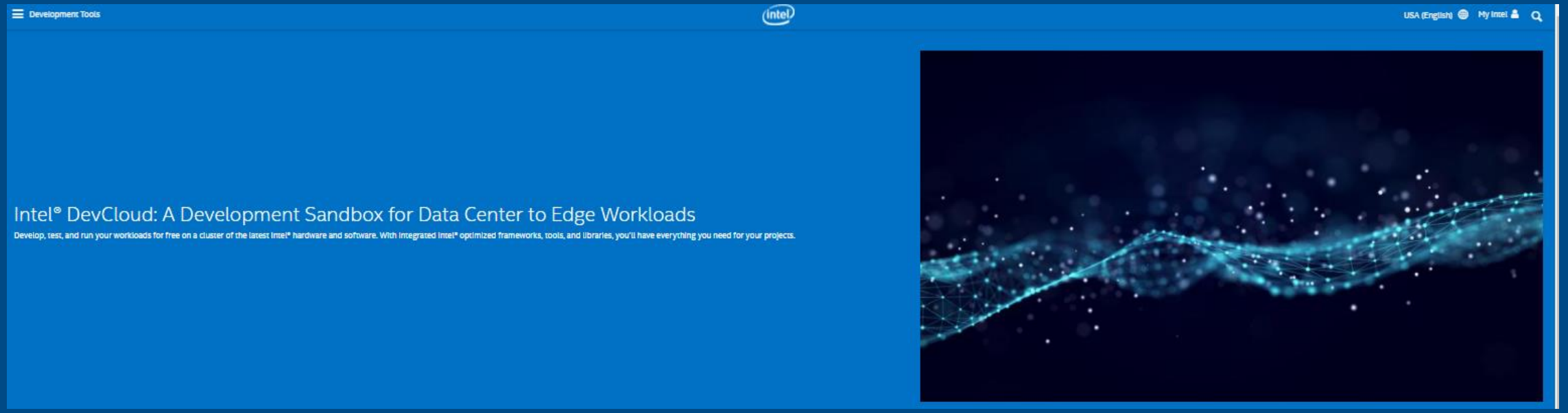
Working in the FPGA Clouds: Development Flows

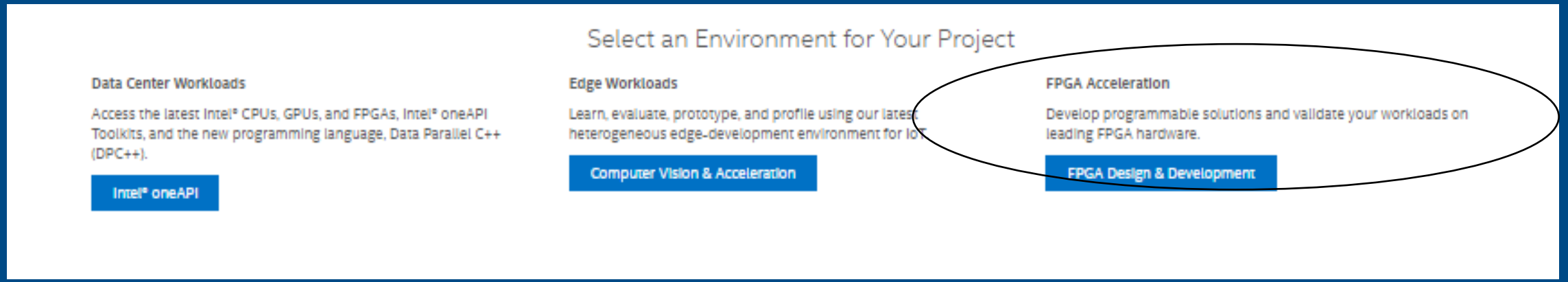


FIM = FPGA Interface Manager

AFU = Acceleration Functional Unit

Website Access for the Intel Devclouds

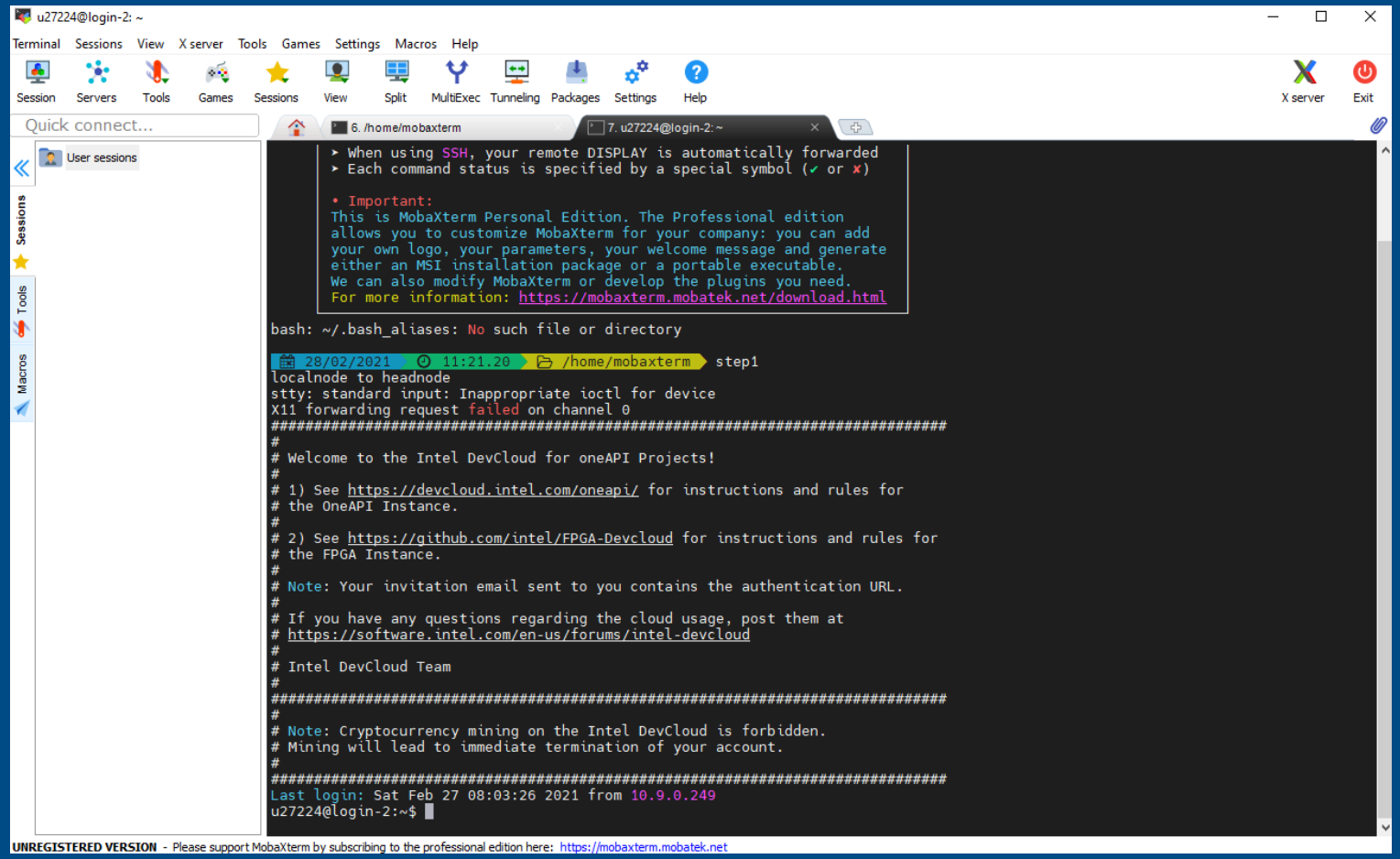




Gaining access to the FPGA Devcloud

- Signup @ https://intelsoftwaresites.secure.force.com/fpgadevcloud
- Check out our github site for instructional material: https://github.com/intel/FPGA-Devcloud
- Quickstart guides for a variety of flows: https://github.com/intel/FPGA-Devcloud/tree/master/main/QuickStartGuides
- You get access for 3 months, look for cancellation notices and extend access. Data is lost if you fail to extend access
- Use batch mode for longer compiles (timeout after 6 hours)! Use walltime extends beyond 6 hour FPGA compiles

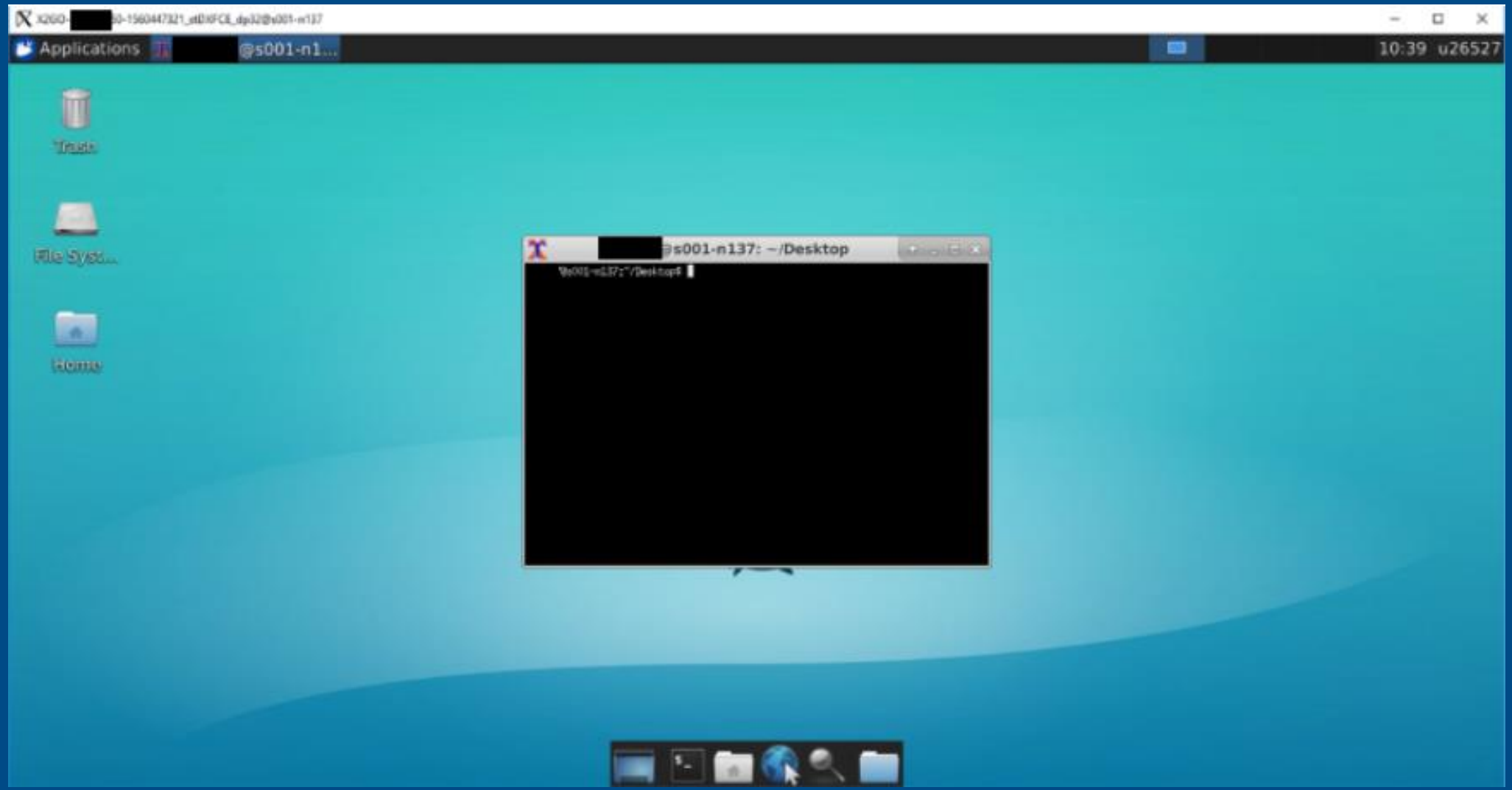
Access method 1: Mobaxterm (multi-tab console)



Linux based – makes PC look like Linux filesystem

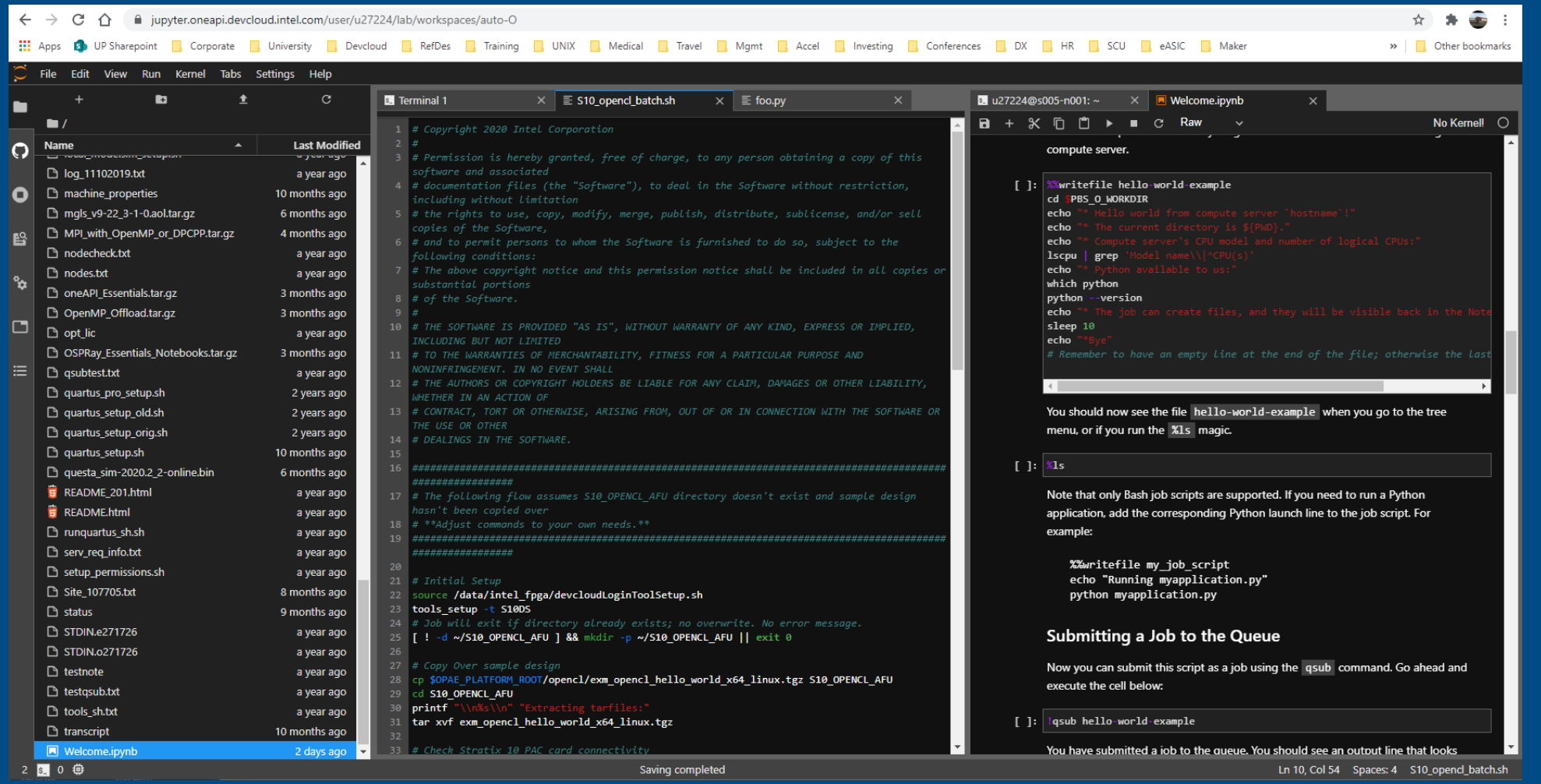
Doesn't support GUI programs – use X2Go

Access method 2: x2go



Multi window system – using sparingly - for Quartus GUI

Access method 3: JupyterLab



Multi tab system through browser – use native editor, not vi; no Quartus GUI

Contacts for Intel FPGA Devcloud help

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Lab – Focus is Access Methods, not language instruction

1. Sign-up (if not done yet – make sure to select FPGA instance)
2. Mobaxterm download, ssh key, etc
3. devcloud_login and tools_setup commands for simplified access
4. Run OpenCL example with emulation
5. Run same example in batch mode
6. Jupyter Lab access

Notes for lab:

- Access to compute machines might get queued, if bottleneck, try interactive lab later
- Interactive sessions consume node for 6 hours, we show interactive mode, however we prefer you use batch processing!
- Walltime command can extend access for 24 hours – see github instructions


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