"A High-Efficiency 3.5GHz Envelope Tracking Power Amplifier for Wireless Communication System Application"

by

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SYNOPSIS

This project involved designing an envelope tracking power amplifier (ET PA) for efficient and high-performance power amplification. The ET PA was designed using Advanced Design System (ADS) and optimized for high efficiency and linearity. The ET PA demonstrated excellent performance, with 54.5% power added efficiency, 9 dB of gain and 25 dB of OIP3 in 3.5GHz. The project also involved developing a simple envelope tracking algorithm to ensure accurate tracking of the input signal envelope, and this envelope tracking power supply (ET PS) was successfully integrated into the ET PA design. Overall, the project demonstrates the feasibility and potential of envelope tracking power amplification for next-generation wireless communications systems.

Keywords: RF Power Amplifier, Advanced Design System, Envelope Tracking, Third-order Interception, Matlab

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STATEMENT OF AUTHORSHIP

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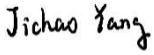
Signature: 

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NOMENCLATE

RF: Radiofrequency

RF PA: Radio Frequency Power Amplifier

ET PA: Envelope Tracking Power Amplifier

ET PS: Envelope Tracking Power Supply

SMPS: Switch Mode Power Supply

PAE: Power Added Efficiency

IQ: In-phase and Quadrature

QPSK: Quadrature Phase Shift Keying

IMD: Intermodulation Distortion

IP3: Third-order Intercept Point

OIP3: Output Third-order Intercept Point

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CHAPTER 1. INTRODUCTION

The pervasiveness of wireless communications systems necessitates that future communication standards require radiofrequency (RF) front ends to be linear to enable high data-rate capabilities using complex modulated signals. Maintaining high linearity is essential to avoid distortion and signal degradation, which can impede efficient and reliable data transmission. Additionally, the energy consumption of wireless transmitters is primarily due to the transmitter block [1]. Therefore, designing efficient transmitter architectures is essential to promote the sustainable use of wireless communication systems and minimize power consumption. This project aims to research and develop RF power amplifiers (RF PAs) that can efficiently and linearly amplify modulated signals.

The project began by designing the RF PA using Advanced Design System (ADS) software [2]. After a type of transistor was chosen, a prototype of the PA would be created and tested using appropriate instruments [2][3] and the details are discussed in Chapter 3.1. Then, the project demonstrated a design of the envelope tracking power amplifier (ET PA) [5], which can boost the efficiency of the PA. The ET PA design focused on the power supply of the PA. The power supply should be capable of tracking the envelope of the input RF signal [6] and feeding an appropriate supply voltage (V_{ds}) to the PA. Chapter 3.2 discusses the detail of the ET PS design process. Finally, the performance and functionality of the ET PA would be tested when injecting IQ signal and by two-tone nonlinear analysis. Chapter 3.3 discusses the design of the IQ modulator and Chapter 3.4 shows the testing and optimizing procedures. The **gain, efficiency, and linearity** performance will judge the overall performance of the PA.

For the applications of ET PA, the key application is in 4G and 5G cellular base station systems [7]. In these systems, ET PA can significantly improve the efficiency of the power amplifiers used in the radio transmitter, resulting in lower power consumption

and reduced operating costs [8]. ET PA can also help to reduce the heat generated by the amplifier, which is a critical consideration in base station design.

CHAPTER 2. BACKGROUND

The introduced background information is ordered by the sequence of appearance of the specific technique in this project thesis.

2.1 Literature Review

RF PA is a type of electronic amplifier that converts low-frequency signals into high-frequency signals. Envelope Tracking (ET) is a currently accepted technique that increases the efficiency of microwave PA compared to conventional class AB or B operation for amplifying time-varying envelope signals, such as most signals used in wireless communication systems today [5]. In the ETPA design, one of the most important parts is to design an effective **switch mode power supply** (SMPS), which controls the power supply (V_{ds}) of the amplifier. Meanwhile, **the linearity** of the PA is also essential since the performance of linearity directly impacts the quality of the amplified signal.

For the SMPS designing research, in [9], a hybrid power supply with a boost converter was introduced for the ETPA design. By boosting the supply voltage from 3.4V to 5V, the output voltage of the supply modulator increases up to 4.5V and the power amplifier shows higher efficiency and wideband. The design focused on 10/20 MHz performance but not the performance in GHz band. In [10], PWM mode buck-boost converter and envelope tracking technologies were implemented to achieve the highest efficiency. The PAE of the power amplifier using a switching power supply can increase by about 10% more than that of the LDO power supply.

For the linearity improvement research, in [11], the nonlinear distortion of the ET PA was discussed. AM-AM and AM-PM distortions are generated because of knee voltage and nonlinear capacitance. In [12], theoretical analysis of GaN HEMT in 2.45 GHz with harmonic injection was discussed and showed the experimental method of how to improve the efficiency and linearity of the specific phase and amplitude of injected second harmonic.

2.2 Classifications of Power amplifier

2.2.1 Class A Power amplifier

Class A power amplifier is a type of electronic amplifier that operates in a linear mode and uses a single active device, typically a bipolar junction transistor (BJT) or a field-effect transistor (FET). In a Class A amplifier, the active device is biased such that it conducts continuously during the entire input signal cycle [13]. The active device is still conducting current when there is no input signal, which makes Class A amplifiers relatively inefficient compared to other amplifier classes.

Despite their low efficiency, Class A amplifiers have a very low level of distortion and produce high-quality, low-distortion output signals [14].

2.2.2 Class B power amplifier

Compared to Class A PAs, class B PAs works at the edge of the cutoff region. This means that no energy can be consumed without an input signal [15]. However, class B PAs suffer from a significant amount of crossover distortion due to the small gap between the positive and negative signals when the two devices switch over, meaning they can only generate half circle of the input signal [16].

2.2.3 Class AB power amplifier

To solve the inefficiency problem of Class A PAs and the distortion problem of Class B PAs, the operating point is set in the middle of the operating points of class A and class B PAs [17]. This is known as Class AB biasing and is commonly used in audio power amplifiers [18]. Class AB biasing ensures that both output transistors are slightly turned on (in the active region) when the input signal is near zero volts, minimizing crossover distortion while maintaining reasonable efficiency.

Overall, the crucial difference between the three types of amplifiers is the choice of bias point. As Fig. 1 shows, different bias point selection leads to different output results (in conduction angle). Class AB PAs have a 180°-360° conduction angle, ensuring a relatively high efficiency and low distortion.

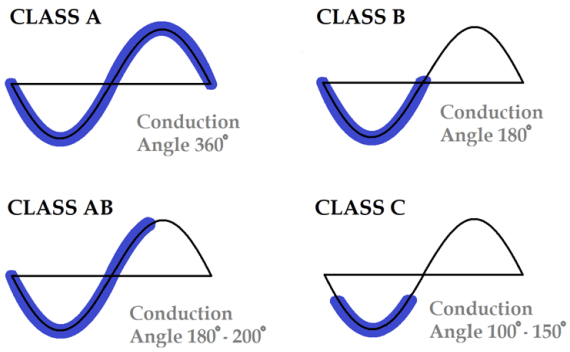

Fig. 1. Operating zone of four types of amplifiers [8]

2.3 Field Effect Transistor (FET) and CGH40006P

Field effect transistor (FET) is a type of transistor that uses an electric field to control current flow in a semiconductor. Typically, there are three terminals in a FET: gate, source and drain [19]. The voltage between the gate and source (V_{gs}) controls the channel's conductivity. The channel allows the carrier to pass through. The voltage between the drain and source (V_{ds}) determines the operation region of the FET and affects the current flow. As V_{ds} increases, three working modes emerge on the FET: cut-off, linear (triode), and saturation. Modes of FET are shown in Fig. 2.

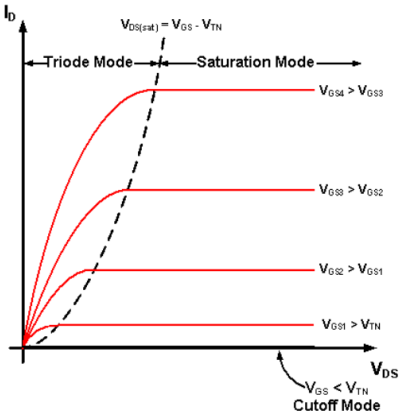

Fig. 2. I_D–V_{ds} Characteristic Curves of an n-Channel Enhancement Mode MOSFET

There are several kinds of FETs being used current days. For example, metal oxide semiconductor FET (MOSFET) is widely used in the integrated circuit for its low cost and low power consumption [20]. Metal semiconductor FET (MESFET) is used in radar systems [21] and high electron mobility transistor (HEMT) is used in high-

frequency applications [22].

In this project, CGH40006P was chosen as the amplifier. The CGH40006P is a HEMT based on gallium nitride (GaN) technology developed by Wolfspeed. This device is designed to operate from a 28-volt rail and is a versatile solution for various RF and microwave applications. The CGH40006P is known for its high efficiency, high gain, and wide bandwidth capabilities, making it ideal for use in both linear and compressed amplifier circuits [23].

The datasheet of CGH40006P can be found in the Appendix. C

2.4 Stability analysis

For PA design, it is essential to know whether the PA works unconditionally stable, which strictly relates to reliability and performance. Unconditional stability means that the power amplifier is stable for any combination of load and source impedance, regardless of the frequency and input power level [24]. In contrast, conditionally stable amplifiers may require specific load or source impedances to remain stable [25].

There are two methods used in this project to test the stability of the RF PA: the Mu test and the stability circle. Fig. 3 shows the circuit model for a small signal stability test.

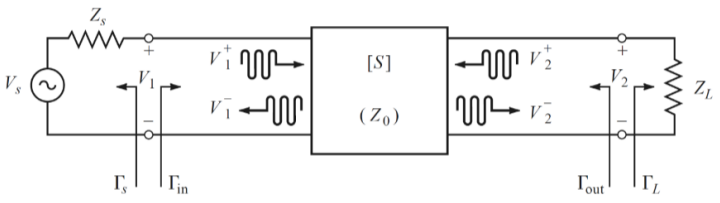

Fig. 3. Small Signal Stability Test [26]

The circuit is unconditionally stable when $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ for all passive source and load impedances. Both the Mu test and stability circle can demonstrate the merit of being unconditionally stable.

For Mu test, a device is unconditionally stable if:

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} > 1 \quad (1)$$

where $\Delta = |S_{11}S_{22} - S_{12}S_{21}|$

For stability circle, when both the source and load circle are away from the unit circle and $|S_{11}| < 1$, the circuit is unconditionally stable since both load and source impedance cannot make the device oscillate in this case.

2.5 Measurement of efficiency

To measure the efficiency of the RF PA, the project involved two methods for efficiency measurement: power added efficiency (PAE) and DC-to-RF efficiency.

For PAE, it is the ratio of the output power minus the input power and the added power (power from the DC source). The formula is shown in (2)::

$$\varepsilon_{PAE} = \frac{P_{out} - P_{in}}{P_{DC}} \quad (2)$$

For DC-to-RF, it is the ratio of the output power and the added power (power from the DC source). The formula is shown in (3):

$$\varepsilon_{DCtoRF} = \frac{P_{out}}{P_{DC}} \quad (3)$$

This project used PAE in most power measurements (power sweep, load pull, etc.). DC-to-RF was used after installing the ET PS since there existed a delay between the input and output power, making PAE less representative for the efficiency measurement.

2.6 Envelope tracking technique

Envelope tracking (ET) is a power amplifier (PA) technique that helps improve wireless communication systems' efficiency and linearity [27]. It is a dynamic power supply technique where the power supply voltage is adjusted in real-time to match the envelope of the input signal. This technique helps minimize the voltage headroom required by the PA, reducing power consumption and heat dissipation. Fig. 4 shows

the basic idea of the topology of the ET PA.

The basic principle of envelope tracking is to maintain a constant ratio between the peak-to-average power ratio (PAPR) of the input signal and the power supply voltage of the PA [28]. This is achieved by using a fast DC-DC converter to track the input signal's envelope and adjust the power supply voltage accordingly.

The benefits of ET include improved efficiency, increased output power, and reduced distortion, making it an ideal technique for modern wireless communication systems that require high data rates and low power consumption. It has found applications in 5G wireless communication systems, satellite communications, and radar systems, among others [9].

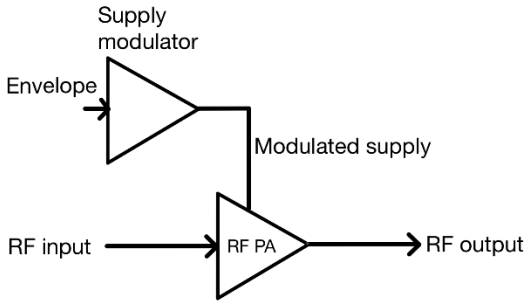

Fig. 4. The representative structure of ET PA

2.7 IQ modulated signal and IQ modulation

IQ modulation is a method used in communication systems to modulate a radio frequency carrier wave with two baseband signals: the in-phase (I) and quadrature (Q) components. The I and Q components are two separate signals, each modulated with the baseband information and combined to form the modulated signal.

The I and Q signals represent two orthogonal axes in the complex plane, with the I component representing the signal's amplitude in the horizontal direction and the Q component representing the signal's amplitude in the vertical direction. By varying the

amplitude and phase of the I and Q components in accordance with the modulating signal, the modulated signal can be used to carry the desired information [29].

Two input signals, I and Q, should be added to a mixer for a typical IQ modulator. Also, the Q signal should have a 90-degree phase shift, which needs a local oscillator (LO) to accomplish. The modulator can basically generate all types of RF signals. Fig. 5 shows the fundamental architecture of the IQ modulator.

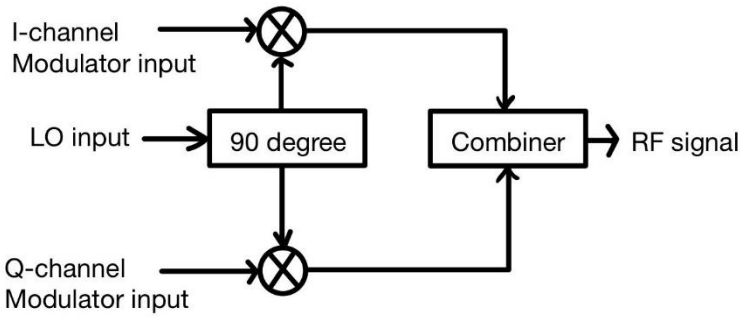

Fig. 5. Fundamental architecture of an IQ modulator

In this project, IQ modulated signal was used as the testing signal of the ET PA. For the final test of the ET PA, IQ modulated signal was involved as the input signal of the ET PA.

2.8 Quadrature Phase Shift Keying (QPSK)

QPSK is a digital modulation scheme that is based on IQ modulation. In QPSK, the digital data is first converted into two-bit symbols, each representing a specific combination of amplitude and phase. The symbols are then mapped onto a constellation diagram, a two-dimensional grid representing the possible combinations of amplitude and phase [30]. The QPSK constellation diagram consists of four equally spaced points on a circle, with each point representing a specific combination of two-bit symbols. The points are located at 0, 90, 180, and 270 degrees on the circle, corresponding to the four possible combinations of amplitude and phase: (1,0), (0,1), (-1,0), and (0, -1). During transmission, the carrier signal is modulated by shifting its

phase according to the symbol being transmitted [31]. For example, if the symbol is (1,0), the phase of the carrier signal is not shifted, while if the symbol is (0,1), the phase of the carrier signal is shifted by 90 degrees.

To achieve QPSK modulation, the I and Q signals are first generated from the digital signal using a digital-to-analog converter (DAC), and then filtered to remove unwanted high-frequency components. The I and Q signals are then modulated onto a carrier wave using an IQ modulator. The resulting modulated signal is then transmitted over a channel. In QPSK, four binary values can be transmitted, and the schematic is shown in Fig. 6.

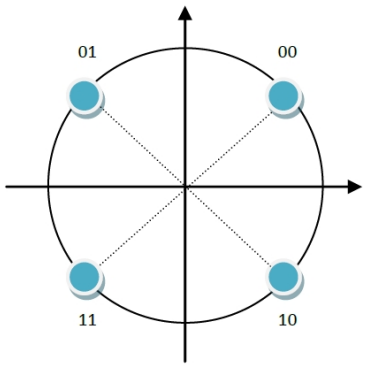

Fig. 6. QPSK modulation schematic diagram [32]

The project involves QPSK for IQ modulation.

2.9 Intermodulation distortion (IMD) and third-order intercept point (IP3)

For a nonlinear system, intermodulation distortions (IMD) appear when signals with more than one tone are present at the input of the signal [26].

If there are two tones in the input port:

$$x(t) = Acos[\omega_1 t + \theta_1] + Bcos[\omega_2 t + \theta_2] \quad (4)$$

The output signal can be expressed as:

$$y(t) = \sum_{r=1}^{\infty} A_{or} cos[\omega_r t + \theta_{or}] \quad (5)$$

where $\omega_r = m\omega_1 + n\omega_2$, ω_1 and ω_2 are the fundamental frequencies. When the absolute value of $m+n$ equals three, the corresponding output is called third-order component. Similarly, the corresponding output is called third-order components when the absolute value of m plus n equals 3.

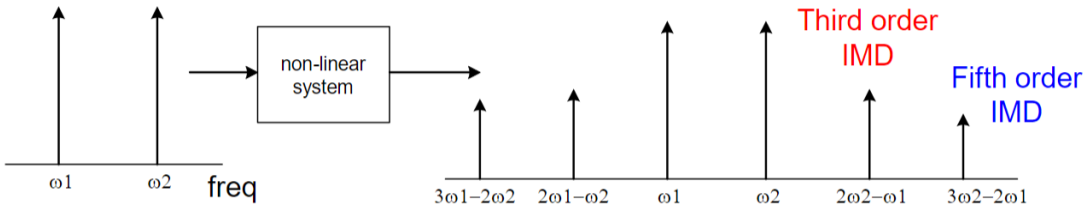

Fig. 7. Emergence of the IMD

The third-order intercept point (IP3) is a specific figure associated with the third-order intermodulation distortion (IMD3). An interception point is reached if the IMD3 and the carrier frequency are extrapolated. The input and output of the interception point are called the third-order input intercept point (IIP3) and third-order output intercept point (OIP3). In real-world applications, IIP3 and OIP3 are virtual values and can never be achieved by an amplifier. They measure the linearity of the PA.

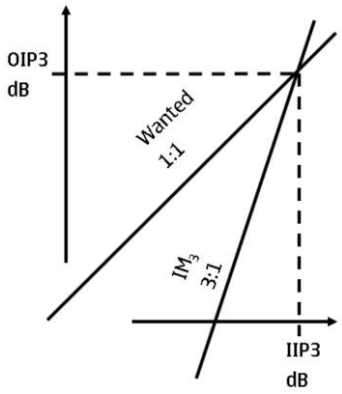

Fig. 8. IIP3 and OIP3 demonstration

In this project, the OIP3, IIP3 and IIP2 were introduced to test the linearity of the ET PA.

CHAPTER 3. PROPOSED WORK

In general, the project mainly focused on the design of the ET PA, which can be divided into the RF PA design and envelope tracking power supply (ET PS) design. They sum up working as an ET PA entity. IQ signal was involved as the input signal for the final testing part.

3.1 RF PA Design

Six steps were taken to obtain a reliable and high-efficient RF PA, and they were all implemented in semester 1. The six steps are introduced in the following content.

3.1.1 Bias Point Determination

As mentioned in the background, the bias point needs to be carefully determined to achieve a high-efficient and low-distortion class AB power amplifier. To observe the working region of the HEMT, DC-IV curve of the HEMT needs to be plotted. The bias point can then be selected based on the DC-IV plot. Fig. 9 shows the DC-IV characterization schematic.

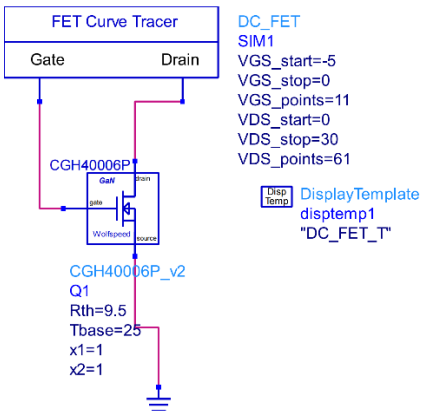

Fig. 9. DC-IV Characterization Schematic

The simulation result was obtained, as Fig. 10 shows. The marker m1 in the graph is the selected bias point of the RF PA. The gate to source voltage (V_{gs}) equals -2.5V and the drain to source voltage equals 28V.

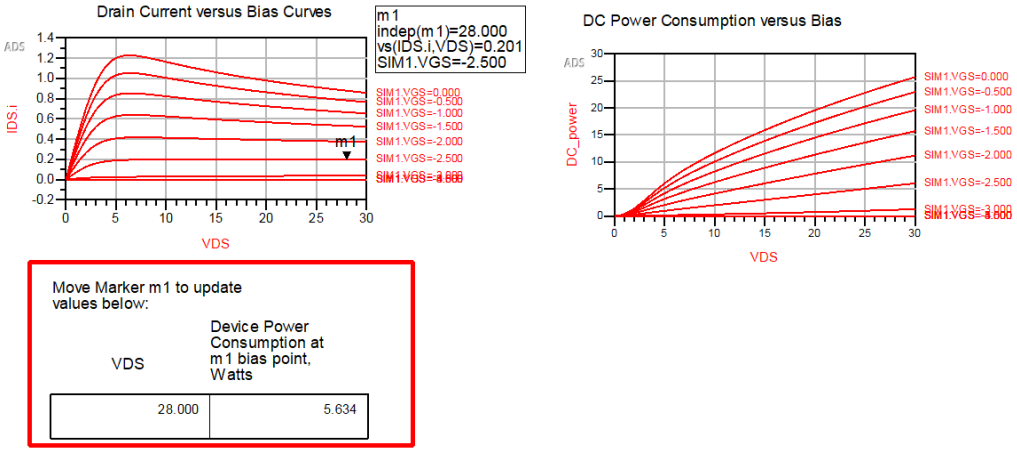

Fig. 10. DC-IV Curve and the chosen bias point

3.1.2 Implementation of the Amplifier Circuit and Stability Test

In order to implement the RF power amplifier (RF PA), it was necessary to have a two DC power supply comprising V_{ds} and V_{gs}. Additionally, suitable AC input and output ports needed to be designed in such a way that the RF input signal would not interfere with the functioning of the DC paths. The simplified structure is shown in Fig. 11

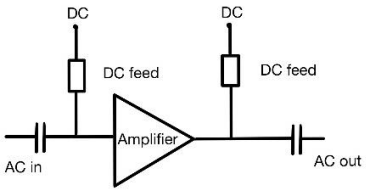

Fig. 11. Schematic diagram of the RF PA

The parameter of the microstrip substrate is listed in Fig. 12. The “LineCalc” tool’s configuration is shown in Fig. 13.

Fig. 12. Settings of the MSub

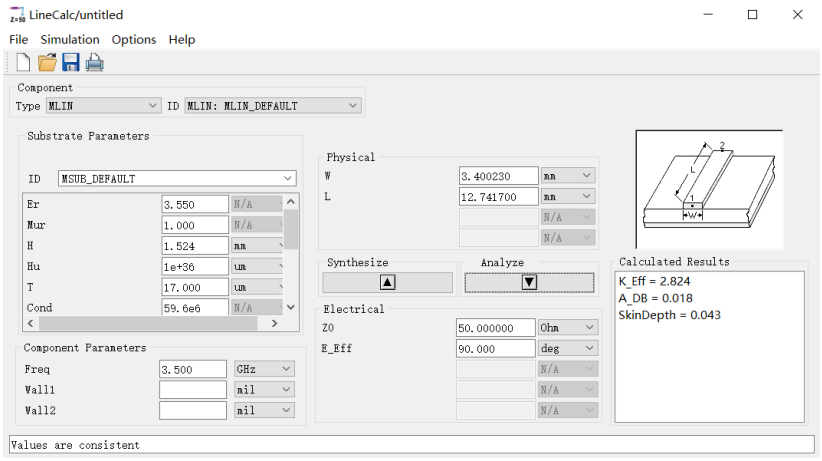

Fig. 13. LineCalc for obtaining the transmission line's parameter

A resistor with a shunt capacitor (known as stability circuit marked green) was added at the input port to ameliorate the instability for low-frequency response to ensure that the amplifier is unconditionally stable. Fig. 14 shows the final topology of the RF PA.

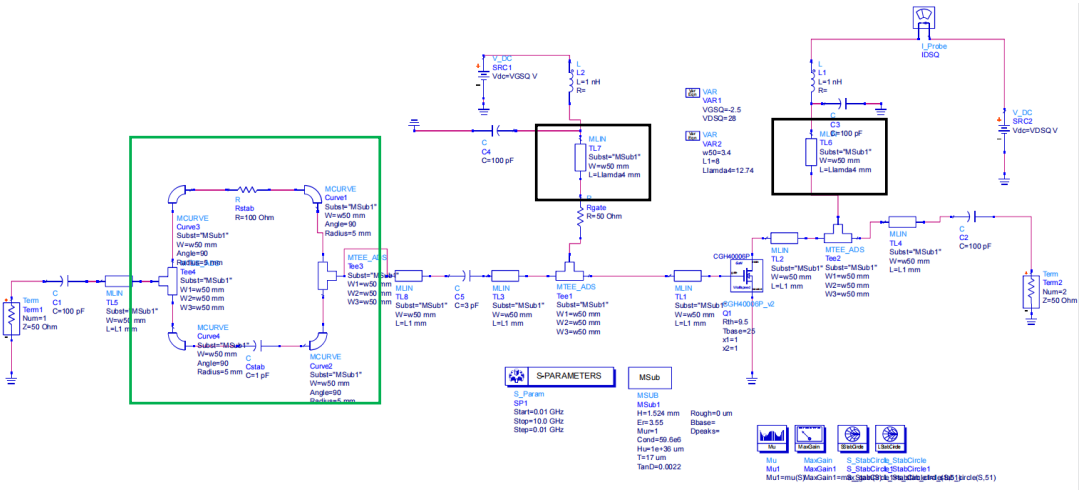

Fig. 14. Final topology of the RF PA

The analysis of the circuit shows as follows:

For the DC feedline (marked in the black rectangle), quarter wavelength feedlines were introduced, which aim to provide a stable DC bias to the circuit and isolate the DC path from the RF signal path. The feedlines minimize the interference between DC and RF signals.

The MLIN and T-junction of the design interconnect different sections of the PA (input port to the amplifier, etc). It controls the integrity of the input microwave signal.

Meanwhile, for real-world wireless applications, the microstrip transmission line is easy to integrate on the printed circuit board (PCB) [33].

As it is mentioned in 2.3 Stability analysis, to achieve unconditional stability for the design, to be specific, the value of Mu should be larger than 1 and the source/load circle should be out of the unit circle, “tuning” was introduced to adjust the values of the specific components in the circuit: The resistors in the DC path and stability circuit, the capacitor in the stability circle. The tuned result is shown in Fig. 15. In the stability circuit, $R_{stab} = 100\Omega, C_{stab} = 1pF$and $R_{dc} = 50\Omega$ Also, the simulation result will be demonstrated and analyzed as follow.

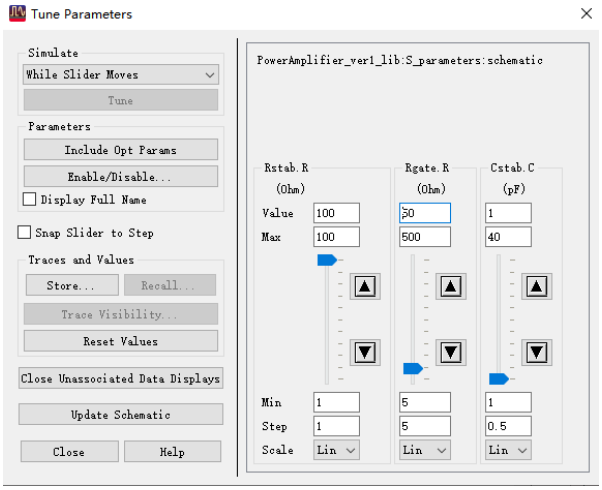

Fig. 15. Tuning window

The mu test and stability circle results are shown in Fig. 16.

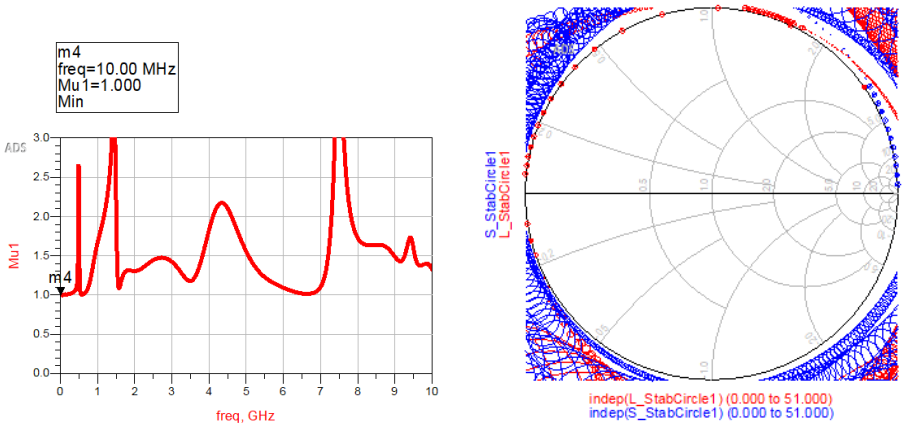

Fig. 16. Results of the stability tests

From 0.01 GHz to 10 GHz, the result of the Mu test was higher than 1 in the frequency band. Also, both load and source circles did not cross the unit circle. Both tests prove that the device is unconditionally stable.

S-parameters and MaxGain simulation were introduced for simulation. The simulation frequency ranged from 0.01 GHz to 10 GHz. By using the "S-parameter" and "MaxGain" tools in ADS, the simulation results are illustrated in Fig. 17,18.

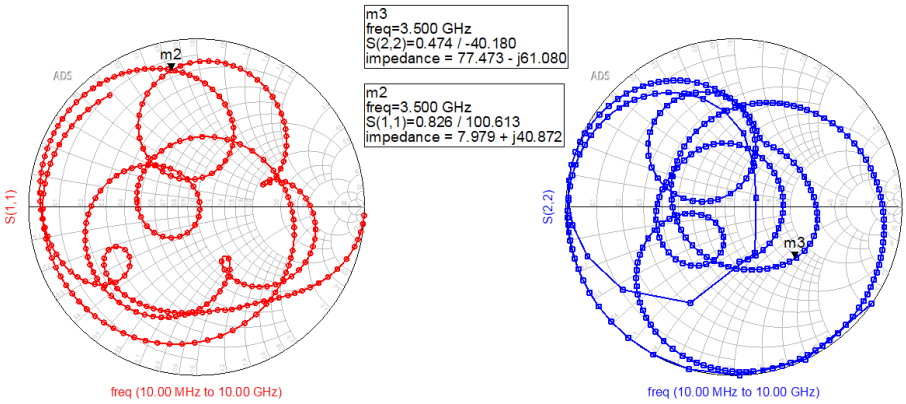

Fig. 17. Simulation results of S_{11} and S_{22}

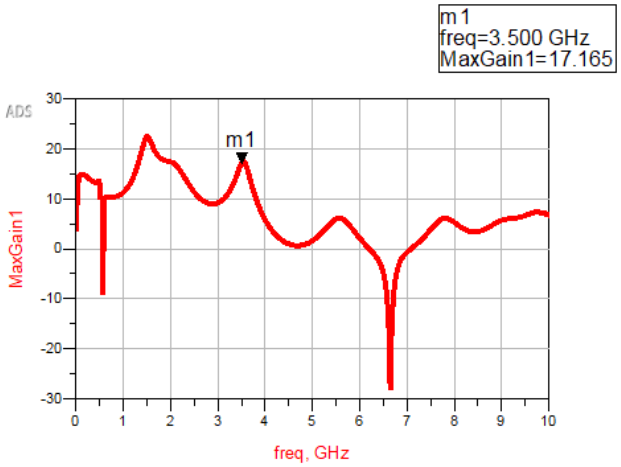

Fig. 18. Simulation result of MaxGain

From the above simulation results, it is known that in 3.5 GHz, the maximum gain of this circuit is 17.165 dB, $S_{22} = 0.474\angle -40.180$ and $S_{11} = 0.826\angle 100.613$.

3.1.3 Circuit Gain Optimization

Although the circuit schematic has been designed and stabilized, optimizing the design for obtaining higher gain is essential, ensuring that the PA works preferably in the following efficiency testing. To optimize the circuit and reach higher gain, the aforementioned three components (in Fig. 15) were tuned to abide by the following criteria:

1. The circuit should be stable: Mu value in the tested frequency band (0-10GHz) should be greater than 1 and no source&load circles cross the unit circle.
2. The gain has to be greater than the previous design. The other parameters (bias point, input and output impedance) should not be changed.

By tuning the values of the three components, the new circuit and the new S parameters results are shown in Fig. 19,20.

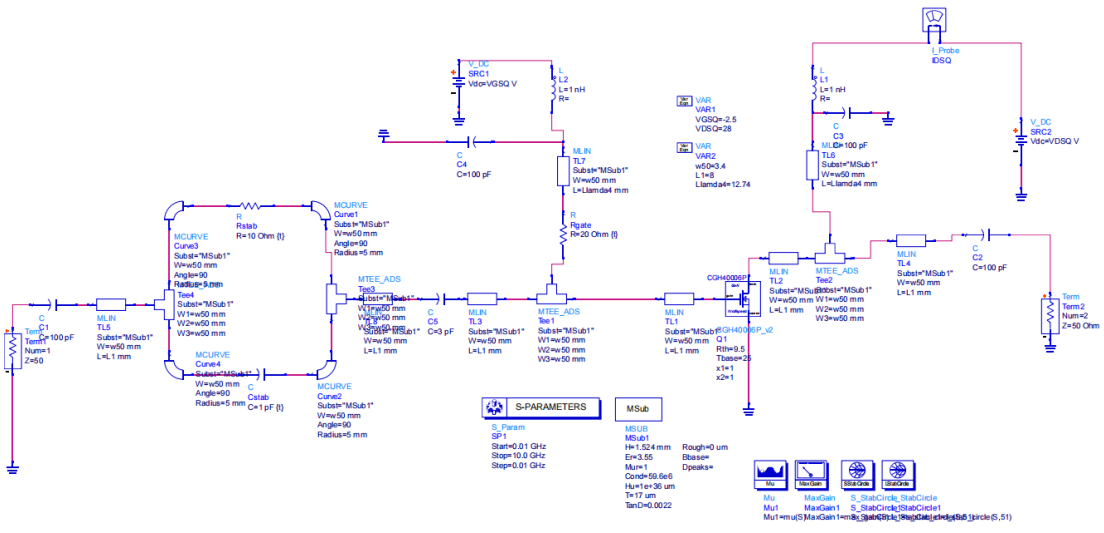

Fig. 19. Optimized circuit schematic

Fig. 20 shows the result of the stability tests. The optimized design passed the stability test since the minimum Mu value is one and the unit circle is clean.

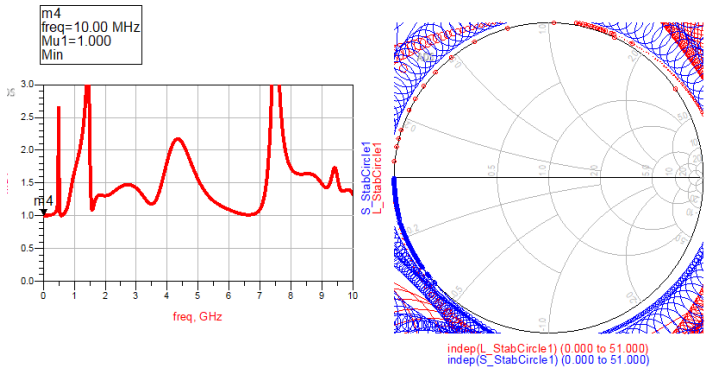

Fig. 20. Stability test results of the optimized circuit

The new S parameters results and Maxgain result are shown in Fig. 21,22.

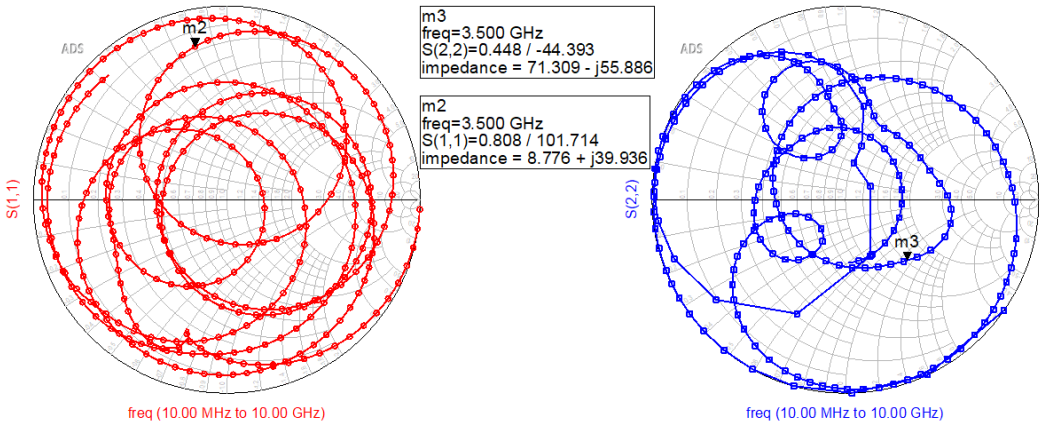

Fig. 21. S parameters (S_{11} and S_{22}) of the optimized circuit

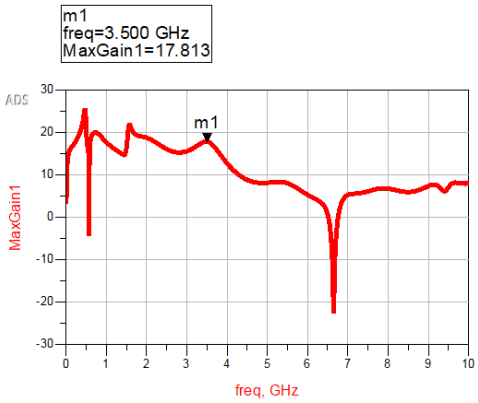

Fig. 22. MaxGain of the optimized circuit

The result shows that $S_{22} = 0.448\angle -44.393$ and $S_{11} = 0.808\angle 101.714$. This data is vital for the matching network design.

Fig. 22 illustrates the MaxGain of the optimized design, reaching 17.813 dB, which is beyond the previous design by 0.648 dB.

3.1.4 Power Sweep

Before the power sweep, the power measurement methods must first be added to the circuit. The configuration is shown in Fig. 23. “Pt” calculates the RMS value of the power and “PAE” calculates the power added efficiency in percent.

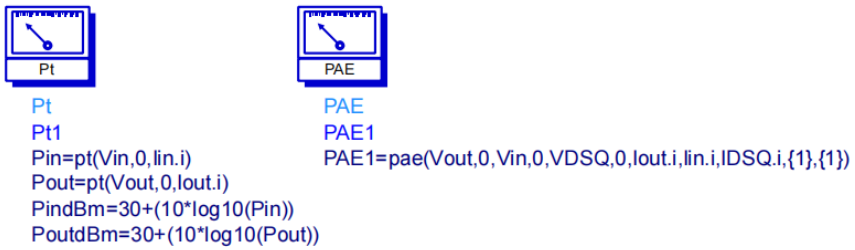

Fig. 23. Power measurement configuration

To maximize efficiency (i.e., PAE) of the schematic, the power sweep for the design needs to be conducted when the input is matched. Through power sweep process, the load impedance in which the PA can achieve maximum PAE can be obtained. The value of the output impedance is essential for the output matching network design.

To realize input matching in an easy way, the input impedance was adjusted to the conjugate of S_{11}, which is $8.776 - j * 39.936\ \Omega$. The adjusted input port is shown in Fig. 24.

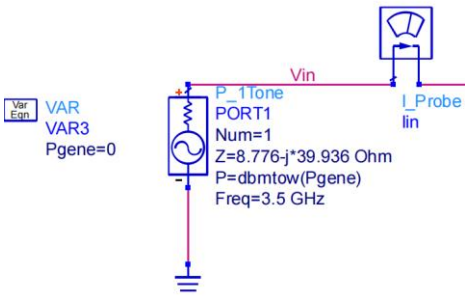

Fig. 24. Adjusted input port

To sweep the input power, which was “Pgene” parameter in this case, the “sweep” part, included in the “harmonic balance”, was configurated as shown in Fig. 25.

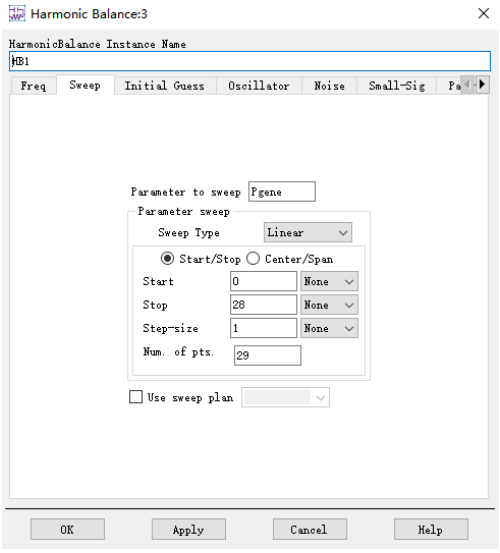

Fig. 25. Harmonic balance configuration for power sweep

After adjusting the input port to achieve input matching, the output port was also changed to enable the parameter sweep. “MagnitudeLoad” and “PhaseLoad” were introduced as the sweeping parameters. “Sweep1” was responsible for the “MagnitudeLoad” sweep and “Sweep2” aimed to sweep “PhaseLoad” followed by “Sweep1”. The parameters were assigned in a wide range for the first time in the sweeping simulation to search for the range which the maximum PAE would exist. “MagnitudeLoad” was from 0 to 0.7 and “PhaseLoad” was from 0 to 350 degree. The simulation configuration is shown in Fig. 26.

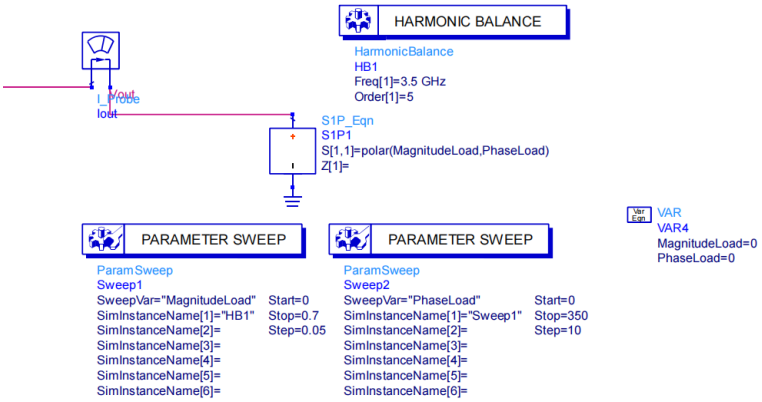

Fig. 26. Simulation configuration for output port

The first-round simulation result is shown in Fig. 27. As the marker illustrated, the

efficiency reached the maximum when the phase is 30 degree and the magnitude is 0.35. Next, for the second-round simulation, the range of the parameters was adjusted to narrow and close to the first-round result. The range of sweeping is limited, and the configuration is shown in Fig. 28.

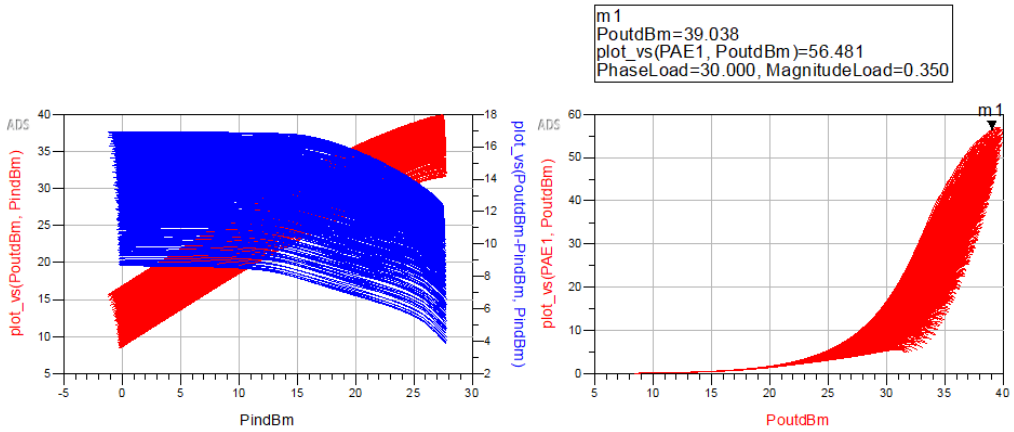

Fig. 27. First round power sweep result

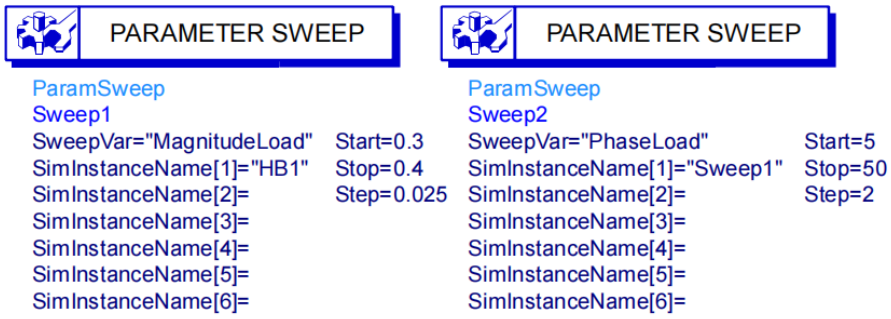

Fig. 28. Simulation configuration for the second-round power sweep

The second-round simulation result is shown in Fig. 29. The efficiency reaches the maximum when phase equals 29 degree and magnitude equals 0.3. Fig. 30 shows the power sweep result when the output impedance was set as the “m1” point in Fig. 29. It can be observed that when Pout equals 39.513dBm, the PAE reaches 59.223%.

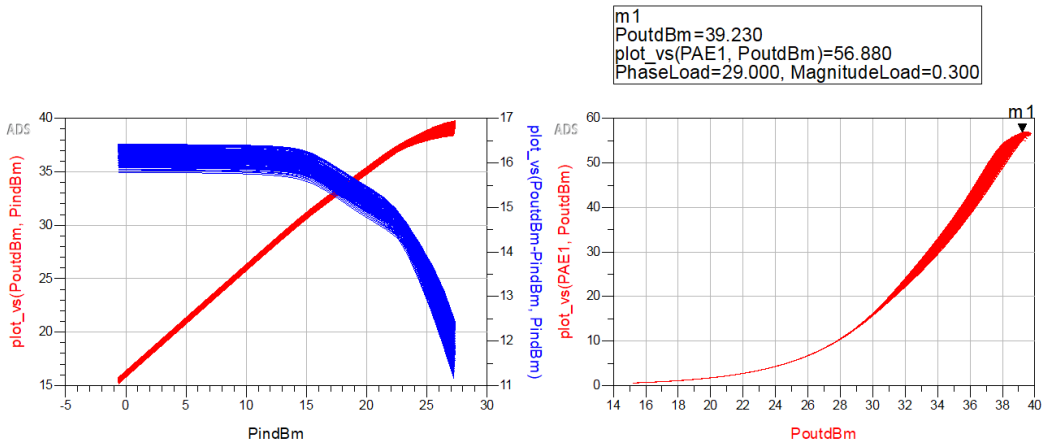

Fig. 29. Second round power sweep result

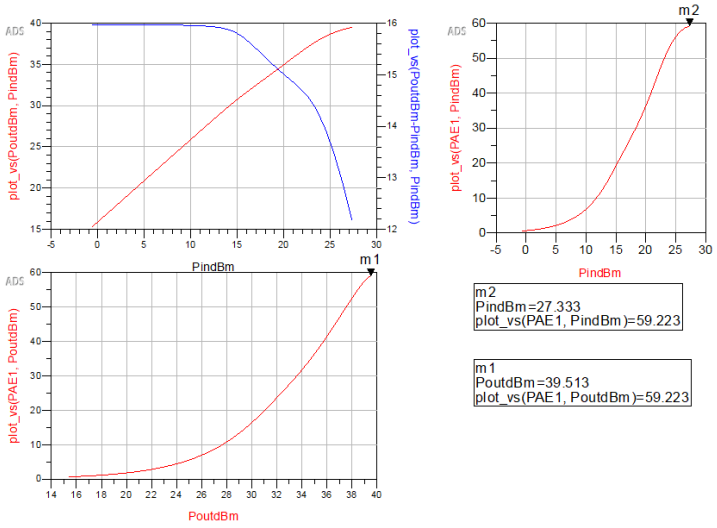

Fig. 30. Simulation result when phase and magnitude was set to 29 degree and 0.3

The impedance can be obtained [26]:

$$Z = Z_0 * \frac{1+\Gamma}{1-\Gamma} \tag{6}$$

where $Z_0 = 50\,\Omega$ and $\Gamma = 0.3 * e^{i*\frac{29*\pi}{180}}$, representing the characteristic impedance and reflection coefficient, respectively.

The result of Z was obtained through Matlab, as shown in Fig. 31, $Z \approx 80.50 + j * 25.73\,\Omega$

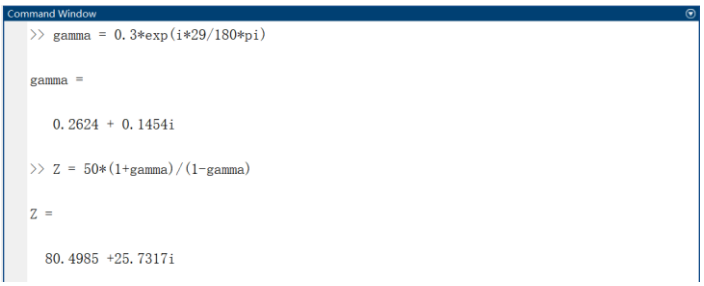

Fig. 31. Result of the output impedance in Matlab

3.1.5 Input and Output Matching Network Design

In order to enhance the efficiency of the PA and avoid reflection of the injected power, the input and output matching network were implemented. The input matching network aimed to minimize the reflection of the PA. To be specific, the input reflection coefficient S_{11} needs to be adjusted to zero. The output matching network aimed to maximize the delivered power. The power sweep result was used in this network's design.

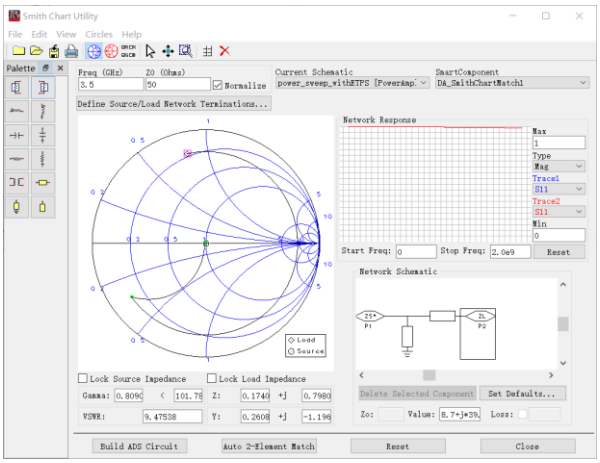

Fig. 32. Smith chart tool for input matching network design

Fig. 32 shows the designing method of the input matching network. In the network schematic, S_{11} was used as load impedance and $Z_0 = 50\,\Omega$ was the source impedance. However, a Libra Microstrip T-Junction must connect with the MLIN to ensure the device works properly. After adding the T-junction, the length needs to be slightly tuned to eliminate the influence of the T-junction. Fig. 33 shows the finished topology of the input matching network. Meanwhile, the S_{11} is demonstrated in Fig.

34, which reveals that the input impedance is matched.

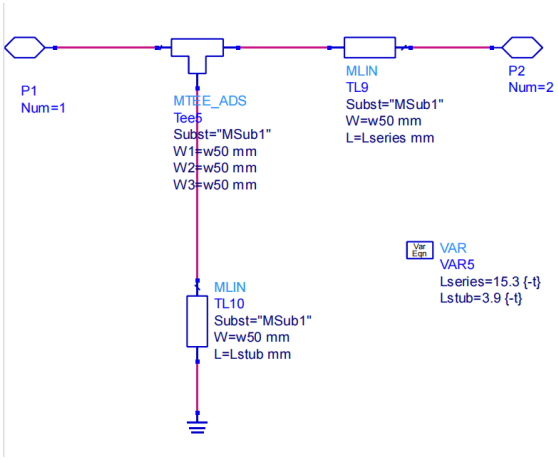

Fig. 33. Input matching network

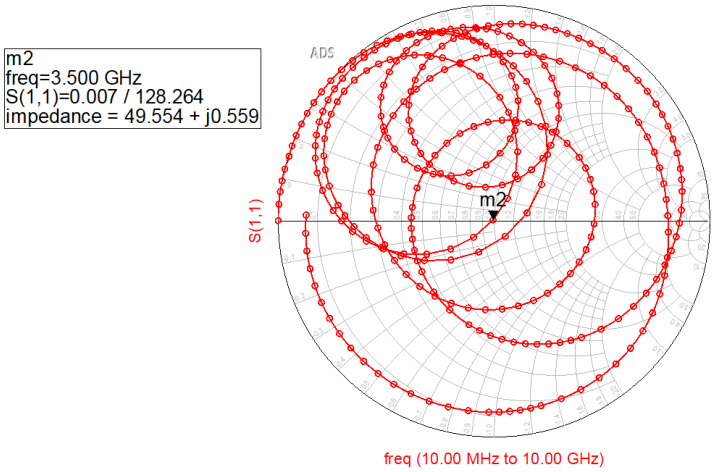

Fig. 34. S_{11} simulation result when adding the input matching network

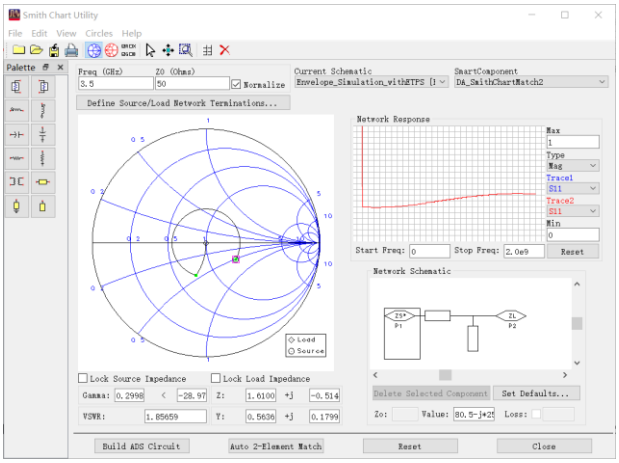

Fig. 35. Smith chart tool for input matching network design

The output matching network design had a difference compared to the input one. To maximize efficiency, instead of using the conjugate of S_{22} as the source impedance, the impedance obtained in the power sweep was applied to achieve the maximum PAE. Fig. 36 shows the topology of the output matching network.

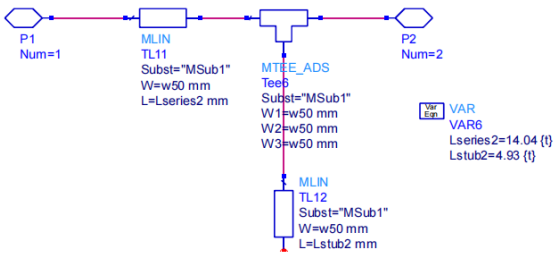

Fig. 36. Output matching network

3.1.6 Load Pull

In reality, the device cannot always work with a 50 Ohm output impedance. Also, load pull needs to be carried out to check the validity of the result in the power sweep. Fig. 37 shows the testing circuit for load pull. The V_{gs} was set to -2.5V and V_{ds} was set to 28V, which corresponded to the configuration before.

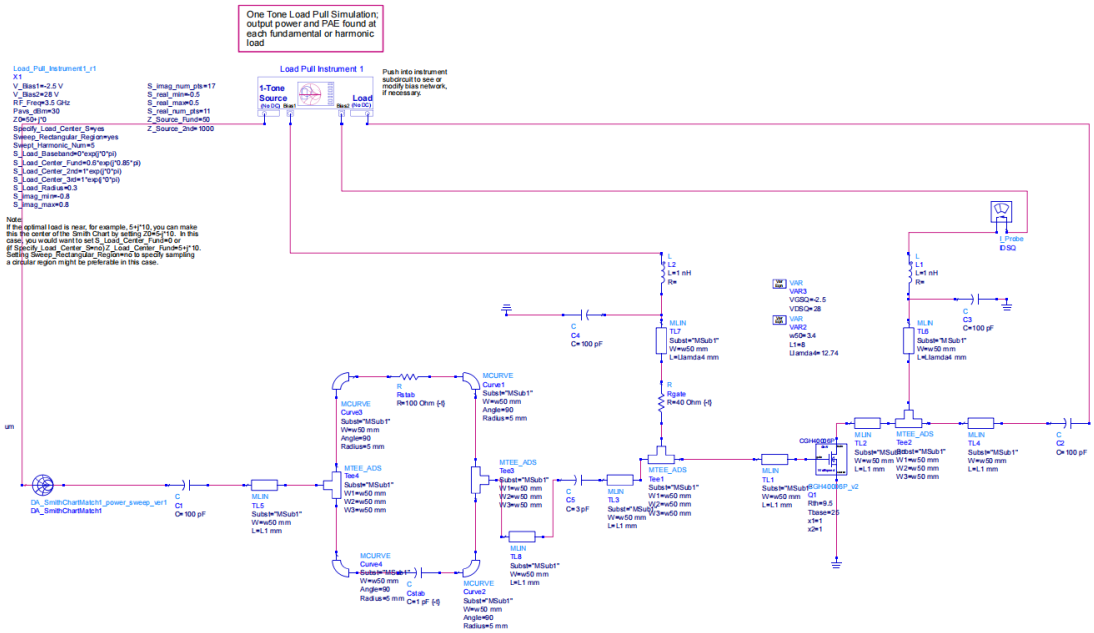

Fig. 37. Circuit for load pull

The testing result is shown in Fig. 38, as shown in the figure, when PAE reaches its maximum, the magnitude of the load is 0.224 and the phase is 25.656, which is close to the result of the power sweep. Also, the simulation plot based on the load pull result is shown in Fig. 39. The PAE is 3 dBm less than the power sweep result, which validates the result from the power sweep since the results are close. The RF PA designing part is finished.

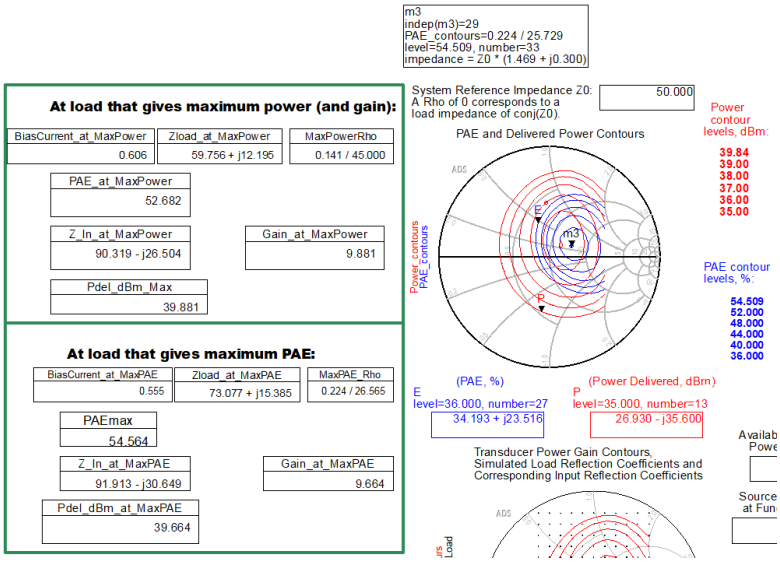

Fig. 38. Result of load pull

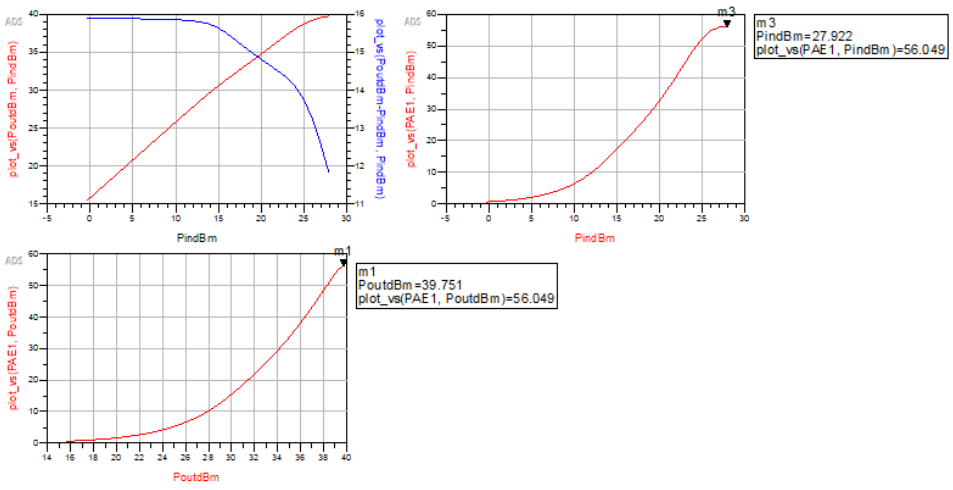

Fig. 39. Plot when phase and magnitude was set to 25.656 degree and 0.224

3.2 ET PS Design

The core idea of envelope tracking is to adjust V_{ds} when the RF input signal varies. A varying drain to source voltage helps the PA maintain high efficiency when input power changes. By sweeping V_{ds}, Fig. 40 was obtained through the sweeping simulation:

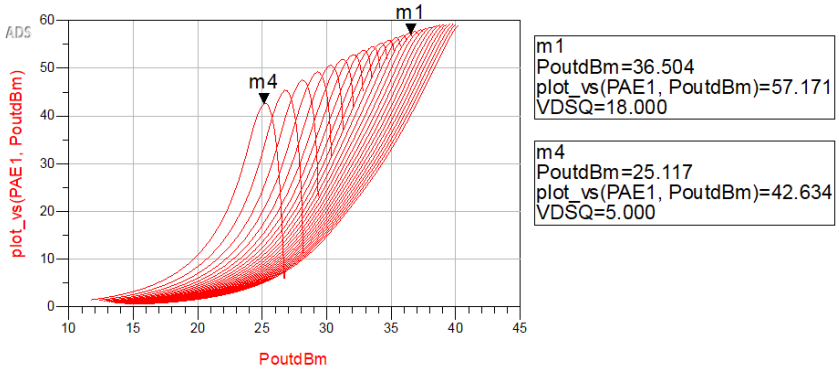

Fig. 40. Pout in dBm versus PAE when sweeping V_{ds}

For a fixed V_{ds}, its efficiency reaches the maximum in a specific input power. However, the efficiency drops dramaticly when it is lower than that power value. Therefore, V_{ds} needs to vary with the fluctuation of the RF input signal power. The ET PS is responsible for tracking the input signal's envelope and adjusting V_{ds} to ensure the high efficiency of the ET PA.

The ET PS design in this project has been divided into three parts: the envelope detector, the comparator and the power returning circuit. The main structure for the comparator was a 3-bit flash convertor. As the circuit shown in Fig. 41, the input port of the flash converter was marked as "xx". As the input voltage increases, the op-amps would be initiated from the bottom to the top. The reference voltage was determined by tuning, ensuring that each op-amp would work in a specific input voltage range. Fig. 42 proves the validity of the circuit as three op-amps work at different thresholds. (*vdsET* is the voltage applied to the FET)

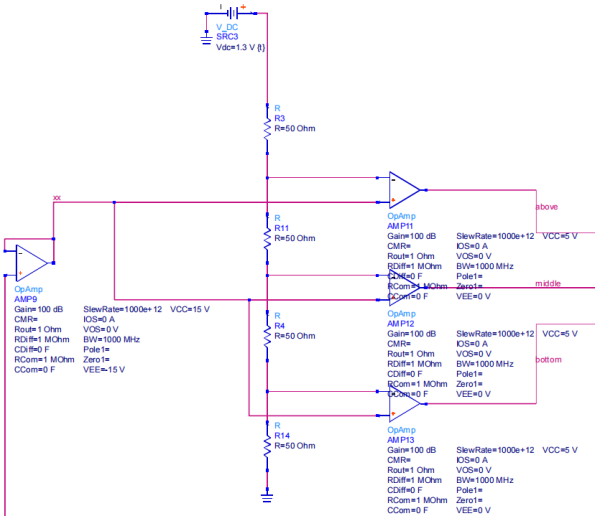

Fig. 41. Flash convertor

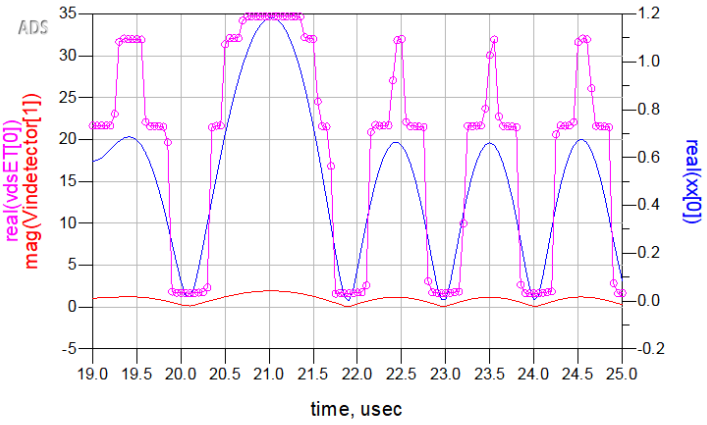

Fig. 42. “Three steps” of the ET PS, DC supply and detected voltage plot

As a sinusoidal wave was injected into the ET PS, three steps were formed corresponding to the input voltage's shape, proving that the three comparators work properly without overlapping.

A summing amplifier, working as the powering returning circuit, was introduced in the ET PS to collect the voltage from the flash converter, as shown in Fig. 43. The gain of the summing amplifier is:

$$A = \frac{V_{out}}{V_{in}} = 1 + \frac{R_f}{R} \tag{7}$$

The gain was set to 7 to avoid saturation when there is less than three input voltage. After summing the voltage, a buffer would send the voltage signal to the drain of the

FET.

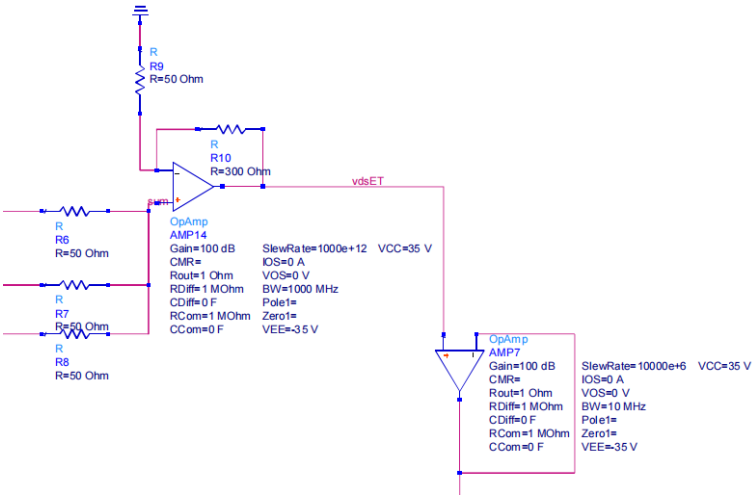

Fig. 43. Summing amplifier with a buffer

To detect the RF input signal and send it into the ET PS, an envelope tracking detector must be added between the comparator and the input port. As shown in Fig. 44, the input power goes into the coupler first, transmitting power to both RF PA (from port 2) and ET PS (from pin 3). The diode (marked by the black rectangle) is used to rectify the RF signal, converting it from an alternating current (AC) waveform to a pulsating direct current (DC) waveform. On the right side of the diode, a low-pass filter (RC filter) was implemented to extract the RF signal after it had been rectified. It also smooths the RF signal and removes the high-frequency noise.

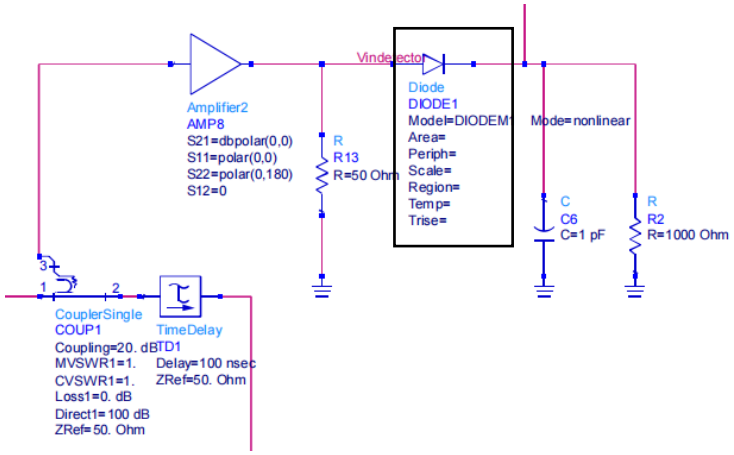

Fig. 44. Envelope tracking detector

For the ET PS simulation analysis, DC-to-RF (Fig. 45) was introduced to measure the efficiency of the circuit since the input power is not in phase with the output power, which invalidates the measurement of PAE.

Fig. 45. DC-to-RF simulation

3.3 IQ Modulator Implementation

The input signal was set in a fixed shape for the previous design and testing. An IQ-modulated signal was introduced into the design to test whether the RF PA is versatile for all types of input signals. To generate an IQ signal that contains information, an IQ modulator was designed in ADS.

To realize the IQ modulator in ADS, the "IQ_Modtuned" component was used for the modulator design. The modulator selects the input harmonic defined by the specified frequency and modulates it according to the I (in-phase) and Q (quadrature) modulation inputs. As Fig. 46 illustrates the symbol of the modulator, the RF carrier is injected into pin1. I data and Q data are injected in pin3 and 4, respectively. The resulting signal is presented in pin2. The finished IQ modulator is shown in Fig. 47.

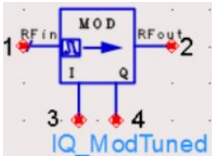

Fig. 46. IQ modulator symbol

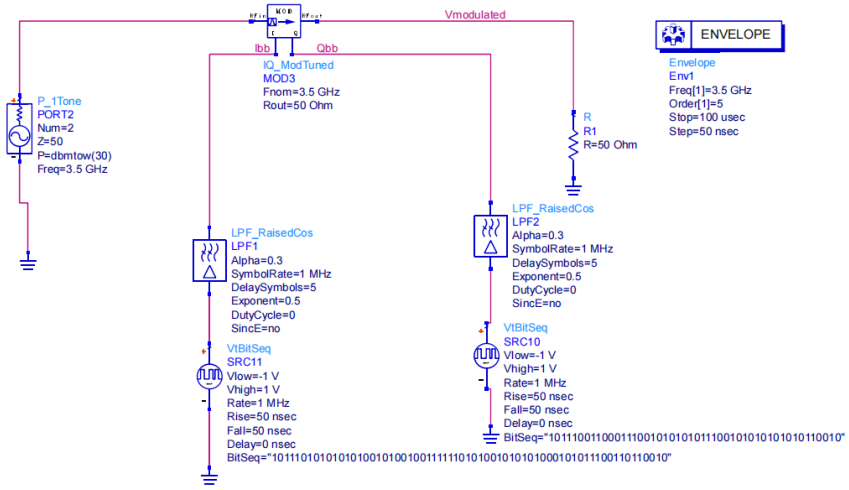

Fig. 47. IQ modulator topology in ADS

The I data and Q data are set randomly. The low pass filter (LPF) between the modulator and the bit sequence generator is selected to filter out high-frequency components to reduce the rate of change of the data signal, making data transmission slower. If the LPFs are deleted, the output of the modulator is shown in Fig. 48.

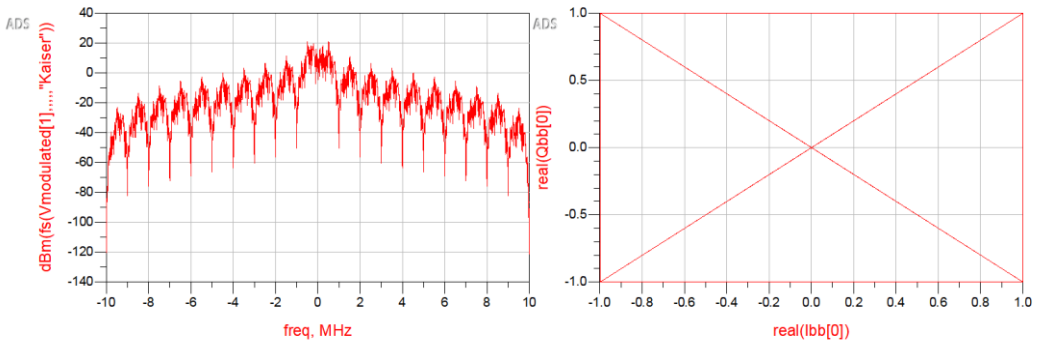

Fig. 48. Modulation result without LPFs

Without the LPFs, the bandwidth of the modulation result is wide and the QPSK cannot work properly since the I and Q data change fast. This is detrimental to information transmission, as it can be observed on the Kaiser window plot (left plot of Fig. 48), since it has poor linearity and cannot modulate expected data. Hence, to remove the influence of high-frequency components, two LPFs were added. Fig. 49 shows the result with the LPFs.

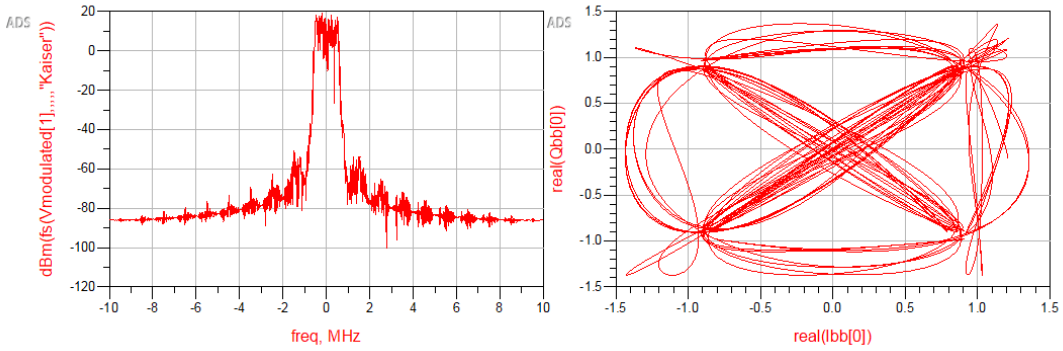

Fig. 49. Modulation result of the IQ modulator with LPFs

The result is much better since the high-frequency components are filtered out in the Kaiser window plot and the QPSK works perfectly.

3.4 Testing and improvement

3.4.1 Circuit testing and solving saturation problem

Now, the overall schematic of the ET PA is finished. Fig. 50 shows the complete picture of the ET PA.

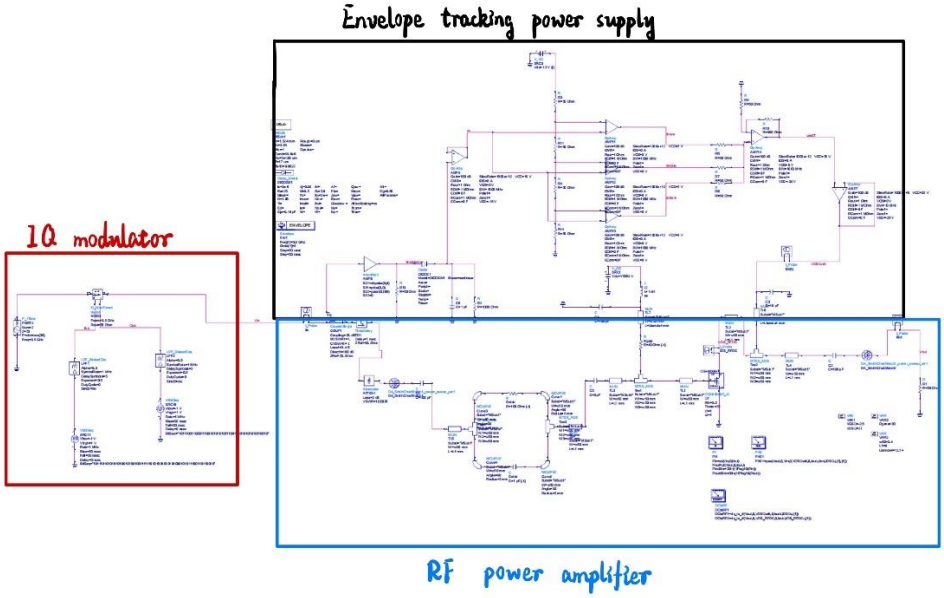

Fig. 50. Full schematic of ET PA

Fig. 51 shows the gain of the ET PA. From the plot, two bumps can be observed at

26dBm and 32dBm. The ET PS generates the boosts by providing the amplifier with three types of DC values (V_{ds}). As a consequence, the gain plot is the superposition of three gain curves.

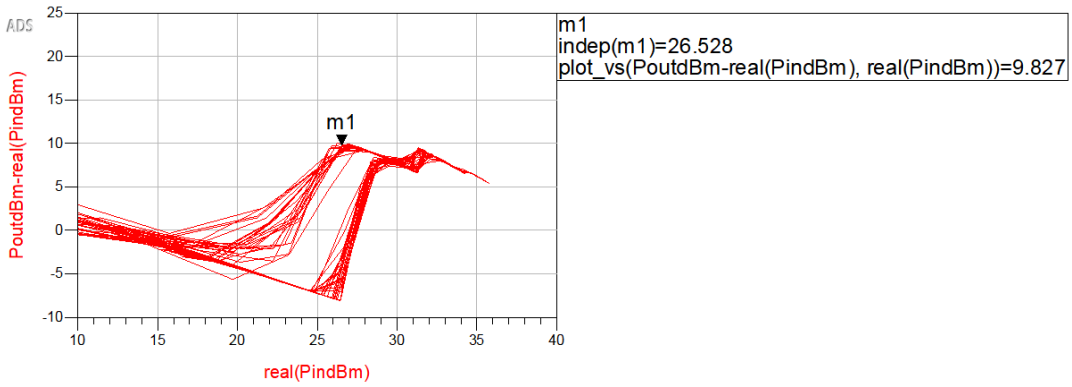

Fig. 51. Gain of the initial ET PA

Table 1 illustrates the parameters which show the performance of the ET PA. From left to right, the parameters represents the average power in the DC path, the input and output ports, and the value drain efficiency, the ratio of the output power to the DC power, the PAE and the gain. The formula for those parameter calculations is shown in Fig. 52.

Table 1. ET PA performance metrics

PdcAVG	PinAVG	PoutAVG	Drain_Eff	PAE	GaindB
11.645	1.261	7.666	65.829	55.004	7.840

Eqn PdcAVG=mean(PDC) Eqn PDC=real(VDS_RFDC[0]).*real(IDS_RFDC.i[0])

Eqn PinAVG=mean(Pin)

Eqn PoutAVG=mean(Pout)

Eqn Drain_Eff=100*PoutAVG/PdcAVG

Eqn PAE=100*(PoutAVG-PinAVG)/PdcAVG

Eqn GaindB=10*log10(PoutAVG/PinAVG)

Fig. 52. Formula for the calculation of parameters in table 1

Fig. 53 shows the output power versus the input power. The plot shows the fault of the

design: when input power (red curve) varies, the output power (blue curve) sometimes saturates and does not change, as the black rectangle indicated in the figure. Improvement towards the ET PS should be introduced to solve the information loss problem caused by power saturation.

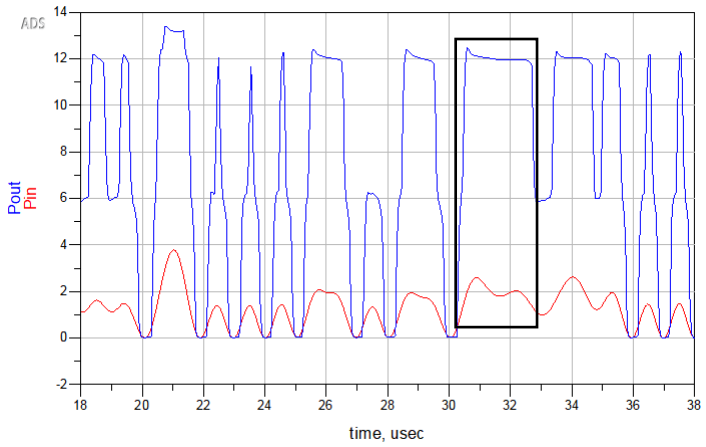

Fig. 53. Output power versus input power (Initial design)

There are two methods for improving the resolution of the ET PS:

1. By adding more comparators, the number of voltage "steps" increases, providing more resolution to solve the saturation problem.
2. Changing the value of resistors, then the sensitivity of the comparator can be changed. To solve the saturation problem, the upper comparators' sensitivity must be adjusted to detect small input voltage fluctuation.

The improved circuit (also the final design) is shown in Fig. 54. As the black rectangle shows, two more comparators were added to the circuit. Moreover, the values of resistors in the reference path were changed, as shown in the green rectangle. The change was introduced because slight fluctuation always occurs around its peak value for the IQ input signal. Therefore, sensitivity towards the envelope power around the peak value needs to be enhanced for the upper comparators, which generate upper steps.

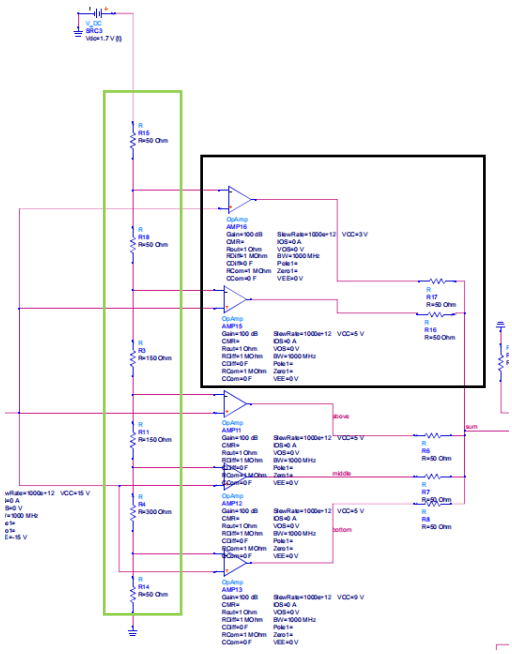

Fig. 54. Improvement on the ET PS

The gain curve is shown in Fig. 55. Compared to the previous gain plot (Fig. 51), the gain dropped but is more stable when the input power is above 22 dBm.

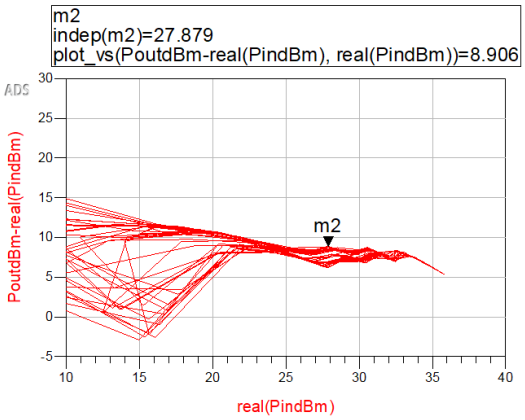

Fig. 55. Gain of the improved ET PA

For the saturation problem, the new design has solved the problem and the result is shown in Fig. 56. As the input power changes, the output power varies simultaneously. The result illustrates that the improvement in the ET PS works and the saturation problem was solved.

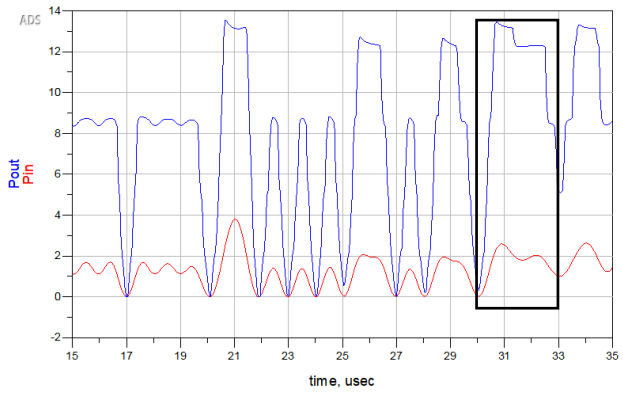

Fig. 56. Output power versus input power (Improved design)

Table 2 illustrates the metrics of the improved ET PA. After adding two more comparators, all the metrics stays at the same level as the previous design.

Table 2. The metrics for the improved ET PA

PdcAVG	PinAVG	PoutAVG	Drain_Eff	PAE	GaindB
11.573	1.264	7.566	65.378	54.459	7.773

Five steps in the vdsET plot can be seen in Fig. 57. This proves the ET PS can operate properly under the new configuration. The supply voltage successfully packed the RF input signal.

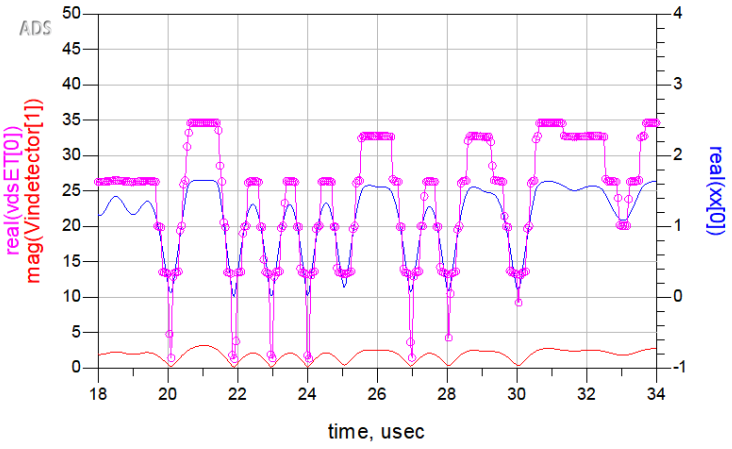

Fig. 57. Five steps of the ET PS

3.4.2 Two-Tone Nonlinear Analysis Using Harmonic Balance

To analysis the linearity of the overall design, the OIP3, which is a measure of the

linearity of an RF device, should be obtained through simulation.

For the system generating harmonic frequencies, one tone input cannot satisfy the demand of intermodulation and IQ modulated signal was too complex for analysis. Hence, a 2-tone port was introduced for generating the harmonic frequency components. Fig. 58 shows the configuration of the port.

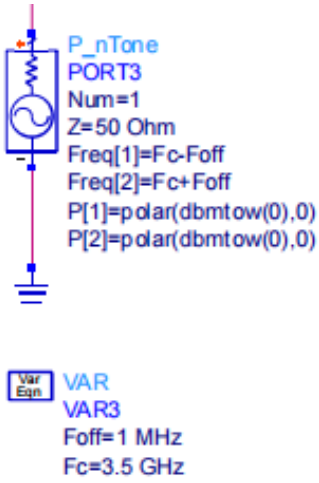

Fig. 58. Configuration of the input port

Two frequency components, one is 3499 MHz and the other is 3501 MHz, can mix with each other and generate intermodulation produces. By setting the Harmonic Balance as shown in Fig. 59. The maximum mixing order was set to 7, which allows more harmonic frequency components to be generated and can be helpful for the result observation.

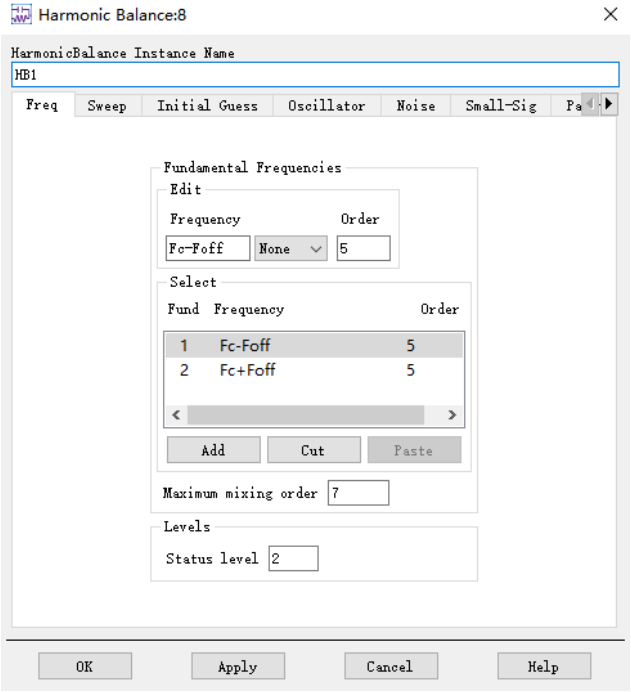

Fig. 59. Harmonic balance configuration window

The simulation result of the input port voltage is shown in Fig. 60. As can be observed, there are a number of tones, and their intermodulation products are closely spaced that only multiple arrays can be seen.

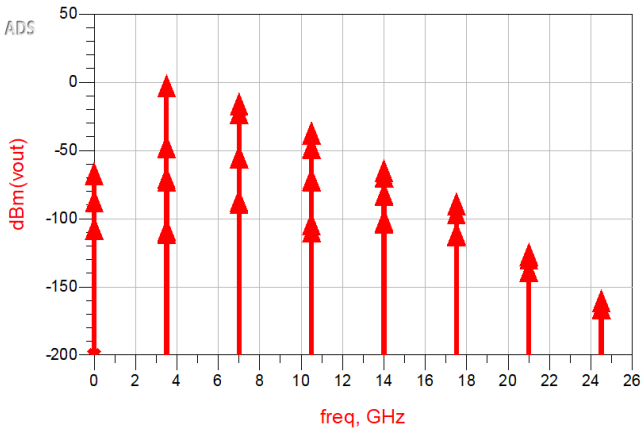

Fig. 60. V_{out} plot spectrum

The zoomed graph is shown in Fig. 61. As the fundamental frequency was zoomed, a clearer view of the harmonic products could be observed. The marker “m3” and “m4” point out the fundamental tones and the products around them are the IMD products. The marker “m1” and “m2” shows the third order product.

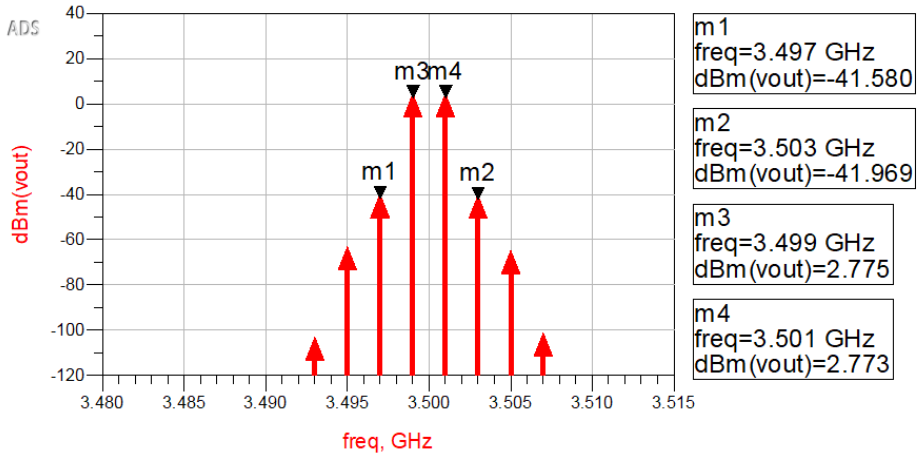

Fig. 61. Zoomed V_{out} plot

To obtain the OIP3 values, the "IP3out" was used for simulation and the configuration is shown in Fig. 62. Aside from the OIP3, IIP3 is also measured. Because there are two sides of tones: the lower side tone and the upper side tone. To test the values of both tones, the parameter marked by a red rectangle measures the upper side tone when it is {0,1} and {1,0} for the lower side tone.

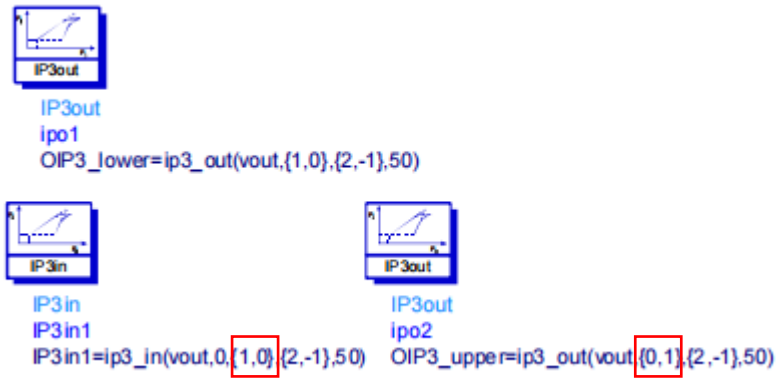

Fig. 62. Configuration of the "IP3out" and "IP3in"

The simulation result, with IIP2 calculated, is shown in Fig. 63. The OIP3 is around 25 dBm, IIP3 is around 25 dBm and IIP2 is much higher, which is approximately 47 dBm. The simulation is correct since IIP2 is much bigger than IIP3.

Eqn IPn=ipn(vout,0,Iout.i,{1,0},{2,-1},2)

OIP3_upper	OIP3_lower	IP3in1	IPn
24.949	24.953	24.953	47.131

Fig. 63. OIP3, IIP3 and IIP2 simulation result in dBm

An OIP3 of 25 dBm suggests that the amplifier has moderate linearity, and its intermodulation distortion performance may be limited. This problem could potentially affect the amplifier's ability to handle complex signals, especially in communication systems where multiple signals are present and high linearity is required.

CHAPTER 4. CONCLUSION

In this project, a 3.5 GHz, high-performance envelope tracking power amplifier is designed and tested under the IQ-modulated signal. The ET PA can achieve a high **power added efficiency (54.5%)** and **high DC-to-RF efficiency (65%).** The gain **reaches and settles in 9 dB** (after P_{in}> 20 dBm), which is considered suitable for the PA design. In most PA designs, the gain is usually less than 10 dB to ensure stability [34]. Therefore, the ET PA design can be applied in various scenarios since it has a reasonable gain. Besides, the linearity **(OIP3 = 25dBm)** of the ET PA is considered sufficient for wireless communication systems and audio applications [35]. It is not exceptionally high but can tolerate some level of distortion.

However, the limitations of the design exist in two aspects: the ET PA matching networks and the ET PS schematic.

Firstly, the matching networks of the PA are hard to design and can be problematic since the HEMT is a nonlinear device. As the supply voltage changes, the impedance also varies. Thus, the matching networks designed under a fixed supply voltage might limit the performance of the ET PA. The practical solutions for the matching network problem are listed below:

- Adaptive matching networks: Implement adaptive or tunable matching networks that can dynamically adjust their impedance based on the changing load conditions. This can be achieved using varactor diodes, tunable capacitors, or Micro-Electro-Mechanical Systems (MEMS) switches [36]. Adaptive matching networks can help maintain optimal performance across various operating conditions and supply voltages.
- Wideband matching techniques: Utilize wideband matching techniques to provide optimal impedance matching over a broader frequency range. Techniques such as multi-section impedance transformers [37], tapered lines [38], and the use of broadband matching networks [39] like the Lumped Element (LE) and Distributed

Element (DE) networks [40] can help improve performance across multiple frequency bands.

- Load-pull analysis [41]: Perform load-pull analysis during the design phase to find the optimal load impedance for the ET PA under different conditions. This analysis can help identify the best impedance matching strategy to maximize efficiency and linearity across various operating points [42].

Secondly, the schematic of the ET PS has a problem with the number of comparators. Five comparators were involved in the IQ-modulated signal testing and could perform properly. However, five comparators might be insufficient for a more sophisticated RF input signal since more steps might be needed.

Future work focuses on improving the matching networks of the ET PA and deploying a more versatile schematic of the ET PS. The load-pull analysis can be implemented for the matching network design since this is the easiest way to improve efficiency.

For the schematic of ET PS, more structures can be implemented to enhance the versatility of the design. For example, digital control [43], which enables advanced modulation, can be introduced to improve the performance of envelope tracking and the power supply's efficiency.

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APPENDIX

Appendix A. Recordings of meetings

B30UB 4th Year Project (Semester 1)

Final-Year Project

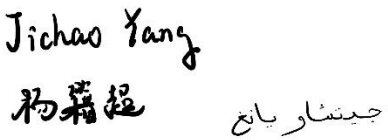
Minutes of Meeting 1 of Supervisor Meeting – DATE 14-9-2022

Present in meeting: Jichao Yang, Selina(Xinqi) Huang, Tong Wu, Minkang Feng, Dr. Souheil Ben Smida.

Location: Online meeting (Microsoft Teams)

Minutes taken by: Jichao Yang

No.	ITEM	ACTION
1.	Introduction to the fourth-year project	Dr. BenSmida presented the related background knowledge, goal and agenda of the fourth-year project. He illustrated the mechanism of the RF PA through PowerPoint handwriting.
2.	Software preparation and license application	Dr. BenSmida mentioned the software being used in this project. The Advanced Design System (ADS) from Keysight. He asked all the students to apply for a student license and showed how to apply on its official website.
3.	Tasks to complete by the next meeting	Dr. BenSmida introduced three PAs, which were Envelope tracking PAs, Doherty PAs and Out-phasing PAs. He taught all the students how to use IEEE Xplore to search for the newest publication

		about the three PAs.
4.	Date of Next Meeting: 21-9-2022 Time: 1:00 PM Location: Online meeting (Microsoft Teams) Minute Taker: Jichao Yang	Signature of Student:  Signature of Supervisor: 

B30UB 4th Year Project (Semester 1)

Final-Year Project

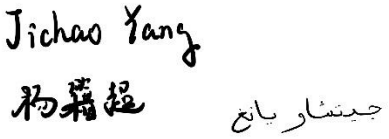
Minutes of Meeting 2 of Supervisor Meeting – DATE 21-9-2022

Present in meeting: Jichao Yang, Selina(Xinqi) Huang, Tong Wu, Minkang Feng, Ruining Sun, Dr. Souheil Ben Smida.

Location: Online meeting (Microsoft Teams)

Minutes taken by: Jichao Yang

No.	ITEM	ACTION
1.	Instrument selection and parameter selection in ADS	Dr. BenSmida introduced a website called website called Wolfspeed (https://www.wolfspeed.com/). He selected a transistor (CGH40006P) and installed the library in the ADS. The biased point was selected after the test through the DC-IV

		curve.
2.	Circuit project building and parameter improvement.	Dr. BenSmida built the RF PA circuit. He tested the amplifier's Mu (Stability), S-parameter and Maxgain. He used tuning in the simulation and introduced the procedures for improving the circuit.
3.	Tasks to complete by the next meeting	Dr. BenSmida sent us the library that includes the FET used in this stage. He asked us to unzip the library and adjust the project, using different biased points and frequencies to design an input and output matching network.
4.	Date of Next Meeting: 28-9-2022 Time: 1:00 PM Location: Online meeting (Microsoft Teams) Minute Taker: Jichao Yang	Signature of Student:  Signature of Supervisor: 

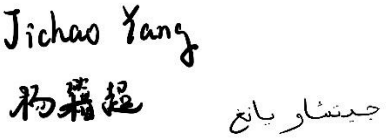
Minutes of Meeting 3 of Supervisor Meeting – DATE 28-9-2022

Present in meeting: Jichao Yang, Selina(Xinqi) Huang, Ruining Sun, Dr. Souheil Ben Smida.

Location: Online meeting (Microsoft Teams)

Minutes taken by: Jichao Yang

No.	ITEM	ACTION
1.	Update on the work done until this meeting	Dr. BenSmida asked the attendees to demonstrate their screens for the input matching and output matching network. Jichao showed his screen and Dr. BenSmida checked his design and asked Jichao how the circuit was matched.
2.	Power monitoring for the circuit	Dr. BenSmida used the PA from the last meeting and detected its functionality. He deleted the simulation parameters and added Pt to see the gain of power through simulation.
3.	Tasks to complete by the next meeting	Dr. BenSmida asked Jichao to make the circuit an input matching network and evaluate its gain. There are only three people attended the meeting and only Jichao responded. So the meeting for this week ended fast.

4	Discussion about the project scope	Jichao asked Prof. BenSmida about relevant materials for the project. Prof. BenSmida said there is no need to learn extra and adequately fulfilling the simulation is the key for the current stage.
5.	Date of Next Meeting: 05-10-2022 Time: 1:00 PM Location: Online meeting (Microsoft Teams) Minute Taker: Jichao Yang	Signature of Student:  Signature of Supervisor: 

B30UB 4th Year Project (Semester 1)

Final-Year Project

Minutes of Meeting 4 of Supervisor Meeting – DATE 5-10-2022

Present in meeting: Jichao Yang, Selina(Xinqi) Huang, Ruining Sun, Tong Wu, Minkang Feng, Prof. Souheil Ben Smida.

Location: Online meeting (Microsoft Teams)

Minutes taken by: Jichao Yang

No.	ITEM	ACTION
1.	Update on the work done until this meeting	Jichao shared his screen and Prof. BenSmida checked his circuit. There had no problem in the circuit so far.

2.	Power sweep for the circuit	In order to find the maximum PAE, Prof. BenSmida added two “parameter sweep” to sweep the PhaseLoad and MagnitudeLoad at the output. The desire parameters were obtained in the simulation.
3.	Input and output matching network building	Prof. BenSmida created two sub-circuits, which were input matching network and output matching network. By using the “Smith chart” in the tools bar, the matching network worked perfectly, with 50-ohm input and output characteristic impedance.
4	Tasks to complete by the next meeting	Prof. BenSmida asked all attendees to build and add the matching network into their design. Plus, the network needs to be constructed by MLIN and TEE, instead of capacitor and inductor.
5.	Date of Next Meeting: 12-10-2022 Time: 1:00 PM Location: Online meeting (Microsoft Teams) Minute Taker: Jichao Yang	Signature of Student: Jichao Yang 杨霁超 جيتشاو يانغ Signature of Supervisor:

B30UB 4th Year Project (Semester 1)

Final-Year Project

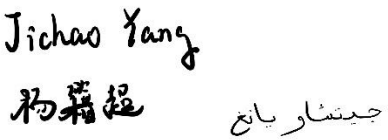
Minutes of Meeting 5 of Supervisor Meeting – DATE 12-10-2022

Present in meeting: Jichao Yang, Selina(Xinqi) Huang, Ruining Sun, Prof. Souheil Ben Smida.

Location: Online meeting (Microsoft Teams)

Minutes taken by: Jichao Yang

No.	ITEM	ACTION
1.	Update on the work done until this meeting	Selina(Xinqi) and Jichao shared their screens and Prof. BenSmida examined their works. Selina(Xinqi) presented her idea of how she built this circuit, from dc-iv to load pull.
2.	Questions within the design	Prof. BenSmida pointed out the problems within each design: Selina(Xinqi) need to do the power sweep before the load pull. All the other part of her design was brilliant. Jichao need to fulfill the load pull. And he had done the previous steps okay.
3	Project guidance	Jichao asked Prof. BenSmida how to make the matching network work properly when TEE is connected. Prof. BenSmida helped Jichao to sweep the parameter (length) of the MLIN to achieve the matching result.

4	Discussion about the project scope	Selina(Xinqi) asked Prof. BenSmida the plan of week 6. And Prof. BenSmida informed us that we need to demonstrate a presentation on what we did in the previous six weeks.
5.	Date of Next Meeting: 19-10-2022 Time: 1:00 PM Location: Online meeting (Microsoft Teams) Minute Taker: Jichao Yang	Signature of Student:  Signature of Supervisor: 

B30UB 4th Year Project (Semester 1)

Final-Year Project

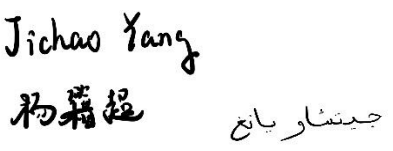
Minutes of Meeting 6 of Supervisor Meeting – DATE 09-11-2022

Present in meeting: Jichao Yang, Prof. Souheil Ben Smida.

Location: Online meeting (Microsoft Teams)

Minutes taken by: Jichao Yang

No.	ITEM	ACTION
1.	Discuss the content of the PowerPoint	Jichao asked Prof. BenSmida to view his presentation PowerPoint. Prof. BenSmida gave instructions and improvements on the content of the PPT.

2.	Issue encountered in ADS simulation related to the implementation of the ET PA	Jichao illustrated his problem that he couldn't obtain the correct waveform in the sweep simulation. Prof. BenSmida helped him by changing the parameter and issue solved.
3.	Ask other students to join the meeting	Jichao asked other students to join the meeting and both Jichao and Prof. BenSmida waited for a while.
4	Discussion about the implementation of the ET PA.	Jichao asked Prof. BenSmida about the next step of designing the ET PA. Prof. BenSmida advised Jichao to research papers about how to implement ETPS (Envelope tracking power supply circuit). Two methods were mentioned: Switching-mode supply and low efficiency opamp.
5.	Date of Next Meeting: 09-11-2022 Time: 1:00 PM Location: Online meeting (Microsoft Teams) Minute Taker: Jichao Yang	Signature of Student:  Signature of Supervisor: 

B30UB 4th Year Project (Semester 1)

Final-Year Project

Minutes of Meeting 6 of Supervisor Meeting – DATE 09-11-2022

Present in meeting: Jichao Yang, Prof. Souheil Ben Smida.

Location: Online meeting (Microsoft Teams)

Minutes taken by: Jichao Yang

No.	ITEM	ACTION
1.	Discuss the content of the PowerPoint	Jichao asked Prof. BenSmida to view his presentation PowerPoint. Prof. BenSmida gave instructions and improvements on the content of the PPT.
2.	Issue encountered in ADS simulation related to the implementation of the ET PA	Jichao illustrated his problem that he couldn't obtain the correct waveform in the sweep simulation. Prof. BenSmida helped him by changing the parameter and issue solved.
3.	Ask other students to join the meeting	Jichao asked other students to join the meeting and both Jichao and Prof. BenSmida waited for a while.
4	Discussion about the implementation of the ET PA.	Jichao asked Prof. BenSmida about the next step of designing the ET PA. Prof. BenSmida advised Jichao to research papers about how to implement ETPS (Envelope tracking power supply circuit). Two methods were mentioned:

		Switching-mode supply and low efficiency opamp.
5.	Date of Next Meeting: 09-11-2022 Time: 1:00 PM Location: Online meeting (Microsoft Teams) Minute Taker: Jichao Yang	Signature of Student:  Signature of Supervisor: 

B30UC 4th Year Project (Semester 2)

Final-Year Project

Minutes of Meeting 1 of Supervisor Meeting – DATE 19-1-2023

Present in meeting: Jichao Yang, Selina(Xinqi) Huang, Ruining Sun, Tong Wu, Dr. Souheil Ben Smida.

Location: Online meeting (Microsoft Teams)

Minutes taken by: Jichao Yang

No.	ITEM	ACTION
1.	Update the work in winter holiday	Jichao and Selina(Xinqi) reported the work done during the winter vacation. Jichao designed the prototype of the power supply system.
2.	Comments and improvement on the circuit	Dr. BenSmida told Jichao that all the circuits should be implemented in ADS

		instead of LTspice. He also introduced the improvement in the circuit and the overall design schematic.
3.	Tasks to complete by the next meeting	Dr. BenSmida asked Jichao to apply a summing amplifier for the design and use ADC DAC to fulfill the circuit function.
4.	Date of Next Meeting: 19-01-2023 Time: 1:00 PM Location: Online meeting (Microsoft Teams) Minute Taker: Jichao Yang	Signature of Student: Jichao Yang 杨霁超 جيتشاو يانغ Signature of Supervisor: Souheil Ben Smida

B30UC 4th Year Project (Semester 2)

Final-Year Project

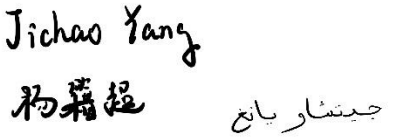
Minutes of Meeting 2 of Supervisor Meeting – DATE 27-1-2023

Present in meeting: Jichao Yang, Selina(Xinqi) Huang, Dr. Souheil Ben Smida.

Location: EM2.27 and Online

Minutes taken by: Jichao Yang

No.	ITEM	ACTION
1.	Update on the work done until this meeting	Jichao showed his work in Dr. BenSmida's office. The summing amplifier was

		designed but the overall schematic has not been done yet.
2.	Schematic discussion	Dr. BenSmida discussed the overall structure of the circuit and let Jichao implement the circuit through ADS in his office.
3.	Simulation and improvement on the circuit	After Jichao implemented the circuit in ADS, Dr. BenSmida helped Jichao to simulate the circuit and point out the parameters that need to adjust.
4.	Assign the work to be done before next meeting	Dr. BenSmida told Jichao about several parameters and options in the simulation that need to be adjusted. Jichao needs to obtain the expected simulation result before the next meeting.
5.	Date of Next Meeting: 27-1-2023 Time: 1:30 PM Location: EM2.27 Minute Taker: Jichao Yang	Signature of Student:  Signature of Supervisor: 

B30UC 4th Year Project (Semester 2)

Final-Year Project

Minutes of Meeting 3 of Supervisor Meeting – DATE 3-2-2023

Present in meeting: Jichao Yang, Selina(Xinqi) Huang, Dr. Souheil Ben Smida.

Location: EM2.27

Minutes taken by: Jichao Yang

No.	ITEM	ACTION
1.	Update on the work done until this meeting	Jichao showed his work in Dr. BenSmida's office. The overall structure of the ET PA have done but the waveform of the power supply needs to be modified
2.	Simulation and improvement on the circuit	Dr. BenSmida found the simulation error in the ET PA. He corrected the error and tested the circuit on ADS.
3.	Assign the work to be done before next meeting	After improving the performance of the amplifier, Dr. BenSmida asked Jichao to adjust the supply voltage in order to achieve the "steps"(envelope).
4.	Date of Next Meeting: 3-2-2023 Time: 1:30 PM Location: EM2.27 Minute Taker: Jichao Yang	Signature of Student: Jichao Yang 杨骥超 جيتشاو يانغ Signature of Supervisor:

B30UC 4th Year Project (Semester 2)

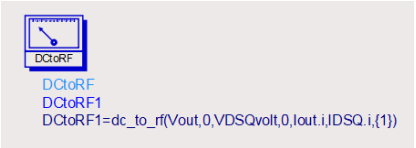
Final-Year Project

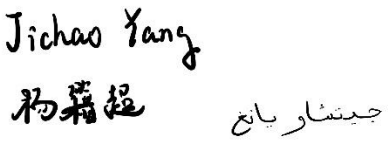
Minutes of Meeting 4 of Supervisor Meeting – DATE 10-2-2023

Present in meeting: Jichao Yang, Selina(Xinqi) Huang, Dr. Souheil Ben Smida.

Location: EM2.27

Minutes taken by: Jichao Yang

No.	ITEM	ACTION
1.	Update on the work done until this meeting	Jichao showed the supply voltage he adjusted. The waveform of the power supply is decent.
2.	Simulation and improvement on the circuit	Dr. BenSmida adjusted the gain in the summing amplifier. Also, the DC-to-RF simulation method replaced the PAE since the input and the output are not in phase. 
3.	Assign the work to be done before next meeting	Although the supply voltage met the standard, the overall efficiency is not ideal and Jichao needs to figure it out before the next meeting.

4.	Date of Next Meeting: 10-2-2023 Time: 1:30 PM Location: EM2.27 Minute Taker: Jichao Yang	Signature of Student:  Signature of Supervisor: 

B30UC 4th Year Project (Semester 2)

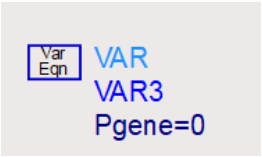
Final-Year Project

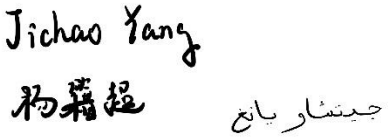
Minutes of Meeting 5 of Supervisor Meeting – DATE 23-2-2023

Present in meeting: Jichao Yang, Dr. Souheil Ben Smida.

Location: EM2.27

Minutes taken by: Jichao Yang

No.	ITEM	ACTION
1.	Update on the work done until this meeting	After trying several methods to detect the efficiency, the voltage is still unideal and Jichao asked Prof. BenSmida for a solution.
2.	Detecting bugs of the circuit	The power of the generator was zero. The bug is fixed. 

3.	Assign the work to be done before next meeting	Prof. BenSmida asked Jichao to design an IQ modulator through Matlab (Simulink).
4.	Date of Next Meeting: 24-2-2023 Time: 1:30 PM Location: EM2.27 Minute Taker: Jichao Yang	Signature of Student:  Signature of Supervisor: 

B30UC 4th Year Project (Semester 2)

Final-Year Project

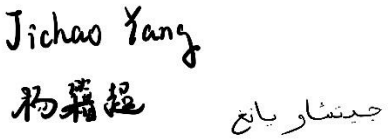
Minutes of Meeting 6 of Supervisor Meeting – DATE 3-3-2023

Present in meeting: Jichao Yang, Selina(Xinqi) Huang, Dr. Souheil Ben Smida.

Location: EM2.27

Minutes taken by: Jichao Yang

No.	ITEM	ACTION
1.	Update on the work done until this meeting	Jichao accomplished the IQ modulator design through Simulink. He showed his work to Prof. BenSmida and Professor will then build the modulator in ADS.
2.	Simulation and improvement on the circuit	Prof. BenSmida tried to build an IQ modulator in ADS, but the modulator needs

		a “modfile()” to generate the modulated RF signal.
3.	Assign the work to be done before next meeting	Prof. BenSmida asked Jichao to write a modfile or use the IQ modulator in ADS to generate the input signal.
4.	Date of Next Meeting: 3-3-2023 Time: 1:30 PM Location: EM2.27 Minute Taker: Jichao Yang	Signature of Student:  Signature of Supervisor: 

B30UC 4th Year Project (Semester 2)

Final-Year Project

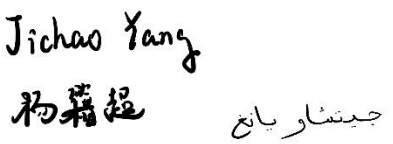
Minutes of Meeting 7 of Supervisor Meeting – DATE 10-3-2023

Present in meeting: Jichao Yang, Selina(Xinqi) Huang, Minkang Feng, Dr. Souheil Ben Smida.

Location: EM2.27

Minutes taken by: Jichao Yang

No.	ITEM	ACTION
1.	Update on the work done until this meeting	Jichao wrote a “modfile()” in txt. file, which can generate the IQ signal in matlab.

2.	Simulation and improvement on the circuit	Prof. BenSmida used another method to generate the IQ signal, by applying the "IQ_ModTune". In the end, the power amplifier can work decently with the input IQ signal.
3.	Assign the work to be done before next meeting	The project is done. Now Jichao needs to start writing the project report.
4.	Date of Next Meeting: 10-3-2023 Time: 1:30 PM Location: EM2.27 Minute Taker: Jichao Yang	Signature of Student:  Signature of Supervisor: 

Appendix B. Overall schematic of the final ET PA design

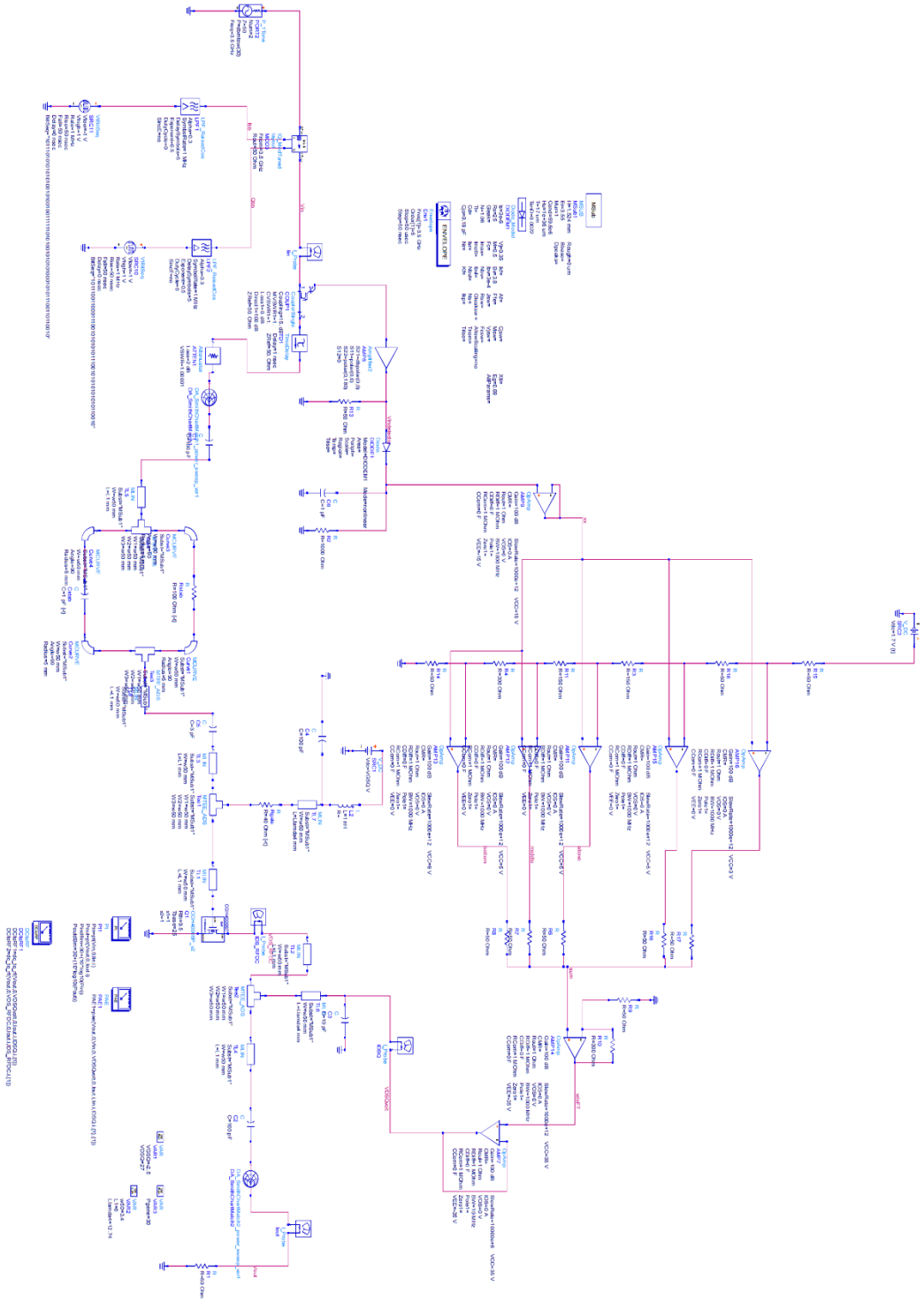


Fig. 64. Overall schematic of the final ET PA design

Appendix C. CGH40006P datasheet [23]

CGH40006P

6 W, RF Power GaN HEMT

Package Type: 440109
PN: CGH40006P

Description

Wolfspeed's CGH40006P is an unmatched, gallium nitride (GaN) high electron mobility transistor (HEMT). The CGH40006P, operating from a 28 volt rail, offers a general purpose, broadband solution to a variety of RF and microwave applications. GaN HEMTs offer high efficiency, high gain and wide bandwidth capabilities making the CGH40006P ideal for linear and compressed amplifier circuits. The transistor is available in a solder-down, pill package.

Features

- Up to 6 GHz Operation
- 13 dB Small Signal Gain at 2.0 GHz
- 11 dB Small Signal Gain at 6.0 GHz
- 8 W typical at P_{IN} = 32 dBm
- 28 V Operation

Applications

- 2-Way Private Radio
- Broadband Amplifiers
- Cellular Infrastructure
- Test Instrumentation
- Class A, AB, amplifiers suitable for OFDM, W-CDMA, EDGE, CDMA waveforms

Absolute Maximum Ratings (not simultaneous) at 25°C Case Temperature

Parameter	Symbol	Rating	Units	Conditions
Drain-Source Voltage	V_{DSS}	120	V	25°C
Gate-to-Source Voltage	V_{GS}	-10, +2		
Storage Temperature	T_{STG}	-65, +150	°C	
Operating Junction Temperature	T_J	225		
Maximum Forward Gate Current	I_{GMAX}	2.1	mA	25°C
Maximum Drain Current[1]	I_{DMAX}	0.75	A	
Soldering Temperature[2]	T_S	245	°C	
Thermal Resistance, Junction to Case[3]	$R_{\theta JC}$	9.5	°C/W	85°C
Case Operating Temperature[3]	T_C	-40, +150	°C	

Notes:
[1] Current limit for long term, reliable operation
[2] Refer to the Application Note on soldering at wolfspeed.com/rf/document-library
[3] Measured for the CGH40006P at P_{DISS} = 8 W.

Electrical Characteristics (T_C = 25°C)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Characteristics[1]						
Gate Threshold Voltage	$V_{GS(th)}$	-3.8	-3.0	-2.3	V_{DC}	V_{DS} = 10 V, I_D = 2.1 mA
Gate Quiescent Voltage	$V_{GS(Q)}$	–	-2.7	–		V_{DS} = 28 V, I_D = 100 mA
Saturated Drain Current	I_{DS}	1.5	2.1	–	A	V_{DS} = 6.0 V, V_{GS} = 2.0 V
Drain-Source Breakdown Voltage	V_{BR}	84	–	–	V_{DC}	V_{GS} = -8 V, I_D = 2.1 mA
RF Characteristics[2] (T_C = 25°C, F_0 = 2.0 GHz unless otherwise noted)						
Small Signal Gain	G_{SS}	11.5	13	–	dB	V_{DD} = 28 V, I_{DQ} = 100 mA
Power Output at P_{IN} = 32 dBm	P_{OUT}	7.0	9	–	W	
Drain Efficiency[3]	η	53	65	–	%	V_{DD} = 28 V, I_{DQ} = 100 mA, P_{IN} = 32 dBm
Output Mismatch Stress	VSWR	–	–	10:1	Ψ	No damage at all phase angles, V_{DD} = 28 V, I_{DQ} = 100 mA, P_{IN} = 32 dBm
Dynamic Characteristics						
Input Capacitance	C_{GS}	–	3.0	–	pF	V_{DS} = 28 V, V_{GS} = -8 V, f = 1 MHz
Output Capacitance	C_{DS}	–	1.1	–		
Feedback Capacitance	C_{GD}	–	0.1	–		

Notes:
[1] Measured on wafer prior to packaging.
[2] Measured in the CGH40006P-AMP
[3] Drain Efficiency = P_{OUT} / P_{DC}

Appendix D. Gantt chart

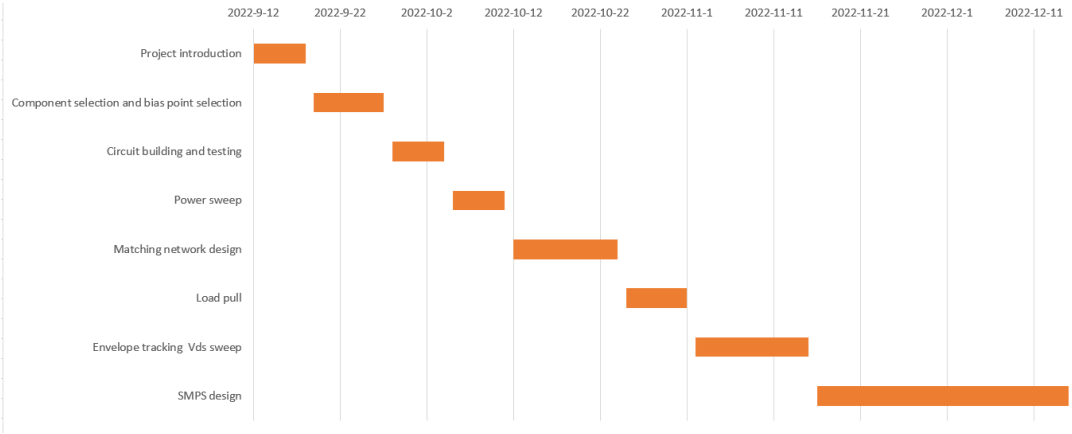


Fig. 65. Gantt chart of first semester (B30UB)

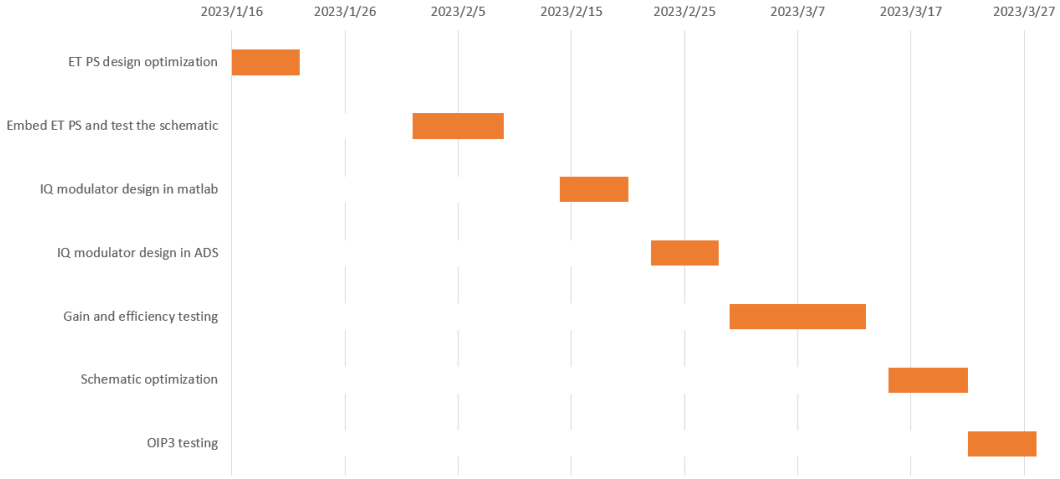


Fig. 66. Gantt chart of second semester (B30UC)