2024 Digital IC Design
Homework 3: matrix multiplier

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Simulation Result

Functional simulation	100	Gate-level simulation	100	Clock width	20 (ns)	Gate-level simulation time	110040 (ns)

pre-sim result of test patterns

```
#  4:Pattern        1038 is PASS !
#  4:Pattern        1039 is PASS !
#  4:Pattern        1040 is PASS !
#  4:Pattern        1041 is PASS !
#  1:Pattern        1042 is PASS !
#  1:Pattern        1043 is PASS !
#  6:Pattern        1044 is PASS !
#  4:Pattern        1045 is PASS !
#  6:Pattern        1046 is PASS !
#  4:Pattern        1047 is PASS !
#  1:Pattern        1048 is PASS !
#  6:Pattern        1049 is PASS !
#  6:Pattern        1050 is PASS !
#  4:Pattern        1051 is PASS !
#  6:Pattern        1052 is PASS !
#  6:Pattern        1053 is PASS !
#  4:Pattern        1054 is PASS !
#  1:Pattern        1055 is PASS !
#  1:Pattern        1056 is PASS !
# Pattern 3 pass
# ---------------------------- Simulation FINISH !!----------------------------
# score =         100/100
# ================================================================================
#
#  \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!
#
# ================================================================================
```

post-sim result of test patterns

```
#  6:Pattern        1037 is PASS !
#  4:Pattern        1038 is PASS !
#  4:Pattern        1039 is PASS !
#  4:Pattern        1040 is PASS !
#  4:Pattern        1041 is PASS !
#  1:Pattern        1042 is PASS !
#  1:Pattern        1043 is PASS !
#  6:Pattern        1044 is PASS !
#  4:Pattern        1045 is PASS !
#  6:Pattern        1046 is PASS !
#  4:Pattern        1047 is PASS !
#  1:Pattern        1048 is PASS !
#  6:Pattern        1049 is PASS !
#  6:Pattern        1050 is PASS !
#  4:Pattern        1051 is PASS !
#  6:Pattern        1052 is PASS !
#  6:Pattern        1053 is PASS !
#  4:Pattern        1054 is PASS !
#  1:Pattern        1055 is PASS !
#  1:Pattern        1056 is PASS !
# Pattern 3 pass
# ---------------------------- Simulation FINISH !!----------------------------
# score =         100/100
# ================================================================================
#
#  \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!
#
# ================================================================================
# ** Note: $stop    : D:/DIC/HW3/SYN/testfixture.v(351)
#    Time: 110040 ns  Iteration: 0  Instance: /testfixture1
```

Synthesis Result

Total logic elements	318
Total memory bit	0
Embedded multiplier 9-bit element	1

your flow summary

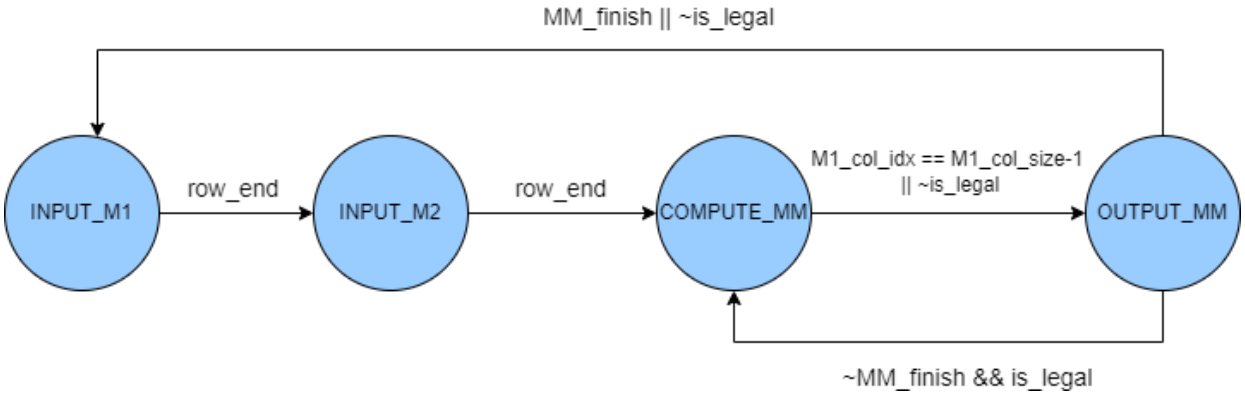
Flow Status	Successful - Thu May 02 16:26:11 2024
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	MM
Top-level Entity Name	MM
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	318 / 55,856 (< 1 %)
Total registers	190
Total pins	36 / 325 (11 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	1 / 308 (< 1 %)
Total PLLs	0 / 4 (0 %)

Description of your design

本設計目的為實現矩陣乘法，由四個模組組成: MM、Controller、Matrix_Reg、Mul_Adder。

1. MM
   Top module，負責子模組接線，包含 Controller、Matrix_Reg、Mul_Adder 三個子模組。

2. Controller
   由狀態機組成，控制 valid、is_legal、change_row、busy 四個輸出訊號，並計算輸入矩陣的 column size 和 row size，以及控制矩陣 1 和矩陣 2 暫存器的 write enable 訊號。狀態機主要分成 **INPUT_M1**、**INPUT_M2**、**COMPUTE_MM**、**OUTPUT_MM** 四個狀態:
   INPUT_M1: 矩陣 1 的暫存器可以記錄矩陣每個元素的值。
   INPUT_M2: 矩陣 2 的暫存器可以記錄矩陣每個元素的值。
   COMPUTE_MM: 開始進行矩陣乘法。
   OUTPUT_MM: 輸出矩陣乘法結果的元素。



   以下為 valid、is_legal、change_row、busy 訊號拉起為 1 的條件:
   valid: 狀態等於 **OUTPUT_MM**。
   is_legal: 矩陣 1 的 column size 等於矩陣 2 的 row size，表示兩矩陣可以相乘。
   change_row: 表示輸出矩陣完成一個 row 的輸出，即矩陣乘法已進行到矩陣 2 的最後一個 column。
   busy: 狀態等於 **COMPUTE_MM** 或 **OUTPUT_MM**，表示此時系統正在進行矩陣運算，無法接收新的矩陣資料。

3. Matrix_Reg
   負責記錄矩陣 1 和矩陣 2 每個元素的值，在狀態為 **COMPUTE_MM 時**，Mul_Adder 會讀取暫存器中的矩陣元素進行矩陣乘法運算，並且將 write index 重置為 0，使下次紀錄新矩陣資料時從 write index = 0 的位置開始存取。

4. Mul_Adder
   包含一組乘法器和加法器，每個 cycle 會到 Matrix_Reg 中讀取矩陣 1 和矩陣 2 的元素，讀

取的 index 為 colume_size * row_idx + column_idx，並進行一個矩陣元素的乘法，接著與暫存相乘結果的暫存器中的值相加後，再存回暫存器中，直到做完矩陣 1 的 row 和矩陣 2 的 column 中所有元素的乘法，表示已完成輸出矩陣的一個元素運算，並將此結果輸出。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (Total cycle used*clock width)*