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SEM: 3rd SEM

BRANCH:EC Branch, B.TECH

SUBJECT: COMPUTER AIDED DIGITAL DESIGN

PROJECT: SCROLL OR MOVING TEXT USING 7 SEGMENTAL LED'S IN SYSTEM VERILOG|FPGA

Scrolling or Moving Text Using 7 Segment LED's in System Verilog | FPGA

Design:

```
module project(
   input logic clock,
   input logic reset,
   output logic a,
   output logic b,
   output logic c,
   output logic d,
   output logic e,
   output logic f,
   output logic g,
   output logic dp,
   output logic [3:0] an
   );
logic [28:0] p;
logic click;
logic [3:0] fourth, third, second, first;
always @ (posedge clock or posedge reset) //ticker
begin
 if(reset)
  p <= 0;
 else if(p == 50000000)
  p <= 0;
 else
  p <= p + 1;
end

logic [3:0] clickcount;
assign click = ((p == 50000000)?1'b1:1'b0);
```

```
always @ (posedge click or posedge reset)
begin
 if(reset)
  clickcount <= 0;
 else if(clickcount == 8)
   clickcount <= 0;
  else
  clickcount <= clickcount + 1;
end

always @ (*)
begin
    case(clickcount)
    0:
    begin
     fourth = 4; //H
     third = 3; //E
     second = 7; //L
     first = 7; //L
    end

    1:
    begin
     fourth = 3; //E
     third = 7; //L
     second = 7; //L
     first = 0; //O
    end
```

```
2:
begin
 fourth = 7; //L
 third = 7; //L
 second = 0; //O
 first = 2; //-
end

3:
begin
 fourth = 7; //L
 third = 0; //O
 second = 2; //-
 first = 1; //T
end

4:
begin
 fourth = 0; //O
 third = 2; //-
 second = 1; //T
 first = 4; //H
end

5:
begin
 fourth = 2; //-
 third = 1; //T
 second = 4; //H
 first = 3; //E
end
```

```
    6:
    begin
     fourth = 1; //T
     third = 4; //H
     second = 3; //E
     first = 8; //R
    end

    7:
    begin
     fourth = 4; //H
     third = 3; //E
     second = 8; //R
     first = 3; //E
    end

    8:
    begin
     fourth = 3; //E
     third = 8; //R
     second = 3; //E
     first = 2; //blank
    end
  endcase

end
```

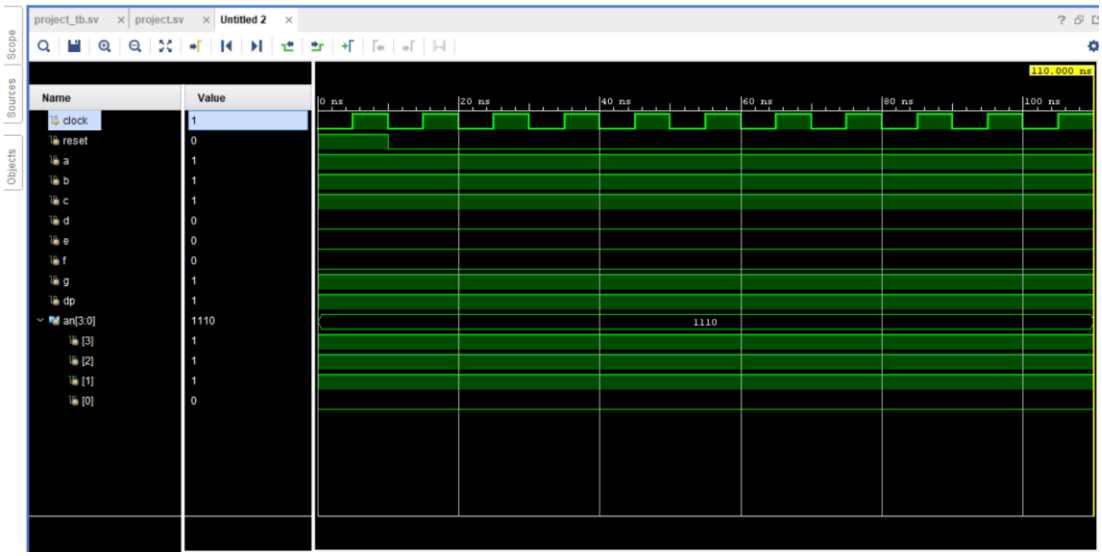
```
localparam N = 18;

logic [N-1:0]count;

always @ (posedge clock or posedge reset)
 begin
  if (reset)
   count <= 0;
  else
   count <= count + 1;
 end

logic [6:0]sseg;
logic [3:0]an_temp;

always @ (*)
 begin
  case(count[N-1:N-2])

   2'b00 :
    begin
     sseg = first;
     an_temp = 4'b1110;
    end

   2'b01:
    begin
     sseg = second;
     an_temp = 4'b1101;
    end
```

```
   2'b10:
    begin
     sseg = third;
     an_temp = 4'b1011;
    end

   2'b11:
    begin
     sseg = fourth;
     an_temp = 4'b0111;
    end
  endcase
 end
assign an = an_temp;

logic [6:0] sseg_temp;
always @ (*)
 begin
  case(sseg)
   4 : sseg_temp = 7'b0001001; //H
   3 : sseg_temp = 7'b0000110; //E
   7 : sseg_temp = 7'b1000111; //L
   0 : sseg_temp = 7'b1000000; //O
   1 : sseg_temp = 7'b0000111; //T
   8 : sseg_temp = 7'b0001000; //R
   default : sseg_temp = 7'b1111111; //blank
  endcase
 end
assign {g, f, e, d, c, b, a} = sseg_temp;
assign dp = 1'b1;
endmodule
```

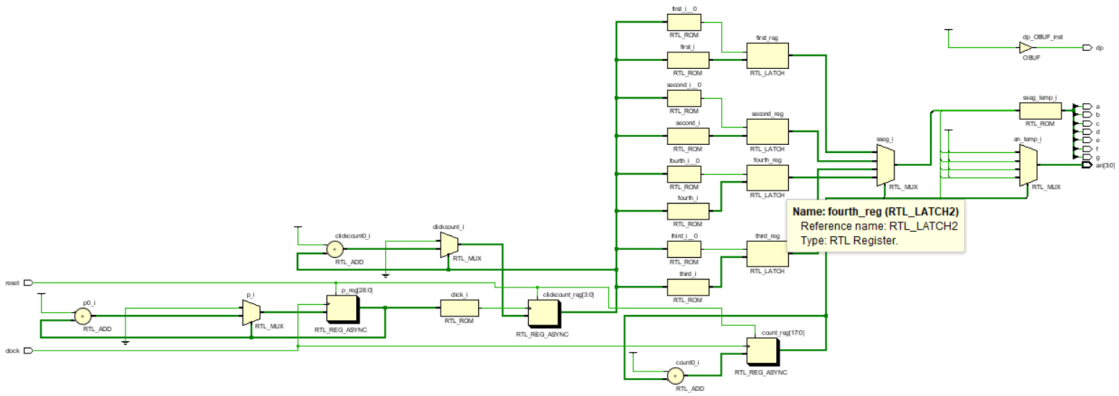
Test bench:

```
module project_tb;


   logic clock;
   logic reset;
   logic a, b, c, d, e, f, g, dp;
   logic [3:0] an;
   project uut (
      .clock(clock),
      .reset(reset),
      .a(a),
      .b(b),
      .c(c),
      .d(d),
      .e(e),
      .f(f),
      .g(g),
      .dp(dp),
      .an(an)
   );
   always #5 clock = ~clock;
   initial begin
      clock = 0;
      reset = 1;
      #10 reset = 0;
      #100 $finish;
end
endmodule
```

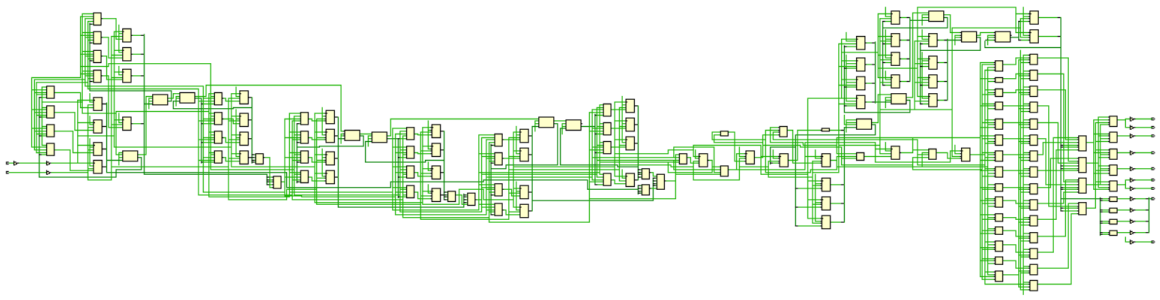
Simulation graph:



RTL Schematic:



Implementation Schematic:



Resource Utilization:

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Bonded IOB (106)	BUFGCTRL (32)
project	56	66	31	56	40	14	1

XDC file:

```
set_property IOSTANDARD LVCMOS33 [get_ports {an[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {an[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {an[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {an[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports a]
set_property IOSTANDARD LVCMOS33 [get_ports g]
set_property IOSTANDARD LVCMOS33 [get_ports reset]
set_property IOSTANDARD LVCMOS33 [get_ports f]
set_property IOSTANDARD LVCMOS33 [get_ports e]
set_property IOSTANDARD LVCMOS33 [get_ports dp]
set_property IOSTANDARD LVCMOS33 [get_ports d]
set_property IOSTANDARD LVCMOS33 [get_ports clock]
set_property IOSTANDARD LVCMOS33 [get_ports b]
set_property IOSTANDARD LVCMOS33 [get_ports c]
set_property PACKAGE_PIN W4 [get_ports {an[3]}]
set_property PACKAGE_PIN V4 [get_ports {an[2]}]
set_property PACKAGE_PIN U4 [get_ports {an[1]}]
set_property PACKAGE_PIN U2 [get_ports {an[0]}]
set_property PACKAGE_PIN W7 [get_ports a]
set_property PACKAGE_PIN W6 [get_ports b]
set_property PACKAGE_PIN U8 [get_ports c]
set_property PACKAGE_PIN U5 [get_ports e]
set_property PACKAGE_PIN V5 [get_ports f]
set_property PACKAGE_PIN U7 [get_ports g]
set_property PACKAGE_PIN V7 [get_ports dp]
set_property PACKAGE_PIN V8 [get_ports d]
set_property PACKAGE_PIN W5 [get_ports clock]
set_property PACKAGE_PIN R2 [get_ports reset]

```

Output: