Low Power CMOS Optoelectronic Receiver Design for LiDAR Systems

Drashti Gorakhiya, Madhu Kanithi, Lily Goldman
Department of Electrical Engineering, California State University Long Beach
Email: DrashtiJyotindrabhai.Gorakhiya01@student.csulb.edu, Madhu.kanithi01@student.csulb.edu, lily.goldman01@student.csulb.edu

ABSTRACT: This paper presents the design and simulation of a low-power CMOS optoelectronic receiver for indoor LiDAR systems using 45nm CMOS technology. The proposed receiver integrates critical components, including a dual-feedback folded-cascode differential trans-impedance amplifier (DFD-TIA), an active single-to-differential converter (ASD), a cross-coupled inverter-based post amplifier (CI-PA), and a two-stage differential amplifier with negative impedance compensation (TDC-NIC). The design addresses challenges such as high trans-impedance gain, wide bandwidth, and low noise required for accurate detection of light pulses. Simulation results demonstrate the receiver's ability to process input signals effectively, achieving significant gains and symmetric output voltages. While the system shows promise in improving sensitivity and signal recovery for LiDAR applications, minor mismatches in output voltages and low bandwidth highlight opportunities for further optimization.

I. INTRODUCTION

Light detection and ranging (LiDAR) sensors initially started in military applications but have grown in popularity as the vision control for autonomous vehicles, meteorology, and even a component in the iPhone camera. LiDAR has been around for over 60 years, starting as an expensive technology. With Moore's law in effect, chips have gotten smaller, more efficient, and easier to produce, decreasing the price.

The technology works by transmitting pulses of light reflecting off the closest surface to the device to be received and processed. These pulses are read using a time-of-flight (ToF) mechanism and converted to distance. The design in this paper uses a time-to-digital converter (TDC) to estimate the distance.

The challenge addressed in this work is the need for efficient and reliable optical receivers in indoor LiDAR systems. Traditional setups often rely on off-chip avalanche photodiodes (APDs), which can introduce signal distortions and limit performance due to factors like bond-wire connections and ESD protection diodes. Designing an effective optical receiver is challenging due to high trans-impedance gain, wide bandwidth, and low noise—all critical for accurately detecting and processing fast light pulses. Most approaches fail because they do not adequately address the integration of components, leading to signal degradation and increased noise, particularly when using external devices that introduce additional complications.

This work presents a CMOS optoelectronic receiver IC that integrates a dual-feedback folded-cascode differential trans-impedance amplifier (DFD-TIA), an active single-to-differential converter (ASD), a cross-coupled inverter-based post amplifier (CI-PA), and a two-stage differential amplifier with negative impedance compensation (TDA-NIC). Key results include an impressive trans-impedance gain, bandwidth, and the ability to recover narrow pulses with a maximum detection range.

While the system shows significant improvements in sensitivity and accuracy for indoor monitoring LiDAR sensors, limitations related to noise spectral density and the complexity of the integration process may present challenges for future optimization and mass production. Ref[6] Ref.[7]

II. LITERATURE REVIEW

In recent research publications, several innovative approaches to CMOS-based optoelectronic receivers for LiDAR systems have amassed.

The reference paper, "A CMOS Fully Differential Optoelectronic Receiver for Short-Range LiDAR Sensors" Ref. [1] by Joo et al. introduced an optoelectronic receiver IC for indoor LiDAR, featuring an on-chip CMOS p+/n-well avalanche photodiode (APD) to reduce signal distortion and packaging costs. The design includes a Dual-Feedback Folded-Cascode Differential Transimpedance Amplifier (DFD-TIA) to enhance signal integrity, an Active Single-to-Differential (ASD) converter for differential signaling, and a Cross-Coupled Inverter-Based Post Amplifier (CI-PA) for optimized output voltage symmetry. These advancements collectively improve the performance and cost-effectiveness of short-range indoor LiDAR sensors.

C. Hong et al. Ref. [2] explained the construction of a linear-mode LiDAR sensor utilizing a multi-channel CMOS trans-impedance amplifier (TIA) array, specifically a voltage-mode CMOS feedforward TIA (VCF-TIA). The VCF-TIA achieves higher trans-impedance gain and lower noise compared to conventional inverter TIAs, improving signal detection and sensitivity. It also features automatic gain control (AGC) to extend its dynamic range and prevent

damage. While cost-effective and energy-efficient, the VCF-TIA's design complexity and limited detection range present challenges. Despite these limitations, it offers twice the gain and superior noise performance over inverter TIAs.

Zheng et al. Ref. [3] examined a linear-array receiver AFE circuit for rotating scanner LiDAR applications. The design includes a cascaded architecture with a trans-impedance preamplifier, post- amplifier, and output buffer, achieving high gain, low noise, and wide bandwidth for detecting sub-nanosecond pulses. Key advancements are improved sensitivity for weak signals and reduced crosstalk. Disadvantages are the design's complexity and higher power consumption.

Yoon et al. Ref [4] described a mirrored current-conveyor trans-impedance amplifier (MCC-TIA) for home monitoring LiDAR sensors, highlighting its innovative input configuration that reduces input impedance, enabling wide bandwidth and efficient narrow-pulse recovery. The design includes a feedforward control-voltage generator for automatic gain control, achieving high gain and low noise performance, though with higher power consumption and complex design requirements. Compared to the voltage-mode CMOS feedforward TIA (VCF-TIA), the MCC-TIA offers wider bandwidth and greater maximum detectable current, while the VCF-TIA is more power-efficient and simpler in design.

Yang et al. Ref [5] developed a low-power, multimode, eight-channel analog front-end (AFE) circuit designed for the direct time of flight (dToF) LiDAR applications. This AFE circuit is highly programmable, supporting various operation, coupling, and gain modes, and works with both anode and cathode coupling with photodiodes. It features a reconfigurable trans-impedance amplifier (TIA) with different states and modes to achieve high gain, low noise, and power savings. Compared to the Wideband Receiver (WBRx) used in 3D ranging LiDAR systems, this AFE circuit offers better programmability and power efficiency, while the WBRx has a wider linear dynamic range and stronger output swing.

III. Circuit DESIGN

The following circuit incorporates 45nm CMOS technology with a 0.8V power supply.

A. DFD-TIA

The photodiode at the front end of the circuit outputs current in 100ns periods. This current is read into the DFD-TIA circuit, as seen in Figure 1, converted into two voltage outputs, MOUT and POUT. At the base it is a dual feedback folded cascode amplifier. The cascode technique is used to obtain a higher DC gain. The goal of the TIA is low noise for high input sensitivity in return.

The circuit implements feedback resistors R1 and R2 to lower the input resistance to around half of what a typical TIA is. R1's path generates a negative voltage leading the input current through M1 and out M3. R2's path leads through M1 and out M5.

M1 and M2 reflect a differential input, but there is only one input node on M1. Typically for these designs, they are fully differential for large voltage swings, but as there is only one input, this is not actualized. An NMOS was chosen for the input for their larger transconductance.

M3-M8 is the cascode portion of the circuit. The cascode is done to keep the circuit symmetrical and to increase the open loop gain. M7 and M8 are the common source loads connected to M3 and M4 to reduce the Miller effect.

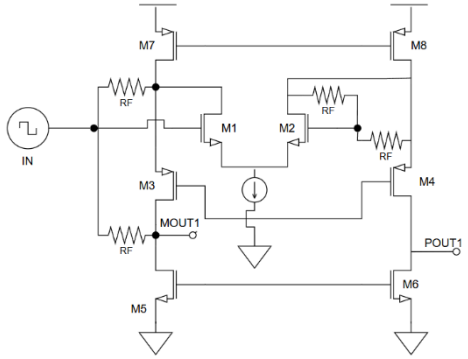


Figure 1 DFD-TIA Schematic

B. ASD

In the DFD-TIA, the ASD converter is utilized to rectify asymmetric signaling that results from a constant output voltage at M4's drain in the absence of input photocurrents delivered to M2. This imbalance may cause the PSRR (Power Supply Rejection Ratio) to deteriorate.

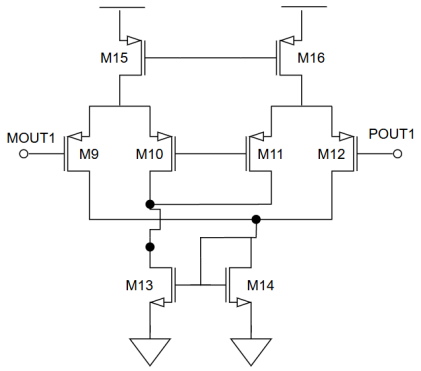


Figure 2 ASD Schematic

In order to provide completely differential signaling, the ASD converter, as seen in Figure 2, stabilizes the DC gate voltages of M5 and M6 through the drain of M13. It is composed of two cross-connected differential pairs (M9–M12). M9 and M12 gates are first subjected to the asymmetric outputs from the DFD-TIA[9]. Stable functioning is ensured by M13 and M14's consistent bias currents.

When an AC signal lowers the gate voltage of M9 (vgv_gvg), the drain current of M9 increases by α\alphaα, and the current of M10 decreases by the same amount. This drop pulls down the source voltage of M10, redistributing the bias currents symmetrically. A similar mechanism occurs for M11 and M12, leading to balanced voltage swings at the differential output nodes.

In essence, the ASD converter operates like a Common-Mode Feedback (CMFB) circuit, achieving symmetric differential outputs while maintaining constant bias currents. This ensures improved PSRR and robust fully differential signaling..

C. CI-PA

The DFD-TIA stage is followed by a CI-PA for the purpose of gain boosting and more symmetric output voltage swings. The schematic of the CI-PA, as in Figure 3, illustrates how the output voltages are boosted by merging the input signals from its own path with another small portion of the other path. Moreover, the CI-PA reduces mismatches from the previous stage due to its cross-coupling-based pseudo-differential structure. Therefore, better symmetry between two output voltages can be obtained even in the cases of large input photocurrents flowing from the on-chip CMOS APD.

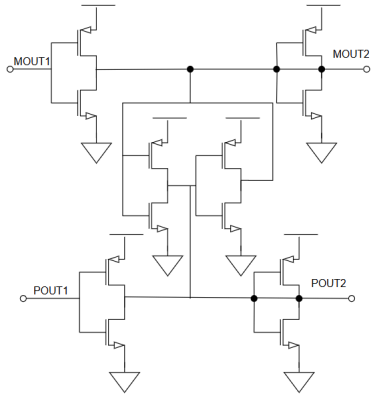


Figure 3 CI-PA Schematic

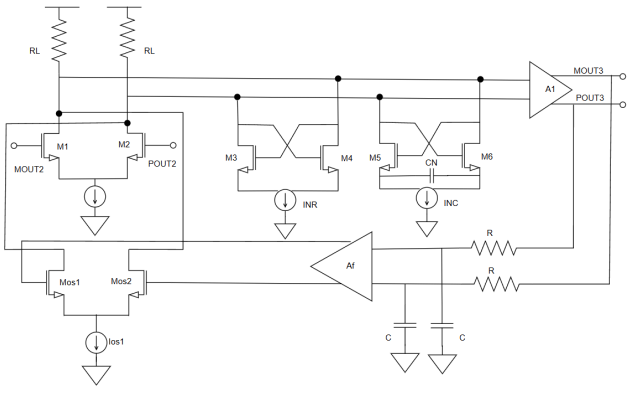


Figure 4 TDC-NIC Schematic

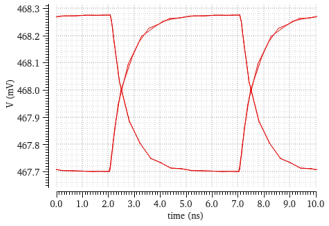
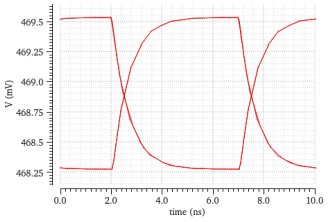
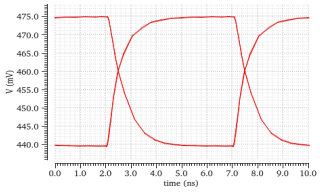
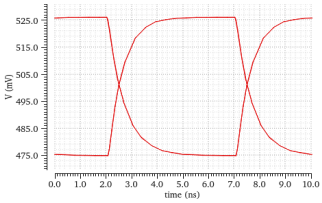
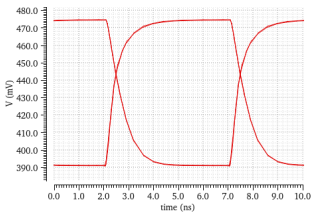
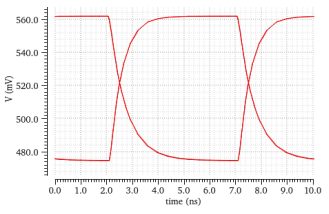
D. TDC-NIC

In the TDA-NIC circuit, referenced in Figure 4, transistors M1 and M2 form a differential input pair that receives the input signals INN and INP [10]. These signals represent the photodetector's current output. The bias current source I1 ensures proper operation of the transistors, enabling differential-mode signal amplification. The resistors RL act as load resistors, converting the differential current into voltage for the next stage.

M3 and M4 form an active load for the differential pair, where the equivalent resistance Req controls the gain of the amplifier. This active load increases the effective resistance while maintaining small size and low parasitic capacitance, enhancing the differential amplifier's voltage gain.

Transistors M5 and M6 with equivalent capacitance Ceq form the Negative Impedance Converter (NIC). The NIC introduces a negative impedance that compensates for the photodiode and amplifier's parasitic capacitance CN, extending the circuit bandwidth. The current source INC biases this stage to ensure proper operation.The feedback amplifier Af introduces a frequency-dependent feedback network composed of resistors R and capacitors C. This feedback stabilizes the circuit while enhancing its frequency response, reducing signal distortion at high speeds.

Table 1 Eye Diagrams of DFD-TIA w/ ASD Voltage Output

MOUT1	POUT1
 Input: 1uA; Output: 0.6mVpp	 Input: 1uA; Output: 1.25mVpp
 Input: 50uA; Output: 35.3mVpp	 Input: 50uA; Output: 51.2mVpp
 Input: 100uA; Output: 84.6mVpp	 Input: 100uA; Output: 87.2mVp

IV. Simulation Results

A. DFD-TIA with ASD

The following simulation for the DFD-TIA with ASD uses 0.8V power supply and 2.33mA bias current. The photo diode is simulated as a pulsed current source with a period of 10ns. Table 1 is the MOUT1 and POUT1 at three different input currents. The goal of the simulation is to have the input current value match the output voltage value and have MOUT1 equal the voltage of POUT1. The simulations fell short of this goal with none of the MOUT1 or POUT1 values matching the input current. The average mismatch between the two signals is 39%. The mismatch improves as the input current increases. For this design the minimum input current should be 100uA.

B. DFD-ASD with CIPA

The following simulation for the DFD-ASD with CIPA uses 0.8V power supply and Ibia's 2.3mA. The simulation results, in Figure 5, reflect a 47db approx value up to 100Hz. The goal for a LiDAR device is to have a dB rolloff at around the 1GHz range. Our design does not meet this specification and further work needs to be done to correct this.

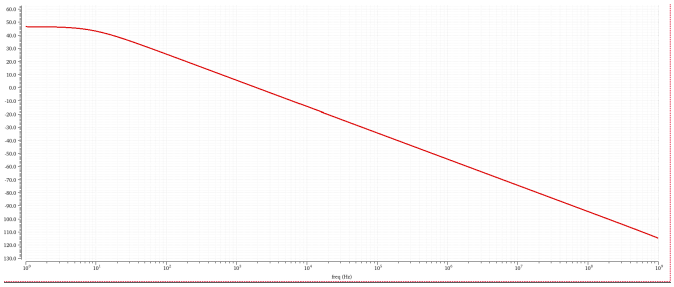


Figure 5 CIPA simulation

For the noise analysis, the Ibias is 2.3mA and Vdd is 0.8V. Generally noise analysis is essential for optimizing the Cross-Coupled Inverter-Based Post Amplifier (CI-PA)[13] to deliver high gain, low noise, and efficient power consumption. By identifying and mitigating thermal, flicker, and power supply noise, the CI-PA can maintain a high signal-to-noise ratio, making it ideal for optical communication systems, LiDAR applications, and high-speed data recovery circuits. Noise optimization ensures reliable and accurate signal amplification, even in low-power and high-frequency scenarios. In Figure 6, the results were 29.38uV/Hz.

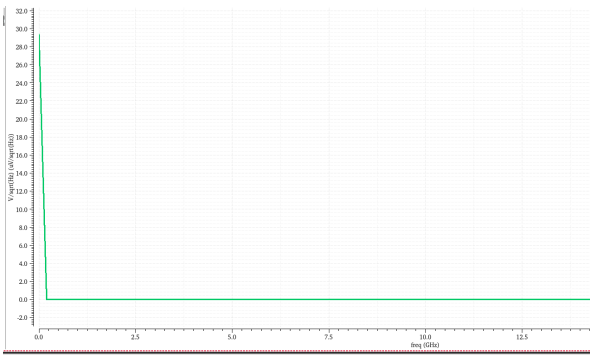


Figure 6 Output Noise for CIPA

Figure 7 is the input noise of CIPA. The results are 2.76 A/sq(HZ).

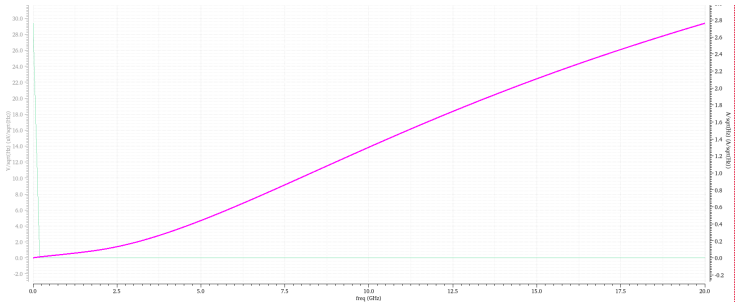


Figure 7 Input Noise for CIPA

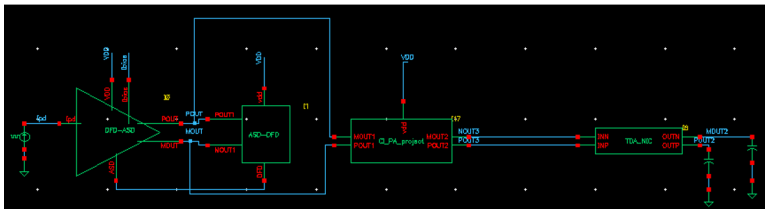


Figure 8 Design with all four blocks integrated

C. DFD-ASD , CIPA with TDA-NIC

The circuit simulation, as in Figure 8, involves two analyses—transient (tran) and AC analysis (ac)—with specific design variables used to parameterize the system. The design variables include Ipd (10µA) and idc (50µA) for bias currents, vdd (0.8V) as the supply voltage, vdc (10mV) for DC bias, and RF (5), likely representing resistance. The results display voltage outputs for various test points At VDC("/POUT") = 605.3mV, the node likely represents the stable DC output. The node VDC("/MOUT3") = -872mV shows a negative voltage, Similarly, VDC("/MOUT2") = -3.271V. the DC voltage is becoming increasingly negative after integrating the Transimpedance Amplifier (TIA) and Noise Injection Circuit (NIC) into the system, it indicates a potential issue with the design or biasing conditions. In a typical LIDAR system, the addition of a TIA should stabilize or increase the output DC voltage because the TIA converts photocurrent into a proportional voltage gain, while the NIC ensures noise reduction and system stability. However, the observed negative voltages at nodes like MOUT3 (-872mV) and MOUT2 (-3.271V) .

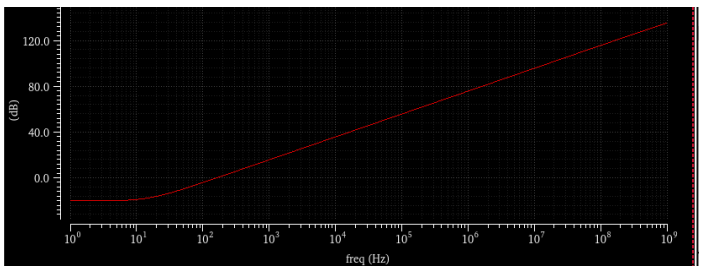


Figure 9 AC analysis

The AC analysis graph in Figure 9 shows the transimpedance gain of the circuit after integrating a Transimpedance Amplifier (TIA) and a Noise Injection Circuit

(NIC) in the LIDAR system. The gain increases with frequency, starting low at lower frequencies and rising linearly on a logarithmic scale, indicating effective amplification of high-frequency signals. This behavior is crucial for LIDAR systems, where the TIA converts weak photocurrents from the photodetector into voltage signals, ensuring sufficient gain for detecting fast, high-frequency light pulses. The NIC enhances stability and reduces noise interference, improving signal quality and performance across the frequency spectrum. This combination allows the system to achieve high-resolution and reliable detection in LIDAR applications.

V. Conclusion

Our paper reflects the design and simulation of a CMOS optoelectronic receiver using 45nm technology. There are four portions of the circuit: DFD-TIA, ASD, CI-PA, and TDC-NIC. The design is inspired from the one in "A CMOS Fully Differential Optoelectronic Receiver for Short-Range LiDAR Sensors" [1].

The design includes a differential voltage output with an average mismatch of 39% in the range of 1uA to 100uA. Therefore, a minimum current for this design should be 100uA. The design has a gain of 47dB along a bandwidth of 100Hz. This falls short from the expected 700MHz bandwidth.

VI. References

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